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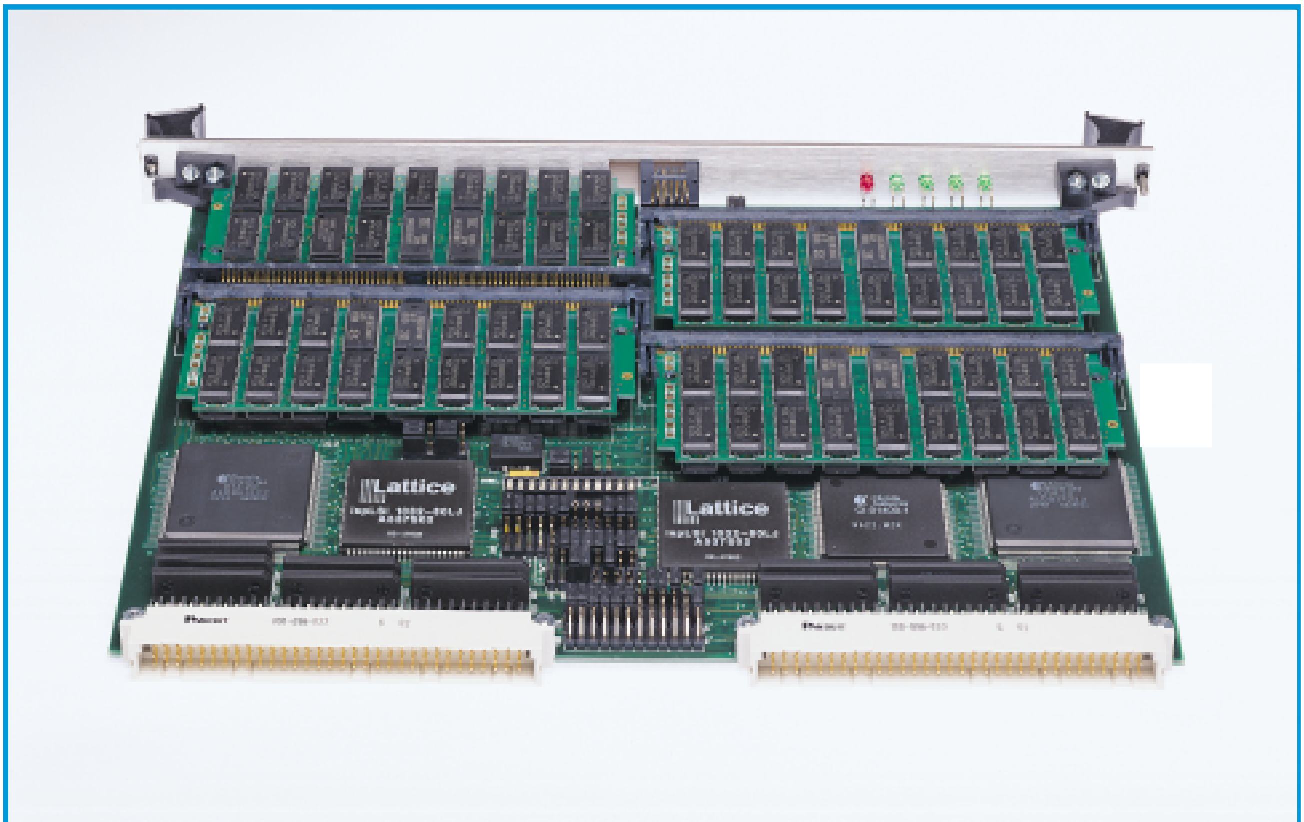
VMEbus

32MB TO 512MB HIGH-SPEED VME, VSB, &VME64
PARITY MEMORY FOR VMEbus SYSTEMS with ALU FUNCTIONS



CI-VME80SE

The CI-VME80se is a high-speed, high-capacity DRAM memory board with VME, VSB and VME64 interfaces. The CI-VME80se is optimized for Block Transfer Cycles yielding a bus transfer rate up to 80 megabytes per second. The memory module has cycle times of 95 nanoseconds and access times of 30 nanoseconds during block cycles. The CI-VME80se is an excellent choice for high-speed DMA and dedicated data acquisition devices that require maximum memory transfer rates into large memory capacities. The CI-VME80se fully supports the current ANSI/VITA 1-1994, ANSI/VITA 1.1-1997 and VSB Rev. C Bus Specifications. Flexible address selections allow the CI-VME80 to be placed into any VMEbus environment. The CI-VME80se has low power requirements of 2.5A (typical) at +5 volts.

FEATURES:

- Up to 80MB per second bus transfer rates
- 32MB to 512MB in one 6U VMEbus slot
- ANSI/VITA 1-1994, ANSI/VITA 1.1-1997
- 64 bit data path for higher data transfer rates
- Byte Parity Error Detection
- Addressable in 24 or 32 bit through 4 Gigabytes
- Memory start and end addresses selectable on 1MB boundaries
- ALU Cycles
- LED indicators for VMEbus, VSB, D64, ALU access, and parity ERROR status

Chrislin Industries, Inc.

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SPECIFICATIONS

CI-VME80se

CHARACTERISTIC	SPECIFICATION
Capacity	32, 64, 128, 256, and 512 megabytes
Cycle Time	95ns BLOCK CYCLE, 195ns SINGLE CYCLE
Access Time Write/Read	30/30ns BLOCK CYCLE, 90/140ns SINGLE CYCLE
Word Size	8, 16, 24, 32, or 64 bits
Memory Addressing	32 or 24 bits, 4 GB maximum selectable on 1 MB boundaries
CSR Addressing	16 bit, selectable on 256 byte boundaries using VMEbus SHORT I/O
Modes of Operation MEMORY CSR	READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS, UNALIGNED TRANSFERS READ, WRITE
ANSI/VITA 1-1994, ANSI/VITA 1.1-1997 Compatibility	SLAVE, A16, A24, A32, D8, D16, D24, D32, D64, RMW, BLT, MBLT, UAT, AD0
VSB Rev. C Compatibility	SLAVE, D32, A32, SAS, ATLAS, AD0, BLT(32)
Address Modifiers	Responds to AM Codes 3F,3E,3D,3B,3A,39,0F,0E,0D, 0B,0A,09,2D, & 29, AM Codes are programmable, ALU Cycles are selected with AM Codes 10-1F
Refresh	Internal, Distributed
Parity/Error Handling	Byte Parity
1 RED, 4 GREEN LED Indicators	RED - Parity Error, GREEN - VME, VSB, D64 & ALU cycles
Designed Temperature Range	Operating: 0 deg. C to +50 deg. C non-condensing Storage: - 20 deg. C to +70 deg. C non-condensing
Power Requirements +5 Volts	TYPICAL MAXIMUM 2.5A 2.9A 64MB Option
Dimensions	160mm x 233.35mm, 6U form factor

CI-VME80 ENHANCED OPERATIONAL FEATURES

Chrislin continues to push the State-of-Technology with the CI-VME80se. Maximum Bus Transfer Rates are provided on the VME64 Bus. The CI-VME80se uses two new custom ASICS that were designed to provide the High-Performance DRAM functions.

A new concept in data-storage has been introduced as a function of Chrislin's NEW Custom Chip Set. A set of common data manipulation functions have been integrated into the CI-VME80se. A typical scenario of a value being added to a memory location involves a processor first reading the location, adding the value to the read data, and finally writing the result back into the original location. The CI-VME80se reduces this process to a third of the conventional method. The complete operation is performed by simply writing the value to the location. All processing is performed by the CI-VME80se during the write cycle. Other supported cycles include Add, Subtract, AND, OR, and Exclusive OR. The basic architecture supports all functions found in the 74S181 ALU. Each of these functions can be performed over the 32bit data word.

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ALU FUNCTIONS

A new concept in Memory design is the ability to perform various ALU functions during a VMEbus write cycle. This functionality has been implemented in the Chrislin ASIC Chip Set. A typical ALU cycle is where the master writes one of the operands to the memory. The previously stored data is used as the second operand. The result is stored back into the same memory location.

To access one of these functions one of two methods may be used. The first method determines the function to be executed by placing the User Defined Address Modifiers (as shown in the table below) during the write cycle. The second method allows the user to program the function via the Control Status Register. The second method allows the ALU to be used with standard off the shelf VMEbus masters. A CSR bit 'M' is used to select either Logical or Arithmetic Functions. A Carry-In bit 'C' is also set in the CSR and selects a second column in the function table. Carry-Outs are ignored and not stored. . The master must first set up the 'M' and 'C' bits in the CSR.

The following table summarizes the available functions in the **ALU1** instruction set. Note that BUS data is represented as A and previously stored MEMORY data is represented as B.

	M = H	M = L; ARITHMETIC OPERATIONS	
AM Code	LOGIC Functions	Cn'=H (no Carry)	Cn'=L (with carry)
10	F=!A	F=A	F=A PLUS 1
11	F=!(A+B)	F=A+B	F=(A + B) PLUS 1
12	F=!AB	F=A+!B	F=(A + !B) PLUS 1
13	F = 0	F = MINUS 1(2's COMPL)	F = ZERO
14	F = !(AB)	F = A PLUS A!B	F = A PLUS A!B PLUS 1
15	F = !B	F = (A + B) PLUS A!B	F = (A + B) PLUS A!B PLUS 1
16	F=A@B	F=A MINUS B MINUS 1	F=A MINUS B
17	F = A!B	F = A!B MINUS 1	F = A!B
18	F=!A+B	F=A PLUS AB	F=A PLUS AB PLUS 1
19	F=!(A@B)	F=A PLUS B	F=A PLUS B PLUS 1
1A	F = B	F = (A + !B) PLUS AB	F = (A + !B) PLUS AB PLUS 1
1B	F = AB	F = AB MINUS 1	F = AB
1C	F=1	F = A PLUS A <	F=A PLUS A PLUS 1
1D	F=A + !B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
1E	F = A + B	F = (A + !B) PLUS A	F' = (A + !B) PLUS A PLUS 1
1F	F=A	F=A MINUS 1	F=A

< Shifted Left to the next most Significant position - M = M bit in the CSR register.

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