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Chrislin Industries, Inc.

CI-VFLASH

TECHNICAL MANUAL

HIGH-SPEED
VME64/VMEbus

FLASH MEMORY

Release 3.2

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1. GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation of the CI-VFLASH memory module for the VMEbus.

1.2 THE MEMORY MODULE

The CI-VFLASH is available in four option sizes as follows:

OPTION	MEMORY CAPACITY	MODULE
64 MEG	16,384Kx32 bits	CI-VFLASH/64
128 MEG	32,768Kx32 bits	CI-VFLASH/128
256 MEG	65,536Kx32 bits	CI-VFLASH/256

1.3 CI-VFLASH MEMORY DESCRIPTION

The CI-VFLASH is a high-density, high-speed Block Transfer FLASH Memory board on the VMEbus. A VME-64 databus allows data transfer rates up to 80 Megabytes/Second. The flash memory is contained on two or four SIMM modules that can be easily installed or removed in the field allowing added user flexibility.

The CI-VFLASH utilizes 28F016SA,28F032SA,28F160S5,28F320S5, or equivalent Flash Chips allowing the user over 100,000 reliable erase/ writes per chip block.

The CI-VFLASH uses a Custom Chip Set developed by Chrislin.
VME64, ANSI/VITA 1-1994 functionality is also provided.

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1.4 OPERATIONAL FEATURES

The CI-VFLASH performs all memory read functions according to ANSI/VITA 1-1994.

Starting and Ending Address selections are done on One Megabyte boundaries.

A Control Status Register (CSR) is provided, and responds to 16 bit SHORT IO Address modifiers. CSR functions include INTERNAL WRITE ENABLE / DISABLE, PROGRAM WRITE ENABLE / DISABLE, and MEMORY ERASE.

The ability to perform a standard VME write cycle to a previously erased memory location requiring no software control is a highlighted feature of the CI-VFLASH. The CI-VFLASH has an internal write and erase state machine which allows the user to write to previously erased memory locations requiring no software control. The memory can be erased through a CSR write sequence or by a manual switch on the front panel. The unit can then be written to using 32 or 64 bit VME or VME64 write cycles, to load new data. Note: The memory must go through a new erase sequence before a location can be written to a second time. These features along with removable flash SIMM modules allows the greatest ease of use and flexibility to the end user.

Block Cycles can be performed on 32 or 64 bit wide locations. Chrislin uses a proprietary cycle management system that delivers excellent access and cycle times.

Block Transfer lengths of up to 4 Kbytes may be performed. Transfers may not cross 4 Kbyte boundaries. The VMEbus master is responsible for ending a Block Transfer.

LED indicators for VMEbus CYCLE, (green) and MEMORY BUSY status indicating write or erase activity (red) are mounted on the front panel.

1.5 POWER REQUIREMENTS

The CI-VFLASH memory module requires the +5 volt supply from the VMEbus/VSB backplane for read operation and +12 volt or +5volt for program operation depending on the FLASH chip utilized. (See the general specifications for current requirements.)

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1.6 GENERAL SPECIFICATIONS

CAPACITY:	64, 128, or 256 Megabytes		
CYCLE TIME READ	100ns BLOCK CYCLE, 180ns SINGLE CYCLE		
ACCESS TIME READ:	35ns BLOCK CYCLE, 150ns SINGLE CYCLE		
CYCLE TIME program write	10us SINGLE CYCLE ONLY		
ACCESS TIME program write	150ns SINGLE CYCLE ONLY		
CYCLE TIME internal write	10us typ. BLOCK AND SINGLE CYCLE		
ACCESS TIME internal write	10us typ. BLOCK AND SINGLE CYCLE		
BOARD ERASE	30 to 150 seconds		
WORD SIZE:	8, 16, 24, 32 or 64 bits-read, 32 or 64 bits-write		
MEMORY ADDRESSING:	A32, 4 GB max. Selectable on 1MB boundaries		
CSR Addressing:	A16, selectable on 256 byte boundaries using VMEbus SHORT I/O		
Modes of Operation: MEMORY	READ, WRITE, PROGRAM WRITE, BLOCK TRANSFERS, UNALIGNED TRANSFERS		
CSR	READ, WRITE		
ANSI/VITA 1-1994 Compatibility:	SLAVE, A16, A32, D8, D16, D24, D32, D64, BLT, MLBT, UAT, AD0		
Address Modifiers:	Responds to AM Codes 3F, 3E, 3D, 3B, 3A, 39, 0F, 0E, 0D, 0B, 0A, 09, 2D,		
Indicators:	RED - memory busy, indicates write or erase operation in progress GREEN - VME/VME64 cycle		
Designed Temperature Range:	Operating: 0 deg. C to +70 deg. C non-condensing		
Power Requirements:	TYPICAL	MAXIMUM	
+5 Volts	1.2A	1.6A	256MB Option
Dimensions:	160mm x 233.35mm, 6U form factor		

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1.7 SWITCHING CHARACTERISTICS

VMEbus Switching Characteristics

Parameter	Description	Min	Max	Notes
SCRA	Single Cycle Read Access Time	150ns		1
SCPWA	Single Cycle program Write Access Time	150ns		1,2
SCIWA	Single Cycle Internal Write Access Time	4.5us	100us	1,3
SCDV	Single Cycle Data Valid Setup	10ns		
SCTR	Single Cycle Time Read	180ns		1
SCTPW	Single Cycle Time Program Write	180ns		1,2
SCTIW	Single Cycle Time Internal Write	4.5us	100us	1,3
AOT	Access Turn Off Time	30ns		
BCAT	Block Cycle Access Time Read	35ns		1
BCATIW	Block Cycle Access Time Internal Write	4.5us	100us	1,3
BCCTR	Block Cycle Time Read	100ns		1
BCCTIW	Block Cycle Time Internal Write	4.5us	100us	1,3
BCDV	Block Cycle Data Valid Setup	10ns		

Notes:

1. Access times are measured from data strobes and inside bus drivers or receivers.

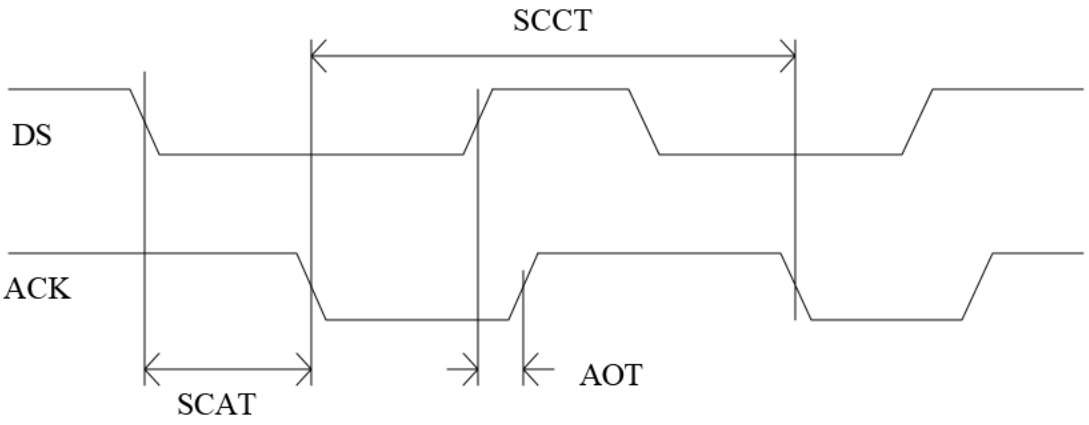
2. When CSR bit 0 is 1 and bit 1 is 0 the CI-VFLASH is written to using standard flash programing. Commands are written to the memory followed by data and then a polling of the memory location reading the chips CSR is performed until a done bit is read indicating completion. The time indicated is only for individual writes to memory not the time for the completion of the write operation.

3. When CSR bits 0 and 1 are true the CI-VFLASH internally controls writes to memory handling all flash protocol internally, making the write appear as any other write to a read/write memory. The typical internal write access time is 6us. This parameter
degrades over the life of the flash parts. At the end of the life of the flash parts (over 100000 plus writes performed) the
access time could be as high as 100us. It is therefore recommended that if the VME master utilizes a bus time out interrupt,
it be set greater than 100us.

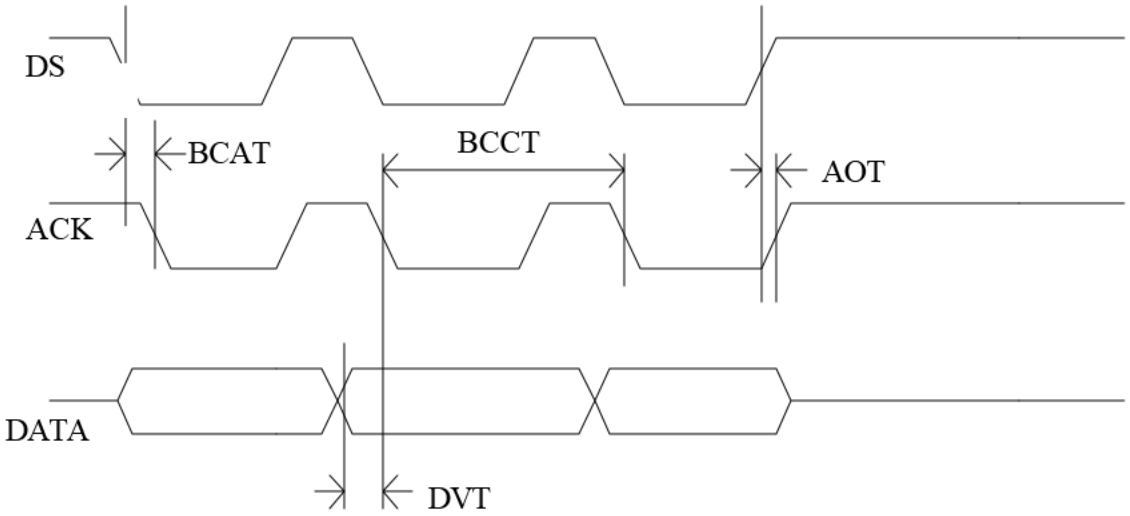
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ACCESS CYCLE TIMING

SINGLE TRANSFER CYCLE



BLOCK TRANSFER CYCLE



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2. HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section describes the handling precautions and the procedure of installation of the CI-VFLASH memory modules.

2.2 HANDLING PRECAUTIONS

The flash memory IC's on the CI-VFLASH module are MOS devices. They are damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC's. Avoid unnecessary handling. When handling IC's wear cotton rather than synthetic clothing.

The CI-VFLASH uses SIMM's for upgradeability and field interchangeability. The modules do not need to be removed for board configuration. If the modules are removed or installed, care needs to be taken not to damage the mating connectors. Before applying pressure to seat the SIMM's in the connector, examine that the key is oriented correctly and all pins are aligned. Only slight pressure is needed to seat the modules in the connector.

2.3 MEMORY ADDRESS SELECTION

The CI-VFLASH has an individually selectable START and END address with 1 megabyte granularity. Refer to drawing 75152 for jumper positions.

Address sections are configured by representing the desired binary address in jumper selections. An installed jumper represents a '1' or HI on the bus. A removed jumper represents a "0" or LOW on the bus..

The address range for the bus is selected with a starting and ending address. Significant address bits used in the selection are A20 through A31 for the bus.

S20 - S31 VMEbus Start Address
E20 - E31 VMEbus End Address

Refer to Table 2.3.1 for examples.
or visit our WEB site www.chrislin.com for a downloadable program for configuring your units.

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2.3.1 STARTING AND ENDING ADDRESS EXAMPLES

S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	VME START ADDRESS
J31	J30	J29	J28	K27	J26	J25	J24	J23	J22	J21	J20	VSB START ADDRESS
O	O	O	O	O	O	O	O	O	O	O	O	00000000 (HEX)
O	O	O	O	O	O	O	O	O	O	O	O	00040000
O	O	O	O	O	O	O	O	O	O	O	O	00080000
O	O	O	O	O	O	O	O	O	O	O	I	00100000
O	O	O	O	O	O	O	O	O	O	I	O	00200000
O	O	O	O	O	O	O	O	O	I	O	O	00400000
O	O	O	O	O	O	O	O	I	O	O	O	00800000
O	O	O	O	O	O	O	I	O	O	O	O	01000000
O	O	O	O	O	O	I	O	O	O	O	O	02000000
O	O	O	O	O	O	I	I	O	O	O	O	03000000
O	O	O	O	O	O	O	O	O	O	O	O	START DEFAULT (all options)

E31	E30	E29	E28	E27	E26	E25	E24	E23	E22	E21	E20	VME END ADDRESS
K31	K30	K29	K28	K27	K26	K25	K24	K23	K22	K21	K20	VSB END ADDRESS
O	O	O	O	O	O	O	O	O	O	O	O	0003FFFF (HEX)
O	O	O	O	O	O	O	O	O	O	O	O	0007FFFF
O	O	O	O	O	O	O	O	O	O	O	O	000FFFFF
O	O	O	O	O	O	O	O	O	O	O	I	001FFFFF
O	O	O	O	O	O	O	O	O	O	I	I	003FFFFF
O	O	O	O	O	O	O	O	O	I	I	I	007FFFFF
O	O	O	O	O	O	O	O	I	I	I	I	00FFFFFF
O	O	O	O	O	O	O	I	I	I	I	I	01FFFFFF
O	O	O	O	O	O	O	I	I	I	I	I	32MB END DEFAULT
O	O	O	O	O	O	I	I	I	I	I	I	64MB END DEFAULT
O	O	O	O	O	I	I	I	I	I	I	I	128MB END DEFAULT
O	O	O	O	I	I	I	I	I	I	I	I	256MB END DEFAULT

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2.4 24-BIT ADDRESS SYSTEMS

24 Bit address decoding is not supported with the CI-VFLASH. The board will respond to 24-Bit Address modifiers, but will decode address bits A20 through A31 for selection.

2.5 VMEbus ADDRESS MODIFIERS

The CI-VFLASH may respond to different combinations of address widths and VMEbus address modifier codes. Shunt area D selects whether 32 bit only modifiers are to be responded to, or 32 or 24 bit modifiers will be responded to. See User Option Section.

The following table summarizes the AM codes that the CI-VFLASH responds to:

3E, 3D 3A, 39, 0E, 0D, 0A, 09	Single Cycle Transfers
3F, 3B, 0F, 0B	32 Bit Block Transfers
3C, 38, 0C, 08	64 Bit MBLT Block Transfers
2D, 29	16 Bit CSR Cycles

2.6 BUS INTERFACE DISABLE

If the VMEbus Bus interface is to be disabled, simply set the starting address greater than the ending address.

2.7 CSR ADDRESS SELECTION

The CI-VFLASH CSR is an 8 bit read/write register. The CSR is selected by a VMEbus 16 bit SHORT SUPERVISORY (2D) or SHORT NON-PRIVILEGED ACCESS (29) Address Modifier code. Address selection uses shunt areas I8 through I15 and CSREN which places the CSR on 256 byte boundaries. Note that shunt labels correspond to address bits. An installed shunt represents a "0" or LOW on the bus whereas a removed shunt represents a "1" or HIGH on the bus. Refer to Table 2.7.1 for examples.

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2.7.1 CSR ADDRESS SELECTION EXAMPLES

CSREN	I15	I14	I13	I12	I11	I10	I9	I8	ADDRESS
0	X	X	X	X	X	X	X	X	DISABLED
I	I	I	I	I	I	I	I	I	0000 - 00FF
I	I	I	I	I	I	I	I	O	0100 - 01FF
I	I	I	I	I	I	I	O	I	0200 - 02FF
I	I	I	I	I	I	O	I	I	0400 - 04FF
I	I	I	I	I	O	I	I	I	0800 - 08FF
I	I	I	I	O	I	I	I	I	1000 - 10FF
I	I	I	O	I	I	I	I	I	2000 - 20FF
I	I	O	I	I	I	I	I	I	4000 - 40FF
I	O	I	I	I	I	I	I	I	8000 - 80FF
I	O	O	O	O	O	O	O	O	FF00 - FFFF
I	I	I	I	I	I	I	I	I	DEFAULT CONFIGURATION

2.8 USER OPTIONS

The following USER OPTIONS are shunt selectable. Refer to drawing 75152 for shunt positions. The CSR (Control Status Register) is initialized to the shunt selections during /SYSRESET. The CSR configuration may then be changed by program control by writing to CSR bits D0-D3. CSR bits D0 and D1 are initialized according to shunt settings at CR0 and CR1 respectively. CSR bits D2 and D3 are used to initiate an erase sequence according to 2.13 and are set to 0 at power-up. D0 thru D3 are the only bits utilized in the CSR.

2.8.1 USER CONFIGURED SHUNT LOCATIONS

SHUNT AREA	**POSITION**	**DESCRIPTION**
CR0	IN	writes Disabled
CR0	OUT(default)	writes Enabled
CR1	IN	internal write state machine Disabled
CR1	OUT(default)	internal write state machine Enabled
A	IN	Decode 24 bit AM Codes
A	OUT(default)	Ignore 24 bit AM Codes
WP (ON SIMM's)	OUT	write protect to flash array disabled
WP	IN	write protect to flash array enabled

All other jumpers are Factory set and must not be modified by the user. See Section 2.8.2

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2.8.2 FACTORY SET SHUNT POSITIONS

CF0, CF1, and CF2 indicate the option size of the CI-VFLASH. These jumpers are set at the factory based on the option size shipped and must not be changed. To insure proper operation of the CI-VFLASH do not change the factory set options.

CF0 indicates the number of flash chips on each SIMM.
CF1 indicates the size of the flash chip used on the SIMMs.
CF2 indicates the number of SIMMs on the module

SHUNT AREA	POSITION	DESCRIPTION
CF0	IN	8 flash chips/SIMM, half populated
CF0	OUT	16 flash chips/SIMM, full populated
CF1	IN	16mbit flash chips utilized
CF1	OUT	32mbit flash chips utilized
CF2	IN	2 SIMMs installed on module
CF2	OUT	4 SIMMs installed on module

OPTION SIZE CONFIGURATION DESCRIPTION

CF0	CF1	CF2	
IN	IN	IN	32 megabytes, 16megabit flash chips, 2SIMMs
OUT	IN	IN	64 megabytes, 16megabit flash chips, 2SIMMs
IN	OUT	IN	64 megabytes, 32megabit flash chips, 2SIMMs
OUT	OUT	IN	128 megabytes, 32megabit flash chips, 2SIMMs
IN	IN	OUT	64 megabytes, 16megabit flash chips, 4SIMMs
OUT	IN	OUT	128 megabytes, 16megabit flash chips, 4SIMMs
IN	OUT	OUT	128 megabytes, 32megabit flash chips, 4SIMMs
OUT	OUT	OUT	256 megabytes, 32megabit flash chips, 4SIMMs

POST AREAS J41 THROUGH J45

Post area J41- J45 are test points. Shunts must not be placed across any posts in this

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area as signals may be shorted.

2.9 WRITE ENABLE CONFIGURATION

CSR bits 0 and 1 control the write mode of the CI-VFLASH. With CSR bit 0 set to 0 at power up (CR0 shunt installed) or writing a 0 to CSR bit 0 disables all writes to the unit. Any write attempt will result in no action and a bus time-out with CSR bit 0 set to 0. With CSR bit 0 set to 1 writes are performed according to the state of CSR bit 1.

With CSR bit 0 set to 1 and CSR bit 1 set to 0 at power-up (CR0 shunt out, CR1 shunt in), or writing a 0 to CSR bit 1 and a 1 to CSR bit 0, the unit is in PROGRAM WRITE MODE. The unit will accept 32 bit single cycle writes only (any other type write cycle will result in no action and a bus time-out). The user is responsible for generating proper program sequences for erasing and writing new information to blocks of memory according to 28F016SA or 28F032SA protocol.(see appendix A for examples of programing technics)

With CSR bit 0 set to 1 and CSR bit 1 set to 1 at power-up (CR0 and CR1 shunt out), or writing a 1 to CSR bit 0 and bit 1 the unit is in INTERNAL WRITE MODE. The unit will accept 32 bit and 64 bit single cycle or block cycle writes only (any other type write cycle will result in no action and a bus time-out). In this mode Flash memory write protocol is handled by an internal state machine. The user simply writes the desired data to the location in memory and all other flash write housekeeping is handled transparent to the user. Locations to be written must have been previously erased.

Please note that flash memory can only be written to once. To rewrite to a location it must be erased first. The CI-VFLASH allows automatic erase of the unit through CSR writing or a front panel switch when CSR bits 0 and 1 are set to 1's, according to section 2.10. See table 2.1 for summary.

2.10 FLASH MEMORY ERASE CONFIGURATION

Erase of the flash memory can be disabled (CSR bit 0 set to 0). Erase functions can be controlled by outside programing (CSR bit 0 set to 1 and CSR bit 1 set to 0). Or erase can be performed by a write sequence to the CSR or a front panel switch (CSR bit 0 and 1 set to 1).

With CSR bit 0 set to 0 no writes of any kind can be performed on the memory, therefore no erase operations can be performed.

With CSR bit 0 set to 1 and CSR bit 1 set to 0 outside program control is enabled. Erase functions, such as block or chip erase of the 28F016SA and 28F032SA can be

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performed through program control. (see Appendix A for programing techniques).

With CSR bit 0 and CSR bit 1 set to 1 the internal state machine can be initiated to perform an erase of the entire memory through a sequence of CSR writes, or by use of a momentary switch on the front panel along with a reset to the system bus.

By first writing a "0111" to D3, D2, D1, D0 respectively followed by "1111" followed by "0111" an internal erase state machine will perform a complete erase to all of the flash memory installed on the CI-VFLASH. This function will take from 30 to 60 seconds to complete. It will be indicated by the busy LED being on. No other memory accesses should be performed during this time. At its completion the LED will go out and the memory is ready for all other functions.

For ease of use, the CI- VFLASH also has a manual erase option requiring no program access to the memory. With CSR bits 0 and 1 set to 1, an operator can hold in the erase momentary switch on the front panel while initiating a reset to the system. This will start the erase sequence as noted in the previous paragraph requiring no software control. For example: The operator pushes in and holds the momentary switch in the depressed position then, while maintaining the switch depressed, initiates a bus reset to the system. The erase sequence will start indicated by the red "busy" LED being illuminated.

See Table 2.1 for summary.

2.11 24/32 BIT VME ADDRESS SELECT

Area A selects whether the CI-VFLASH will respond to only 32 bit Address modifiers or 24 bit and 32 bit modifiers. Note that the CI-VFLASH decodes address bit A20-A31. If the CI-VFLASH will be accessed by a 32 address bit master use the 32 bit configuration. If a 24 bit master will access the board, the 24/32 bit setting should be used. During an A24 cycle the upper address lines are decoded by the board. They must either be driven or pulled to some known state.

Some problems that have been noticed over the years is that some controller boards place buffer space in the 24 bit address modifier space. If the memory board is configured to respond to both 24 and 32, it may redundantly respond to the controllers address space.

If you need to place the CI-VFLASH into 24 bit address space take care in setting up your bus addresses for all boards. If you are going to access the board with 32 bit address modifiers leave the shunt installed at area A.

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2.12 WRITE PROTECT SHUNT ON FLASH SIMM's

When the WP shunt is installed on a flash SIMM, the write protect signal to all the flash chips on that SIMM is low enabling the protect function which can be utilized through program control. The 28F016SA flash chips have a LOCK BLOCK COMMAND which when performed will write protect individual blocks within the chip when the WP signal is low.

2.13 CONTROL / STATUS REGISTER

The CSR is accessible from the VMEbus using Short IO Space Modifiers 29 and 2D hex. The CSR can be used to control user selectable options and to perform an erase board function. When /SYSRESET is applied to the board, the CSR register is loaded with the configuration of the USER selectable jumpers. Only data bits D0,D1,D2,D3, are used. Data bits D4 through D8 are read only and indicate whether the unit has firmware supporting 28F016 and 28F032(all ones), or 28F160 and 28F320 (all zeros).

CSR BITS		STATE		FUNCTION
D0	D1	D2	D3	
0	X	X	X	no write functions or erase functions allowed
1	0	X	X	Program write functions allowed. 32 bit write single cycle only. All other write cycles no response, bus timeout.
1	1	X	X	Internal state write/erase functions allowed. 32 bit single/block write,64 bit block write cycles allowed.All other write cycles no responce,bus timeout. Internal state machine controls flash write and erase functions. Locations written to must have been previously erased to ensure stored data integrity
1 to 1	1 to 1	1 to 1	0 to 0	Initiates erase memory state machine. Results in the erase of the entire memory array. Indicated by busy LED on. Takes about 50 seconds. During this time any access to the CI-VFLASH will result in no responce, bus timeout.

TABLE 2.1 SUMMARY CSR USE

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3 USE AND OPERATION

3.1 USE

The CI-VFLASH is a high density, nonvolatile, in-circuit rewritable storage device. It can be used in any application where high speed read access is required along with inherent nonvolatility. The in-circuit rewritability makes the CI-VFLASH a prime candidate for applications where data must be updated frequently replacing the use of less efficient EPROM or EEPROM.

The CI-VFLASH utilizes 28F16SA or 28F032SA, or equivalent flash memory devices. These flash devices are similar to EEPROM in that an erase sequence must be performed prior to writing. Unlike EEPROM these devices offer much higher densities at lower power, with much lower cost. The trade-off is EEPROM is byte erasable, where flash devices are only block erasable . The chip block size is 64 kbytes. The CI-VFLASH supports a 64bit word length for VME64 applications. 4 28F016SA or 28F032SA's are accessed at once in 16 bit mode. Therefore, the minimum system block size that can be erased when a write is required is 256 kbytes. This means when a location needs to be updated with new data, the entire 256 kbyte block where thedata resides must first be stored elsewhere. The 256 kbyte block must then be erased. Finally, the 256 Kbyte block with new data must be written back.

Write and erase functions to Flash memory require a sequence of commands to the Flash chips themselves. These commands are performed under software code designed for the specific end user application of the CI-VFLASH. The CI-VFLASH has an internal state machine that when enabled through a start-up configuration or a write to the onboard CSR can control writes and board erase functions. This feature can simplify or eliminate end user software code depending on the application.

With the internal state machine enabled, a write to Flash memory locations can be performed by standard 32bit VME write/block write or 64bit VME64 write/block write, provided the locations had been previously erased.

Also the total flash memory contained on the CI-VFLASH can be erased by a simple 3 cycle write sequence to the on board CSR. Block erase must still be performed through software control when required.

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3.2 OPERATION

The CI-VFLASH performs 8, 16, 24, 32 or 64 bit data READS as described in the VMEbus specification. WRITES are performed according to CSR control bits described in section 2 to allow the most flexibility to the user. Writing can be controlled through standard Flash program control (PROGRAM WRITE), or handled by built in state machines (INTERNAL WRITE) contained on the unit.

VMEbus Address selection for memory cycles is either 24 or 32 bits depending on the Address Modifiers presented. Address bits A20-A31 are decoded for each type of cycle. If A24 Address Modifiers are used, the user must insure that the upper address lines are terminated in a state that will select the board.

Since Block Transfers (BLT) are used for maximum data throughput, only 32 and 64 bit wide BLT transfers are supported.

BLT cycles use a proprietary Memory Management Scheme that allows fast cycle times on the VMEbus. Data is available for the Master to read before the Master requests the data. DTACK is driven within 35 ns allowing the Master to digest the data and prepare for the next cycle. Note that this access time is the same for all cycles within a Block Burst. This allows synchronous cycles after the master receives the first acknowledge from the Memory.

Data is latched for both read and write cycles. The Chrislin Chip Set includes SWAP buffers that align 8, 16, and 32 bit data to the internal 64 bit data word.

Because of the programmable nature of the internal state machines, the CI-VFLASH could easily be modified to respond in various MASTER/SLAVE environments. Chrislin supplies custom configurations for many customers.

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3.2.1 PROGRAM WRITE MODE OPERATIONS

When in PROGRAM WRITE MODE as defined in section 2.9 the CI-VFLASH requires program control to perform all functions of erase and write. The CI-VFLASH utilizes a 28F016SA or 28F032SA or equivalent depending on the option size. The basic COMMAND DEFINITIONS are listed in table 3.1 with a more detailed list in Appendix B. For a complete description of all command and programing information refer to a 28F016SA or 28F032SA or equivalent specification. The CI-VFLASH utilizes the flash chips in 16 bit mode. Only 32bit VME write cycles are allowed when in program write mode. Two flash chips are accessed in any given cycle. The memory array is organized in groups of two flash chips of 1meg by 16 bits.

Because the chips are used in 16 bit mode, when writing commands only data bits D0 through D7 and D16 through D23 have command information. Bits D8 through D15 and D24 thru D31 are don't care bits. For example: To write 12345678 hex to location 10000000 hex, the programer would first write xx40xx40 hex to location 10000000 hex followed by a write of 12345678 hex to location 10000000. Then monitor the chips CSR's by reading the location 10000000 until completion bit's are received xx80xx80. Then write xxFFxxFF hex to location 10000000 hex to place the chips back in read mode. Where xx above are don't care bits.

The 28F016SA and 28F032SA flash chips are organized in 32 32K x 16 bit blocks. A read or a write to a single location of 32 bits addresses two chips and alternating locations ping pong between two SIMM modules. Therefore, when performing block commands such as BLOCK ERASE or LOCK BLOCK the minimum contiguous address space that can be erased or lock is 256KBYTEs. The BLOCK COMMAND must be performed at two consecutive longword locations. All program commands must be performed by 32bit longword write operations. The user can program down to chip level by only performing the command on the lower or upper 16 bits of the longword , but for block operations this will result in every 4th 16bit location of a 256kbyte block having the operation performed.

The relationship between block and chip commands and memory space affected is described in table 3.2.

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TABLE 3.1

COMMAND note	OPER	ADDR	DATA	OPER ADDR DATA
Read Array 2	LWW	AA	XXFFXXFFH**	Read AA AD
Read CSR* 1	LWW	AA	XX70XX70H	Read AA XXCDXXCDH
Clear CSR*	LWW	AA	XX50XX50H	
Word Write	LWW	WA	XX40XX40H	LWW WA WD
Block Erase /Confirm	LWW	BA	XX20XX20H	LWW BA XXD0XXD0H
Erase All Unlocked Blocks/Confirm 3	LWW	AA	XXA7XXA7H	LWW AA XXD0XXD0H
Lock Block /Confirm	LWW	BA	XX77XX77H	LWW BA XXD0XXD0H

notes:
1. The CSR* is automatically available after device enters data write, or erase operations. Csr bit 7 is done bit "1" is done. Bits 6-3 are status bits normally read as "0". Bits 2-0 are not used , read "0".
2. After a command sequence is completed a Read Array command must be issued to place the unit back into read mode.
3. 28F016 and 28F032 chip erase command is A7, 28F160 and 28F320 chip erase command is 30.

ADDRESS	DATA	OPER
AA = any longword address BA = any longword block address WA= any longword write address X = don't care	MD = memory data CD = csr data WD = write data H = preceeding is in hexadecimal	LWW=longword write

* Refers to chip CSR not Board CSR.

** The comand codes are in data bits d0-d7 & d16-d23 of the longword. Two Flash chips are accessed in parrallel for the 32 bit longword. One for data bits d0-d15 and the other for data bits d16-d31.

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TABLE 3.2
RELATIONSHIP OF FLASH BLOCK AND CHIP COMMANDS TO MEMORY SPACE

COMMAND	WHERE TO PERFORM COMMAND OPERATION	MEMORY SPACE AFFECTED
block erase lock block	2 consecutive longword locations	256 kbytes
all chip commands ie:erase all blocks	2 consecutive longword locations	8 megabytes

3.2.2 INTERNAL WRITE MODE OPERATIONS

When in INTERNAL WRITE MODE as described in section 2.9, program write operations are disabled. In INTERNAL WRITE MODE the CI-VFLASH can be erased by a write sequence to the Board CSR, or manual erase can be performed using a front panel switch (see section 2.10). The erase function erases the entire unit only (all memory on the Board is erased), no block erase is allowed. In INTERNAL WRITE MODE memory writes are performed on longwords 32bit, or double longwords 64bit only. Memory writes are performed with standard VME, VME64 write cycles. Written locations must have been previously erased. The internal state machine performs all the program sequences required for flash write transparent to the user. Access and cycle time for writes in this mode are 8us max.

Please note that Flash memory is written to by flipping bits from a "1" to a "0" at bit locations required. It assumes the location is all "1's" prior to the write which is the erased condition of the location after an erase has been performed. A memory location can be written only once to insure proper data. It should be erased prior to the next write to the same location. If a write is performed on a location already written to, only bits that were a "1" prior to the write can be assured of the proper state. Bits that were a "0" prior to the write will remain in that state.

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3.2.3 WRITE PROTECTION TECHNIQUES

The user of flash memory must protect from unintentional writes and erase to the memory array. The CI-VFLASH allows many levels of write protection to the user, from total hardware disable / enable to various software controlled disable / enable. Options to the user are summarized in TABLE 3.3

TABLE 3.3

WRITE PROTECTION DESCRIPTION	SHUNT POSITIONS			
	CSREN	CR0	CR1	WP
Hardware write protect. No writes or erase can be performed under any conditions	out	in	in	x
Write protection under software control. Internal state machines for write and erase disabled. No individual SIMM WP.	out	out	in	out
Write protection under software control. Internal state machines for write and erase disabled. Individual SIMM WP.	out	out	in	in / out
Write protection under internal state machines No external software control allowed. If SIMM's programed for WP previously are protected.	out	out	out	in/ out
Write protection and modes can be changed by writing to CSR for use as needed by user.	in	in/ out	in/ out	in/ out

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4.0 INTERFACE PINOUTS

4.1 CI-VFLASH P1 PIN ASSIGNMENTS

PIN	ROW A	ROW B	ROW C
1	D00	--	D08
2	D01	--	D09
3	D02	--	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	--	/BG3IN	--
11	GND	/BG3OUT	_
12	/DS1	--	/SYSRESET
13	/DS0	--	/LWORD
14	/WRITE	--	AM5
15	GND	--	A23
16	/DTACKAM0	A22	
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	--	A17
22	/IACKOUT	--	A16
23	AM4	GND	A15
24	A07	--	A14
25	A06	--	A13
26	A05	--	A12
27	A04	--	A11
28	A03	--	A10
29	A02	--	A09
30	A01	--	A08
31	--	+5VSTBY	+12v
32	+5V	+5V	+5V

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4.2 CI-VFLASH P2 PIN ASSIGNMENTS

PIN	ROW A	ROW B	ROW C
1	-	+5V	-
2	-	GND	-
3	-	--	-
4	-	A24	-
5	-	A25	-
6	-	A26	-
7	-	A27	-
8	-	A28	-
9	-	A29	-
10	-	A30	-
11	-	A31	-
12	-	GND	-
13	-	+5V	-
14	-	D16	-
15	-	D17	-
16	-	D18	-
17	-	D19	-
18	-	D20	-
19	-	D21	-
20	-	D22	-
21	-	D23	-
22	-	GND	-
23	-	D24	-
24	-	D25	-
25	-	D26	-
26	-	D27	-
27	-	D28	-
28	-	D29	-
29	-	D30	-
30	-	D31	-
31	-	GND	-
32	-	+5V	-

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APPENDIX A

PROGRAM TECHNIQUES FOR THE CI-VFLASH

The following simple pseudo code is presented to give the user ideas for programming erase and write functions for the CI-VFLASH.

*The following code controls block erase of a single 256 Kbyte block on the CI-VFLASH. A1 will contain the beginning address of the block to be erased. A0 will contain the address of the board CSR register.

```
        move.l      "CSR address",A0        *load A0 with board CSR address
        move.w       #01,(A0)               * ensure board in program write mode
                                            * this code not necessary if state of board known to be
                                            *program write mode

        move.l       "beg address of block",A1 * load A1 with block address to be erased
        move.l      A1,A2                   * load A2 with block address to be erased
        add.l       #4,A2                   *load A2 with next longword location
        move.l      #$00200020,(A1)         * load 1st two chips of block with erase command
        move.l      #$00d000d0,(A1)         *load 1st two chips of block with confirm command
        move.l      #$00200020,(A2)         * load 2nd two chips of  block with erase command
        move.l      #$00d000d0,(A2)         *load 2nd two chips of block with confirm command
erasewait:
        move.l      (A1),D0
        move.l      (A2),D1
        cmp.l       #$00800080,D0           * wait until chips indicate erase complete
        bne         erasewait
        cmp.l       #$00800080,D1
        bne         erasewait

        move.l      #$00ff00ff,(A1)         *places flash chips back to read mode. Only required
        move.l      #$00ff00ff,(A2)         * when no further writes or erase  required to chips.
```

* The following code controls board erase of the CI-VFLASH using the CSR board erase sequence. A0 will contain the board CSR register address.

```
        move.l      "CSR address",A0        *load A0 with board CSR address
        move.w      #$07,(A0)               * start erase board command
        move.w      #$0f,(A0)               * confirm erase board command
        move.w      #$07,(A0)               * second confirm erase board command

80 secondwait loop:
        * place wait loop here.  CI-VFLASH will not respond during erase sequence, bus timeout will
         occur. After wait user can verify all FF in all locations indicating erased state, or can begin writing
         new data to the board.
```


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*The following code controls a longword write to a single CI-VFLASH location under program write mode. A0 will contain the address of the board CSR register. The A1 register will contain the address to be written. The D0 register will contain the data to be written.

```
            move.l      "CSR address",A0        *load A0 with board CSR address
            move.w      #01,(A0)                * ensure board in program write mode
            move.l      "address to write",A1   * load A1 with address to be written
                                                * this code not necessary if  state of board known to be
                                                *program write mode

            cmp.l       #$ffffffff,(A1)         * checks to make sure the address is erased and in read
            bne         errorrte                *mode, jumps to error routine if not
                                                *This code only added for protection not necessary if state
                                                *of board known

            move.l      "data to write",D0      *load D0 with data to write
            move.l      #$00400040,(A1)         *load address with write command
            move.l      D0,(A1)                 *write data to location

writewait:
            move.l      (A1),D1                 *wait until chip indicates write complete
            cmp.l       #$00800080,D1
            bne         writewait

            move.l      #$00ff00ff,(A1)         *place chips back in read mode. Only required if no
                                                *further writes required.

errorrte:   *place error routine here if required
```

*The following code controls a longword write to a single CI-VFLASH location under internal write mode. A0 will contain the address of the board CSR register. The A1 register will contain the address to be written. The D0 register will contain the data to be written.

```
            move.l      "CSR address",A0        *load A0 with board CSR address
            move.w      #11,(A0)                * ensure board in internal write mode
            move.l      "address to write",A1   * load A1 with address to be written
                                                * this code not necessary if state of board known to be
                                                * internal write mode

            cmp.l       #$ffffffff,(a1)         * checks to make sure the address is erased and in read
            bne         errorrte                *mode, jumps to error routine if not
                                                *This code only added for protection not necessary if state
                                                *of board known
            move.l      "data to write",d0      *load d0 with data to write
            move.l      d0,(a1)                 *write data to location

            * NOTE: NO WAIT LOOP REQUIRED
```


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APPENDIX B
COMPLETE COMMAND DEFINITIONS

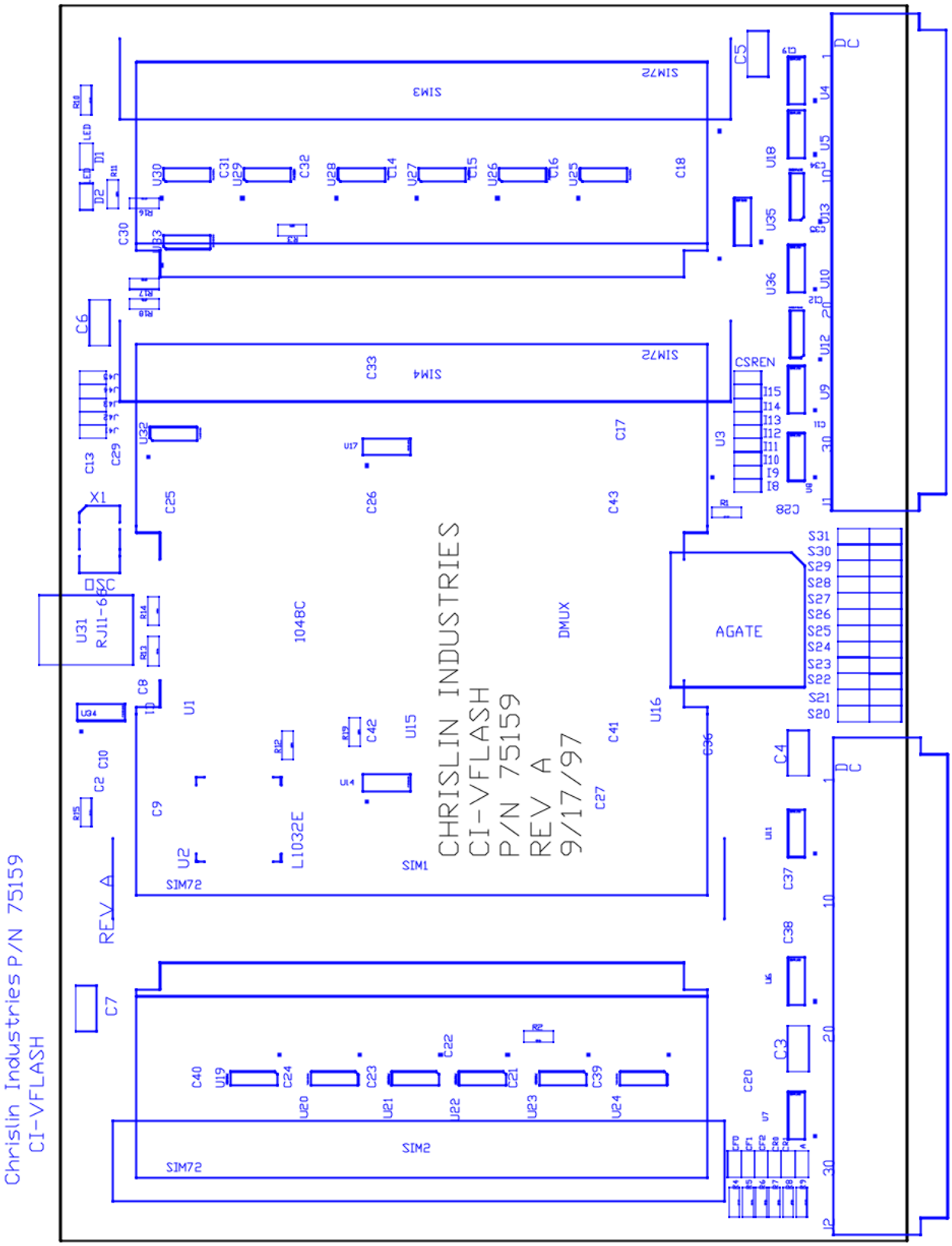
Command	First Bus Cycle			Second Bus Cycle			Third Bus Cycle			notes
	Oper	Addr	Data	Oper	Addr	Data	Oper	Addr	Data	
Read Array	WRITE	X	FFH	READ	AA	AD				
Intelligent Identifier	WRITE	X	90H	READ	IA	ID				
Read Comp. Status Reg	WRITE	X	70H	READ	X	CSRD				
Clear Status Reg.	WRITE	X	50H							
Write	WRITE	X	40H	WRITE	WA	WD				
Alternate Write	WRITE	X	10H	WRITE	WA	WD				
Block Erase/Confirm	WRITE	X	20H	WRITE	BA	D0H				
Erase Suspend/Resume	WRITE	X	B0H	WRITE	X	D0H				
Read Extended Status Reg.	WRITE	X	71H	READ	RA	GSRD BSRD				1
Page Buffer Swap	WRITE	X	72H							2
Read Page Buffer	WRITE	X	75H	READ	PA	PD				
Single Load to Page Buf.	WRITE	X	74H	WRITE	PA	PD				
Sequential Load to Page Buffer	WRITE	X	E0H	WRITE	X	WC	WRITE	X	00H	3,4
Page Buffer Write To Flash	WRITE	X	0CH	WRITE	X	WC	WRITE	WA	00H	4
Lock Block/Confirm	WRITE	X	77H	WRITE	BA	D0H				
Upload Staus Bits	WRITE	X	97H	WRITE	X	D0H				
Upload Device Info	WRITE	X	99H	WRITE	X	D0H				
Erase all unlocked blocks	WRITE	X	A7H	WRITE	X	D0H				5
Abort	WRITE	X	89H							

ADDRESS
BA= Block Address
PA=Page Buffer Address
RA=Extended Reg Address
WA=Write Address
X = Don't Care

DATA
AD=Array Data
PD=PageBuffer Data
BSRD= BSR Data
GSRD= GSR Data
WC=Word Count
WD=Write Data

NOTES
1. RA can be the GSR or any BSR address. Detail explanation beyond the scope of this manual. Consult chip specifications or factory for more detail if use required.
2. This command allows the user to swap between 2 available 256 byte page buffers
3. PA and PD (whose count is given in cycles 2 and 3) are supplied starting in the 4th cycle not shown
4. WC=00h corresponds to a word count of 1, 7Fh corresponds to max word count of 128.
5. The erase all block command for 28F016 and 28F032 is A7 followed by D0, erase all block command for 28F160 and 28F320 is 30 followed by D0.

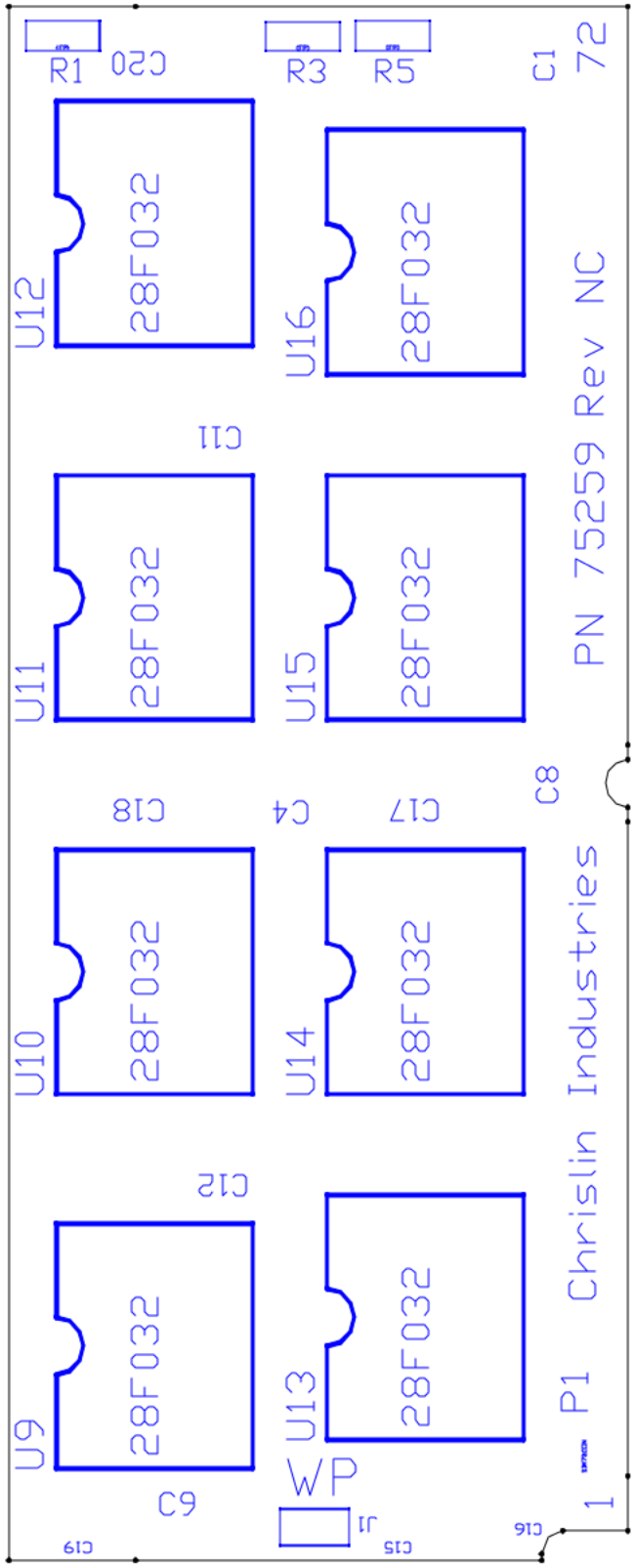
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