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Chrislin Industries, Inc.

CI-VME40

TECHNICAL MANUAL

High-Speed
VMEbus/VSB
DUAL-PORTED
DYNAMIC MEMORY

Release 3.01
Oct 1995

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1.1 INTRODUCTION

This manual describes the elements of operation and installation of the CI-VME40 dynamic memory module for the VMEbus and VSB.

1.2 THE MEMORY MODULE

The CI-VME40 is available in five option sizes as follows:

OPTION	MEMORY CAPACITY	MODULE
4 MEG	1024Kx32 bits with parity	CI-VME40/4
8 MEG	2048Kx32 bits with parity	CI-VME40/8
16 MEG	4096Kx32 bits with parity	CI-VME40/16
32 MEG	8192Kx32 bits with parity	CI-VME40/32
64 MEG	16384Kx32 bits with parity	CI-VME40/64
128 MEG	32768Kx32 bits with parity	CI-VME40/128

1.3 CI-VME40 MEMORY DESCRIPTION

The CI-VME40 is an high-density, high-speed Block transfer Dram Memory board with a Dual-Port interface that allows memory cycles to be performed to both the VSB VMEbus simultaneously. Byte Parity Error Detection circuitry is provided for data integrity.

1.4 OPERATIONAL FEATURES

The CI-VME40 performs all memory functions according to VMEbus REV C.1 and the VSB REV C protocols for byte, word, and long word operations (8, 16, 24 and 32 bit data transfers).

Read-Modify Write cycles, Unaligned transfers, Block transfers, Address Pipelining, Locked Bus cycles and Address Only cycles are all supported.

Starting and Ending Address selection may be selected for each port (VMEbus and VSB) on 512KByte boundaries within any 128 Megabyte partition.

A Control Status Register (CSR) is provided, and responds to a 16 bit SHORT I0 Address. CSR functions include ERROR ENABLE, ERROR DETECT.

Block transfer cycles are highlighted as the CI-VME40's strongest feature. Block Cycles are performed on 32 bits wide locations. Chrislin uses a proprietary cycle management system that delivers access and cycle times that are not available elsewhere in the industry.

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Block transfer lengths of up to 1024 bytes (256 32-bit transfers) may be performed on either bus. Transfers may not cross 1024 byte boundaries. The VMEbus master is responsible for ending a Block Transfer. The VSB master will be notified by the deassertion of AC during the last cycle.

VSB Cycles are initiated on PAS to absorb the delay between PAS and DS. Refresh cycles are performed for PAS only cycles.

LED indicators for VME CYCLE, VSB CYCLE (green) and parity error status (red) are mounted on the front panel.

1.5 POWER REQUIREMENTS

The CI-VME40 memory module requires only the +5 volt supply from the VMEbus/VSB backplane. See the general specifications on page 5 for current requirements.

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1.6 GENERAL SPECIFICATIONS

CAPACITY:	128MB, 64MB, 32MB, 16MB, 8MB or 4MB
WORD SIZE:	8, 16, 24 or 32 bits.
ADDRESSING:	MEMORY: 32 or 24 bits, 4 Gbytes maximum. Selectable on 512 Kbyte boundaries. VME and VSB configured independently. CSR: 16 bits, selectable on 256 byte boundaries using VMEbus SHORT I/O.
MODES OF OPERATION:	MEMORY: READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS, UNALIGNED TRANSFERS. CSR: READ, WRITE
CONTROL STATUS REGISTER:	ERROR ENABLE ERROR DETECT.
VME REV C COMPATIBILITY:	SLAVE, A16, A24, A32, D8, D16, D24, D32, RMW, BLT, UAT, ADO
ADDRESS MODIFIERS:	Responds to AM Codes 3F, 3E, 3D, 3B, 3A, 39, 0F, 0E. 0D, 0B, 0A, 09, 2D and 29. AM Codes are programmable.
VSB REV C COMPATIBILITY:	SLAVE, D32, A32, SAS, ADO, BLT(32).
REFRESH:	Internal, Distributed.
INDICATORS	Parity Error, VME Cycle, VSB Cycle LEDs.
POWER REQUIREMENTS	+5V 32MB 64MB 128MB Typical 2.3A 2.4A 2.6A Maximum 2.5A 2.6A 3.0A
OPERATING TEMP:	0 TO + 70 DEG C NON-CONDENSING
FORM FACTOR:	6 U
SIZE:	160mm X 233.35mm

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1.7 SWITCHING CHARACTERISTICS

VMEbus Switching Characteristics

Parameter	Description	Min	Notes
SCRA	Single Cycle Read Access Time	140ns	1
SCWA	Single Cycle Write Access Time	90ns	1
SCDV	Single Cycle Data Valid Setup	10ns	
SCCT	Single Cycle Time	195ns	
AOT	Access Turn Off Time	20ns	
BCAT	Block Cycle Access Time	20ns	
BCCT	Block Cycle Time	84ns	
BCDV	Block Cycle Data Valid Setup	10ns	

VSB Switching Characteristics

Parameter	Description	Min	Notes
SCRA	Single Cycle Read Access Time	20ns	2
SCWA	Single Cycle Write Access Time	50ns	2
SCDV	Single Cycle Data Valid setup	10ns	
SCCT	Single Cycle Time	195ns	
AOT	Access Turn Off Time	20ns	
BCAT	Block Cycle Access Time	20ns	
BCCT	Block Cycle Time	84ns	
BCDV	Block cycle Data Valid Setup	10ns	

Notes:

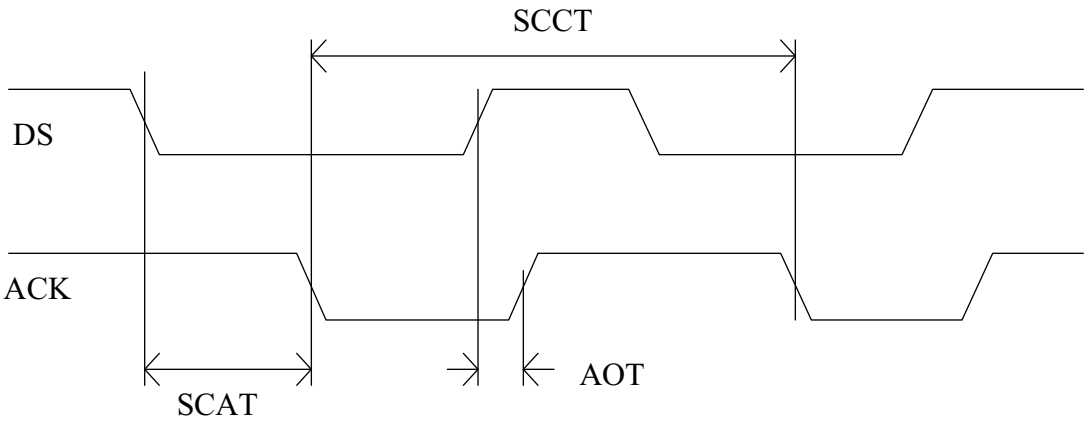
1. Access times are measured from data strobes and inside bus drivers and receivers.

2. VSB access times measured from data strobe given a PAS to DS delay of 130ns. Minimum access time from PAS is the same as that of the VMEbus.

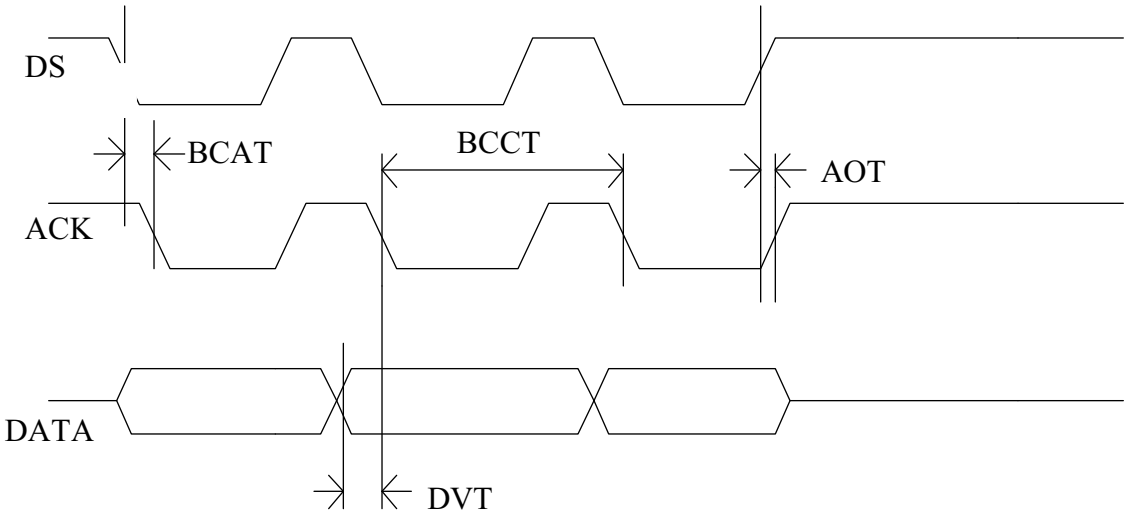
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ACCESS CYCLE TIMING

SINGLE TRANSFER CYCLE



BLOCK TRANSFER CYCLE



CHRISLIN	
CI-VME40	
73058 DRAWING NO	RELEASE 1.0 REV
	3/01/90 DATE

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2. HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section describes the handling precautions and the procedure of installation of the CI-VME40 memory modules.

2.2 HANDLING PRECAUTIONS

The memory IC's on the CI-VME40 module are MOS devices. They are damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC's. Avoid unnecessary handling. When handling IC's wear cotton rather than synthetic clothing.

The CI-VME40 uses a Mezzanine Memory Array (Piggy-Back Board) for added density. The Array does not need to be removed for board configuration. If the Array needs to be removed or installed, care needs to be taken not to damage the mating connector. Before applying pressure to seat the connector, examine that all pins are aligned.

2.3 MEMORY ADDRESS SELECTION

The CI-VME40 has an individually selectable START and END address with 512K byte granularity in one 128 megabyte partition (32 bit address). The VMEbus addresses may be selected independent from the VSB addresses. Refer to drawing 73052 for shunt positions.

To make the address selection, first select the 128 megabyte partition at shunt areas S27 to S31 (VMEbus) and J27 to J31 (VSB). Note that shunt labels correspond to address bits. As in all address shunt areas, an installed shunt represents a "0" or LOW on the bus where a removed shunt represents a "1" or HI on the bus. Refer to Table 2.3.1 for examples..

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2.3.1 PARTITION ADDRESS EXAMPLES

S31 J31	S30 J30	S29 J29	S28 J28	S27 J27	VMEbus PARTITION VSB PARTITION
I	I	I	I	I	00000000 - 07FFFFFF
I	I	I	I	O	08000000 - 0FFFFFFF
I	I	I	O	I	10000000 - 17FFFFFF
I	I	O	I	I	20000000 - 27FFFFFF
I	O	I	I	I	40000000 - 47FFFFFF
O	I	I	I	I	80000000 - 87FFFFFF
O	O	O	O	O	F8000000 - FFFFFFFF
I	I	I	I	I	DEFAULT CONFIGURATION

I = SHUNT IN
O = SHUNT OUT

START and END address offsets within the previously selected partition uses shunt areas S19 - S26 (START address) and E19 - E26 (END address for the VMEbus and shunt areas J19 - J26 (START address) and K19 - K26 (END address for the VSB. This can be thought of a deselection of some portion of the partition. The starting and ending selection can move either of the boundaries from the selected partition window. If all of the starting jumpers are installed and all of the ending jumpers are removed then the complete 128 meg partition window will be selected.

Note that shunt labels correspond to address bits. As in all address shunt areas, an installed shunt represents a "0" or LOW on the bus where a removed shunt represents a "1" or HI on the bus. Refer to Table 2.3.2 for examples.

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2.3.2 STARTING AND ENDING ADDRESS EXAMPLES

S26 J26	S25 J25	S24 J24	S23 J23	S22 J22	S21 J21	S20 J20	S19 J19	VME START ADDRESS VSB START ADDRESS
I	I	I	I	I	I	I	I	00000000 (HEX)
I	I	I	I	I	I	I	O	00080000
I	I	I	I	I	I	O	I	00100000
I	I	I	I	I	O	I	I	00200000
I	I	I	I	O	I	I	I	00400000
I	I	I	O	I	I	I	I	00800000
I	I	O	I	I	I	I	I	01000000
I	O	I	I	I	I	I	I	02000000
O	I	I	I	I	I	I	I	04000000
O	O	I	I	I	I	I	I	06000000
O	O	O	I	I	I	I	I	07000000
O	O	O	O	O	O	O	O	07800000
I	I	I	I	I	I	I	I	START DEFAULT

E26 K26	E25 K25	E24 K24	E23 K23	E22 K22	E21 K21	E20 K20	E19 K19	VME END ADDRESS VSB END ADDRESS
I	I	I	I	I	I	I	I	0007FFFF (HEX)
I	I	I	I	I	I	I	O	000FFFFF
I	I	I	I	I	I	O	O	001FFFFF
I	I	I	I	I	O	O	O	003FFFFF
I	I	I	I	O	O	O	O	007FFFFF
I	I	I	O	O	O	O	O	00FFFFFF
I	I	O	O	O	O	O	O	01FFFFFF
I	O	O	O	O	O	O	O	03FFFFFF
O	O	O	O	O	O	O	O	07FFFFFF
I	I	I	I	I	O	O	O	4MB END DEFAULT
I	I	I	I	O	O	O	O	8MB END DEFAULT
I	I	I	O	O	O	O	O	16MB END DEFAULT
I	I	O	O	O	O	O	O	32MB END DEFAULT
I	O	O	O	O	O	O	O	64MB END DEFAULT
O	O	O	O	O	O	O	O	128MB END DEFAULT

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2.4 24-BIT ADDRESS SYSTEMS

24 Bit address decoding is supported if the CI-VME40 is configured to decode 24 bit Address Modifiers. See section 2.5.

2.5 VMEbus ADDRESS MODIFIERS

The CI-VME40 may respond to different combinations of address widths and VMEbus address modifier codes. Shunt area C selects whether 32 bit only modifiers are to be responded to, or 32 or 24 bit modifiers will get a response. See User Option Section.

2.6 VSB ADDRESS SPACES

The CI-VME40 can be configured to respond to either VSB SYSTEMS ADDRESS SPACE or VSB ALTERNATE ADDRESS cycles. The board is shipped to respond to SYSTEM SPACE. The user must contact the factory for a preprogrammed PAL if ALTERNATE SPACE is to be used.

2.7 DUAL-PORT ADDRESS OVERLAPPING

Although each bus can be configured independently, the lower Bus addresses are used to address the memory array. This will cause certain addresses on one bus to access other addresses on another bus. Care must be taken when choosing bus addresses. For example a 4MB memory board is configured to respond to VMEbus addresses 100000h to 500000h and VSB address 0h to 400000h, the following overlap will exist:

VMEbus	VSB
400000 - 500000	000000 - 100000
100000 - 200000	100000 - 200000
200000 - 300000	200000 - 300000
300000 - 400000	300000 - 400000

Notice that the memory board has a 4MB redundancy. An 8MB board would similarly have an 8MB redundancy.

2.8 BUS INTERFACE DISABLE

If either the VMEbus or VSB Bus interface is to be disabled, simply set the starting offset greater than the ending offset.

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2.9 CSR ADDRESS SELECTION

The CI-VME40 CSR is an 8 bit read/write register. The CSR is selected by a VMEbus 16 bit SHORT SUPERVISORY (2D) or SHORT NON-PRIVILEGED ACCESS (29) Address Modifier code. Address selection uses shunt areas I8 through I15 which places the CSR on 256 byte boundaries. Note that shunt labels correspond to address bits. An installed shunt represents a "0" or LOW on the bus where a removed shunt represents a "1" or HI on the bus. Refer to Table 2.9.1 for examples.

2.9.1 CSR ADDRESS SELECTION EXAMPLES

I15	I14	I13	I12	I11	I10	I9	I8	ADDRESS
I	I	I	I	I	I	I	I	0000 - 00FF
I	I	I	I	I	I	I	0	0100 - 01FF
I	I	I	I	I	I	O	I	0200 - 02FF
I	I	I	I	I	O	I	I	0400 - 04FF
I	I	I	I	O	I	I	I	0800 - 08FF
I	I	I	O	I	I	I	I	1000 - 10FF
I	I	O	I	I	I	I	I	2000 - 20FF
I	O	I	I	I	I	I	I	4000 - 40FF
O	I	I	I	I	I	I	I	8000 - 80FF
O	O	O	O	O	O	O	0	FF00 - FFFF
I	I	I	I	I	I	I	I	DEFAULT CONFIGURATION

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2.10 USER OPTIONS

The following USER OPTIONS are shunt selectable. Refer to drawing 73052 for shunt positions. The CSR (Control Status Register) is initialized to the shunt selections during SYSRESET. The CSR configuration may then be changed by program control by writing to CSR bits D0-D3.

2.10.1 USER CONFIGURED SHUNT LOCATIONS

SHUNT AREA	POSITION	DESCRIPTION	
A	IN	Standard Access Time	
A	OUT	Fast Access Time	
B		Not Used	
C	OUT	Responds to only 32 bit Modifiers	
C	IN	Responds to 24 or 32 bit Modifiers	
D		FACTORY SET	
E		FACTORY SET	
F		FACTORY SET	
G	IN	Error Disabled	CSR D2 = 0
G	OUT	Error Enabled	CSR D2 = 1
H		Not Used	
I		Not Used	
J		Not Used	

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2.11 ERROR ENABLE

Byte Parity is always checked on any type of read cycle. The ERROR LED will light and stay lit whenever an error occurs. Error trapping is controlled by the user. Shunt area G is used to enable/disable error trapping. By installing the shunt at area G, DTACK/ACK will always be asserted in response to a valid memory cycle. Removing the shunt will allow BERR/ERR to be asserted whenever a parity error occurs.

Note that if a location is read before it is initialized, a false error will be indicated. If error status is to be monitored, system software needs to initialize memory.

2.12 VSB ADDRESS SPACE

The CI-VME40 can respond to either VSB SYSTEM Space cycles or ALTERNATE Space Cycles. The board is shipped with SYSTEM Space decode logic. The user must contact the factory for a preprogrammed PAL to decode ALTERNATE Space.

2.13 24/32 BIT VME ADDRESS SELECT

Area C selects whether the CI-VME40 will respond to only 32 bit Address modifiers or 24 bit and 32 bit modifiers. If the CI-VME40 will be accessed by a 32 address bit master use the 32 bit configuration. If a 24 bit master will access the board in the 24/32 bit setting should be used.

Some problems have been noticed over the years that some controller boards place buffer space in the 24 bit address modifier space. If the memory board is configured to respond to both 24 and 32, it may redundantly respond to the controllers address space.

If you need to place the CI-VME40 into 24 bit address space take care in setting up your bus addresses for all boards. If you are going to access the board with 32 bit address modifiers leave the shunt installed at area C.

2.14 BLOCK TRANSFER ACCESS SPEED

Area A selects the Block Transfer Access speed of the Memory. With this jumper installed, Block Transfer Access times are guaranteed to be at lease 30ns or greater. In this configuration, the AC signal is also guaranteed to occur prior to the ACK signal at the end of the Slave's address range.

With area A removed, the board will provide the fastest possible access time. This is typically 20ns.

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2.15 CONTROL / STATUS REGISTER

The CSR is accessible from the VMEbus side using Short IO Space Modifiers 29 and 2D hex. The CSR can be used to control user selectable options and to check the status of the Error LED.

2.16 ERROR DETECT CSR BIT

The red LED will be lit and D0 of the CSR will be a '1' when a parity error has occurred. This bit is cleared when /SYSRESET is asserted or a write cycle to the CSR is performed.

2.17 ERROR ENABLE CSR BIT

Error trapping is set at /SYSRESET time according to shunt area G. The CSR can be used to change the initial setting. When CSR bit D2 is set to a '1' error trapping is enabled. Clearing this bit disables error trapping.

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2.18 THEORY OF OPERATION

The CI-VME40 performs 8, 16, 24, or 32 bit data transfers as described in the VMEbus and VSB specifications. VMEbus Address selection for memory cycles is either 24 or 32 bits depending on the Address Modifiers presented. User definable AM codes is possible by reprogramming a PAL. Cycle types include READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS, UNALIGNED TRANSFERS, ADDRESS ONLY and ADDRESS PIPELINING.

VSB address selections always uses 32 address bits and responds to the SYSTEM or ALTERNATE ADDRESS SPACE. Cycle types include READ, WRITE, LOCK, BLOCK TRANSFERS, AND ADDRESS ONLY.

Refresh is internal and distributed. Refresh requests occur every 15 microseconds. AS or PAS only cycles perform refresh cycles and could be used to control refresh cycles in special applications. Refresh Cycles have the highest priority in the arbitrator but are postponed during BLOCK TRANSFERS. This allows uninterrupted BLOCK TRANSFERS. CAS before RAS Refresh cycles are implemented.

Since Block Transfers (BLT) are used for maximum data throughput, only 32 bits wide BLT transfers are supported. Speed and not flexibility was the design goal for the CI-VME40.

BLT cycles use a proprietary Memory Management Scheme that allows the fastest possible cycle times on the VME and VSB busses. Data is available for the Master to read before the Master requests the data. DTACK/ACK is driven within 20ns allowing the Master to digest the data and prepare for the next cycle. Note that this access time is the same for all cycles within a Block Burst. The CI-VME40 does not use caching or interleaving methods that usually result in two different access times. Typically boards that use this method have along access time for a normal cycle and a short access time for the cached or interleaved cycle. The CI-VME40 can perform back-to-back BLT cycles every 84ns!

Data is latched for both read and write cycles. The VMEbus interface includes SWAP buffers for D16 and D8 compatibility. A synchronized four grant arbitration system is used. Arbitration priorities rank as follows: Refresh requests, VSB requests, VMEbus request, and CSR requests. The VMEbus may lock out the VSB by performing READ-MODIFY-WRITE or BLOCK TRANSFER cycles. The VSB may lock out the VMEbus by asserting the LOCK signal and then perform any number of various cycles.

Because of the programmable nature of the internal state machines, the CI-VME40 could easily be modified to respond in various MASTER/SLAVE environments. For example a synchronous block transfer protocol could be implemented.

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3 SPECIAL APPLICATIONS

3.1 VMEbus READ MODIFY WRITE CYCLES

With the standard CI-VME40, RMW cycles take the lowest priority in the controller's state machines. VSB single cycles along with block transfer cycles on both busses take the highest priority.

To accommodate those customers who use external memory for semaphore processing, the CI-VME40 can be ordered with FAST RMW cycle support. This feature (at this time) disables the VSB interface. Block transfer cycles on the VMEbus are still supported.

The RMW cycle is characterized by a 150ns read access time followed by a 20ns write access time and a total cycle time of 350ns.

3.2 SYNCHRONOUS TRANSFERS

The CI-VME40 can be strobed in a synchronous manner during block transfers. The master must wait for the first acknowledge to come from the memory, after which synchronous transfers may follow at a 100ns rate (ignoring acknowledges from the memory). Faster rates have been achieved in this mode, but it is up to the user to verify successful operation.

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4 INTERFACE PINOUTS

4.1 CI-VME40 P1 PIN ASSIGNMENTS

PIN	ROW A	ROW B	ROW C
1	D00	--	D08
2	D01	--	D09
3	D02	--	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	--	/BG3IN	--
11	GND	/BG3OUT	/BERR
12	/DS1	--	/SYSRESET
13	/DS0	--	/LWORD
14	/WRITE	--	AM5
15	GND	--	A23
16	/DTACKAM0	A22	
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	--	A17
22	/IACKOUT	--	A16
23	AM4	GND	A15
24	A07	--	A14
25	A06	--	A13
26	A05	--	A12
27	A04	--	A11
28	A03	--	A10
29	A02	--	A09
30	A01	--	A08
31	--	+5VSTBY	--
32	+5V	+5V	+5V

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4.2 CI-VME40 P2 PIN ASSIGNMENTS

PIN	ROW A	ROW B	ROW C
1	VSBAD0	+5V	VSBAD1
2	VSBAD2	GND	VSBAD3
3	VSBAD4	--	VSBAD5
4	VSBAD6	A24	VSBAD7
5	VSBAD8	A25	VSBAD9
6	VSBAD10	A26	VSBAD11
7	VSBAD12	A27	VSBAD13
8	VSBAD14	A28	VSBD15
9	VSBAD16	A29	VSBAD17
10	VSBAD18	A30	VSBAD19
11	VSBAD20	A31	VSBAD21
12	VSBAD22	GND	VSBAD23
13	VSBAD24	+5V	VSBAD25
14	VSBAD26	D16	VSBAD27
15	VSBAD28	D17	VSBAD29
16	VSBAD30	D18	VSBAD31
17	GND	D19	GND
18	-	D20	GND
19	/DS	D21	GND
20	/WR	D22	GND
21	SPACE0	D23	SIZE0
22	SPACE1	GND	/PAS
23	/LOCK	D24	SIZE1
24	/ERR	D25	GND
25	GND	D26	/ACK
26	GND	D27	AC
27	GND	D28	/ASACK1
28	GA0	D29	/ASACK0
29	GA1	D30	/CACHE
30	GA2	D31	/WAIT
31	/BGIN	GND	-
32	-	+5V	/BGOUT

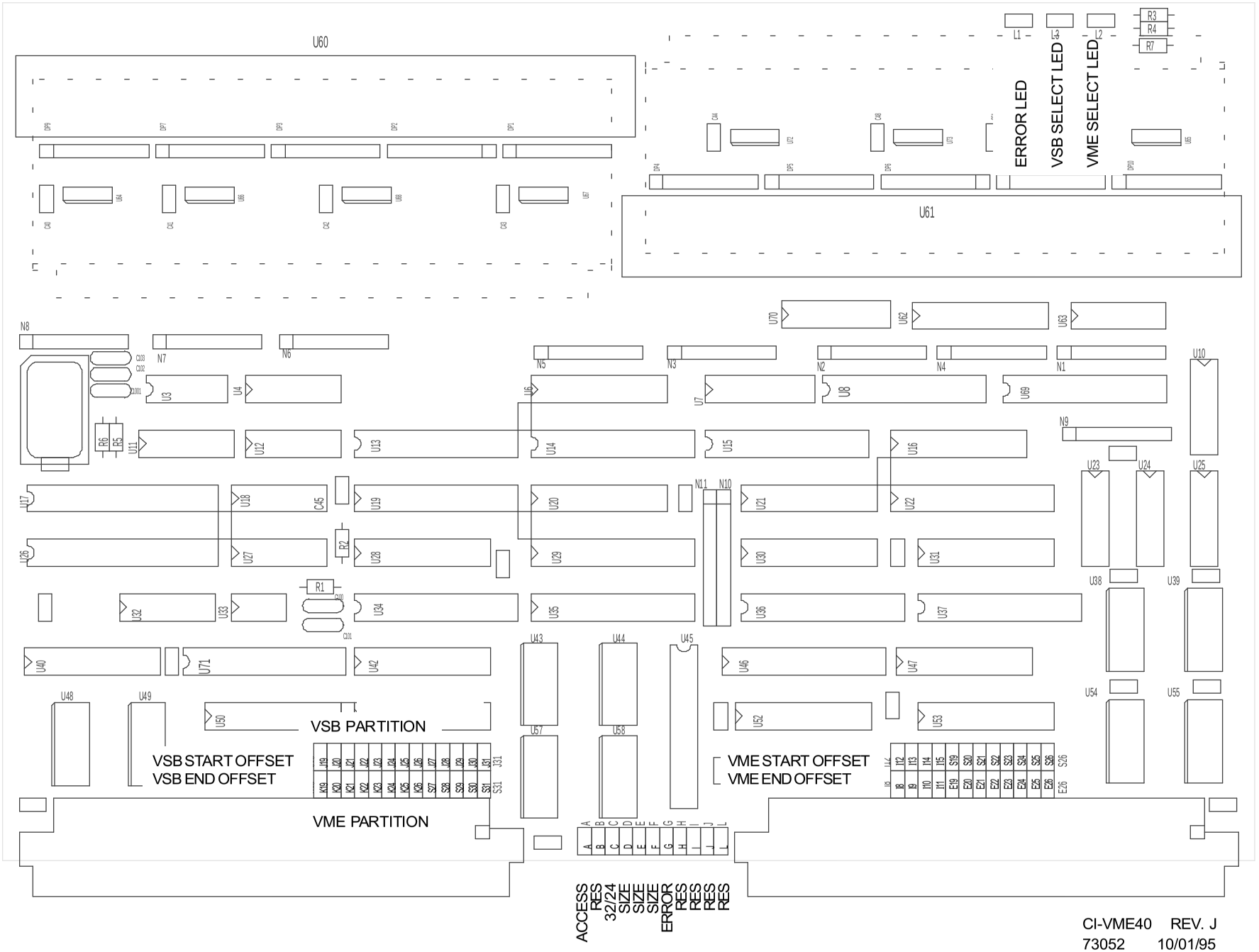
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4.3 CI-VME40 P3 PIN ASSIGNMENTS

1	GND	33	+5V
2	P3 IN	34	P0 IN
3	P3 OUT	35	P0 OUT
4	D31	36	D7
5	D30	37	D6
6	D29	38	D5
7	D28	39	D4
8	D27	40	D3
9	D26	41	D2
10	D25	42	D1
11	D24	43	D0
12	P2 IN	44	/CAS3
13	P2 OUT	45	/CAS2
14	D23	46	/CAS1
15	D22	47	/CAS0
16	D21	48	/RAS2
17	D20	49	/RAS3
18	D19	50	/WRITE
19	D18	51	A10
20	D17	52	A9
21	D16	53	A8
22	P1 IN	54	A7
23	P1 OUT	55	GND
24	D15	56	A6
25	D14	57	A5
26	D13	58	A4
27	D12	59	A3
28	D11	60	GND
29	D10	61	A2
30	D9	62	A1
31	D8	63	A0
32	+5V	64	+5V

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