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Chrislin Industries, Inc.

CI-VME4G

TECHNICAL MANUAL

HIGH-SPEED
VME64
VMEbus/VSB
DUAL-PORTED
DYNAMIC MEMORY

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1. GENERAL INFORMATION

1.1 INTRODUCTION

This manual describes the elements of operation and installation of the CI-VME4G dynamic memory module for the FPDP and VMEbus.

1.2 THE MEMORY MODULE

The CI-VME4G is available in seven option sizes as follows:

OPTION	MEMORY CAPACITY	MODULE
64 MEG	16,384Kx32 bits with parity	CI-VME4G/64
128 MEG	32,768Kx32 bits with parity	CI-VME4G/128
256 MEG	65,536Kx32 bits with parity	CI-VME4G/256
512 MEG	131,072Kx32 bits with parity	CI-VME4G/512
1 GIG	262,144Kx32 bits with parity	CI-VME4G/1024
2 GIG	524,288Kx32 bits with parity	CI-VME4G/2048
4 GIG	1,048,576Kx32 bits with parity	CI-VME4G/4096

1.3 CI-VME4G MEMORY DESCRIPTION

The CI-VME4G is a high-density, high-speed Block Transfer DRAM Memory board with a Dual-Port interface that allows memory cycles to be performed to both the VSB and VMEbus simultaneously. A VME64 data bus allows data transfer rates up to 80 Megabytes/Second. VSB transfers data at up to 40 Megabytes/Second.

The CI-VME4G can be ordered without the VSB interface. This configuration has the same VMEbus features but lacks the VSB interface. The sections in this manual regarding the VSB should be ignored for this version of the board.

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1.4 OPERATIONAL FEATURES

The CI-VME4G performs all memory functions according to ANSI/VITA 1 for the VMEbus interface and VSB REV C for the VSB interface. Supported VMEbus cycle types include byte, word, and long word operations (8, 16, 24 and 32 bit data transfers), Read-Modify Write cycles, Unaligned transfers, 64 bit Block transfers, Address Pipelining, and Address Only cycles.

Starting and Ending Address selection may be selected for VMEbus accesses on One Megabyte boundaries.

A Control Status Register (CSR) is provided, and responds to 16 bit SHORT IO Address modifiers. Starting and Ending address configurations are written to the CSR and then stored into nonvolatile EEPROM.

Block transfer cycles are highlighted as the CI-VME4G's strongest feature. Block Cycles can be performed on 32 or 64 bit wide locations.

Block Transfer lengths of up to 2 Kbytes may be performed on VMEbus. Transfers may not cross 2 Kbytes boundaries. The VMEbus master is responsible for ending a Block Transfer.

Up to 512 Refresh Requests can be queued for extended or delayed Block Transfers. To provide the fastest possible Block Transfers, Refresh Requests are queued until the burst is complete. This allows burst durations of up to 8 milliseconds. All pending Refresh Requests will be executed in burst mode once the burst cycle is complete. Each refresh cycle requires 80 nanoseconds to execute.

LED indicators for VMEbus CYCLE, D64 CYCLE, D32 CYCLE, ALU CYCLE (green) and are mounted on the front panel.

1.5 POWER REQUIREMENTS

The CI-VME4G memory module requires only the +5 volt supply from the VMEbus/FPDP back plane. (See the general specifications for current requirements.)

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1.6 GENERAL SPECIFICATIONS

CAPACITY:	64, 128, 256, 512 or 1024, 2048 and 4096 Megabytes
CYCLE TIME:	100ns BLOCK CYCLE, 195ns SINGLE CYCLE
ACCESS TIME WRITE/READ:	30/30ns BLOCK CYCLE, 90/140ns SINGLE CYCLE
WORD SIZE:	8, 16, 24, 32 or 64 bits
MEMORY ADDRESSING:	A32, 4 GB maximum. Selectable on 1MB boundaries
CSR Addressing:	A16, selectable on 256 byte boundaries using VMEbus SHORT I/O
Modes of Operation:	
MEMORY	READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS,UNALIGNED TRANSFERS
CSR	READ, WRITE
ANSI/VITA 1 Compatibility:	SLAVE, A16, A32, D8, D16, D24, D32, D64, RMW, BLT, MLBT, UAT, AD0
Address Modifiers:	AM Codes 3E, 3D, 3A, 39, 0E, 0D, 0A, 09, 2D
Refresh:	Internal, Distributed and Queued
Indicators:	GREEN - VME,VSB,MBLT and BLT cycles
Designed Temperature Range Operating:	0deg. C to +70deg. C non-condensing
Power Requirements:	+5 Volts 4GB Option
TYPICAL	1.5A
MAXIMUM	2.6A
Dimensions:	160mm x 233.35mm, 6U form factor

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2. HANDLING AND INSTALLATION

2.1 INTRODUCTION

This section describes the handling precautions and the procedure of installation of the CI-VME4G memory modules.

2.2 HANDLING PRECAUTIONS

The memory IC's on the CI-VME4G module are MOS devices. They are damaged by static electricity discharge. Always handle MOS IC's so that no discharge will flow through the IC's. Avoid unnecessary handling. When handling IC's wear cotton rather than synthetic clothing.

The CI-VME4G uses SDRAM DIMM memory modules for added density. If the Array needs to be removed or installed, care needs to be taken not to damage the mating connector. Before applying pressure to seat the connector, examine that all pins are aligned.

2.3 MEMORY ADDRESS SELECTION

The CI-VME4G has an individually selectable START and END address with 1 megabyte granularity. These address configurations define the VMEbus and VSB address range that the board will respond to. The board will be selected when the address is GREATER or EQUAL to the START address AND LESS than the END address. The values for START and END are programmable via the CSR register and stored into EEPROM. The EEPROM values are read at power up and give the START and END registers a default value.

2.4 24-BIT ADDRESS SYSTEMS

24 Bit address decoding is partially supported on the CI-VME4G. The board will respond to 24-Bit Address modifiers, but will decode address bits A20 through A31 for selection. It is up to the system integrator to guarantee this condition will exist if A24 selection is required.

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2.5 VMEbus ADDRESS MODIFIERS

The CI-VME4G may respond to different combinations of address widths and VMEbus address modifier codes.

The following table summarizes the AM codes that the CI-VME4G responds to:

3E, 3D 3A, 39, 0E, 0D, 0A, 09	Single Cycle Transfers
0F, 0B	32 Bit BLT Block Transfers
3C, 38, 0C, 08	64 Bit MBLT Block Transfers
2D, 29	16 Bit CSR Cycles

2.7 VSB ADDRESS SPACES

The CI-VME4G is configured to respond to VSB SYSTEMS ADDRESS SPACE. VSB ALTERNATE ADDRESS cycles can be configured by the factory.

2.8 DUAL-PORT ADDRESS OVERLAPPING

Although each bus can be configured independently, the lower Bus addresses are used to address the memory array. This will cause certain addresses on one bus to access other addresses on another bus. Care must be taken when choosing bus addresses. For example a 4MB memory board is configured to respond to
VMEbus addresses 100000h to 500000h and VSB address 0h to 400000h, the following overlap will exist:

VMEbus	VSB
400000 - 500000	000000 - 100000
100000 - 200000	100000 - 200000
200000 - 300000	200000 - 300000
300000 - 400000	300000 - 400000

Notice that the memory board has a 4MB redundancy. An 8MB board would similarly have an 8MB redundancy.

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2.9 CSR ADDRESS SELECTION

The CI-VME4G CSR is a set of 16 bit read/write register. The CSR is selected by a VMEbus 16 bit SHORT SUPERVISORY (2D) or SHORT NON-PRIVILEGED ACCESS (29) Address Modifier code. Address selection uses shunt areas IO0 through IO7 which places the CSR on 256 byte boundaries. Note that shunt labels correspond to address bits A8 through A15. An installed shunt represents a "1" or HI on the bus where a removed shunt represents a "0" or LOW on the bus. Refer to Table 2.6.1 for examples.

2.9.1 CSR ADDRESS SELECTION EXAMPLES

A15	A14	A13	A12	A11	A10	A9	A8	ADDRESS
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	
O	O	O	O	O	O	O	O	0000 - 00FF
O	O	O	O	O	O	O	I	0100 - 01FF
O	O	O	O	O	O	I	O	0200 - 02FF
O	O	O	O	O	I	O	O	0400 - 04FF
O	O	O	O	I	O	O	O	0800 - 08FF
O	O	O	I	O	O	O	O	1000 - 10FF
O	O	I	O	O	O	O	O	2000 - 20FF
O	I	O	O	O	O	O	O	4000 - 40FF
I	O	O	O	O	O	O	O	8000 - 80FF
I	I	I	I	I	I	I	I	FF00 - FFFF
O	O	O	O	O	O	O	O	DEFAULT CONFIGURATION

2.10 CSR PROGRAMMING

OFFSET	DEFAULT	DESCRIPTION
00x	EEPROM	VME Starting Address
02x	EEPROM	VME Ending Address
04x	EEPROM	VSB Starting Address
06x	EEPROM	VSB Ending Address
08x	DIMM	DIMM Size Configuration

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2.10.1 STARTING ADDRESS

This register contains 12 bits that are compared with the VMEbus address lines A31-A20. An identical register is allocated for the VSB as well. The address needs to be equal to or greater than this value for the board to be selected. Note that board selection is determined by both the STARTING and ENDING ADDRESS selection to be valid.

Bit	Description
11:0	Starting Address Selection
15:12	Reserved

2.10.2 ENDING ADDRESS

This register contains 12 bits that are compared with the VMEbus/VSB address lines A31-A20. The address needs to be less than this value for the board to be selected. An identical register is allocated for the VSB also.

Bit	Description
11:0	Ending Address Selection
15	Window Page register enable. If this bit is set then the page window bits defined in the starting address register is now enabled. (currently not used)
14:12	Reserved

.

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2.10.3 DIMM Size

The onboard controller reads information from the DIMMs to configure local logic. This value is for debugging purposes. Note that only Chrislin approved DIMMs will work in this board. Use of any other module will void the warrenty.

Writing a 0100h to this register will store the contents of the selection registers into EEPROM that will used as the power up default values.

Bit	Description
3:0	Dram chip type. 0001 = 64 Mbit 0010 = 128 Mbit 0011 = 256 Mbit
6:4	Number of banks (# of 64 bit banks) 000 = 1 sided module 001 = 2 sided module 011 = ½ populated large module (4 banks) 111 = Full large module (8 banks)
7	Number of modules 0 = 1 module installed 1 = 2 modules installed

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3.1 THEORY OF OPERATION

The CI-VME4G performs 8, 16, 24, 32 or 64 bit data transfers as described in the VMEbus specification. VMEbus Address selection for memory cycles is 32 bits. Address bits A20-A31 are decoded for each type of cycle. If A24 Address Modifiers are used, the user must insure that the upper address lines are terminated in a state that will select the board. Cycle types include READ, WRITE, READ-MODIFY-WRITE, BLOCK TRANSFERS, UNALIGNED TRANSFERS, ADDRESS ONLY and ADDRESS PIPELINING.

VSB address selections always uses 32 address bits and responds to the SYSTEM or ALTERNATE ADDRESS SPACE. Cycle types include READ, WRITE, LOCKED, BLOCK TRANSFERS, AND ADDRESS ONLY.

Refresh is internal and distributed. Refresh requests occur every 15 microseconds. Refresh Cycles have the highest priority in the arbitrator but are postponed during BLOCK TRANSFERS. This allows uninterrupted BLOCK TRANSFERS. Up to 512 Refresh cycles are queued during long Block Transfers. Refresh cycles are execute in a burst mode once the block cycles is complete. Each Refresh Cycles takes 80 ns to execute.

Since Block Transfers (BLT) are used for maximum data throughput, only 32 and 64 bit wide transfers are supported.

BLT cycles use a proprietary Memory Management Scheme that allows the fastest possible cycle times on the VMEbus. Data is available for the Master to read before the Master requests the data. DTACK/ACK is driven within 30 ns allowing the Master to digest the data and prepare for the next cycle. Note that this access time is the same for all cycles within a Block Burst.

The CI-VME4G does not use caching or interleaving methods that usually result in two different access times. Typically boards that use this method have a long access time for a normal cycle and a short access time for the cached or interleaved cycle. The CI-VME4G can perform back-to-back BLT cycles in less than 100ns.

Data is latched for both read and write cycles. The Chrislin Chip Set includes SWAP buffers that align 8, 16, and 32 bit data to the internal 64 bit data word. A synchronized four grant arbitration system is used. Arbitration priorities rank as follows: Refresh requests, VMEbus request (includes D64 cycles), VSB Requests and CSR requests.

Because of the programmable nature of the internal state machines, the CI-VME4G could easily be modified to respond in various MASTER/SLAVE environments. Chrislin supplies custom configurations for many customers.

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3.2 ALU Functions

A new concept in Memory design is the ability to perform various ALU functions during a VMEbus write cycle. This functionality has been implemented in the Chrislin ASIC Chip Set. A typical ALU cycle is where the master writes one of the operands to the memory. The previously stored data is used as the second operand. The result is stored back into the same memory location.

To access one of these functions one of two methods may be used. The first method determines the function to be executed by placing the User Defined Address Modifiers (as shown in the table below) during the write cycle. The second method allows the user to program the function via the Control Status Register. The second method allows the ALU to be used with standard off the shelf VMEbus masters. A CSR bit 'M' is used to select either Logical or Arithmetic Functions. A Carry-In bit 'C' is also set in the CSR and selects a second column in the function table. Carry-Outs are ignored and not stored. . The master must first set up the 'M' and 'C' bits in the CSR.

The following table summarizes the available functions. Note that BUS data is represented as A and previously stored MEMORY data is represented as B.

Z	M = H	M = L; ARITHMETIC OPERATIONS	
AM	LOGIC	Cn'=H	Cn'=L
Code	Functions	(no Carry)	(with carry)
10	F=!A	F=A	F=A PLUS 1
11	F=!(A+B)	F=A+B	F=(A + B) PLUS 1
12	F=!AB	F=A+!B	F=(A + !B) PLUS 1
13	F = 0	F = MINUS 1(2's COMPL)	F = ZERO
14	F = !(AB)	F = A PLUS A!B	F = A PLUS A!B PLUS 1
15	F = !B	F = (A + B) PLUS A!B	F = (A + B) PLUS A!B PLUS 1
16	F=A@B	F=A MINUS B MINUS	F=A MINUS B
17	F = A!B	F = A!B MINUS 1	F = A!B
18	F=!A+B	F=A PLUS AB	F=A PLUS AB PLUS 1
19	F=!(A@B)	F=A PLUS B	F=A PLUS B PLUS 1
1A	F = B	F = (A + !B) PLUS AB	F = (A + !B) PLUS AB PLUS 1
1B	F = AB	F = AB MINUS 1	F = AB
1C	F=1	F = A PLUS A <	F=A PLUS A PLUS 1
1D	F=A + !B	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
1E	F = A + B	F = (A + !B) PLUS A	F' = (A + !B) PLUS A PLUS 1
1F	F=A	F=A MINUS 1	F=A

< Shifted Left to the next most Significant position -
M = M bit in the CSR register.

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4.1 P1 PIN ASSIGNMENTS

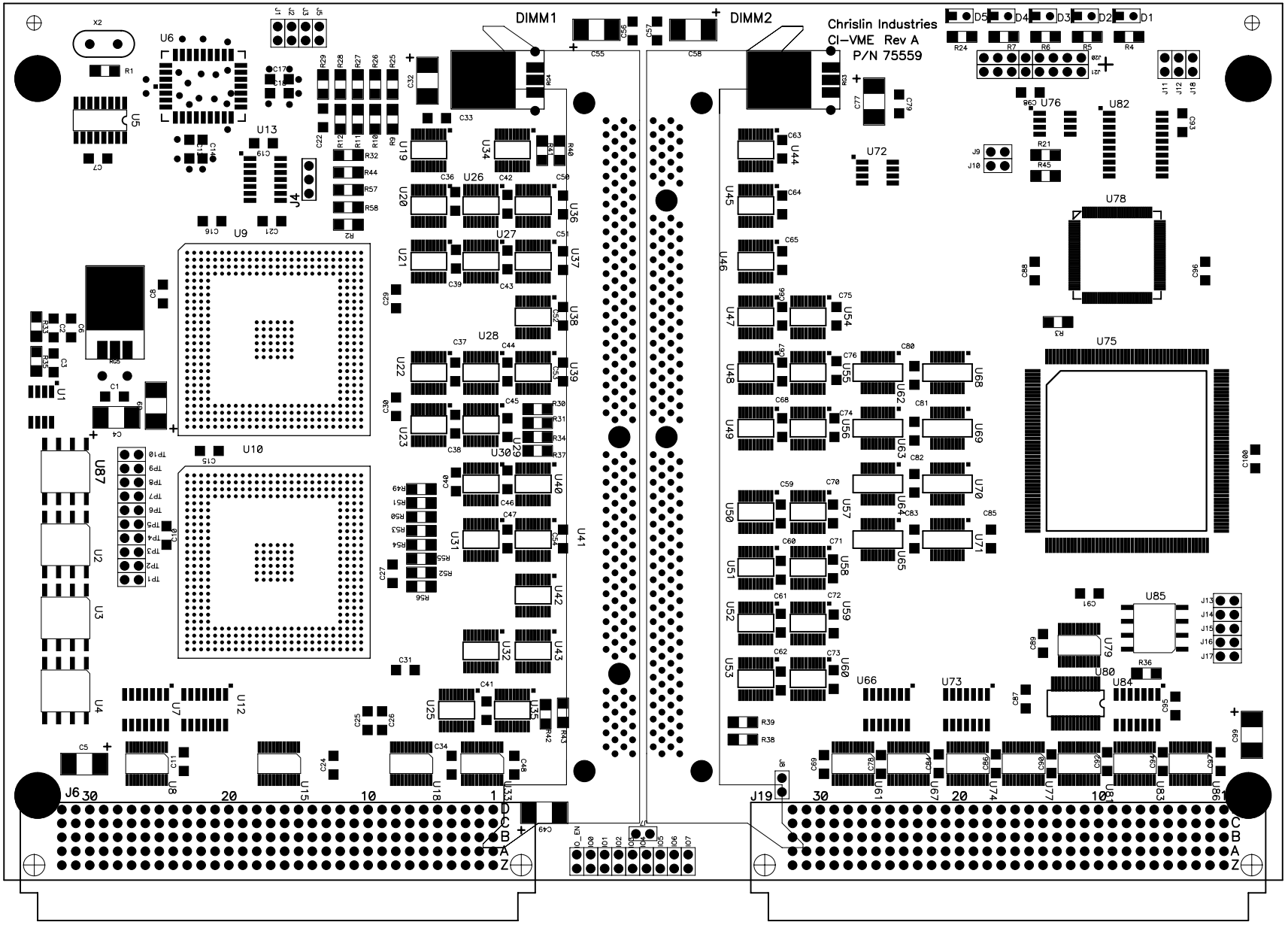
PIN	ROW A	ROW B	ROW C
1	D00	--	D08
2	D01	--	D09
3	D02	--	D10
4	D03	/BG0IN	D11
5	D04	/BG0OUT	D12
6	D05	/BG1IN	D13
7	D06	/BG1OUT	D14
8	D07	/BG2IN	D15
9	GND	/BG2OUT	GND
10	--	/BG3IN	--
11	GND	/BG3OUT	/BERR
12	/DS1	--	/SYSRESET
13	/DS0	--	/LWORD
14	/WRITE	--	AM5
15	GND	--	A23
16	/DTACK	AM0	A22
17	GND	AM1	A21
18	/AS	AM2	A20
19	GND	AM3	A19
20	/IACK	GND	A18
21	/IACKIN	--	A17
22	/IACKOUT	--	A16
23	AM4	GND	A15
24	A07	--	A14
25	A06	--	A13
26	A05	--	A12
27	A04	--	A11
28	A03	--	A10
29	A02	--	A09
30	A01	--	A08
31	--	+5VSTBY	--
32	+5V	+5V	+5V

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4.2 P2 PIN ASSIGNMENTS

PIN	ROW A	ROW B	ROW C
1	VSBAD0	+5V	VSBAD1
2	VSBAD2	GND	VSBAD3
3	VSBAD4	--	VSBAD5
4	VSBAD6	A24	VSBAD7
5	VSBAD8	A25	VSBAD9
6	VSBAD10	A26	VSBAD11
7	VSBAD12	A27	VSBAD13
8	VSBAD14	A28	VSBAD15
9	VSBAD16	A29	VSBAD17
10	VSBAD18	A30	VSBAD19
11	VSBAD20	A31	VSBAD21
12	VSBAD22	GND	VSBAD23
13	VSBAD24	+5V	VSBAD25
14	VSBAD26	D16	VSBAD27
15	VSBAD28	D17	VSBAD29
16	VSBAD30	D18	VSBAD31
17	GND	D19	GND
18	-	D20	GND
19	/VSBDS	D21	GND
20	/VSBWR	D22	GND
21	SPACE0	D23	SIZE0
22	SPACE1	GND	/PAS
23	LOCK	D24	SIZE1
24	/ERR	D25	GND
25	GND	D26	/ACK
26	GND	D27	AC
27	GND	D28	/ASACK1
28	GA0	D29	/ASACK0
29	GA1	D30	/CACHE
30	GA2	D31	/WAIT
31	BGIN	GND	-
32	-	+5V	BGOUT

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