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CM-AD-45 User's Manual

12 bit, 32 Channel, 100 Ksps
Analog to Digital Module

CM-AD-45

12 bit, 32 Channel, 100 Ksps A/D Module

User's Manual

CM Computer
Updated Documentation

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1

Chapter 1.- Introduction.

1.1.- Board Description.

The **CM-AD-45** is a general purpose 12 bit resolution A/D conversion module. It incorporates 32 single-ended input channels (or 16 differential channels). This unit is designed for 6U VMEbus applications.

The board is a high performance slave unit designed with low heat dissipation CMOS technology. As a direct result of its superior design and functionality it can be successfully used in many of today's engineering applications.

The **CM-AD-45** offers the user the following basic features:

a) Automatic on-board conversion capability.

The on-board circuitry performs all tasks relative to multiplexing, sampling and conversion of input signals.

This feature reduces VMEbus traffic, frees the master CPU from A/D conversion tasks and simplifies application software written for the **CM-AD-45**.

b) VMEbus interface through dual port RAM.

This module incorporates dual port RAM as the transparent communication mechanism between the A/D converter and the VMEbus master CPU.

When mapped in the VMEbus addressing range, the **CM-AD-45** appears as an A24/D16 slave RAM board.

The dual port RAM supports data buffers of up to 2K samples (16 bits per sample). It converts and stores all 32 input channels in real time. The board is capable of filling the dual port RAM buffer in single step, or in free running cyclic operation.

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c) Programmable conversion speed.

The **CM-AD-45** is capable of performing up to 100K samples per second at 10 µsec conversion rate. The user can select conversion speeds from four steps: 10, 20, 40 or 80 µsec per sample. A/D conversions may be performed in multiplexed or fixed channel mode.

When operating in *multiplexed mode*, the board will sample all input channels on a sequential basis until completion of all 32 inputs per sampling cycle. Each channel is sampled, converted and stored in RAM, resulting in consecutive channels being stored in consecutive RAM locations.

When operating in *fixed channel mode*, the user can select a specific channel that will be continuously sampled, converted and stored in consecutive memory positions. This allows sustained conversion rate of 100K samples per second and dedicates the 2048 Word storage buffer to the selected channel.

d) Interrupt generation capability (VMEbus Interrupter).

The **CM-AD-45** incorporates a local VMEbus Interrupter which asserts interrupts once the 32 or 2048 Word storage buffer is filled (end of A/D sampling cycle). The Interrupter is level selectable and provides a user defined pair of Status-ID vectors. Interrupts are enabled/disabled through the Module Control Register (MCR).

e) Wide range of input AC/DC voltages.

The 32 input channels are provided with complete and flexible input voltage management. The board allows Unipolar and Bipolar operation, and accept all industry standard DC input voltage ranges from 5 to 100 Volts (from ±2.5 to ±100 Volts in Bipolar).

The board will also accept input current loop levels (mA) most commonly used in industrial instrumentation.

The **CM-AD-45** input channels are fault and over voltage protected by using new generation MAX388 multiplexers. These devices are protected up to 110 Volts. When installing the industry standard DG508 devices, this protection is obtained by means of extra Zener diodes.

f) On-board Module Control Register (MCR).

A 16 bit write only register is dedicated for programming and customizing the board operational parameters. Writing a word in the MCR allows the user to select the input voltage range, the conversion speed, RAM storage buffer size, Built-In-Test, multiplexed or fixed channel operation mode, etc.

All on-board functions are managed through the Module Control Register, making the **CM-AD-45** an extremely easy to program unit.

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g) VME64x 5 row P2. Metric type 95 pin P0.

The 32 input channels are wired through a new generation 160 pin VME64x DIN connector located on the VMEbus P2. An optional P0 connector is additionally implemented for keying-slot purposes.

h) On-board Built-In-Test capability.

This module incorporates specific Built-In-Test circuitry which is enabled under software control.

The BIT feature allows testing all on-board TTL and analog chips by means of wrap-around loops which disconnect the external analog application signals and connect internally generated test signals in order to verify correct module operation.

i) Software Compatibility with the Predecessor CM-AD-35 module.

The **CM-AD-45** is backward compatible with the **CM-AD-35**. It is a direct **CM-AD-35** replacement and therefore can be used in all applications previously designed with the **CM-AD-35** module.

Since the **CM-AD-35** has been a popular board with hundreds of units delivered to our customers, **CM Computer** has taken special care in ensuring backward compatibility. However, the **CM-AD-45** significantly increases **CM-AD-35** performance by adding more I/O flexibility, incorporating many extra features and a significantly VME64 improved design.

j) Low cost.

In spite of integrating 32 single ended or 16 differential A/D channels, the **CM-AD-45** is a cost effective professional unit, which invariably results in a competitive advantage when compared to similar products on the market.

k) Military and Industrial versions. Two mechanical formats.

The **CM-AD-45** module is available in 4 different temperature ranges, all 100% compatible. Additionally the module PCB is manufactured in two different mechanical versions:

- CM-AD-45/A: Module designed according to the VMEbus IEC-297 Standard. This classic version is provided with front panel. It simultaneously wires all analog input signals through two type-D cannon connectors on the front panel and the 160 pin VME 64x connector on the VMEbus P2.

- CM-AD-45/B: Module designed according to the Military VMEbus P1101.2 specification for Conduction Cooled Eurocards. The military version, intended for avionics-type ATR enclosures is provided with wedge-locks and has a dummy front panel with no I/O capability. Therefore it can only wire all input signals through the 160 pin VME64x connector located on the VMEbus P2.

Both mechanical versions are available with conduction cooled PCB provided with thermal overlay.

All **CM Computer** products are originally designed for military environments and therefore accept full military grade components and implement conduction cooled PCB. Industrial versions are available at a lower cost since these are populated with industrial grade components.

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1.2.- CM-AD-45 Applications.

The potential applications covered by the **CM-AD-45** module are many and diverse. This type of module can be used as a general purpose Analog-to-Digital input board in any commercial, industrial, or military VMEbus project.

The following application examples, classified by areas, are only a fraction of the existing possibilities.

a) Industrial applications.

- Industrial control of chemical plants, factories, refineries.
- Automation of buildings and hotels, sport pavilions, stadiums.
- Traffic control for large cities. Railway control.
- Automation of laboratories.
- Power station and electrical grid control.
- Surveillance, fire detection, etc.
- Artificial vision systems.
- Numerical control machinery. Robotics. Artificial intelligence.

b) Military applications.

- Navigation and flight computers for ships and aircraft.
- Weapon systems control.
- Radar and sonar detection. Target and trajectory calculation.
- Signal processing. Data link.
- Electronic warfare. Electronic countermeasure equipment.
- Intelligent weapons, torpedoes, missiles.
- Automation of war headquarters and tactical rooms.

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1.3.- CM-AD-45 Ordering Information.

This section shows all the **CM-AD-45** standard configurations and options:

CM-AD-45 **/V** **/T** **/M**

Module Name

PCB Mechanical Version

A = IEC 297 Standard Mechanics with front panel. J2 and front panel I/O connectors.

B = IEEE P1101.2 Military Mechanics with wedgelocks and dummy front panel. J2 I/O connector.

Board Temperature Range

C = Commercial range (0 to +60 °C). Only available with fiberglass PCB.

I = Industrial range (-20 to +70 °C). Only available with fiberglass PCB.

R+ = Military Rugged+ range (-40 to +85 °C). Only available with conduction cooled PCB.

883 = Full Military 883 range (-50 to +90 °C). Only available with conduction cooled PCB.

Board Version

1 = 32 single-ended channel (16 differential) A/D board, 100 Ksps, 4 KB dual port RAM, WITHOUT input 10:1 attenuator and current resistor per channel.

2 = 32 single-ended channel (16 differential) A/D board, 100 Ksps, 4 KB dual port RAM, WITH input 10:1 attenuator and current resistor per channel.

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1.4.- CM-AD-45 Technical Datasheet.

This section includes a copy of the **CM-AD-45** datasheet and summarizes the main characteristics and features of this module. The original datasheet shows several color photographs of both Commercial and Military versions.

This manual describes the **CM-AD-45** board hardware features and technical characteristics. It is specifically oriented toward application engineers, programmers, and system integrators who wish to implement this module in their projects.

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Chapter 2.- General Considerations.

This section contains information concerning the terminology and conventions used in this manual, safety rules, complementary and recommended documentation as well as legal restrictions concerning the described product.

2.1.- Manual Terminology.

The terminology used in this manual is intended to be generally compatible "with similar product manuals and common VMEbus literature terminology.

A signal is defined as "asserted" at logic '0' if the function associated with the signal line is valid or initiated by either a low level or falling edge on the signal line. The mnemonics of active low signals are marked with the suffix "*". For example, the BERR* signal is asserted (active or true) at logic '0' since when this signal is at '0' level it provokes a system Bus Error.

Most of the VMEbus signals are in asserted state when they are at logic '0' and this is noted by an asterisk. Those signals asserted at logic '1' are named without an asterisk. Note that a signal asserted at logic '0' is "negated" (inactive or false) at logic '1'.

IMPORTANT

The information in this manual has been carefully checked and supervised. However, no responsibilities are assumed for any inaccuracies that may be detected. **CM Computer** would appreciate any comments, suggestions or questions concerning this module and its manual.

2.2.- Other Documentation of Interest.

It is highly recommended that the user read all possible complementary information on the VMEbus specifications. The following manual is recommended:

- **"The VMEbus Specification Rev C & D".** Edited by the VMEbus International Trade Association.

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2.3.- VMEbus Compatibility.

The **CM-AD-45** board and other **CM** VMEbus modules have been designed according to the **ANSI/ IEEE STD 1014-1987 IEC 821 & 297** specifications for VME compatible products.

This product is electrically and mechanically compatible with other VMEbus products available on the market; therefore, you can easily interchange and interconnect them.

This product has successfully passed a compatibility test performed by the VMEbus Anomaly Trigger detector (VBAT). This equipment, used in conjunction with a 200 MHz and 96 channel Logic Analyzer, automatically recognizes more than 30 violations of the VMEbus specifications in real time.

The remainder of the **CM VMEbus** boards have also been similarly tested and proven to be compatible.

CM Computer has performed several compatibility tests between the **CM-AD-45** and other products on the market, obtaining satisfactory results each time. For the proper operation of the **CM-AD-45** board it is necessary to insert it in VME compatible racks and backplanes.

CM Computer has tested this product with several racks and backplanes on the market (CM, Schroff, Augat, AEG, etc).

2.4.- Proprietary Rights and Patents.

The **CM-AD-45** board and the remainder of the **CM VME** compatible set, has been entirely designed by **CM Computer** which has all manufacturing, distribution, reproduction and modification rights.

Non authorized partial or total reproduction of this product and its documentation and/or violation of the above rights, will result in legal prosecution.

The specifications and design of the **CM-AD-45** board are subject to change without notice.

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2.5.- Guarantee.

All the VMEbus modules manufactured by **CM Computer** include a 2 year guarantee that covers free replacement in case of malfunction or design failure.

Guarantee does not cover failures provoked by boards incorrectly used, short circuits, overloading, or any operational conditions exceeding the limits specified in the present manual.

If you come across any problems or have any questions using this product please contact your authorized distributor.

To preserve all rights included in this guarantee, general recommendations, specifications and operating procedures described in the present manual must be followed.

2.6.- Safety Rules.

This VMEbus module can be implemented in many different projects and applications. The following recommendations and safety precautions are of vital importance for all users and system integrators.

IMPORTANT

This module implements integrated circuits sensitive to electrostatic discharges. The user should avoid touching the module with his hands and should observe the basic precautions when dealing with this kind of technology.

The user must avoid touching or removing the module from the backplane while functioning. Do not replace components with the power cable connected.

IMPORTANT

This module can provoke extremely dangerous electrical discharges. To minimize shock hazard it is the user's responsibility to create a safe working environment, avoiding all types of risks to human life and to the equipment. The cabinet, rack, chassis and other metallic parts involved in any application must be safety grounded.

IMPORTANT

This module radiates electromagnetic energy and if not installed and used properly, may occasionally cause interference to radio communications. The amount of energy radiated is in compliance with FCC rules class A 15J electronic equipment. If the use or application of this equipment causes any interference all necessary measures required to correct it must be supplied by the user.

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IMPORTANT

Avoid connecting cables on the board application connectors while functioning. Voltage discharges may damage the board input channel's components.

IMPORTANT

CM Computer is continuously searching for ways to improve its products. Therefore, the specifications, features and design of the modules described in the present manual may change without prior notice.

IMPORTANT

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Chapter 3.- Functional Description.

This chapter explains the sub modules and functional blocks that comprise the **CM-AD-45** board. The objective is to introduce and familiarize the user with the board contents and technical features. More detailed information on each functional block can be found in later chapters of this manual.

3.1.- Functional Blocks.

- Input channels.

The **CM-AD-45** implements 32 independent single-ended analog input channels. These channels are multiplexed and amplified before Analog to Digital conversion.

Two single-ended channels can be jumper configured in order to constitute a differential channel. The **CM-AD-45** offers 16 standard differential channels per board.

- A/D converter.

This board incorporates the high quality industry standard Analog Devices AD-1674 converter. This 12 bit resolution device is an improved version of the classic AD-574.

The AD-1674 performs at 10 µsec sampling time (100 Ksps), and includes an on-chip Sample-and-Hold Amplifier.

The converter is available in three different temperature ranges from commercial to full MIL-STD-883. There are two standard accuracy options of ±1LSB and ±1/2 LSB.

- Analog input ranges.

The **CM-AD-45** accepts DC voltages in Unipolar or Bipolar ranges. Additionally, channels can be individually jumper configured to manage DC current inputs up to 50 mA.

Voltage ranges accepted are those commonly used in industrial and military applications: 0-5 V, 0-10 V, ±5V, ±10V and ±2.5V at full scale.

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The **CM-AD-45/2** version incorporates a 10:1 voltage attenuator per channel. Enabling the attenuator, allows operation with input voltage ranges above 10 Volts, such as 0-50 V, 0-100 V, ±50V, ±100V and ±25V.

The analog input stage incorporates a software controlled gain amplifier whose voltage gain is programmable through the Module Control Register. The combination of the programmable gain amplifier and the input voltage attenuator allows a wide variety of board input voltage ranges.

The **CM-AD-45** is also well suited for sampling AC input waveforms up to 50 KHz. The on-board AD converter is fully specified for frequency domain AC parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth.

- Analog input stage.

Each input channel individually incorporates protective circuitry that prevents damage to the input devices caused by input overload, voltage peaks, etc. The protective circuitry allows continuous, safe and reliable operation with over voltages up to 120 Volts, and supports even higher short, transitory peaks on the input lines.

The analog input stage incorporates four single-ended 8-channel multiplexers. The board supports two different generations of analog multiplexers: the industry standard DG-508 or the new generation fault and over voltage protected MAX-388.

When installing the DG-508 devices, the board provides the necessary channel input over voltage protection by means of a discrete component network based on bipolar Zener diodes.

When the board is populated with the MAX-388, the zeners and protection networks are unnecessary and can be avoided.

The on-board analog amplifiers can be configured as *single-ended* or *differential*. The configuration is done by jumpers, such that that two single-ended input channels may constitute a single differential channel.

The **CM-AD-45** incorporates high slew rate operational amplifiers (17 V/µs), featuring low noise and high precision.

- Input impedance.

The channel input impedance is fixed by four resistor arrays RP1, RP2, RP3 & RP4. These resistors are usually mounted on sockets.

The board is supplied factory fitted with resistor arrays of 470KΩ. This is the default input impedance per channel. However, the channel input impedance can be user modified in order to obtain any value between 10K and 5 MΩ. This is achieved by means of replacing the four resistor array by another array of the desired value. More details concerning input impedance can be found in the following chapters.

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- Dual port RAM memory.

4 KB of dual port static RAM, 16 bit wide, is provided as the transparent communication mechanism between the board and the VMEbus.

The **CM-AD-45** can be programmed to operate with data buffers of 16/32 or 2048 Words. The size of the buffers and its operational mode can be user selected through the Module Control Register.

The VMEbus master can read any RAM location at any time. This is required for reading updated conversion values of the input channels. The master is not allowed to write to RAM buffer. This is hardware protected since the RAM is intended to be a *read-only* device.

Each conversion value is stored in 12 bit natural binary format. This is the format directly obtained from the AD converter chip.

The **CM-AD-45** dual port RAM is a rapid response device, performing VMEbus data read cycles in about 300 nsec.

- Self multiplexing & conversion circuitry.

This unit performs all tasks relative to input channel multiplexing, A/D conversion and data storage in the dual port RAM. It can operate in "one step" or "free running" mode, performing up to 100 Ksps. As soon as a new conversion value is available, it is updated in the dual port RAM.

The local multiplexing-conversion circuitry does not include a dedicated processor since it is implemented with fast programmable logic. This unit is managed by several bits of the Module Control Register.

- Module Control Register (MCR).

The Module Control Register (MCR) is a 16 bit write-only latch. It is accessed by the VMEbus master by writing a Word in the SRAM base address. The MCR is the only programmable register of the **CM-AD-45** board.

Since it is accomplished with output latches, the written Word can not be directly read back in a transparent manner. Reading the Module Control Register address will access the first RAM position. This corresponds to converted data of input channel 1, not to the value previously written to the Module Control Register.

The MCR is cleared by the VMEbus SYSRESET* line. All MCR bits are cleared to logic 0 after asserting SYSRESET*. This is the default MCR configuration. The board is designed to operate in the most standard case when all bits of the Module Control Register are set to logic 0.

The MCR performs the following basic functions:

- Defines the RAM storage buffer size.
- Enable/Disable VMEbus interrupts.
- Select the board A/D sampling rate.
- Enable/Disable the Built-In-Test wrap-around circuitry.
- Selects those channels to be multiplexed/sampled.

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-Built-In-Test.

The **CM-AD-45** features on-board Built-In-Test capability through dedicated circuitry. The module incorporates two voltage references and dedicated Built-In-Test relays. The relays can be switched on/off from the Module Control Register and are capable of testing the input channels in wrap-around mode. The relays are distributed in such a way as to allow testing all on-board analog and TTL chips. Built-In-Test cycles do not depend on the external application and can be dynamically executed under software control.

Built-In-Test relays are capable of switching-off and isolating specific input channels from the external application voltage. Simultaneously it applies a local testing reference voltage to the analog multiplexers. The reference test voltage "replaces" the external application voltage on the channel under test. This creates a wrap-around loop which allows checking the complete analog input stage as well as all TTL chips available on its signal path up to the VMEbus data buffers.

The Built-In-Test is also useful for asserting interrupts after the BIT cycle. This allows testing the other sections of the **CM-AD-45** module.

- VMEbus Interrupter.

The VMEbus Interrupter I(2-7) is a functional block whose purpose is to assert interrupts on the VMEbus prioritized interrupts lines IRQ2* to IRQ7* (all levels except IRQ1*).

The VMEbus Interrupter can be enabled/disabled through bit 1 of the Module Control Register.

Interrupts are intended for indicating end of current sampling cycle (converted data RAM buffer full).

The Status-ID Vector supplied by the **CM-AD-45** during IACK* cycles can be user configured via a set of jumpers. A 4x2 jumper block allows definition of the 4 MSBs (Most Significant Bit) of the supplied Status-ID Vector. The 2 LSB (Least Significant Bit) are automatically defined by the Interrupter according to the programmed RAM buffer size (16/32 or 2048 Words).

- VMEbus slave interface.

The **CM-AD-45** incorporates a slave type interface in accordance with the IEEE 1014, IEC 821/297 rev. D specification for VMEbus compatible products. The interface location monitor responds to A24/D16 Standard VMEbus address cycles. Two 4x2 jumper blocks provide up to 256 mapping possibilities within the standard VMEbus range.

This module occupies 4KB of addressing space in the VMEbus. This space corresponds to the dual port RAM.

The **CM-AD-45** data and address lines are properly buffered and latched to/from the VMEbus backplane. The module includes a DTACK* generator which will assert DTACK* during any valid Word access. Additionally, it incorporates a BERR* generator which asserts BERR* in response to non supported Byte or Long Word accesses.

The **CM-AD-45** is an input/output slave module and therefore supports VMEbus Read/Write data transfers. Write cycles are supported only in order to latch data into the MCR.

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- VMEbus RESET monitoring.

The **CM-AD-45** monitors the VMEbus backplane SYSRESET*. This signal will reset internal units when asserted on the bus. SYSRESET* affects as follows:

- The Module Control Register is cleared after reset, setting all bits to logic 0.
- The board disables interrupts, operating in free running mode sampling all channels @ 100 Ksps.
- While SYSRESET* is asserted, the MCR can not accept any configuration from the master CPU.

- Front panel LED indicators (CM-AD-45/A mechanics only) .

There are 3 LED indicators implemented on the board's front panel. These LEDs monitor the board status as affected by the VMEbus, input channel multiplexing and sampling. A LED is illuminated if its associated functionality is activated.

A green LED labeled "SEL" indicates master accesses to the board (board SELected). It is driven by the Location Monitor which is illuminated when the master accesses the **CM-AD-45** module.

A yellow LED labeled "CONV" is associated with A/D converter operation. It is driven by the converted busy pin STS. This LED is illuminated when the board is sampling and converting data. Otherwise, it will be switched-OFF (board A/D stopped).

A second yellow LED labeled "MUX" is associated with the input multiplexers. It is illuminated when the board is multiplexing all input channels (multiplexed mode). It will switched-OFF when the board is stopped or when operating in fixed channel mode.

- Front panel application connector.

The **CM-AD-45** board implements two 25 pin Cannon application connectors on its front panel. These type-D connectors provide 32 signal input pins plus ground. These pins are needed to wire the board to the 32 (16) external voltage sources. The front panel connectors are only available in the **CM-AD-45/A** mechanical version.

- VMEbus P2 application connector.

All input signals available at the module front panel are simultaneously wired to a second 160 pin VME64x DIN connector located at the VMEbus P2.

The use of the P2 connector is optional since a block of 32+2 jumpers allow connection or removal of all input signals assigned to P2. This set of jumpers can be useful to avoid unnecessary signal noise when the module is exclusively wired through the front panel. Analog input signals are assigned on P2 in rows a & c since these are defined as user free by the VMEbus specs.

The P2 rear connector is available in all mechanical versions. It is mandatory for I/O purposes in the wedge-lock version **CM-AD-45/B**.

Due to the dual input connector capability when using both wiring possibilities simultaneously, the user should avoid short circuits between input signals.

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- VMEbus P0 connector.

This module fits an optional 95 pin P0 connector. P0 is an auxiliary part intended only for keying slot purposes. No input analog signals are assigned to P0.

- CM-AD-45 PCB jumpers.

The on-board PCB jumpers perform the following functions:

- Two jumper blocks allow mapping of the **CM-AD-45** module within the VMEbus A24/D16 address range. Each **CM-AD-45** module takes up one 4KB block.
- A jumper block defines the VMEbus Interrupter IRQ level.
- A jumper block defines the Status-ID vector supplied by the Interrupter.
- A set of jumpers configures the input channels as type single-ended or differential.
- A jumper per channel connects the 10:1 input attenuator or configures the channel to accept voltage or current.
- A block of jumpers allow connection or removal of input signals to/from the VMEbus P2 application connector.

3.2.- CM-AD-45 Block Diagram.

Figure 3.1 illustrates the **CM-AD-45** block diagram.

This A/D module is easy to use and program. ***Figure 3.1*** shows how the **CM-AD-45** implements the following functional units:

- 32 input channels. Each input channel is composed of protective circuitry, input attenuator, and current-to-voltage high precision resistor.
- Four analog 8-channel multiplexers.
- High speed instrumentation OP-Amp. These can be configured as voltage follower or differential amplifiers according the input signals type.
- Built-In-Test multiplexer. This device is used for BIT purposes only.
- Built-In-Test relays. These devices are used for BIT purposes only.
- Programmable gain & polarity OP-Amp. This unit is controlled by two MCR bits.
- 100 Ksps A/D converter. Includes on-chip Sample-and-Hold amplifier.
- Dual Port SRAM. This device is addressed and filled by the on-board circuitry. Output data from the A/D converted is stored in consecutive memory positions.
- Timing, multiplexing and sampling circuitry. Accomplished by counters and programmable logic. This sequential unit performs all task relative to multiplexing, conversion, and addressing and filling of the RAM.
- Module Control Register. This is a 16 bit write-only latch-register.
- VMEbus interface. Includes the Address Decoder, DTACK* and BERR* generators, and VMEbus Interrupter.

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OBSERVATION

Each one of these blocks will be more extensively explained in the following chapters.

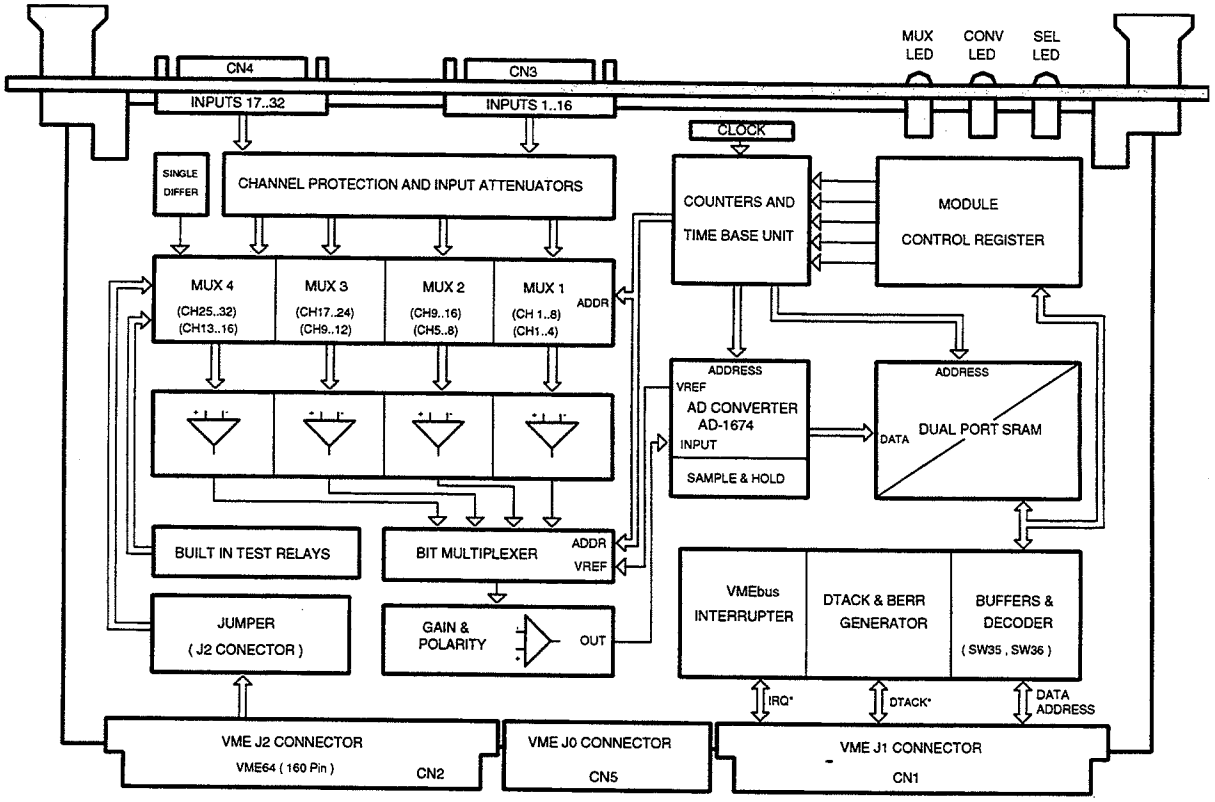


Figure 3.1.- CM-AD-45 block diagram.

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Chapter 4.- Technical Specifications.

This chapter defines the mechanical, electrical and functional specifications of the **CM-AD-45** board. Additionally, complementary sections are dedicated to explanation of temperature versions, input voltage specifications, jumper configuration and application connector pin-out.

4

4.1.- Mechanical Specifications.

The **CM-AD-45** is fully compliant with standard, double height, Euroboard size (233x160 mm).

Figure 4.1 shows the **CM-AD-45/A** silk screen and component layout. The external dimensions and tolerances are fully compatible with the VMEbus specs. IEC-297 and IEC-603.

Figure 4.2 shows the **CM-AD-45/B** board silk screen and component layout. This version has no connectors on the front panel and is provided with wedge-locks for insertion in a military avionics-type enclosure. The mechanical dimensions and wedge-lock location of the **CM-AD-45/B** is compatible with the VMEbus P1101.2 Conduction Cooling for Eurocards specification.

Figure 4.3 details the **CM-AD-45/A** & **CM-AD-45/B** front panels, offering a description of the panel's mechanical dimensions and drill holes. The module front panel, when inserted in a 19" rack, occupies one slot size (4hp).

OBSERVATION

All module versions are provided with a P1 96 pin DIN 41612 connector, intended connection to any standard VMEbus J1 backplane on the market.

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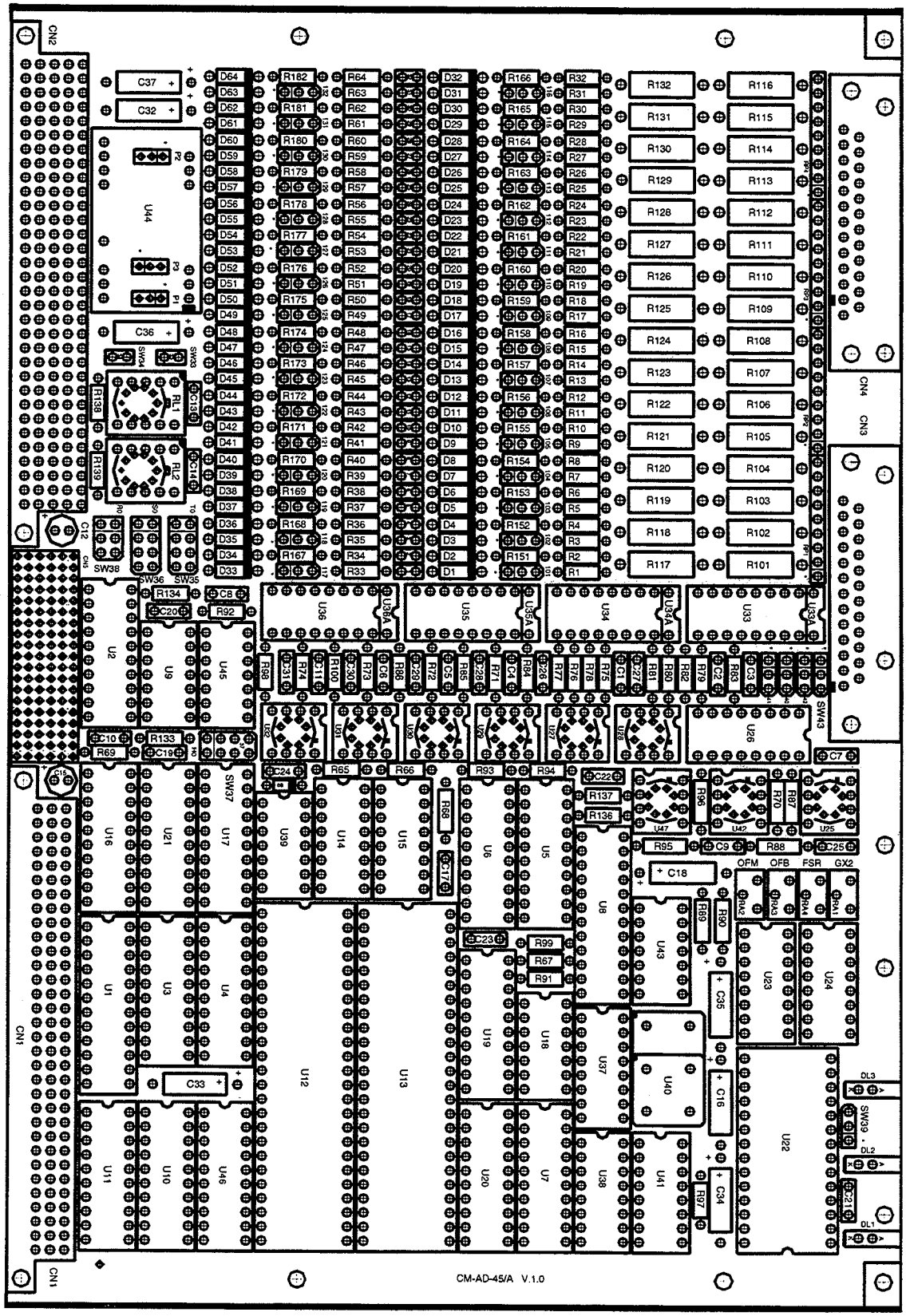


Figure 4.1.- CM-AD-45/A Silk screen and component layout.

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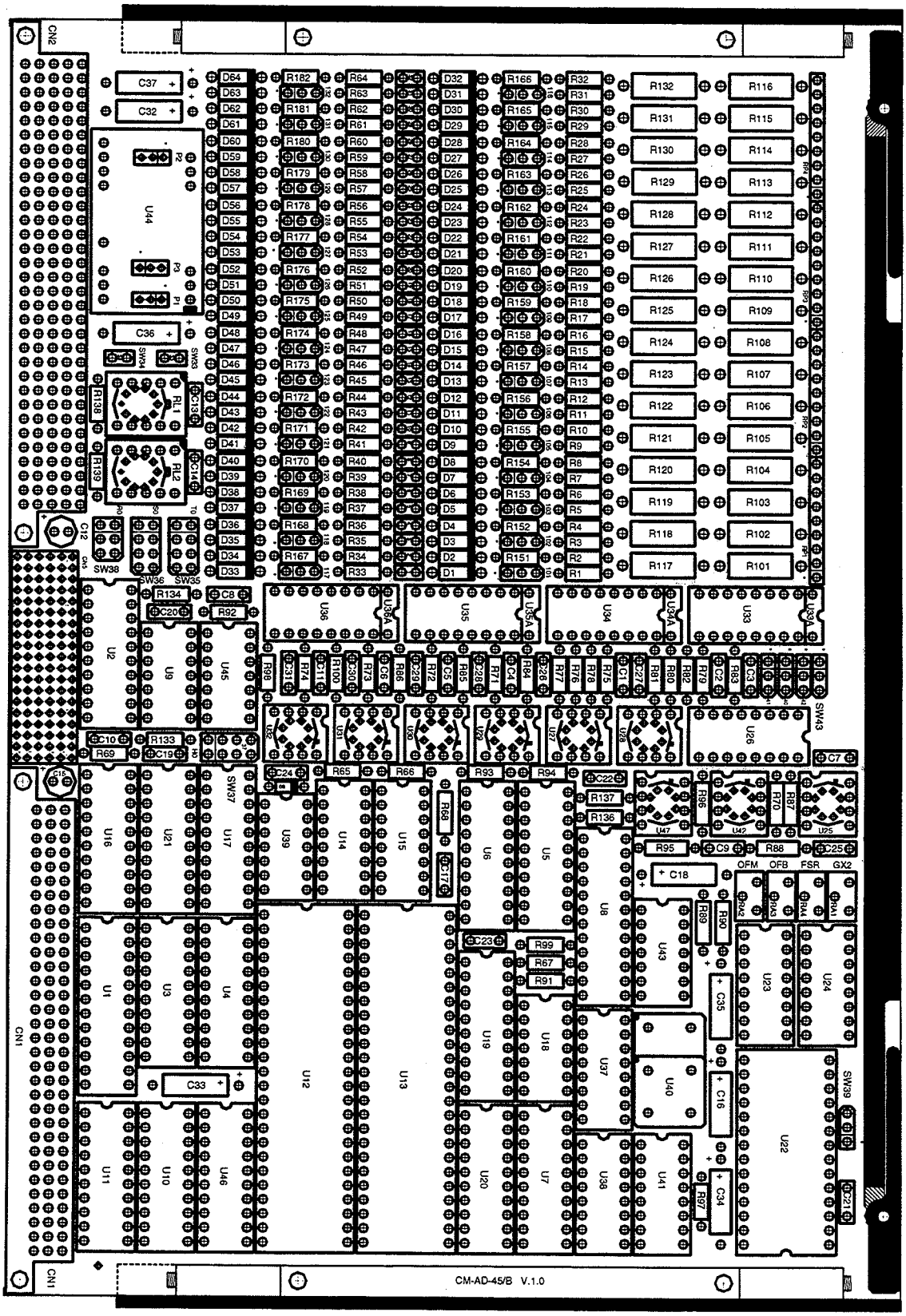


Figure 4.2.- CM-AD-45/B Silk screen and component layout.

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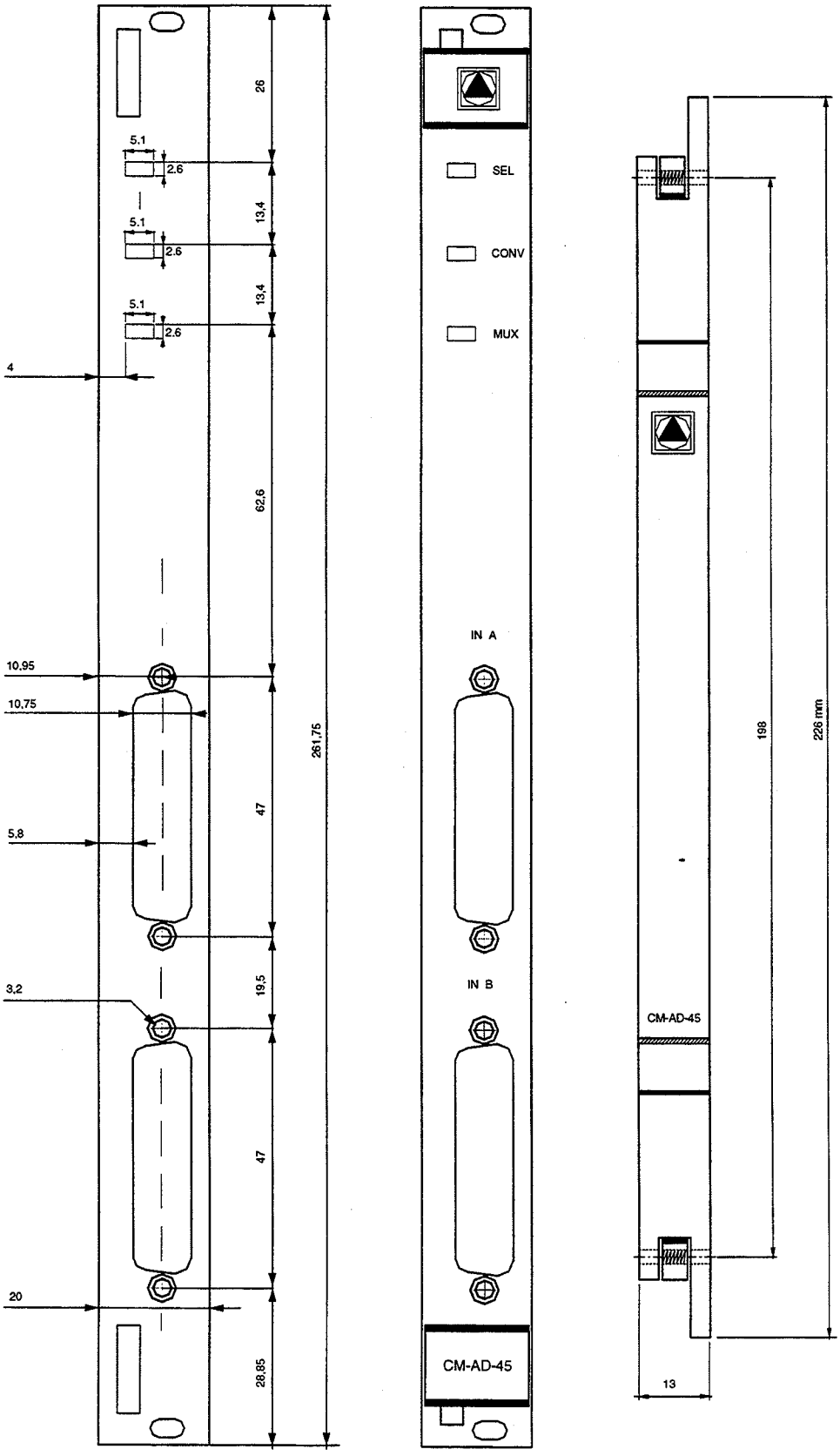


Figure 4.3.- CM-AD-45/A & CM-AD-45/B front panel.

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4.2.- PCB Specifications.

The **CM-AD-45/A** & **CM-AD-45/B** implement a multilayer, high quality PCB design which offers the user the following advantages:

- Entirely developed by CAD and accomplished by photoplotter.
- 100% electrically tested.
- PCB external layers provided with component silk screen and anticorrosion solder mask.
- Class 5 PCB design; track widths up to 150 microns.
- No external signal tracks available either on the soldering or component side. This feature prevents track corrosion as well as the risk of track breakage.
- Shielding layer connected to ground. This results in minimum external electromagnetic radiation and minimum parasite noise on-board.
- SMD decoupling capacitors for each IC located on the solder side.
- Military versions supplied with sophisticated, cooled PCB which is provided with metallic thermal overlay.

The military PCB offers three additional features:

- Very high capability to withstand shock and vibration; better than MIL-STD-810 requirements (Methods 514 and 516).
- Highly improved component heat dissipation for both free-air convection or when inserted in a conduction cooled rack.
- All components work at an average homogeneous temperature at all points of the module. This feature, combined with CMOS design, greatly increases component life and MTBF rating.

OBSERVATION

All **CM-AD-45** mechanical versions and temperature ranges, including the cooled PCB series, are mechanically compatible with VMEbus standard enclosures available on the market. Additionally, the user can combine CM's military modules with commercial modules in the same enclosure.

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4.3.- Electrical Specifications.

The **CM-AD-45** incorporates the most advanced technology by using low power and high speed HCT, ACT and FCT CMOS chips featuring operation speeds up to 120 MHz. It implements a high degree of logic integration by using high speed 15 nsec CMOS GALs.

Since this module implements TTL digital units the main power supply voltage is +5 VCC. It is necessary to supply the auxiliary +12 VDC voltage in order to power most analog devices.

Table 4.4, below, shows the **CM-AD-45** voltage and current requirements. Voltage tolerances are also specified.

VMEbus Power	Supply Voltage	Voltage Tolerance
Main supply VCC	+5 VDC @ 350 mA	+4.85 to +5.25 VDC
Auxiliary supply	+12 VDC @ 135 mA	+11.7 to +13 VDC

Table 4.4.- CM-AD-45 power requirements.

OBSERVATION

All required supply voltages are available on any standard J1 VMEbus backplane and are applied to the board through the P1 DIN 41612 connector.

The **CM-AD-45** is a low heat product with a power consumption of about 3 Watts.

Table 4.4 rates should be considered as typical values. Slight power consumption deviations may be encountered depending on the board temperature range or board operation.

IMPORTANT

Operation exceeding the maximum specified supply voltage may cause permanent damage to the module circuitry. Damage caused in this manner is not covered by the guarantee.

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4.4.- Temperature Ranges.

The **CM-AD-45/A** & **CM-AD-45/B** boards have been designed to operate in 4 different temperature ranges: Commercial, Industrial, Militarized-Rugged and full Military-883. All temperature range modules are 100% compatible at the functional and programming levels meaning that all software developed for any board range will run on the others.

Commercial version:

The commercial version incorporates low cost integrated circuits in plastic package rated from 0 to +70 °C. The module is specified for an operational range from 0 to +60 °C.

This version is subjected to a "basic level" quality test.

The reference for the commercial version is: **CM-AD-45 C**.

Industrial version:

The industrial version incorporates industrial class integrated circuits in plastic packages rated from -40 (-25) to +85 °C. The module is specified for an operational range from -20 to +70 °C.

This version is subjected to a "medium level" quality test.

The reference for the industrial version is: **CM-AD-45 I**.

Military-Rugged + version:

The military rugged version is manufactured with ceramic package TTL integrated circuits. Digital logic is based on 54XX series integrated circuits and is rated for -55 to +125 °C. This version includes conduction cooled PCB with metallic thermal overlay. The I/O connectors and passive components are qualified per MIL-C-55302 or MIL-C-24308. The module is specified for an operational temperature range from -40 to +85 °C.

This version is subjected to an "advanced level" quality test.

The reference for the Military-Rugged version is **CM-AD-45 R+**.

Full Military-883 version:

This full Military-883 version incorporates a conduction cooled PCB and ceramic MIL-STD-883B/C qualified components (-55 to +125 °C).

Connectors and passive components have the same MIL-STD qualification specified in the R+ version. The board has an operational temperature range from -50 to +90 °C.

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This module is subjected to an "advanced level" quality test, with certificate for MIL-STD-810D, methods 501.2 and 502.2.

The reference for the full Military-883 version is **CM-AD-45 883**.

IMPORTANT

Operation exceeding the maximum specified temperature range may cause permanent damage to the module circuitry. Damage caused in this manner is not covered by the guarantee.

IMPORTANT

CM Computer recommends that the module not be operated during extended periods of time near the maximum specified temperature limits since this will result in premature degradation of components and a reduction in the useful life of the board circuitry.

In those projects in which the environmental conditions are very severe or when the module is frequently required for operation near the maximum temperature limits, the purchase of a superior temperature range module (i.e. Military-Rugged rather than Industrial) is recommended.

OBSERVATION

Since all temperature versions are software compatible, when developing military projects it is possible to use a low cost commercial **CM-AD-45 C** for prototypes or software development and implement the **CM-AD-45 R+** or **CM-AD-45 883** in the final application.

OBSERVATION

The input resistor arrays are supplied by default mounted on sockets. In military applications, the sockets can be a cause of malfunction due to mechanical shocks, vibrations, etc. In such applications, **CM** suggests fixing the resistors by welding the two end pins.

OBSERVATION

Some reliability considerations should be kept in mind for the on-board jumper blocks which will be customized by the user. In those modules destined for military applications the original plastic jumper supplied with the board should be removed and the pins bound with wire wrapped cable or by soldering.

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4.5.- Jumper Connections.

The on-board switches and jumpers allow specific hardware configurations.

This section introduces each jumper function with the objective of assisting the user when customizing the module for specific requirements.

The attached **CM-AD-45** PCB silk screen details switch lay-out. The PCB silk screen is labeled with generic "SWXX" notation *(see **Figure 4.5**)*. Each switch or jumper block has a reference position which is denoted by the "A" character or a dash (-).

Jumpers are two pin switches with no reference position. A jumper allows two possibilities: jumper removed (OFF) or jumper inserted (ON). When a jumper plastic bridge is inserted it short circuits the two jumper pins. When it is removed both pins are left unconnected.

Jumper blocks are arrays of single jumpers which define a common function. Each single jumper within a block is named with a letter followed by a number. For example, SW35 is a 4x2 jumper block composed of 4 individual jumpers named as T0 (-), T1, T2 & T3.

The **CM-AD-45** jumpers are grouped and described according to their functional use. The set of jumpers to be customized by the user are the following:

a) VME64x P2 input signal wiring. Jumpers SW1 to SW34.

A block of jumpers allow connecting or removal of input signals to rows a & c of the VMEbus P2 VME64x connector. This set of jumpers is labeled as follows: -

- SW1 connects/removes input channel 1.
- SW2 connects/removes input channel 2.
- . . . . . .
- SW31 connects/removes input channel 31.
- SW32 connects/removes input channel 32.
- SW33 connects/removes the analog ground to row c.
- SW34 connects/removes the analog ground to row a.

When all these jumpers are removed, the VMEbus P2 rows a and c input terminals are fully isolated with respect to the **CM-AD-45** internal circuitry.

IMPORTANT

Notice that the set of P2 jumpers are intended for isolating the **CM-AD-45** input signals with respect to P2 rows a and c. In order to avoid noise, remove all jumpers in those applications using input signals only through the front panel connectors.

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b) VMEbus address mapping. Jumper blocks SW35 and SW36.

There are two 4x2 jumper blocks for selecting the VMEbus address range. Both jumper blocks are extensively explained in Chapter 5.

c) Interrupter Status-ID Vector configuration. SW37.

The Status-ID Vectors supplied by the **CM-AD-45** Interrupter in response to valid IACK* cycles are user defined. Jumper block SW37, 4x2 size, is intended for this purpose. By means of SW37 the user can define the 4 MSB bits of the supplied Status-ID Vectors. *See **Section 9.4** for details.*

d) Interrupter priority level selection. SW38.

A 3x2 jumper block, reference SW38, allows selection of the desired Interrupt priority level on the VMEbus. This jumper block selects one of the 6 priority levels available on the bus (IRQ2* through IRQ7*). *See **Section 9.4** for details.*

e) A/D Converter FSR configuration. SW39.

This 3x1 switch selects the AD-1674 converter chip FSR.

- Insert jumper in position A for a chip input scale of 0-20 V unipolar or ±10 V bipolar.
- Insert jumper in position B for a chip input scale of 0-10 V unipolar or ±5 V bipolar.

f) SW40, SW41, SW42 & SW43.

These four 3x1 switches define the **CM-AD-45** analog input type: single-ended or differential.

- Connect the 4 jumpers to position A for configuring the board as 32 single-ended channels.
- Connect the 4 jumpers to position B for configuring the board as 16 differential channels.

g) Input attenuattor & DC current configuration. SW101 thru SW132.

This set of 32 switches, 3x1 size enable/disable the 10:1 voltage input attenuator and current resistor. Each switch is completely independent and affects only its associated channel.

SW101 is assigned to input channel 1.
SW102 is assigned to input channel 2.
. . . . . .
SW132 is assigned to input channel 32.

- Remove all plastic jumpers when the board is configured as differential inputs.
- Remove all plastic jumpers of those channels receiving input voltages less than or equal to 10 Volts either in unipolar or bipolar.
- Insert jumper in position A of those channels receiving input voltages higher than 10 Volts either in unipolar or bipolar. This connects the 10:1 input voltage attenuators.
- Insert jumper in position B of those channels receiving DC current in mA range. This connects the 100 Ω current to voltage resistor.

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OBSERVATION

The **CM-AD-45** board is usually factory fitted by default as follows:

- Board mapped in VMEbus address $C6 0000.
- VMEbus IRQ4* level (Interrupter).
- Default IRQ* Status ID vectors: $81 & $82.
- A/D converter configured for 0-10 VFSR.
- Attenuators disabled (direct input ranges).
- Input current resistors disabled (voltage inputs).
- Inputs received by front panel and P2 connectors. J2 jumper set enabled.
- Input impedance fixed to 470 KΩ.

IMPORTANT

The user must be careful when changing the **CM-AD-45** board jumper configuration. Before changing any jumper, the user should study each associated section and figure in this manual in order to be sure of its function within the module. If an incorrect configuration is performed the board may not work properly.

It is also recommended that a copy of the original factory jumpers default configuration be made before making any changes.

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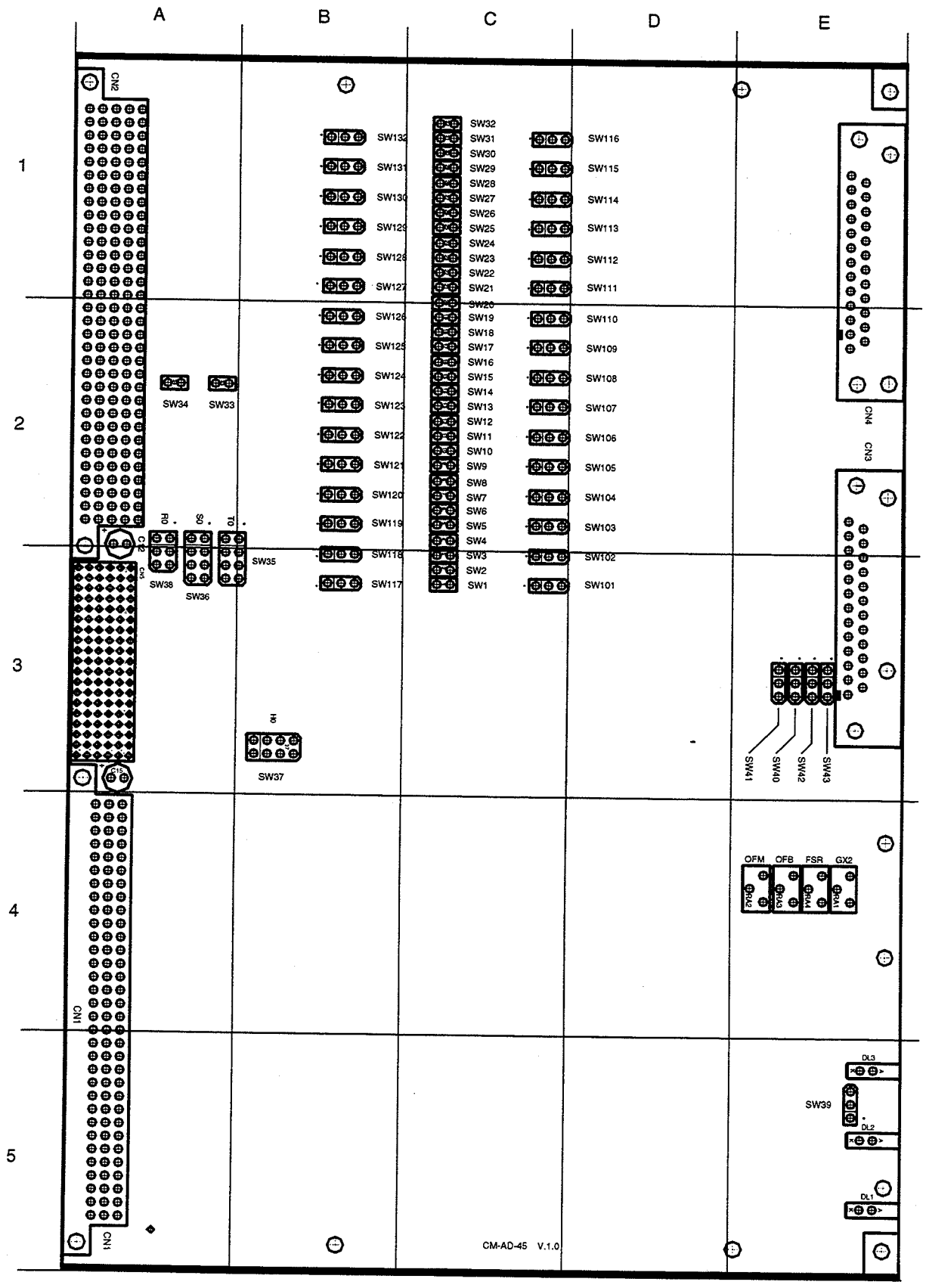


Figure 4.5.- CM-AD-45 jumper layout.

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4.6.- Front Panel Application Connectors.

The **CM-AD-45** module offers very flexible I/O signal wiring since all I/O signals are available both on front panel and P2.

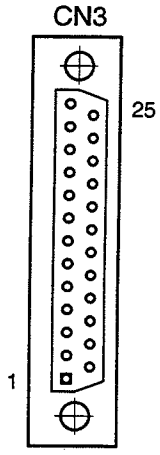
The front panel connector is cannon 25 pin Type D compatible. This is a male, angled solder pin for PCB mounting, row separation of 2.54 mm. This part is manufactured by HARTING Germany with P/N=0966322780.

There are two cannon connectors labeled as "INA" and "INB" in the front panel. These connectors are pin-out compatible with the predecessor **CM-AD-35** module.

OBSERVATION

The front panel connectors are industry standard, and therefore the female model needed for wiring the application signals can be found easily in several vendor catalogues (HARTING, FCT, AMP, AMPHENOL, etc).

Figure 4.6 shows the connector CN3 (INA) signal pin-out. This connector wires input channels 1 thru 16 in single-ended mode, or input channels 1 thru 8 in differential mode.

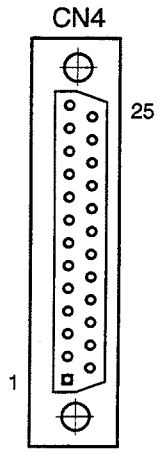


PIN	Single-ended	Differential	PIN	Single-ended	Differential
1	Channel 1	Channel 1+	14	Channel 9	Channel 1-
2	Channel 2	Channel 2+	15	Channel 10	Channel 2-
3	GND	GND	16	GND	GND
4	Channel 3	Channel 3+	17	Channel 11	Channel 3-
5	Channel 4	Channel 4+	18	Channel 12	Channel 4-
6	GND	GND	19	GND	GND
7	Channel 5	Channel 5+	20	Channel 13	Channel 5-
8	Channel 6	Channel 6+	21	Channel 14	Channel 6-
9	GND	GND	22	GND	GND
10	Channel 7	Channel 7+	23	Channel 15	Channel 7-
11	Channel 8	Channel 8+	24	Channel 16	Channel 8-
12	GND	GND	25	GND	GND
13	GND	GND			

Figure 4.6.- CM-AD-45 Front panel INA connector pin-out assignment.

Figure 4.7 shows the CN4 connector (INB) signal pin-out. This connector wires input channels 17 thru 32 in single-ended mode, or input channels 9 thru 16 in differential mode.

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PIN	Single-ended	Differential	PIN	Single-ended	Differential
1	Channel 17	Channel 9+	14	Channel 25	Channel 9-
2	Channel 18	Channel 10+	15	Channel 26	Channel 10-
3	GND	GND	16	GND	GND
4	Channel 19	Channel 11+	17	Channel 27	Channel 11-
5	Channel 20	Channel 12+	18	Channel 28	Channel 12-
	GND	GND	19	GND	GND
7	Channel 21	Channel 13+	20	Channel 29	Channel 13-
8	Channel 22	Channel 14+	21	Channel 30	Channel 14-
9	GND	GND	22	GND	GND
10	Channel 23	Channel 15+	23	Channel 31	Channel 15-
11	Channel 24	Channel 16+	24	Channel 32	Channel 16-
12	GND	GND	25	GND	GND
13	GND	GND			

Figure 4.7.- CM-AD-45 Front panel INB connector pin-out assignment.

4.7.- P2 Application Connector.

The board implements a 5 row VME64x connector on P2. The connector soldered on the **CM-AD-45** is the model manufactured by HARTING GERMANY. This is a 5 row male connector, 160 contact, angled solder pins for PCB mounting with row separation of 2.54 mm.

The VMEbus P2 connector is Type C compatible. This connector class II reference is HARTING P/N=02011602101. The same connector in Class I is HARTING P/N=02011601101.

OBSERVATION

The **CM-AD-45** P2 connector is standard and therefore the female model needed for wiring the application signals can be found easily by the user in several vendor catalogues. For example, the Harting female unit for VMEbus backplane is: P/N=02021602301.

The VME64x P2 application connector pin-out is shown in ***Table 4.8.*** This connector wires the 32 analog input signals plus ground.

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PIN	Row z	Row a			Row b	Row c			Row d
	z	Single	Differential	Jumper	b	Single	Differential	Jumper	d
1	N.C.	N.C.	N.C.	-	Vcc	N.C.	N.C.	-	N.C.
2	N.C.	N.C.	N.C.	-	TTL GND	N.C.	N.C.	-	N.C.
3	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
4	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
5	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
6	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
7	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
8	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
9	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
10	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
11	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
12	N.C.	N.C.	N.C.	-	TTL GND	N.C.	N.C.	-	N.C.
13	N.C.	N.C.	N.C.	-	Vcc	N.C.	N.C.	-	N.C.
14	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
15	N.C.	N.C.	N.C.	-	N.C.	N.C.	N.C.	-	N.C.
16	N.C.	AN GND	AN GND	SW34	N.C.	AN GND	AN GND	SW33	N.C.
17	N.C.	CH1	CH1+	SW1	N.C.	CH9	CH1-	SW9	N.C.
18	N.C.	CH2	CH2+	SW2	N.C.	CH10	CH2-	SW10	N.C.
19	N.C.	CH3	CH3+	SW3	N.C.	CH11	CH3-	SW11	N.C.
20	N.C.	CH4	CH4+	SW4	N.C.	CH12	CH4-	SW12	N.C.
21	N.C.	CH5	CH5+	SW5	N.C.	CH13	CH5-	SW13	N.C.
22	N.C.	CH6	CH6+	SW6	TTL GND	CH14	CH6-	SW14	N.C.
23	N.C.	CH7	CH7+	SW7	N.C.	CH15	CH7-	SW15	N.C.
24	N.C.	CH8	CH8+	SW8	N.C.	CH16	CH8-	SW16	N.C.
25	N.C.	CH17	CH9+	SW17	N.C.	CH25	CH9-	SW25	N.C.
26	N.C.	CH18	CH10+	SW18	N.C.	CH26	CH10-	SW26	N.C.
27	N.C.	CH19	CH11+	SW19	N.C.	CH27	CH11-	SW27	N.C.
28	N.C.	CH20	CH12+	SW20	N.C.	CH28	CH12-	SW28	N.C.
29	N.C.	CH21	CH13+	SW21	N.C.	CH29	CH13-	SW29	N.C.
30	N.C.	CH22	CH14+	SW22	N.C.	CH30	CH14-	SW30	N.C.
31	N.C.	CH23	CH15+	SW23	TTL GND	CH31	CH15-	SW31	N.C.
32	N.C.	CH24	CH16+	SW24	Vcc	CH32	CH16-	SW32	N.C.

Table 4.8.- CM-AD-45 VME64x P2 application connector pin-out.

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4.8.- Technical Specification Summary.

SPECIFICATIONS		BOARD RANGE			
		COMMERCIAL	INDUSTRIAL	MIL-RUGGED+	MIL-883
Weight		405 g	430 g	630 g	660 g
Physical Dimensions	*Height*	233.35 mm	233.35 mm	233.35 mm	233.35 mm
	Depth	160 mm	160 mm	160 mm	160 mm
	Thickness	1.7 ± 0.1 mm	1.7 ± 0.1 mm	1.7 ± 0.1 mm	1.7 ± 0.1 mm
Temperature (Methods 501.3 & 502.3)	*Operating*	0 °C to +60 °C	-20 °C to +70 °C	-40 °C to +85 °C	-50 °C to +90 °C
	Storage	-40 °C to +85 °C	-50 °C to +90 °C	-55 °C to +125 °C	-55 °C to +125 °C
Power Consumption		3.4 Watts	3.4 Watts	3.6 Watts	3.6 Watts
Vibration (Method 514.4)	*Sine*	2g from 5 to 2,000 Hz	2g from 5 to 2,000 Hz	5g from 5 to 2,000 Hz	5g from 5 to 2,000 Hz
	Random	0,002 g^2/Hz from 10 to 2,000 Hz	0,002 g^2/Hz from 10 to 2,000 Hz	0,1 g^2/Hz from 10 to 2,000 Hz	0,1 g^2/Hz from 10 to 2,000 Hz
Shock (Method 516.4)		20g peak sawtooth 11 ms	20g peak sawtooth 11 ms	40g peak sawtooth 11 ms	40g peak sawtooth 11 ms
Altitude (Method 500.3)		50,000 ft	50,000 ft	50,000 ft	50,000 ft
Humidity (Method 507.3)	*Operating*	0 to 95% non-condensing	0 to 95% non-condensing	0 to 95% non-condensing	0 to 95% non-condensing
	Non-Operating	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing	0 to 100% condensing
Acceleration (Method 513.4)		Up to 10g	Up to 10g	Up to 15g	Up to 15g
Salt Fog (Method 509.3)		5% ClNa 48h	5% ClNa 48h	5% ClNa 48h	5% ClNa 48h
IC Package		Plastic	Plastic-Ceramic	Ceramic	Ceramic
IC Temperature		0 °C to +70 °C	-25 °C to +85 °C -40 °C to +85 °C	-55 °C to +125 °C	-55 °C to +125 °C
IC Screening		N/A	N/A	883 in some parts	MIL-STD 883
Conduction Cooled PCB		N/A	N/A	YES	YES
Air Flow (max. T^a)		150 ft/min	150 ft/min	200 ft/min	200 ft/min
Board MTBF (25 °C)		110,000 Hours	165,000 Hours	215,000 Hours	240,000 Hours
Other		MIL-883 & MIL-Rugged+ boars are in compliance with MIL-STD-810E			

Figure 4.22.- CM-AD-45 Technical Specification Summary.

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Chapter 5.- VME Address Map.

This chapter contains details on the memory range occupied by the **CM-AD-45** module when connected to a VMEbus backplane.

5.1.- CM-AD-45 Address Decoder.

The address decoder is a functional block intended for mapping in a flexible manner, one or more **CM-AD-45** modules within the VMEbus standard addressing range ***(see Figure 5.1)***.

Each board occupies a 4 KB address block (2048 Words of dual port RAM). Two jumper blocks, SW35 & SW36, provide up to 256 mapping possibilities. This module is a slave unit with a generic address type **"$Z6 YXXX"**, where "Z" & "Y" are defined by the user through the on-board jumpers.

SW36 (S0, S1, S2 & S3) is a 4x2 jumper block which defines the module x1MB mapping base address. SW36 jumper is a "Z" nibble selector. The user can select among 16 possibilities, each one associated with 1 of the 16 MB available in the standard VMEbus range *(see **Figure 5.1**)*.

S3	S2	S1	S0	Board Address
OFF	OFF	OFF	OFF	$F6 YXXX
OFF	OFF	OFF	ON	$E6 YXXX
OFF	OFF	ON	OFF	$D6 YXXX
OFF	OFF	ON	ON	$C6 YXXX
OFF	ON	OFF	OFF	$B6 YXXX
OFF	ON	OFF	ON	$A6 YXXX
OFF	ON	ON	OFF	$96 YXXX
OFF	ON	ON	ON	$86 YXXX
ON	OFF	OFF	OFF	$76 YXXX
ON	OFF	OFF	ON	$66 YXXX
ON	OFF	ON	OFF	$56 YXXX
ON	OFF	ON	ON	$46 YXXX
ON	ON	OFF	OFF	$36 YXXX
ON	ON	OFF	ON	$26 YXXX
ON	ON	ON	OFF	$16 YXXX
ON	ON	ON	ON	$06 YXXX
Y = According to SW35; XXX = 4KB board range				

Figure 5.1.- Board 1MByte boundary mapping versus SW36.

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Once the 1MB boundary has been selected via SW36, the board offers another 4x2 jumper block SW35 (T0, T1, T2 & T3) which defines the module address Y nibble. This allows the insertion of up to 16 **CM-AD-45** modules in the same backplane per each 1MB boundary selected in SW36 *(see **Figure 5.2**)*.

T3	T2	T1	T0	Module N°	Board Address Range
OFF	OFF	OFF	OFF	16	$Z6 F000 - $Z6 FFFF
OFF	OFF	OFF	ON	15	$Z6 E000 - $Z6 EFFF
OFF	OFF	ON	OFF	14	$Z6 D000 - $Z6 DFFF
OFF	OFF	ON	ON	13	$Z6 C000 - $Z6 CFFF
OFF	ON	OFF	OFF	12	$Z6 B000 - $Z6 BFFF
OFF	ON	OFF	ON	11	$Z6 A000 - $Z6 AFFF
OFF	ON	ON	OFF	10	$Z6 9000 - $Z6 9FFF
OFF	ON	ON	ON	9	$Z6 8000 - $Z6 8FFF
ON	OFF	OFF	OFF	8	$Z6 7000 - $Z6 7FFF
ON	OFF	OFF	ON	7	$Z6 6000 - $Z6 6FFF
ON	OFF	ON	OFF	6	$Z6 5000 - $Z6 5FFF
ON	OFF	ON	ON	5	$Z6 4000 - $Z6 4FFF
ON	ON	OFF	OFF	4	$Z6 3000 - $Z6 3FFF
ON	ON	OFF	ON	3	$Z6 2000 - $Z6 2FFF
ON	ON	ON	OFF	2	$Z6 1000 - $Z6 1FFF
ON	ON	ON	ON	1	$Z6 0000 - $Z6 0FFF
Z according to SW36					

Figure 5.2.- Board addressing versus SW35 (Y selector).

OBSERVATION

The **CM-AD-45** is delivered factory fitted with SW35 & SW36 configured with the board base address at "$C60000".

OBSERVATION

The **CM-AD-45** VMEbus addressing range maintains backward compatibility with the previous generation **CM-AD-35** modules. Therefore, those customers using the older **CM-AD-35** can work with the **CM-AD-45** without modification of any software driver developed for the previous board at any base address.

OBSERVATION

When multiple **CM-AD-45** modules are inserted in a backplane these can be mapped in consecutive addresses, resulting in stacking of all available channel buffers in memory, one after the other.

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Chapter 6.- Module Control Register.

This chapter is dedicated to the **CM-AD-45** Module Control Register. The MCR is the only programmable section of the **CM-AD-45** board.

6.1.- CM-AD-45 MCR Memory Mapping.

The following table, ***Table 6.1***, shows the on-board register allocation when mapped at the generic VMEbus address. The table shows both readable and writeable addresses.

Read Cycles	Write Cycles	Word Offset Address	VME Address
Dual port RAM Word 0	Module Control Register	Word 0 (Base Address+0)	$Z6 Y000
Dual port RAM Word 1	Not Implemented	Word 1 (Base Address+2)	$Z6 Y002
Dual port RAM Word 2	Not Implemented	Word 2 (Base Address+4)	$Z6 Y004
.....	.....	.....	.....
Dual port RAM Word 2047	Not Implemented	W 2047 (Base Addr+4094)	$Z6 YFFE

Table 6.1.- CM-AD-45 internal Word register allocation.

Once the board address has been selected by configuring SW35 & SW36, each module occupies 2048 consecutive 16 bit Word memory positions.

In read mode, all these Words correspond to the on-board dual port RAM. These positions can be read by the VMEbus master at any moment in order to obtain the current input channel conversion data.

In write mode, the first Word corresponds to the Module Control Register. The user must configure the board for its application by programming the appropiated bits in the MCR.

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6.2.- Module Control Register bits.

Each Control Register bit function is summarized in the following ***Table 6.2.***

BIT	NAME	SECTION	DESCRIPTION	LOGIC STATE
0	BUFSIZE	RAM ADDRESS	Defines the SRAM storage buffer size (see chapter 5)	0...32/2x16 Words 1...2048 Words
1	IRQENA	INTERRUPTER	Enables/Disables the on-board Interrupter which asserts a VMEbus IRQ* at the end of the current sampling cycle.	0...No IRQ (disabled) 1...End of cycle IRQ*
2	FREE/STOP	CYCLE CONTROLLER	Selects a single step cycle (1 mux-sampling cycle & stop), or free running operation (indefinite mux-sampling cycles).	0...Free-running 1...Single step cycle
3/4	SPEED	TIME BASE	Selects the A/D converter sampling rate among 4 different speed options.	0/0...100Ksps-10µs 0/1...50Ksps-20µs 1/0...25Ksps-40µs 1/1...12.5Ksps-80µs
5/6	GAIN POLARITY	AD CONVERTER	Select the input range. These 2 bits define the input range Gain and Polarity. The board input range also depends on SW39 and the 10:1 attenuator.	0/x...Gain x1 1/x...Gain x2 x/0... Unipolar x/1... Bipolar
7	MUX-FIXED	CYCLE CONTROLLER	Controls the analog multiplexer operation. Selects between incremental multiplexing (counter-up) or fixed channel selection according to MCR Bits 8 thu 12.	0...Multiplexed cycle 1...Fixed channel
8	A0	MUX ADDRESS	Defines fixed channel address A0.	00000...Channel 1 00001...Channel 2
9	A1	MUX ADDRESS	Defines fixed channel address A1.	00010...Channel 3 .....
10	A2	MUX ADDRESS	Defines fixed channel address A2.	....
11	A3	MUX ADDRESS	Defines fixed channel address A3.	..... 11101...Channel 30
12	A4	MUX ADDRESS	Defines fixed channel address A4.	11110...Channel 31 11111...Channel 32
13	MUX-BIT	MUX 3	Selects normal channel sampling or Built In Test cycle.	0...Input ch. sampling 1...BIT voltage samp.
14	CH1/16 BIT	MUX1 & MUX2	Enable Built In Test mode of channels 1 thru 16.	0...BIT Disabled 1...BIT Enabled
15	CH17/32 BIT	MUX3 & MUX4	Enable Built In Test mode of channels 17 thru 32.	0...BIT Disabled 1...BIT Enabled

Table 6.2.- Module Control Register bits.

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6.3.- Programming the Module Control Register.

Programming the Module Control Register is achieved by writing a 16 bit value in the board base address. The data stored in the MCR is directly latched from the VMEbus D00-D15 data bus.

IMPORTANT

The MCR is accomplished with output latches and therefore the written value can not be read back through software. The latches have a "clear" pin driven by the VMEbus SYSRES*. Therefore all MCR bits are cleared to logic '0' after asserting the SYSRES* line.

It is recommended that **CM-AD-45** programmer define a software variable in RAM which is used to update and store the Module Control Register current value. This Word size variable would contain the current MCR value so it might be called "copy_mcr" for example. The use of this auxiliary variable would allow the programmer to manipulate individual bits of the Module Control Register prior to copying the contents of the variable into the MCR.

OBSERVATION

Clearing all Module Control Register bits will set the **CM-AD-45** to its basic operational mode. In this case no interrupts or extra Built-In-Test functions are activated and the **CM-AD-45** is functionally similar to the **CM-AD-35**. MCR Bits 14 and 15 were not used in the **CM-AD-35** and have been incorporated in the **CM-AD-45** in order to improve the module BIT capability.

Table 6.3 shows the relationship between the VMEbus D00-D15 data lines and the 16 input channels read by the master during a Word access.

D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

Table 6.3.- MCR bits versus VMEbus D00-D15 lines.

IMPORTANT

The **CM-AD-45** counting and multiplexing circuitry is reset every time the master accesses the MCR (Word write cycle). When the access is completed, the on-board counters are released again, so it will start counting and multiplexing starting from input channel 1. This is necessary since the status of the current RAM buffer multiplexed channel would be unpredictable if the MCR were to change configuration in the middle of an in progress multiplexing-sampling cycle.

OBSERVATION

Incidental information describing the functionality of the Module Control Register bits may be found throughout this user's manual.

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Chapter 7.- Analog to Digital Conversion.

This chapter focuses on the input stage and analog signal path of the **CM-AD-45** board. Complementary sections will help the user to calibrate the board when required.

7.1.- CM-AD-45 Input Stage.

The functional block diagram of the **CM-AD-45** input stage is shown in ***Figure 7.1.***

This stage is repeated for each channel. It is composed of:

a) A parallel resistor, connected between the input signal and ground. This resistor fixes the Zin impedance (usually 470KΩ). The Zin resistor eliminates noise, especially from inused channels that remain disconnected from the external application.

b) The Zin resistor is complemented by a current-to-voltage high precision resistor Rma. This is a 100Ω impedance that can be optionally grounded by connecting jumper SWxx to position B. This is required when operating with current input signals.

c) The next stage is composed of the 10:1 voltage attenuator (impedances RP & RAT).

The RAT impedance can be optionally grounded by connecting jumper SWxx to position A. This is required when operating with input voltages above 10 Volts of full scale range. The board input impedance is 10KΩ for these ranges.

d) Signals obtained from the resistor network are properly multiplexed and applied to single-ended or differential gain controlled amplifiers.

e) Analog signals, after being properly scaled and amplified, are sampled and converted to digital levels by means of the AD1674 chip.

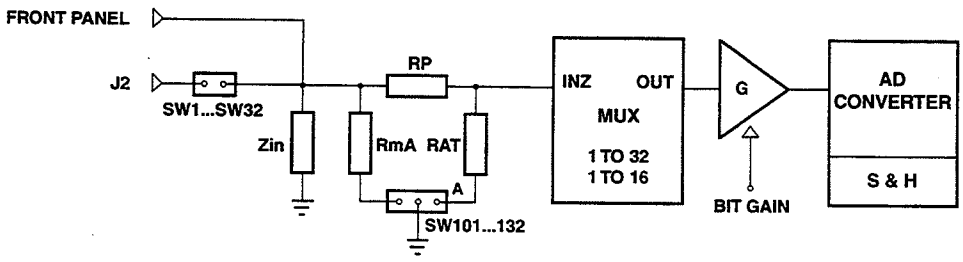


Figure 7.1. CM-AD-45 input stage block diagram.

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7.2.- CM-AD-45 Input Impedance Considerations.

The **CM-AD-45** input impedance is fixed by the resistor arrays RP1, RP2, RP3 & RP4.

The factory default 470 KΩ value is well suited for most voltage input ranges and sampling rates. However, there is an exception in case the of a bipolar range operating at 100 Ksps. In this case some accuracy degradation may occur.

This accuracy limitation may somtimes appear when operating at full sampling speed, using bipolar range and with high impedance input resistors. The combination of the three factors makes the input multiplexers operate at the limit of their settling time, especially during multiplexing transitions between consecutive channels of different polarity. Accuracy may be affected slightly in this case.

If the sampling rate is kept to 50 Ksps the factory supplied impedance resistors will guarantee peak accuracy in bipolar ranges.

In those applications which mandate 100 Ksps and bipolar range, the board input impedance must be decreased in order to maintain full accuracy. This inproves discharge of multiplexer internal capacitance, allowing better settling time. In this case, resistor arrays must be set in the range from 10 KΩ to 20 KΩ. This can be done by removing the factory resistors from sockets and replacing them by 10 KΩ parts.

OBSERVATION

Do not use high voltage input ranges above 25 Volts when installing 10 KΩ input impedance resistors. The power disipation of the array may exceed the manufacturer limits for this component.

7.3.- Direct Input Voltage Range (Volts).

The **CM-AD-45** supports a wide variety of input voltage ranges. All input channels can be driven with DC or AC.

The board voltage scale is defined by the following factors:

- Bit "Gain" of the Module Control Register (bit 5).
- Bit "Polarity" of the Module Control Register (bit 6).
- The A/D converter scale. This is jumper selectable at either 10 or 20 Volts through SW39.
- The input 10:1 attenuator status. If disabled, the board accepts unipolar/bipolar direct ranges up to an absolute value of 10 or 20 Volts FSR. If enabled, the board accepts input ranges up to10 times higher.

This section focuses on those boards configured with disabled attenuators (direct voltage ranges).

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Configuring SW39 in position B sets the AD1674 for 10 Volts FSR. For this case, ***Figure 7.2*** shows the **CM-AD-45** direct input ranges versus the Module Control Register bits 5 & 6.

10:1 Attenuator	SW39 Switch	Bit5 (Gain)	Bit6 (Polarity)	Input Range (Volts)
DISABLED	B (0-10 V)	0 (x1)	0 (Unipolar)	0-10 V
DISABLED	B (0-10 V)	0 (x1)	1 (Bipolar)	±5 V
DISABLED	B (0-10 V)	1 (x2)	0 (Unipolar)	0-5 V
DISABLED	B (0-10 V)	1 (x2)	1 (Bipolar)	±2.5 V

Figure 7.2.- Direct input ranges (SW39 in position B = 10 Volt scale).

Configuring SW39 in position A sets the AD1674 for 20 Volts FSR. For this case, ***Figure 7.3*** shows the **CM-AD-45** direct input ranges versus the Module Control Register bits 5 & 6.

10:1 Attenuator	SW39 Switch	Bit5 (Gain)	Bit6 (Polarity)	Input Range (Volts)
DISABLED	A (0-20 V)	0 (x1)	0 (Unipolar)	Not implemented
DISABLED	A (0-20 V)	0 (x1)	1 (Bipolar)	±10 V
DISABLED	A (0-20 V)	1 (x2)	0 (Unipolar)	Not implemented
DISABLED	A (0-20 V)	1 (x2)	1 (Bipolar)	±5 V

Figure 7.3.- Direct input ranges (SW39 in position A = 20 Volts).

7

OBSERVATION

Internally, the **CM-AD-45** OP-Amps can drive a maximum linear voltage of ±12 Volts. This is an obvious device limit since these amplifiers are powered with ±15 VDC obtained through an on-board DC/DC converter.

The amplifier output range limits the board operation in some scales when the converter is configured for 20 Volts FSR. This explains why same ranges are not inplemented in ***Figure 7.3.***

7.4.- 10:1 Input Voltage Attenuator (CM-AD-45/2).

Each channel is fitted with an independent 10:1 input attenuator. This unit is not available in version **CM-AD-45/1**. Connecting the attenuators is optional in single-ended channels. Boards operating in differential mode can not use attenuators.

Since attenuators are independent of the channel, they can be enabled/disabled individually. This means that some input channels may be selected for operation with direct input ranges (attenuator disabled), while other channels can be configured with enabled attenuators (input ranges above 10 Volts).

A set of switches (SW101 thru SW132) are implemented to enable/disable attenuators. SW101 corresponds to channel 1, while SW132 configures attenuator of channel 32.

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If 10:1 input attenuators are enabled and SW39 is placed in position B, ***Figure 7.4*** shows the accepted input voltage ranges as a function of the MCR bits 5 & 6.

10:1 Attenuator	SW39 Switch	Bit5 (Gain)	Bit6 (Polarity)	Input Range (Volts)
ENABLED	B (0-10 V)	0 (x1)	0 (Unipolar)	0-100 V
ENABLED	B (0-10 V)	0 (x1)	1 (Bipolar)	±50 V
ENABLED	B (0-10 V)	1 (x2)	0 (Unipolar)	0-50 V
ENABLED	B (0-10 V)	1 (x2)	1 (Bipolar)	±25 V

Figure 7.4.- 10:1 reduced voltage input ranges (SW39 in position B = 10 Volts).

If 10:1 input attenuators are enabled and SW39 is placed in position A, ***Figure 7.5*** shows the accepted input voltage ranges as a function of the MCR bits 5 & 6.

10:1 Attenuator	SW39 Switch	Bit5 (Gain)	Bit6 (Polarity)	Input Range (Volts)
ENABLED	A (0-20 V)	0 (x1)	0 (Unipolar)	Not implemented
ENABLED	A (0-20 V)	0 (x1)	1 (Bipolar)	±100 V
ENABLED	A (0-20 V)	1 (x2)	0 (Unipolar)	Not implemented
ENABLED	A (0-20 V)	1 (x2)	1 (Bipolar)	±50 V

Figure 7.5.- 10:1 reduced voltage input ranges (SW39 in position A = 20Volts).

7.5.- Input Current Range (mA).

All values shown in ***Figures 7.2 to 7.5*** refer to input voltage signals. When dealing with current input signals, switches SW101 to SW132 must be properly wired to position B.

The **CM-AD-45** maximum input current allowed is 50 mA. The board has a high precision 100 Ω resistor which acts as a current-to-voltage converter. The resistor ratio is 50 mA = 5 Volts. For example, if the board operates at ±2.5 V FSR, the available current range is 0 to ±25 mA.

The 100 Ω resistor can be factory fitted for a different value upon customer request.

The **CM-AD-45/1** version does not include current-to-voltage precision resistors. This item is implemented by default in the **CM-AD-45/2** version.

IMPORTANT

Current input ranges can be used only in single ended mode and with disabled attenuators.

Current input resistors are independent with respect to channel and can be individually enabled/ disabled. Some channels may operate with input voltages, while other channels may operate with input currents.

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The set of switches SW101 to SW132 are used to enable/disable current inputs. SW101 corresponds to channel 1 while SW132 affects channel 32.

OBSERVATION

The **CM-AD-45** supported current ranges are compatible with most commonly used industrial and military current ranges, typically 4-20 mA or 0-20 mA.

7.6.- A/D Sampling Characteristics.

The **CM-AD-45** board performs up to 100,000 A/D conversions per second. ***Figure 7.6*** shows a sinewave sample, measured at the A/D converter input pin. The board is configured to operate in fixed channel mode. The channel 1 of the oscilloscope shows the A/D converter-busy pin (STS). Channel 2 measures the input waveform. This is a 25 KHz & 3 VRMS sinewave applied to converter pin 13.

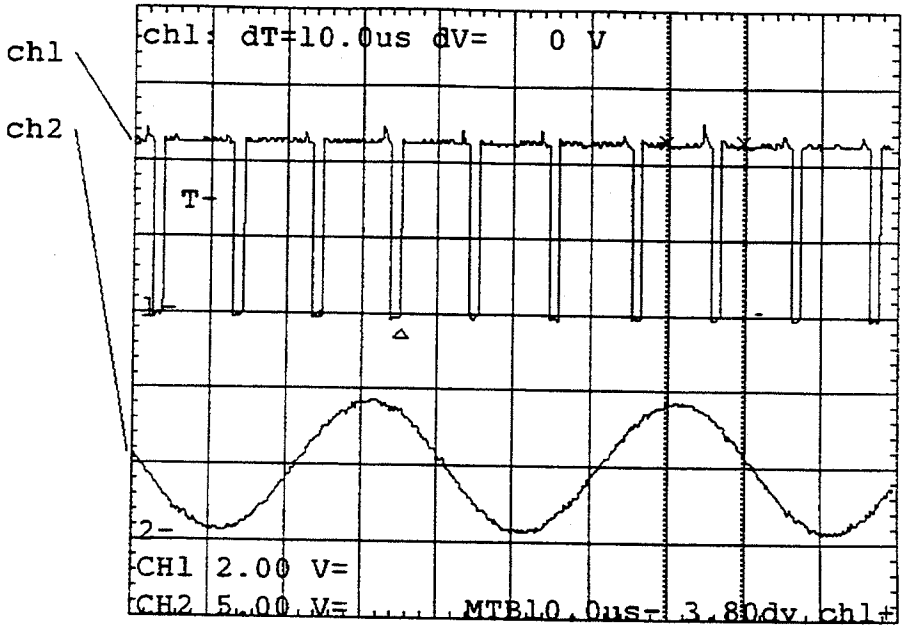


Figure 7.6.- CM-AD-45 25 KHz sinewave A/D sampling (Oscilloscope).

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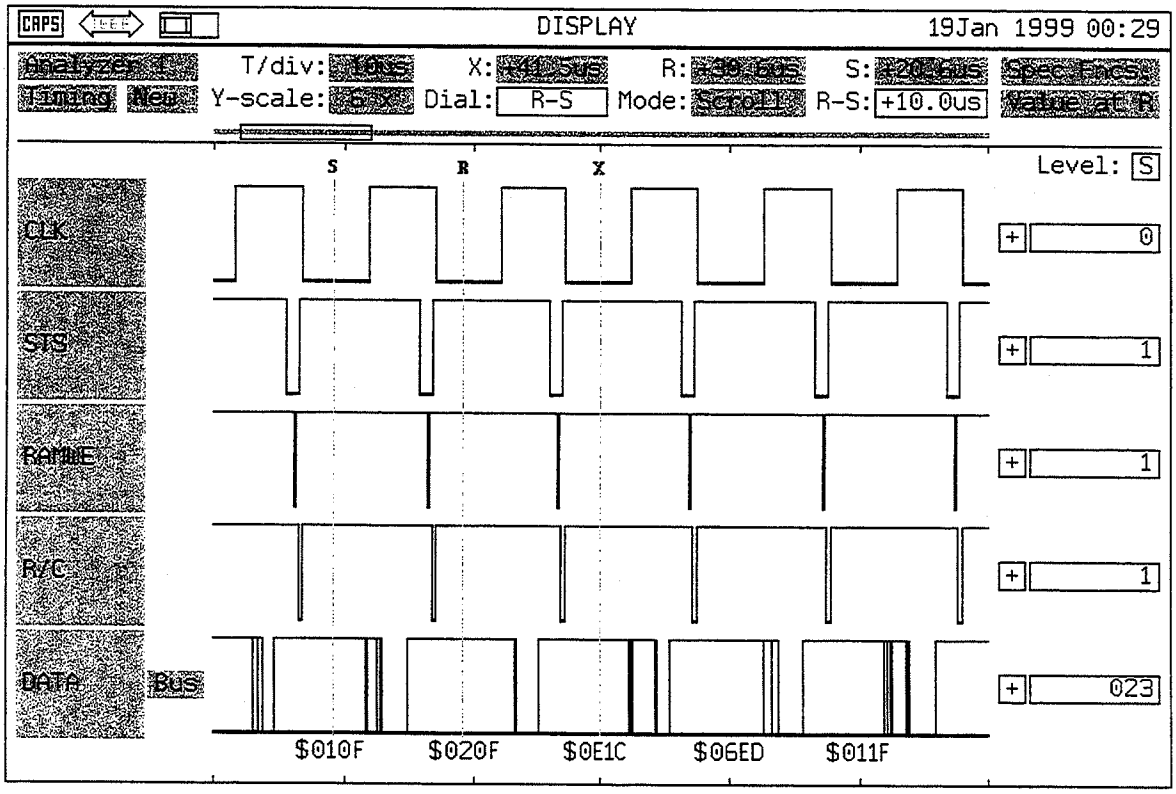


Figure 7.7.- CM-AD-45 25 KHz sinewave A/D sampling (Logic Analyzer).

Figure 7.7 shows the digital waveforms measured in the example of ***Figure 7.6.*** In this case, data is measured using a Logic Analyzer instead of a Digital Storage Oscilloscope. The **CM-AD-45** operates at 100 Ksps. This results in 4 samples per input waveform period (25 KHz sinewave).

The list of LA channels displayed in ***Figure 7.7*** are the following:

- CLK: 100 KHz time base sampling clock.
- STS: A/D Converter "busy" pin.
- RAMWE: Dual Port RAM "write enable" pulse.
- R/C: A/D Converter "start" conversion pulse.
- DATA: A/D Converter output data (12 bits Hex).

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7.7.- A/D Sampling Rate.

The **CM-AD-45** sampling rate is selected through bits 3 & 4 of the Module Control Register. The following options are available to the user.

Bit3	Bit4	Sampling speed	Conversion time
0	0	100 ksps	10 µsec
0	1	50 ksps	20 µsec
1	0	25 ksps	40 µsec
1	1	12.5 ksps	80 µsec

Table 7.8.- Board A/D sampling rate versus MCR bits 3 & 4.

OBSERVATION

The user can take advantage of the 100 Ksps maximum speed when sampling high frequency AC signals. When dealing with slower industrial applications in DC, it is recommended that the lowest rate (12.5 Ksps) be selected. This will minimize the VMEbus master dedication overhead required for reading the dual port RAM buffer.

7.8.- AC Input Signal Frequency.

The on-board converter AD1674 is fully specified for AC parameters (such as S/(N+D) ratio, THD, and IMD). With both AC and DC specifications the AD1674 is ideal for use in signal processing and traditional measurement applications. The following dynamic performance curves can be found in the AD1674 data sheet:

- Harmonic Distortion vs. Input frequency.
- S/(N+D) vs. Input Frequency and Amplitude.
- S/(N+D) vs. Input Amplitude.
- Nonaveraged 2048 Point FFT at 100 KSPS, fIN = 25.049 KHz.
- IMD Plot for fIN = 9.08 KHz (fa), 9,58 KHz (fb).

The **CM-AD-45** input amplifier stage is specified for DC to 50 KHz.

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7.9.- On-board A/D Converter Output Format.

The **CM-AD-45** circuitry does not process the data output format supplied by the AD-1674 converter chip. Therefore, converted data is directly stored into the dual port SRAM buffers. These RAM Words are directly read by the VMEbus master.

The 12 LSB bits of the VMEbus data bus (D00-D11) contains the converted data *(see **Figure 7.9**)*.

VMEbus RAM Word (16 Bits)						
BIT	**0**	**0**	**0**	**MSB**	**(12Bit AD conversion data)**	**LSB**
D15	D14	D13	D12	D11	D10 . . . D01	D00

Figure 7.9.- Dual port RAM Word data format.

Bit 15 (D15 of the VMEbus) contains Built-In-Test information as follows:

- The bit is read at logic 0 when the **CM-AD-45** is operating in standard sampling mode (sampling input channels).
- The bit is read at logic 1 while the board is in Built In Test MUX mode and all channels are sampling the internal +5 VDC test reference voltage. In this case, MCR Bit 13 is set to logic 1.

OBSERVATION

Bits on VMEbus data lines D12-D14 are tied to logic 0 and therefore will be read as 0.

7.10.- AD-1674 Output Data Format.

The **AD-1674** output data format is detailed in the following tables:

Unipolar mode:

AD1674 Input range scale: 0-10 Volts (SW39 to "B").

Output Binary Data	Output Hex Data	Analog Input Voltage	Comment
0000 0000 0000 to 0000 0000 0001	$000 to $001 (+1/2 LSB)	1.22 mV above ground (+1.22mV)	Unipolar offset
1111 1111 1110 to 1111 1111 1111	$FFE to $FFF (1 1/2 LSB)	3.66 mV below 10 V (9.9963 V)	Unip. full scale

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AD1674 Input range scale: 0-20 Volts (SW39 to "A").

Output Binary Data	Output Hex Data	Analog Input Voltage	Comment
0000 0000 0000 to 0000 0000 0001	$000 to $001 (+1/2 LSB)	2.44 mV above ground (+2.44 mV)	Unipolar offset
1111 1111 1110 to 1111 1111 1111	$FFE to $FFF (1 1/2 LSB)	7.32 mV below 10 V (19.992 V)	Unip. full scale

Bipolar mode:

AD1674 Input range scale: ±5 Volts (SW39 to "B").

Output Binary Data	Output Hex Data	Analog Input Voltage	Comment
0000 0000 0000 to 0000 0000 0001	$000 to $001 (1/2 LSB)	1.22 mV above minus full scale (-4.9988 V)	Bipolar offset
0111 1111 1111 to 1000 0000 0000	$7FF to $800 (1/2 LSB)	1.22 mV below midrange (-1.22 mV)	Midrange scale
1111 1111 1110 to 1111 1111 1111	$FFE to $FFF (1 1/2 LSB)	3.66 mV below full scale (4.9963 V)	Bipolar full scale

AD1674 Input range scale: ±10 Volts (SW39 to "A").

Output Binary Data	Output Hex Data	Analog Input Voltage	Comment
0000 0000 0000 to 0000 0000 0001	$000 to $001 (1/2 LSB)	2.44 mV above minus full scale (-9.9975 V)	Bipolar offset
0111 1111 1111 to 1000 0000 0000	$7FF to $800 (1/2 LSB)	2.44 mV below midrange (-2.44 mV)	Midrange scale
1111 1111 1110 to 1111 1111 1111	$FFE to $FFF (1 1/2 LSB)	7.32 mV below full scale (9.9926 V)	Bipolar full scale

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7.11.- Measurement Accuracy.

This board incorporates a 12 bit A/D converter with an accuracy error of ±1 LSB (optionally ±1/2 LSB).

The **CM-AD-45** measurement accuracy depends on the input range (scale) and the operating temperature.

a) Accuracy versus input voltage range (DC).

When a direct input range is selected up to 20 Volts, the 10:1 input attenuator is not connected. The board performs approximately 0.05% of full scale accuracy at calibration point ±20 °C. In the case of differential inputs the accuracy is limited to 0.1% of full scale approximately.

When operating with voltage ranges which require the isertion of the 10:1 attenuator (Vin > 20 Volts.), the board accuracy is decreased to approximately 0.2%.

Current input ranges in mA will perform at 0.1% full scale accuracy approximately.

b) Accuracy with respect to temperature.

This parameter is especially significant in military boards, since the CM 883 version is specified from -50 to +90 °C of operating range (-40 to + 85 °C for R+ versions). This results in 140 °C (or 125 °C) of difference between the low and high temperature limits.

The worst case will be when fitting a 50 ppm/°C converter. A board calibrated at room temperature may suffer up to 0.3% of accuracy drift at -40 °C.

When fitting a 10 ppm/°C converter accuracy drift will be better than 0.1% in the full 883 board temperature range.

c) Accuracy with respect to A/D sampling rates.

Above specified accuracy rates are valid for boards running at 50 Ksps or lower sampling rate. The **CM-AD-45** accuracy can be slightly decreased when running at 100 Ksps, due to input multiplexers limited settling time. Therefore, for those applications requiring higher measurement accuracy as a key parameter, CM recommends programming the board for 50 Ksps or lower.

OBSERVATION

In order to avoid analog parasite noise, the use of shielded cables is recommended for all input signals. Non used channels should be tired to GND.

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7.12. Built-In-Test Circuitry.

The **CM-AD-45** features on-board dual Built-In-Test capability through dedicated circuitry. The module incorporates two Built-In-Test relays, a Built-in-Test dedicated multiplexer and two test voltage signals. A general diagram of the BIT circuitry is shown in ***Figure 7.10.***

Each BIT relay tests two input multiplexers simultaneously, covering 16 channels in single-ended mode (8 differential). This architecture allows testing all on-board TTL chips.

A BIT relay can be switched on/off through a bit in the Module Control Register and is capable of testing two input channels in wrap-around mode.

The BIT Multiplexer acts as an analog switch that applies the test voltage to those amplifiers driving the A/D converter input. This device is switched on-off through a bit in the Module Control Register. The BIT multiplexer operation is backwards compatible with the **CM-AD-35**.

The **CM-AD-45** incorporates two voltage references intended for BIT purposes. These voltage references have a ±2% tolerance and supply +5 VDC and +2.5 VDC.

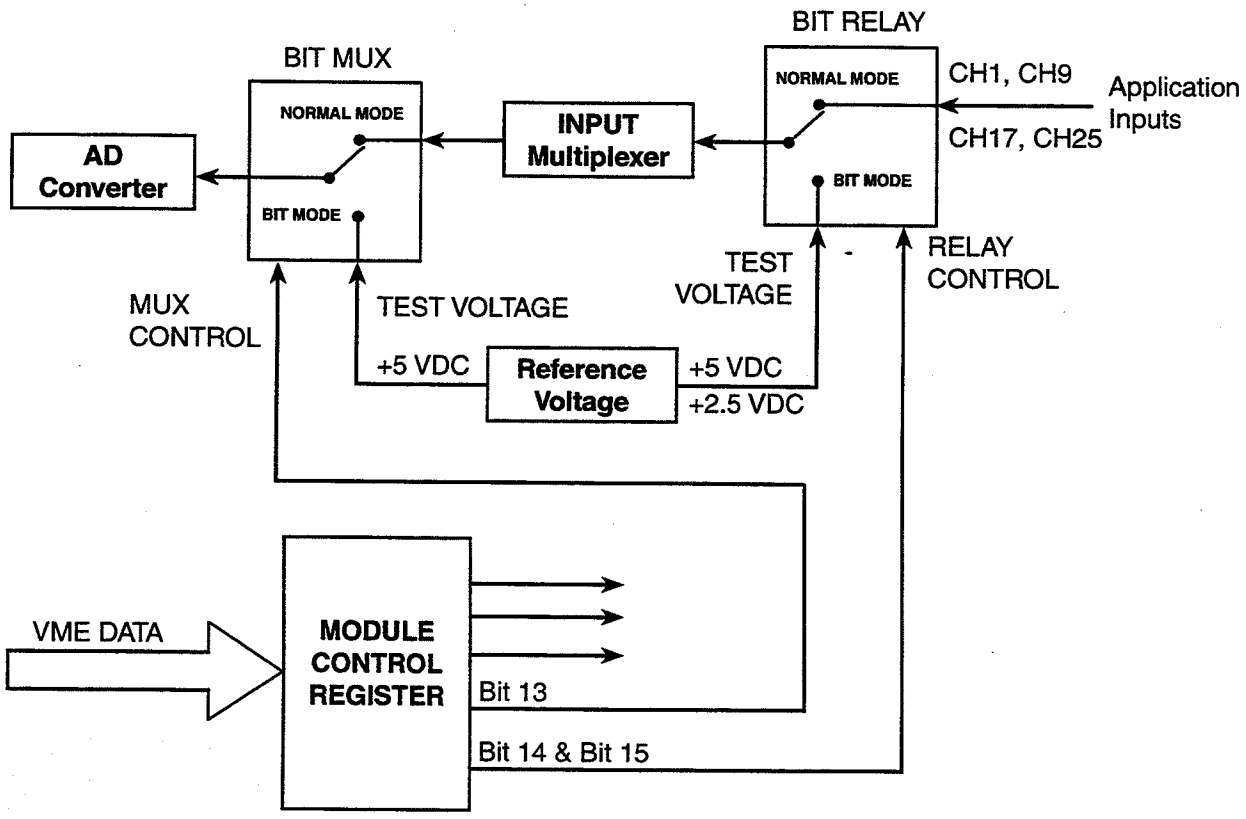


Figure 7.10.- Built-In-Test diagram.

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Figures 7.11 & 7.12 shows the channels assigned to each BIT Relay, and also describes the tested multiplexers and test voltage applied in each case.

BIT Relay	MCR Control Bit	Test Channel	Multiplexer	Test Voltage
Relay 1	Bit 14	CH1, CH9	MUX1 & MUX2	+5 VDC
Relay 2	Bit 15	CH17, CH25	MUX3 & MUX4	+5 VDC

Figure 7.11.- Built-In-Test Relays. Channels tested in single-ended mode.

BIT Relay	MCR Control Bit	Test Channel	Multiplexer	Test Voltage
Relay 1	Bit 14	CH1	MUX1 & MUX2	+2.5 VDC
Relay 2	Bit 15	CH9	MUX3 & MUX4	+2.5 VDC

Figure 7.12.- Built-In-Test Relays. Channels tested in differential mode.

Each Built-In-Test relay is capable of switching off and isolating two input channels from its associated external application voltage. Simultaneously it applies the local test voltage to the isolated area of the channels under test. These test signals "replace" the external application voltage, thus creating a wrap-around loop which allows checking the channel's multiplexers, the analog amplifiers, A/D converter as well as all TTL chips available on its signal network up to the VMEbus data buffers.

OBSERVATION

Built-In-Test cycles do not depend on the external application signals and can be dynamically executed under software control. During BIT cycles no input voltage from the external application is needed by the channels under test.

Since the test voltages are +5 VDC and +2.5 VDC, during BIT cycles the board input range must be set to 0-10 V FSR.

For BIT cycles using +5 VDC this results in conversions done in the middle of the scale. Data stored in the RAM buffer will have a value of $7FF approximately (+5 VDC ±2%).

For BIT cycles using the +2.5 VDC this results in conversions done at the quarter point of the scale. Data stored in the RAM buffer will have a value of $3FF approximately (+2.5 VDC ±2%).

OBSERVATION

Dedicated software is necessary during BIT cycles in order to properly perform the test loop described above. A simple software driver running on the master CPU is required in order to manage the Module Control Register, wait for switching delays, execute a multiplexing sampling cycle, read data on RAM, compare values, and close the test loop. This driver is available from **CM Computer**.

Built-In-Test cycles are also very useful for generating interrupts under software control. The asserted interrupts allows testing the VMEbus Interrupter.

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OBSERVATION

Wait at least 10 msec after switching the BIT relays before starting A/D conversions. This timing delay will provide for relay switching-time and prevent false conversions during switching transitions. This settling time is not required for the BIT multiplexer.

By setting to logic 1 Bit 13 of the Module Control Register, the board will start a Built In Test cycle using the dedicated multiplexer. While executing the mux BIT cycle, the +5VDC test voltage is applied through the multiplexer to the second stage amplifiers and A/D converter.

The test voltage replaces all input channel signals. A/D converted values are stored in the dual port RAM buffer. The BIT cycle fills with converted data the 32 or 2048 Word RAM buffer.

BIT MUX	MCR Control Bit	Test Channel	RAM Buffer	Test Voltage
Multiplexer	Bit 13	All	$87FF	+5 VDC

Figure 7.13.- Built-In-Test in Multiplexed mode.

OBSERVATION

During BIT cycles using the BIT Multiplexer the RAM buffer data MSB (Bit15) is set to logic 1.

7

IMPORTANT

The conbination of BIT cycles in Relay mode and in multiplexer mode allows testing 100% of the CM-AD-45 chips. Comparing the results obtained in each type of Built-in-Test may be usefull in order to identify faulty sections of the board.

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7.13.- Calibration.

The **CM-AD-45** module has been properly calibrated before customer delivery; the customer does not usually need to adjust it. However, board calibration is usually necessary when changing the position of SW39.

Calibration can also be useful in order to compensate voltage drops in the external wires, or due to fine adjustment in the application range, or when correcting accuracy drift after years of operation, etc.

This module incorporates 4 precision trimming resistors intended for calibration purposes. The calibration procedure is extremely simple provided that the steps explained below are carefully followed.

a) RA2 (OFM):

This 100 KΩ trimming resistor adjusts the A/D converter unipolar offset.

To adjust this parameter, program the board to operate in unipolar 0-10 VDC range. Notice that in this range the ±1/2 LSB step is equal to 1.22 mV.

Apply to the desired input channels a 0 Volt test input voltage.

Adjust RA2 resistor until the A/D converter outputs a $000 to $001 hexadecimal readout.

OBSERVATION

The unipolar offset can also be adjusted using an input value of 100 or 200 mVDC. Then, adjust RA2 until the exact equivalent digital value is obtained.

b) RA4 (FSR):

This 100 Ω trimming resistor adjusts the A/D converter full scale range. It is used either for unipolar or bipolar mode.

Unipolar adjustment.

Once the unipolar offset has been calibrated via RA2, the FSR adjustment can be performed in the unipolar 0-10 VDC range. The appropiate test input voltage ranges from +9.5 to +10 VDC.

If test input voltage is 10 VDC, then adjust RA4 resistor until the A/D converter outputs $FFE to $FFF hexadecimal readout. Otherwise, when using a test input voltage between +9.5 and +10 Volts, adjust RA4 to obtain the exact equivalent digital value.

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Bipolar adjustment.

Program the board for the ±5 VDC range. The FSR bipolar adjustment can be performed using any test input voltage ranging from +4.5 to +5 VDC.

If test input voltage is +5 VDC, then adjust RA4 resistor until the A/D converter outputs the $FFE to $FFF hexadecimal readout. Otherwise, when using a test input voltage between +4.5 and +5 Volts, adjust RA4 to obtain the exact equivalent digital value.

OBSERVATION

Adjusting RA4 in bipolar mode must be done after adjusting bipolar offset RA3.

c) RA3 (OFB):

This 100 Ω trimming resistor adjusts the A/D converter bipolar offset. To achieve this adjustment, program the board to operate in ±5 VDC range.

Use an stable input test voltage between -4.5 and -5 VDC. If using -5 VDC as test voltage, then adjust RA3 until the A/D converter outputs a $000 to $001 hexadecimal readout.

d) RA1 (Gx2):

This 500 Ω trimming resistor adjusts the programmable gain amplifier. This device is adjusted when operating at gain x2.

The programmable gain amplifier takes place in the following board input ranges: 0-5, 0-50, ±2.5 and ± 25 V.

The 0-50 and ±25 V ranges require connecting the 10:1 input attenuators.

In order to adjust RA1, program the board to operate in the 0-5 VDC range. Prior to this step, RA2 and RA4 must be calibrated as described in steps a) & b) of this section.

Use an input test voltage between +4.5 and +5 VDC. Then adjust RA1 until the exact digital value is obtained.

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Chapter 8.- Dual Port RAM Buffers.

8.1.- SRAM Data Buffers.

The **CM-AD-45** can fill the dual port RAM using buffers of different sizes. All buffers contain converted data and are properly self-updated by the on-board circuitry.

The buffer characteristics depend on two factors *(see **Table 8.1**):*

- Bit 0 of the Module Control Register. This bit defines the buffer size. It is user programmable in order to select buffers of 32 or 2048 Word of size.
- The board input channel configuration (SW40, SW41, SW42 & SW43). This can be 32 channel single-ended or 16 channel differential.

Bit 0	Input type	Number of input channels	Buffer size	Total RAM buffer
0	Single-ended	32 Channels	32 Words	32 Words
0	Differential	16 Channels	2x16 Words	32 Words
1	Single-ended	32 Channels	64x32 Words	2048 Words
1	Differential	16 Channels	128x16 Words	2048 Words

Table 8.1.- CM-AD-45 dual port RAM data buffer size.

A multiplexing-sampling cycle can be defined as the action of selecting and converting-to-digital all input channels. Each multiplexing sampling cycle fills a dual port RAM buffer with updated converted data.

This module can operate in two basic modes:

a) Multiplexed input channel mode.

All channels are multiplexed, sampled, converted, and stacked in memory in a consecutive manner, one channel after the other.

b) Fixed channel mode.

A single input channel is user selected through Bits 8 thru 12 of the MCR. Multiplexers are fixed after selecting this channel. Then successive conversions are performed up to filling the RAM buffer. All data stored in the RAM buffer correspond to conversions of the selected channel.

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OBSERVATION

The **CM-AD-45** mode of operation, multiplexed or fixed channel, is defined through Bit 7 of the MCR.

8.2.- Channel Sampling/Multiplexing Mode.

In this mode all input channels are multiplexed, sampled, converted, and stacked in memory in a consecutive manner, one channel after the other.

The Bit 0 of the MCR defines the storage buffer size as follows:

a) Setting Bit 0 to logic 0 configures the board to operate with a RAM buffer of 32 Words. The RAM buffer size is 16 or 32 Words per sampling cycle.

When the number of channels is 32 (single-ended), the buffer is 32 Word size. When the number of channels is 16 (differential), the buffer is 16 Word size, but the board will fill 2 consecutive buffers, 16 Words each (2x16). *See **Table 8.1**.*

b) Setting Bit 0 lo logic 1 configures the board to operate with a RAM buffer of 2048 Words. This is the full RAM size.

The multiplexing-sampling circuitry will fill the RAM with several sampling cycles. Each cycle is of equal in length to the number of channels. Sampling cycles are stacked up to filling the whole dual port RAM as follows:

- 64 consecutive multiplexing-sampling cycles, 32 Words each. This is the case of 32 single-ended analog inputs. *See **Figure 8.2**.*

- 128 consecutive multiplexing-sampling cycles, 16 Words each. This is the case of 16 differential analog inputs. *See **Figure 8.3.***

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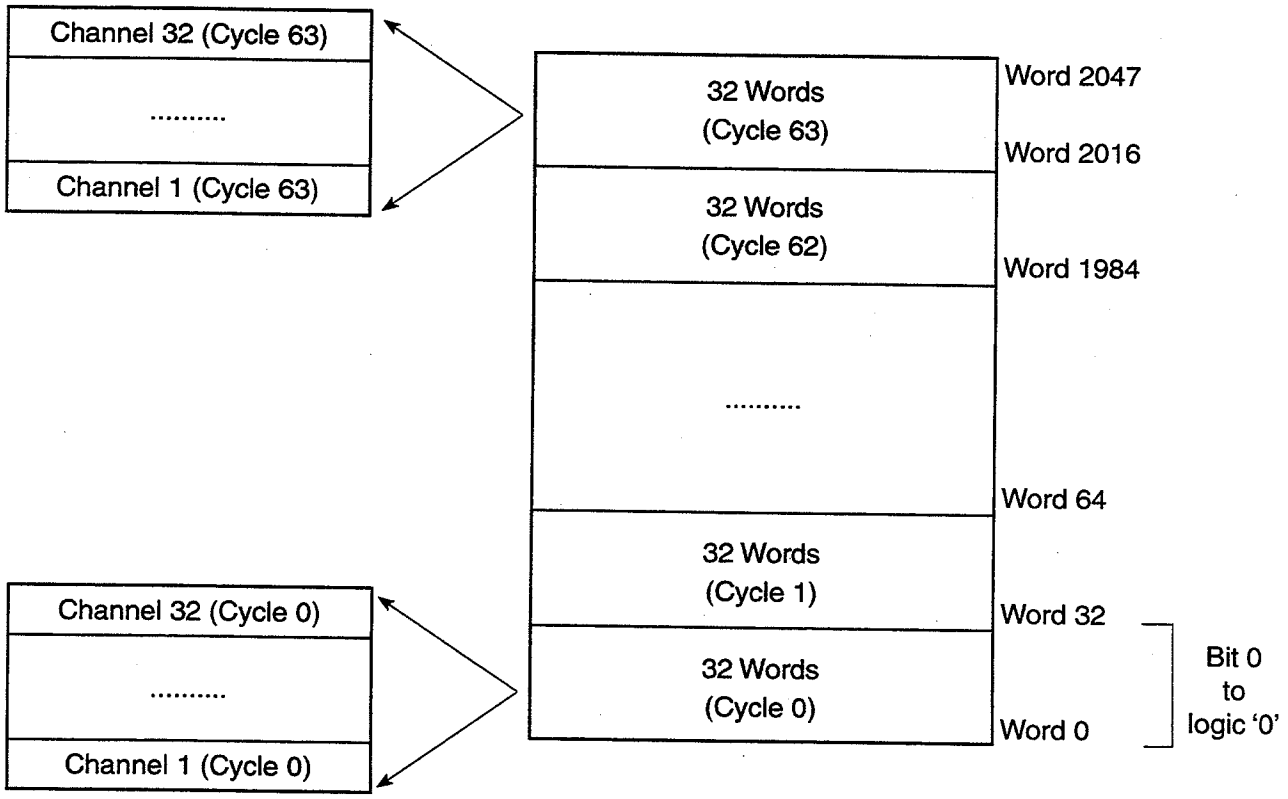


Figure 8.2.- Sampling cycles & data addressing in RAM (single-ended).

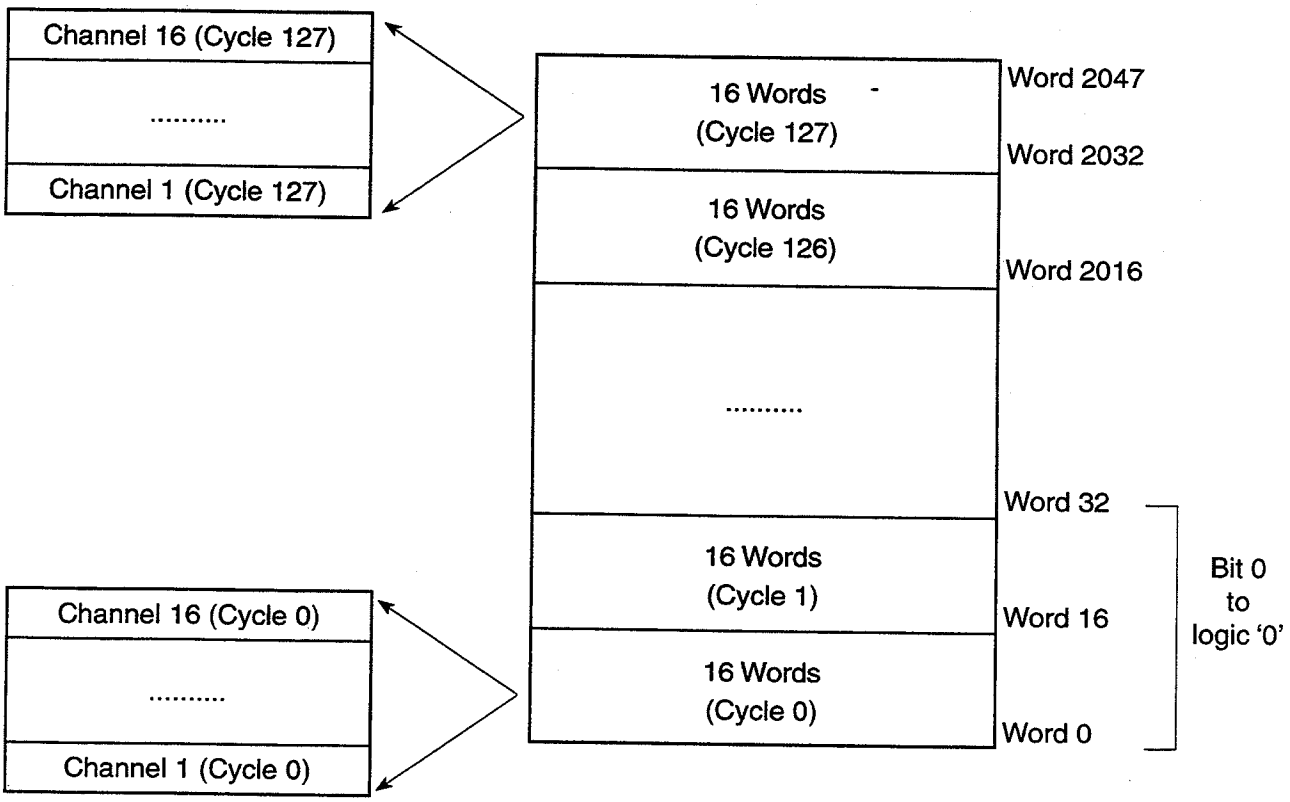


Figure 8.3.- Sampling cycles & data addressing in RAM (differential).

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8.3.- Fixed Channel Mode.

The **CM-AD-45** is capable of stopping the channel multiplexers and dedicating all A/D conversions to a specific, user selected input channel. This feature can be useful when sampling a channel at high speed is required. The entire RAM buffer can be dedicated to the selected channel thus increasing the channel tracking period and buffer depth.

The fixed channel is selected via Bit 8 thru Bit 12 of the MCR. These bits define an A0-A4 address bus capable of selecting 1 of the possible 32 channels.

Operating in fixed channel mode increases the channel sampling speed by 32 times with respect to standard multiplexed operation. In the case of boards configured with differential inputs, the ratio is 16 times. The fixed channel sampling mode does not affect the RAM buffer filling mechanism which operates normally regardless of the multiplexers status.

The size of the RAM buffer is user defined via the MCR Bit 0 as usual.

a) Bit 0 to logic 0. If selected buffer size is 32 Words, the buffer structure is identical to that described in ***Figures 8.2 & 8.3,*** but now all samples are fully dedicated to the fixed channel.

When the board is type single-ended, the buffer size is 32 Words. When the board is type differential, the buffer size is 16 Words, but the board will fill 2 consecutive buffers, 16 Words each.

b) Bit 0 to logic 1. If selected buffer size is 2048 Words, the **CM-AD-45** sampling circuitry will perform 2048 consecutive samples of the input fixed channels. This will fill the total available RAM size.

Figures 8.4 & 8.5 describe the **CM-AD-45** RAM data storage organization when operating in fixed channel mode and 2048 Word buffer. In this figures, "Channel X" means the selected fixed channel.

Operating at 100 Ksps, this mode offers a sampling-storage window of 20.48 ms dedicated to a single analog input.

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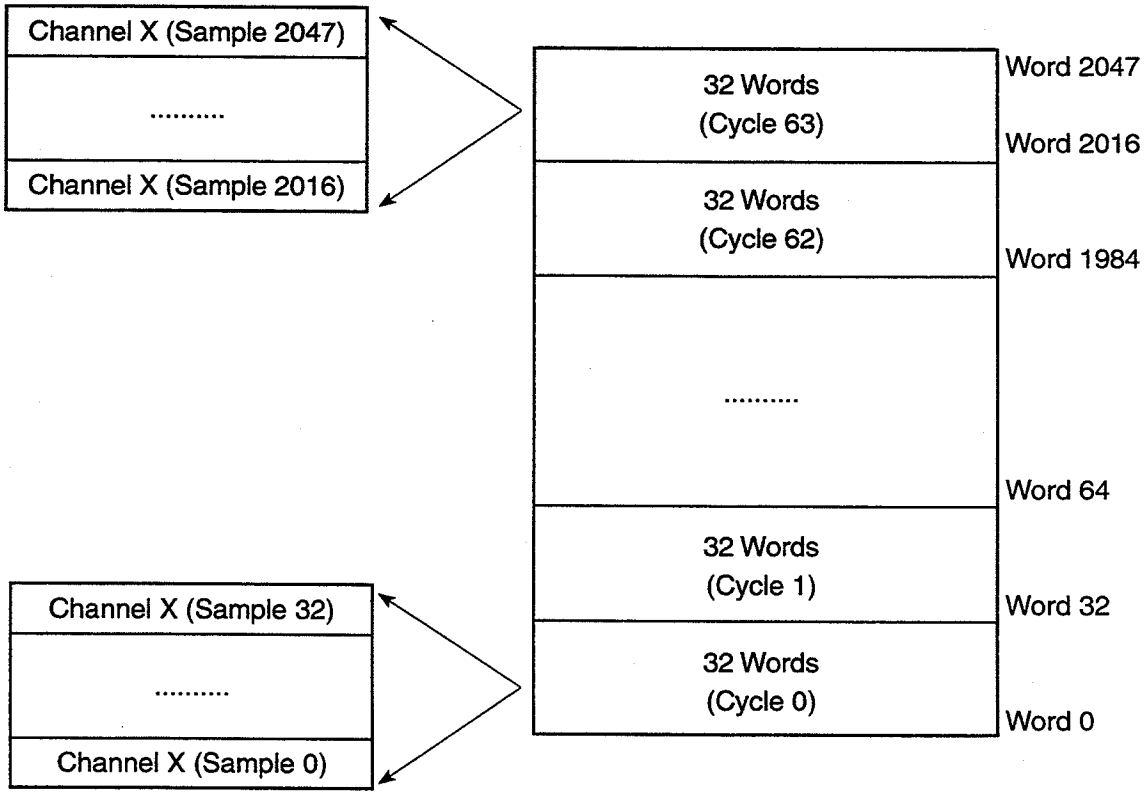


Figure 8.4.- Fixed channel data addressing in SRAM (single-ended).

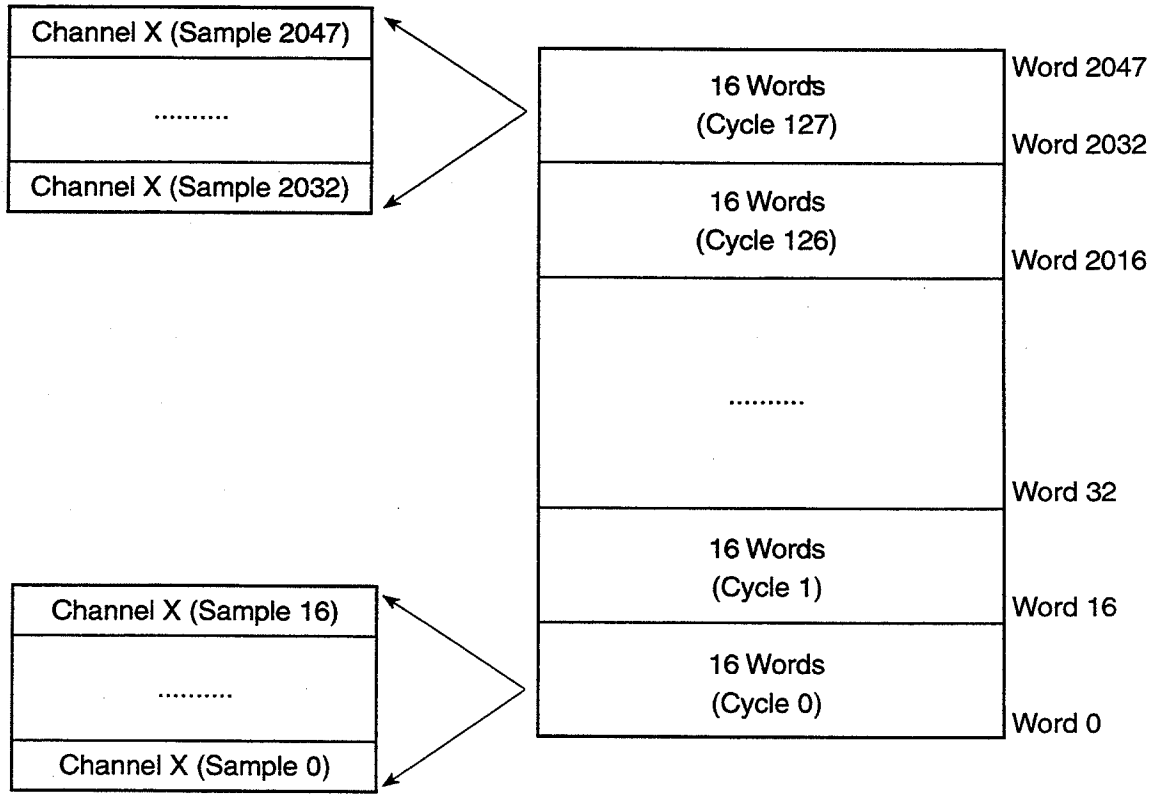


Figure 8.5.- Fixed channel data addressing in SRAM (differential).

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8.4.- Sample Cycle Period.

This section is useful for estimating the time spent by the **CM-AD-45** per multiplexing-sampling cycle.

For example, a board sampling at 100 Ksps offers the following figures:

- Channel sampling period (1 channel A/D conversion) = 1/100Ksps = 10 µsec.

- Multiplexing-sampling cycle period (32 channels multiplexed & converted) = 32x10 µsec = 320 µsec. This is also the channel sampling period, understood as the time between two consecutive samples of the same input channel. This time is measured from sample of Channel 1 (Cycle 0) to sample of Channel 1 (Cycle 1).

- Total SRAM buffer filling time (64 mux-sampling cycles, 32 channels each) = 64x320 µsec = 20.480 msec.

OBSERVATION

The above conclusions are fully applicable when the **CM-AD-45** module is configured to sample 16 differential input channels.

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Chapter 9.- VMEbus Interface.

The **CM-AD-45** has been designed for total compatibility with all VMEbus equipment or module existent on the market.

Therefore this board can be connected to any standard VMEbus backplane together with other 3U and 6U modules manufactured by other suppliers.

9.1.- P1 VMEbus Connector.

The P1 connector is essential for correct board operation. The pull-up resistors in the VMEbus backplane provide logic 1 to various signals. These signals are monitored by the logic circuitry implemented in the board, and are indispensable for proper operation.

As mentioned in earlier chapters, the **CM-AD-45** only supports the standard A24/D16 addressing mode. The implemented interface complies with IEEE 1014, IEC 821/297 rev. C specifications for VMEbus compatible products. This module only supports Word aligned access format.

The board includes only 16 bit read and write registers. Byte or Long Word accesses are illegal because the board is not capable of handling 8 or 32 bit data.

All P1 pins, which are driven or monitored by the **CM-AD-45**, are located according to the VMEbus IEEE 1014 and IEC 821 spec pin-out assignment. The board monitors the following P1 pins:

A01/A23 address bus.
AM0/AM5 address modifier codes.
D00/D15 data bus.
AS*, DS0*, DS1* address and data strobe lines.
SYSCLK, IACK*, LWORD*, and WRITE* lines.
BERR* and DTACK* lines.
IRQ2* thru IRQ7* interrupt lines.
IACKIN* and IACKOUT* daisy chain lines.
SYSRESET* line.
GND, +12 V and +5 V supply lines.

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IMPORTANT

This module propagates with active logic the IACKIN* & IACKOUT* daisy chain signals.

IMPORTANT

This module propagates with a PCB track wire the following arbitration daisy chain signals:

- BG0IN* & BG0OUT* daisy chain.
- BG1IN* & BG1OUT* daisy chain.
- BG2IN* & BG2OUT* daisy chain.
- BG3IN* & BG3OUT* daisy chain.

The user does not need to insert the corresponding jumpers in the backplane slot occupied by a **CM-AD-45** board in order to ensure daisy chain signal propagation.

OBSERVATION

The **CM-AD-45** will exclusively respond to A24/D16 standard data transfer cycles. This module does not monitor the A24-A31 VMEbus address lines.

9.2.- VMEbus Data Transfer Cycles.

The **CM-AD-45** performs the following VMEbus data transfer cycles:

a) Read cycle (R).

Figure 9.1 shows a typical timing diagram measured on the VMEbus backplane while a master module is performing a "Read" cycle to the **CM-AD-45** dual port RAM.

b) Write cycle (W).

Figure 9.2 shows a typical timing diagram measured on the VMEbus backplane while a master module is performing a "Write" cycle to the **CM-AD-45** (accessing the MCR).

c) Interrupt Acknowledge cycle (IACK).

Figure 9.3 shows a typical timing diagram measured on the VMEbus backplane while a master module is performing a "IACK" cycle to the **CM-AD-45**.

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OBSERVATION

Since the **CM-AD-45** board implements a VMEbus Interrupter it will respond to Interrupt Acknowledge Cycles (IACK* active). See ***Figure 9.3.***

This board does not support Block Transfers (BLT) or Read Modify Write cycles (RMW).

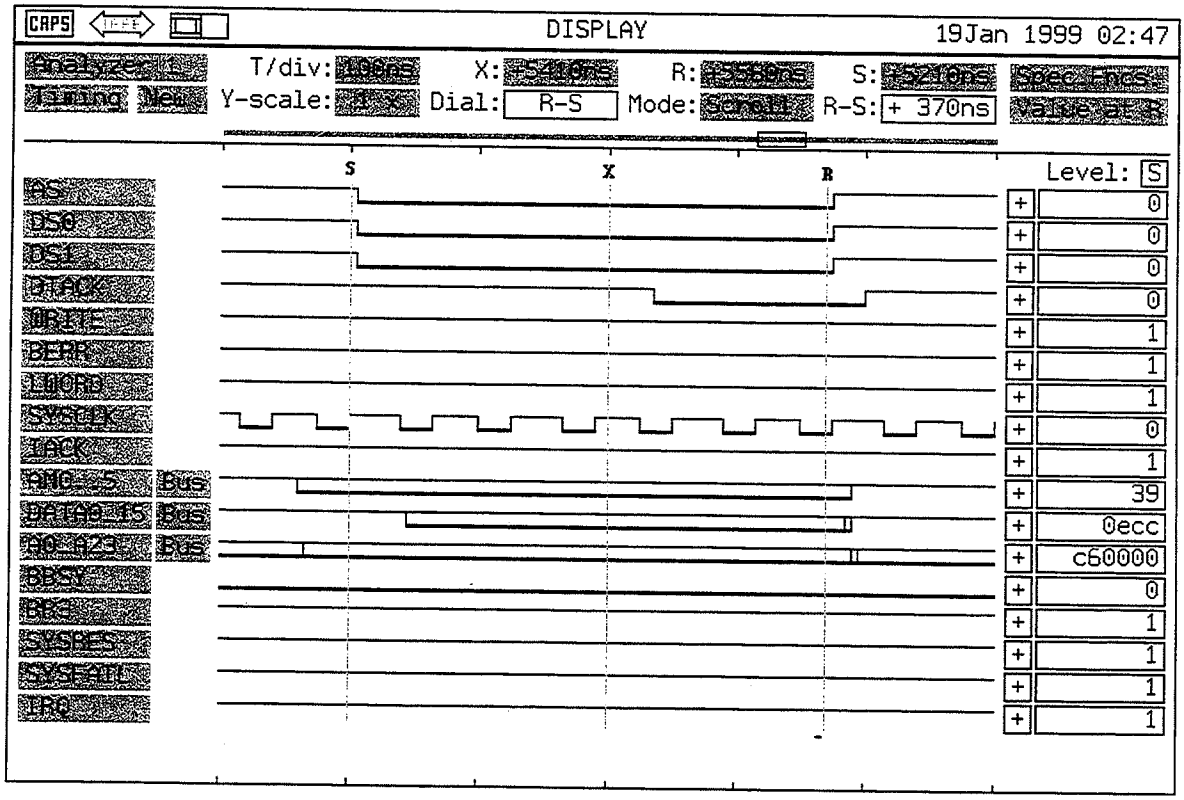


Figure 9.1.- VMEbus Read cycle timing diagram.

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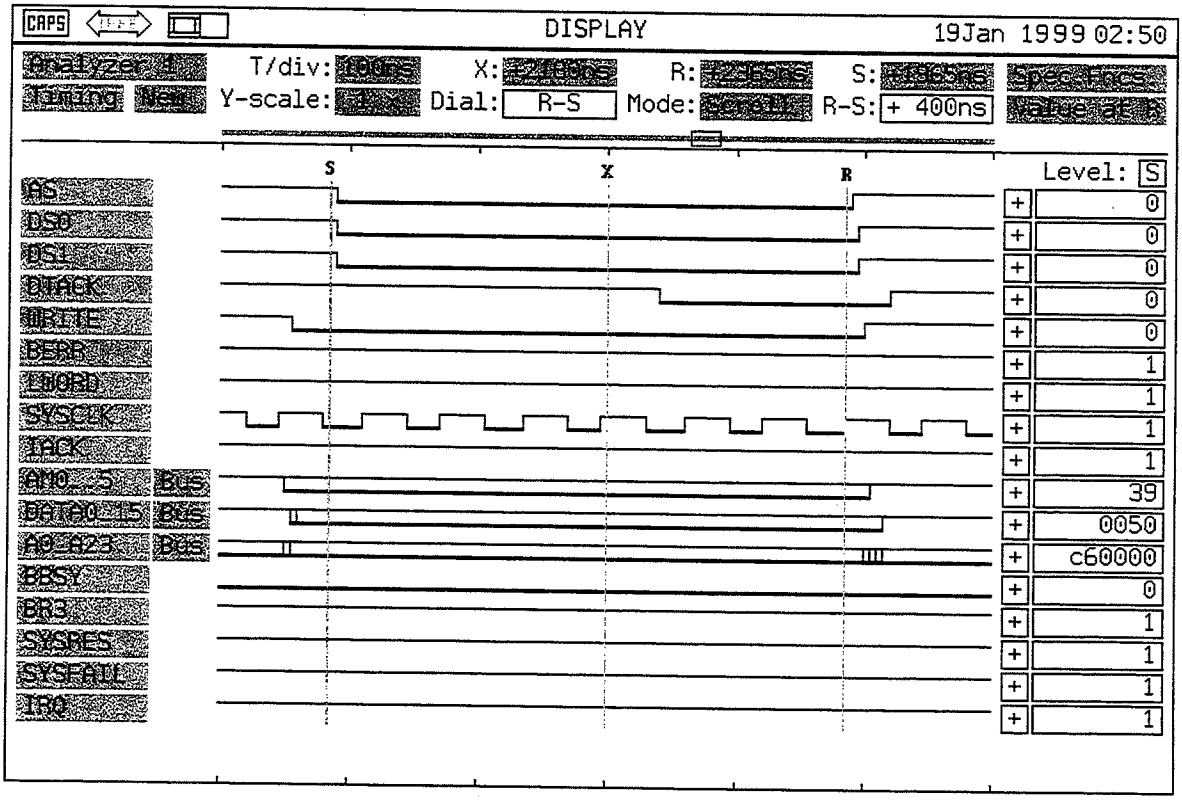


Figure 9.2.- VMEbus Write cycle timing diagram.

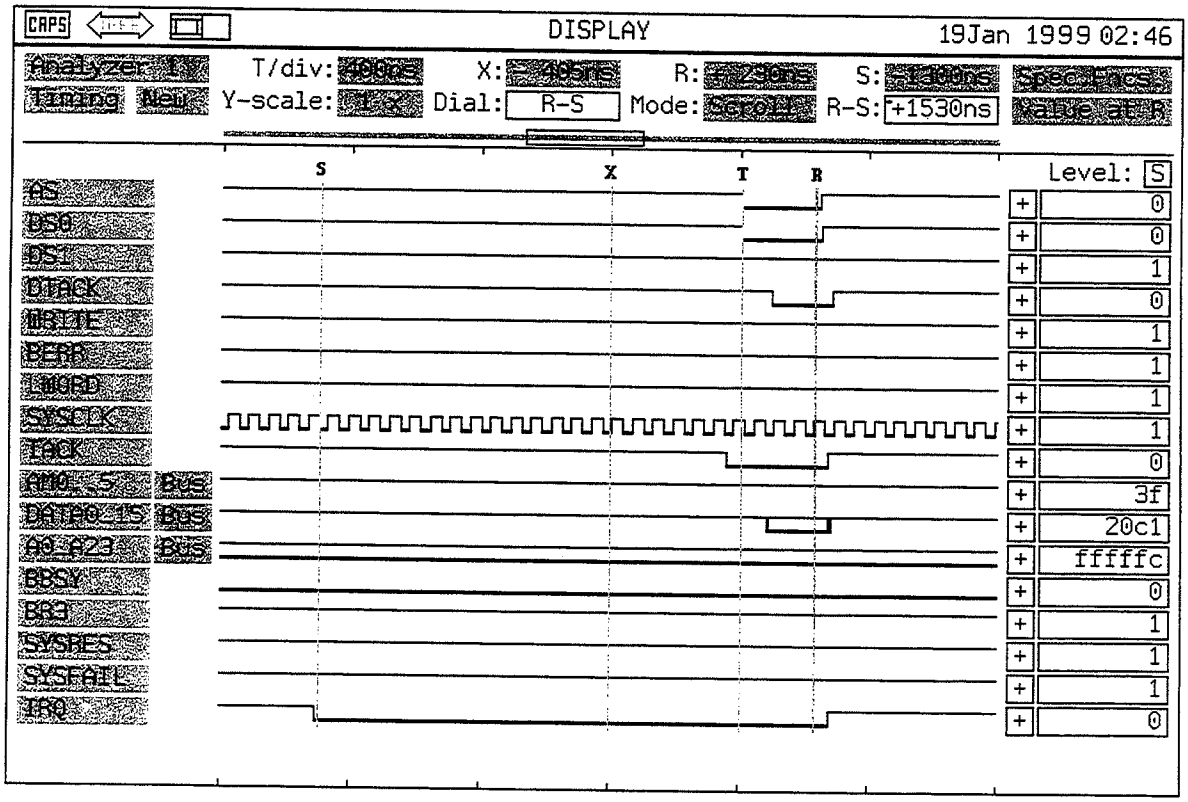


Figure 9.3.- VMEbus IACK cycle timing diagram.

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9.2.1.- Address Modifier Codes (AM0-AM5).

This board monitors and responds to the following "Address Modifier Codes" when it is accessed by a VMEbus master:

Standard cycles....AM0-AM5.....$39, $3A, $3D, $3E.

9.3.- CM-AD-45 Access Time.

The **CM-AD-45** inserts 2 wait states when it is accessed by a master CPU. Each wait state inserts a SYSCLK period delay of 62 ns.

The on-board circuitry will assert DTACK* approximately 200 nsec after the VMEbus lines are stable and validated by the master. However, the total amount of time used in a VMEbus access to the **CM-AD-45** depends on the master.

The access cycle can be divided in three phases *(see **Figure 9.1**)*:

a) VMEbus master addressing and settling of valid data. This time depends on the master CPU. Typically about 50 nsec.

b) CM-AD-45 response time. The module needs this time for address decoding and for supplying or latching valid data from the VMEbus D00-D15 lines (200 nsec typical).

c) VMEbus master acknowledgment of the "DTACK*" signal and cycle completion (end of cycle). This time also depends on the master (about 50-100 nsec typical).

9.4.- On-board VMEbus Interrupter.

The **CM-AD-45** is provided with an on-board Interrupter type I (2-7) which can assert interrupts on any of the VMEbus interrupts request lines IRQ2* through IRQ7*. The desired IRQ level is jumper selectable via SW38.

The Interrupter operation can be enabled/disabled via the Module Control Register Bit 1. Interrupts are primarily intended to advise the master CPU when the current sampling cycle is completed and data stored in the RAM buffer is ready to be read.

The Interrupter is type D08 (O). All supplied vectors are 8 bits wide and the remaining VMEbus lines other than D00-D07 are not driven by the Interrupter. The supplied Status-ID Vector is user programmable by means of jumper block SW37.

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The Interrupter's main functions can be summarized as follows:

1) Asserts a VMEbus interrupt provided that the unit is enabled in the MCR and the current sampling cycle is completed. Once the interrupt is asserted, the board will stop conversions only if Bit 2 of the MCR is set to logic 1. Otherwise the assertion of interrupts will not stop the free running multiplexing-sampling process, and a new cycle will be initiated automatically.

2) Places a Status-ID Vector D08(O) during IACK* cycles which match the IRQ* priority level asserted by the Interrupter. Reading the Status-ID Vector on the VMEbus releases the pending interrupt. This mechanism is known as type ROAK (Release On Acknowledge).

3) Propagates the IACK* daisy chain (IACKIN*/IACKOUT*). This occurs when the Interrupter receives an IACKIN* signal validated by AS* & DS0* and no interrupt has been generated by the Interrupter or when a priority mismatch occurs. The daisy chain propagation delay time is 40 nsec approx. The IACKOUT* signal will be negated 20 ns approx. after the VMEbus DS0* is negated.

OBSERVATION

The Interrupter releases any pending interrupt in response to the VMEbus SYSRESET* signal being asserted.

OBSERVATION

The supplied Status-ID Vector depends only on SW37 and the type of sampling cycle. It is independent of the VME IRQ* level selected on SW38.

Table 9.4 shows the VMEbus IRQ* level selection versus the jumper block SW38. Among the 8 available possibilities, two options are not implemented and will disable IRQs.

R2	R1	R0	VMEbus IRQ*
OFF	OFF	OFF	DISABLED
OFF	OFF	ON	DISABLED
OFF	ON	OFF	IRQ2*
OFF	ON	ON	IRQ3*
ON	OFF	OFF	IRQ4*
ON	OFF	ON	IRQ5*
ON	ON	OFF	IRQ6*
ON	ON	ON	IRQ7*

Table 9.4.- VMEbus IRQ level selection versus SW38.

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9.5.- VMEbus Interrupter Status-ID Vector.

The supplied Status-ID vector (1 Byte) is composed of two nibbles. The low nibble encodes the interrupting source. The high nibble is user defined by jumpers. The board can supply two different vectors for each SW37 configuration. These vectors are type $X1 and $X2.

Table 9.5 shows the Status-ID vector versus the on-board interrupting source.

Interrupting Source	D03	D02	D01	D00	$Vector
End of 32/2x16 Words mux-sampling cycle (Bit 0 of MCR to logic 0)	0	0	1	0	$X2
End of 2048 Words mux-sampling cycle (Bit 0 of MCR to logic 1)	0	0	0	1	$X1
X = High nibble according SW37					

Table 9.5.- Status-ID vector low nibble options.

As shown in ***Table 9.5***, two vectors are available versus the current dual port RAM data buffer size. The Interrupt Servicing Routine will take advantage of the vector 2 LSB information in order to read the proper buffer of the dual-port RAM. VMEbus data lines D02 & D03 are tied to logic 0 during IACK* cycles.

The Status-ID vector high nibble X is user defined according to ***Table 9.6***. There are 16 vector options versus the four bits of jumper block SW37. Therefore, up to 16 **CM-AD-45** boards connected to the same backplane can supply different vectors.

H3	H2	H1	H0	D7	D6	D5	D4	$Vector
OFF	OFF	OFF	OFF	0	0	0	0	$F1 or $F2
OFF	OFF	OFF	ON	0	0	0	1	$E1 or $E2
OFF	OFF	ON	OFF	0	0	1	0	$D1 or $C2
OFF	OFF	ON	ON	0	0	1	1	$C1 or $C2
OFF	ON	OFF	OFF	0	1	0	0	$B1 or $B2
OFF	ON	OFF	ON	0	1	0	1	$A1 or $A2
OFF	ON	ON	OFF	0	1	1	0	$91 or $92
OFF	ON	ON	ON	0	1	1	1	$81 or $82
ON	OFF	OFF	OFF	1	0	0	0	$71 or $72
ON	OFF	OFF	ON	1	0	0	1	$61 or $62
ON	OFF	ON	OFF	1	0	1	0	$51 or $52
ON	OFF	ON	ON	1	0	1	1	$41 or $42
ON	ON	OFF	OFF	1	1	0	0	$31 or $32
ON	ON	OFF	ON	1	1	0	1	$21 or $22
ON	ON	ON	OFF	1	1	1	0	$11 or $12
ON	ON	ON	ON	1	1	1	1	$01 or $02
Low nibble according the current RAM buffer size.								

Table 9.6.- Interrupt Status-ID vector High nibble versus SW37.

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How to obtain the Status-ID vector?

- High nibble X: user selected according to SW37.

Example: board with SW37 configured as H3=ON, H2=ON, H1=OFF, H0=ON. High nibble is 2.

- Low nibble: automatically provided by the board according to the programmed buffer size in the MCR Bit 0. Options are $X2 and $X1.

Example: board performing sampling cycles of 2048 Word each. Low nibble is 1.

The interrupt Status-ID vector is $21. This vector must be attached by the master CPU in order to jump to the associated interrupt servicing routine for this example board.

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Chapter 10.- CM-AD-45 Board Support Package.

This chapter describes the **CM-AD-45** Software Package. The objective of this section is to provide the user with an introduction to the main functions and their use.

10.1.- CM-AD-45 Software Package.

The **CM-AD-45** Software Package **(CM-AD-45/SFP)** is written in C language and tested under the VxWorks 5.3 Operating System. If required, the code can be easily adapted or recompiled to any other standard ANSI C compiler existing on the market.

The package is comprised of a floppy-disk and an explanatory manual. The code is supplied in Sun-4 format (PC format is also available).

This package can be purchased from **CM Computer** at low cost. Once the user acquires a license the software does not require any further royalties for its use.

10.2.- Software Package Description.

This VxWorks compatible driver has been designed to program and display the analog input voltages of the A/D channels corresponding to up to 16 **CM-AD-45** boards, which can be simultaneously connected to a VMEbus backplane.

Main parameters for the driver are the VMEbus base address of the first **CM-AD-45** module, and the number of **CM-AD-45** boards connected to the backplane. These two parameters must be indicated in the header file (ad45.h), in order to properly initialize and dimension the software internal variables. This can be done using the directives "#define AD45_BADDRS" and "#define AD45_NBOARDS".

By default, the parameter AD45_BADDRS is defined as address $C60000 (this address can be changed by switches in the PCB). Additionally, AD45_NBOARDS is defined as 1 (the range of this parameter is from 1 thru 16). The default parameters assume that there is only one **CM-AD-45** installed, and its VMEbus base address is $C60000.

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When installing more than one board, the remaining SW35 jumper (for each additional board) must be configured to be contiguous in memory (stacked). Each contiguous configuration of jumper block SW35 increases by 1 the board index ("board_id" argument used in all BSP functions). This is because the program assumes that each board address follows the previous board address (no free memory spaces between them).

When the program is compiled without warnings or errors it is ready to be loaded and executed in memory.

IMPORTANT

This program is supplied in C source code, therefore allowing the user to modify, customize, adapt, extend it, etc, if needed by the application. No further licenses are required once the user has purchased one original BSP license from **CM Computer**. The user is not allowed to re-sell this program to any third company.

CM Computer has issued this **CM-AD-45** software driver with the unique intention of providing the user with base code and programming examples for this module. **CM Computer** does not assume any responsibility derived from the use or implementation of the drivers contained in this software package in any user application or project.

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10.3.- Main Function Description.

This package consists of eleven "user" functions intended to initialize, configure and read the **CM-AD-45** input channels. These C functions are the following:

1.- STATUS iniad45 (short board_id, u_char vector)

Initialization function. It initializes the Module Control Register, Interrupt Status-ID vector, and all internal variables corresponding to the selected **CM-AD-45** board.

2.- STATUS ad45set_sw39 (short board_id, short SW39)

Get and stores the SW39 switch status. This function provides information to the software about the current configuration of the on-board SW39 switch. The switch position defines the A/D converter scale. It is needed by the software, and must be supplied by the user.

3.- STATUS ad45set_sw40_41_42_43 (short board_id, short SW40_41_42_43)

Get and stores the SW40, SW41, SW42 & SW43 switches status. This function provides information about the current configuration of the SW40, SW41, SW42 & SW43 on-board switches. These switches define if the selected board is configured for input signal type single-ended (32 channels) or differential (16 channels). This hardware information is needed by the software, and must be supplied by the user.

4.- STATUS ad45set_attenuator (short board_id, short ch_ini, short ch_end, short att)

Get and stores the channel attenuator configuration of the selected boards and channels. The position of the associated switches (SW101 thru SW132), will define the 10:1 input attenuators status (enable or disabled). The input channels attenuator status are needed by the software, and must be supplied by the user.

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5.- STATUS ad45set_MCR (char board_id, char bufsize, char irq_ena, char free_stop, char speed, char mux_fixed)

Configures the selected **CM-AD-45** Module Control Register with the desired operating parameters. The configurable parameters are the following:

board_id: *Board identification number. Selects a board in the backplane.*
bufsize: *Defines RAM storage buffer size.*
irq_ena: *Enables/Disables the on-board VMEbus Interrupter.*
free_stop: *Selects single step cycle or free running operation.*
speed: *Selectes the sampling rate.*
mux_fixed: *Selects the multiplexer addressing source.*

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6.- STATUS ad45fix_ch (short board_id, short channel)

Selects the channel to be considered as fixed in the selected **CM-AD-45** board. This function controls the BIT7,.., BIT12 bits of the MCR.

7.- STATUS ad45set_gain_pol (char board_id, char gain, char polarity)

Defines the input amplifier Gain, and the input channel Polarity parameters. For this purpose, the function controls BIT5 and BIT6 of the selected **CM-AD-45** MCR.

8.- STATUS ad45get_InputChannel (short board_id, short ch_ini,short ch_end)

Channel voltage value function. This function read the current input voltage of the selected channels (in mV), of the selected **CM-AD-45** board.

9.- short ad45get_MCR (short board_id)

MCR status function. This function read the current MCR status of the selected **CM-AD-45** board.

10.- int ad45BitMux (short board_id, short bit_type)

Module Testing Function. This function performs a multiplexed mode Built-In-Test cycle on the selected board, and checks if the BIT has been successfully passed.

11.- int ad45BitRelay (short board_id, short bit_type)

Module Testing Function. This function performs a relays mode Built-In-Test cycle on the selected board, and checks if the BIT has been successfully passed.

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10.4.- Auxiliary Screen Display Functions.

1.- STATUS ad45display_InputChannel (short board_id, short ch_ini, short ch_end)

Channel Voltage Display Function. This function shows the input voltage of the selected channels (in mV), of the selected **CM-AD-45** board.

2.- STATUS ad45display_MCR (short board_id)

Displays the current Module Control Register status of the selected board.

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Chapter 11.- Appendix.

This chapter describes complementary aspects of the **CM-AD-45** board, such as other available manuals, complementary set of VMEbus boards, etc.

11.1.- CM-AD-45. Other Available Manuals.

The current manual, ref: **CM-AD-45 MAP**, is an application manual intended for programmers, engineers and system integrators. Additionally, **CM Computer** edits another manual related to this board. This is the following:

- Maintenance manual: CM-AD-45 MMT.

This manual is intended to facilitate **CM-AD-45** hardware maintenance. It is a useful document for those companies who implement the **CM-AD-45** in large military application projects. This manual speeds up checking, maintenance and failure location detection in the module. Additionally, the documentation describes the board's submodules and operation. It includes the basic schematic diagrams, a set of scope waveforms, and logic analyzer figures captured at critical points of the board circuitry.

The maintenance manual covers the following topics:

1. Electrical and mechanical schematics.
2. Source code for built-in-test software.
3. NATO part number list (classified list of pieces and spares).
4. Functional description and maintenance procedures.

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OBSERVATION

The module maintenance manual is intended for CM internal use only. It is not a standard product. However **CM Computer** may supply this manual to some customers under special conditions such as large orders, special military projects, non disclosure agreements, etc.

OBSERVATION

CM Computer company is authorized to supply electronic equipment for the NATO forces with the number 7684B. Additionally, this company is registered in the Spanish Defense Department (DGAM) with the number 9015.

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11.2.- Complementary VMEbus Boards.

The **CM-AD-45** board described in this manual is part of a complete 3U and 6U VMEbus compatible board set, manufactured by **CM Computer**.

This set is comprised of a large variety of functional modules, such as 68020/30/40/60 based CPU modules, expansion memory boards, communication controllers, A/D & D/A conversion modules, graphic controllers, synchro and resolver conversion modules, SCSI, ARINC-429 and MIL-STD-1553 controllers, Ethernet boards, discrete input & output modules, ARINC-ATR Military enclosures, power supplies, backplanes, etc.

There are more than 50 boards which are available in four temperature ranges, offering up to 200 different models.

This board set is described in the datasheets and catalogues available from **CM Computer**.

11.3.- CM Computer VME Module Quality Control Levels.

Depending on the module temperature range delivered, **CM Computer** offers 3 different quality levels.

Basic level:

Includes a post-manufacturing visual inspection and general module adjustment (when necessary).

A 6 hour continuous operation test in a VME backplane, performed with a module specific software testing program.

A 30 min. 55 °C. temperature operation test.

Medium level:

Includes a post-manufacturing visual inspection and general module adjustment.

A 12 hour continuous operation test in a VME backplane, performed with a module specific software testing program.

A 1 hour 65 °C temperature operation test.

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Advanced level:

Includes a post-manufacturing visual inspection, general module adjustment.

A 24 hour continuous operation test in a VME backplane, performed with a module specific software testing program.

A 6 hour continuous temperature operation test at -25 °C, plus a 6 hour continuous operation test at +75 °C.

Optional 30 min mechanical test, withstanding 50 to 500 Hz, 2 g amplitude sinusoidal vibration.

OBSERVATION

All tests include a final visual inspection, operational test, packaging, and custom delivery.

IMPORTANT

On written request from the customer and at no extra cost all military modules (R+ and 883 series) will include a MIL-STD-810D certificate for Methods 501.2 and 502.2. When delivering 883 modules this certificate can be complemented with the components screening "certificate of compliance" for MIL-STD-883.

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