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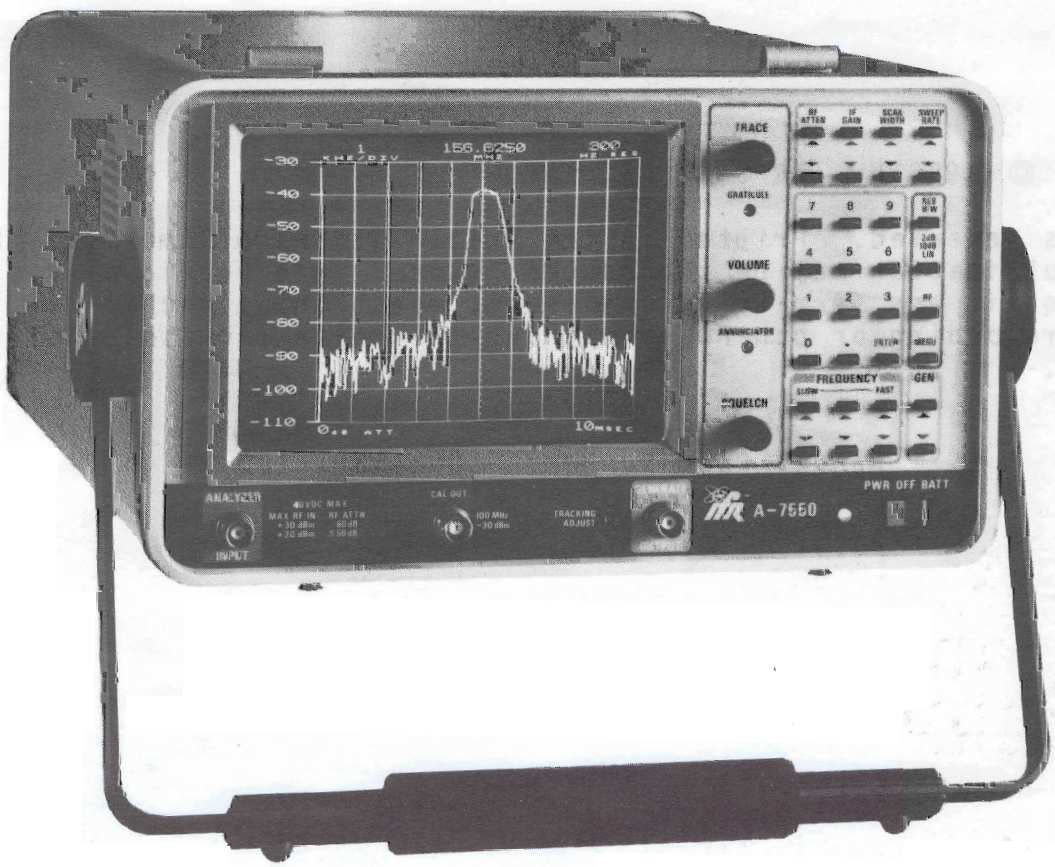
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MAINTENANCE MANUAL

A-7550
SPECTRUM ANALYZER



10200 West York Street/Wichita Kansas 67215 U.S.A./(316) 522-4981/TWX 910-741-6952

1002-5301-100

800-835-2350

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Wichita, Kansas

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Manual Part Number: 1002-5301-100

WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

CAUTION

INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FETs, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USE IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO OR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

NOTE

Remove any built-in power source, such as a battery, before laying PC Boards on conductive mat or storing in conductive bag.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

THE USE OF SIGNAL GENERATORS FOR MAINTENANCE AND OTHER ACTIVITIES CAN BE A SOURCE OF ELECTROMAGNETIC INTERFERENCE TO COMMUNICATION RECEIVERS, WHICH CAN CAUSE DISRUPTION AND INTERFERENCE TO COMMUNICATION SERVICE OUT TO A DISTANCE OF SEVERAL MILES.

USERS OF THIS EQUIPMENT SHOULD SCRUTINIZE ANY OPERATION WHICH RESULTS IN RADIATION OF A SIGNAL (DIRECTLY OR INDIRECTLY) AND SHOULD TAKE NECESSARY PRECAUTIONS TO AVOID POTENTIAL COMMUNICATION INTERFERENCE PROBLEMS.

LIST OF EFFECTIVE PAGES

The manual pages listed below which are affected by a current change or revision, are so identified by a revision number and an asterisk.

Date of issue for original and changed pages are:

Original ..... 0 ..... October 1, 1986

TOTAL NUMBER OF PAGES IN THIS MANUAL IS 202 **CONSISTING OF FOLLOWING:**

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PREFACE

SCOPE

This manual contains maintenance instructions for the A-7550 Spectrum Analyzer. The information in this manual will enable the technician to:

1. Service, test, repair or replace any major assembly or module within the test set.

2. Maintain the operating condition of the set to expected performance standards.

3. Understand the principles of operation as they relate to the overall operation of the set as well as to individual circuits.

ORGANIZATION

This manual is divided into six major sections:

SECTION 1 - INTRODUCTION

Briefly describes the electrical and mechanical configuration of the A-7550, intended to familiarize the technician with the overall structure of the set.

SECTION 2 - THEORY OF OPERATION

Describes the A-7550 circuit theory on three levels of complexity, a simplified overview, a functional theory of interactive modules, and a detailed theory of each module. Appropriate block diagrams accompany each discussion.

SECTION 3 - PERFORMANCE EVALUATION

Contains "covers on" functional checkout procedures for evaluating the performance of the A-7550 in each of its modes of operation and major functions.

SECTION 4 - CALIBRATION

Contains step-by-step calibration procedures for use at normal calibration intervals or after making repairs or replacements.

SECTION 5 - TECHNICAL DATA

Contains component layout drawings for all mechanical assemblies, PC Board assemblies, interconnect diagrams, circuit schematics, waveforms and charts reflecting voltage levels keyed to test points.

APPENDICES

Contains useful supplementary care, maintenance, and operational data.

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SECTION 1 - INTRODUCTION

1-1 GENERAL

This section briefly describes the internal electrical and mechanical configuration of the A-7550. An "exploded" composite drawing, Figure 1-1, is an aid to the technician in identifying and locating major modules which comprise the A-7550. Figure 1-2 describes the controls, connectors and indicators.

1-2 ELECTRICAL DESCRIPTION

The A-7550 is a spectrum analyzer that is microprocssor controlled, digitally synthesized and capable of displaying signals of interest from 100 kHz to 1 GHz, at an input level up to +30 dBm. Individual modules which make up each major circuit are listed in Table 1-1.

Power Distribution Power Supply	Receiver 0-60 dB Attenuator Receive IF Analyzer IF Log Amp 10.7 MHz Receiver (Option) Quasi-Peak (Option)
Video Processor Sweep Digitizer Video Processor	
Control Processor Control Processor PC Board Interface PC Board Keyboard CRT GPIB Interface PC Board (Option) RS-232 Interface PC Board (Option)	Frequency Synthesis Reference Oscillator 1st LO Sampling Loop 1350-2350 MHz VCO Synthesizer #1 Synthesizer #2 2nd LO Summing Loop
Generator Tracking Generator with 0-75 dB Output Attenuator (Option)	

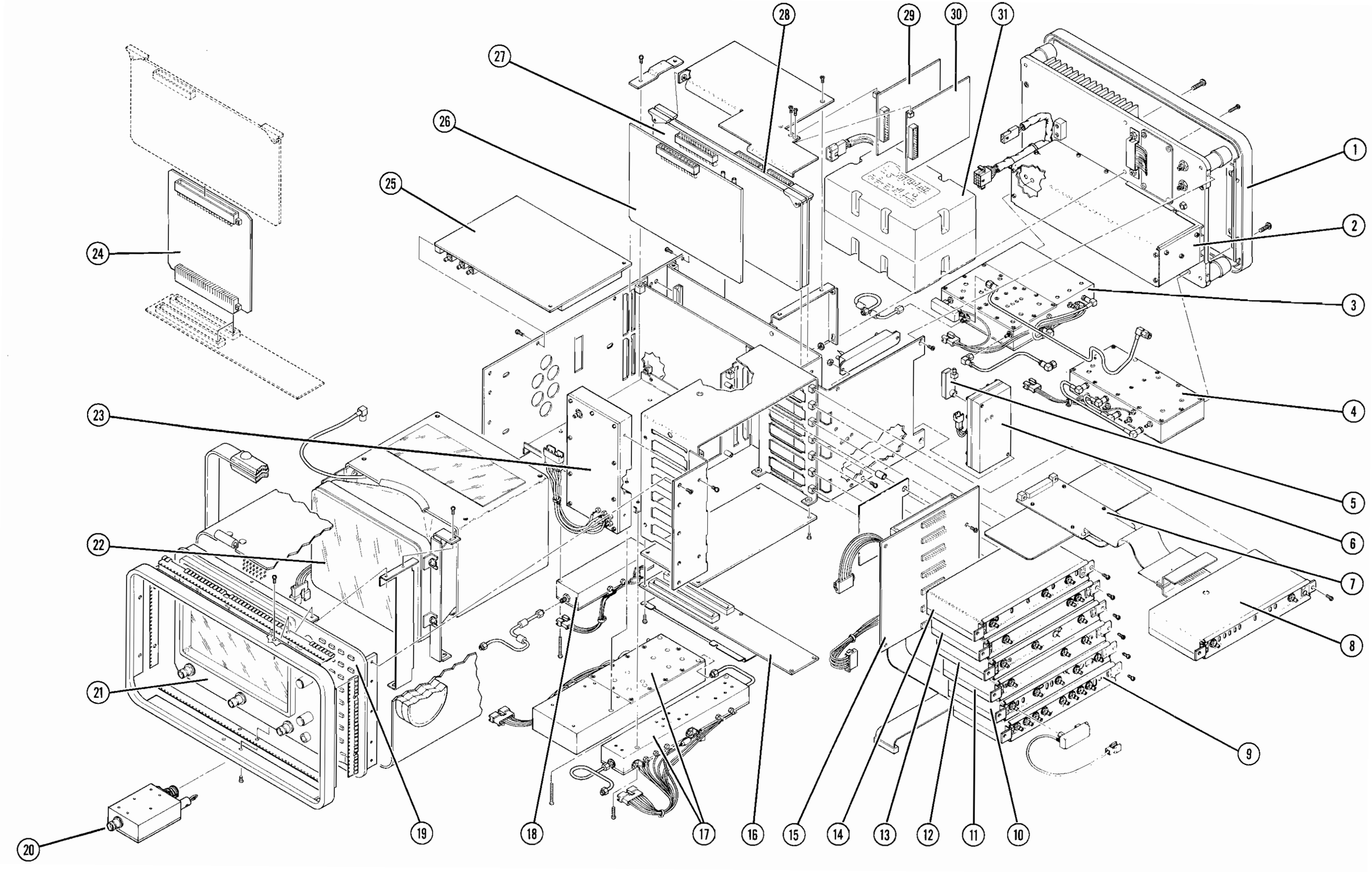
Table 1-1 A-7550 Major Electrical Circuits

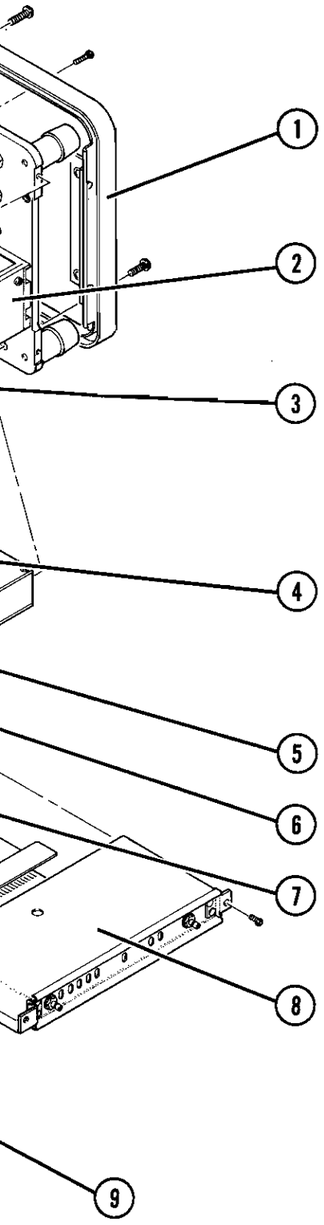
1-3 MECHANICAL DESCRIPTION

Mechanically, the A-7550 consists of groups listed in Table 1-2. Options are included in the composite drawing for reference. Refer to Figure 1-1 for the location of each module.

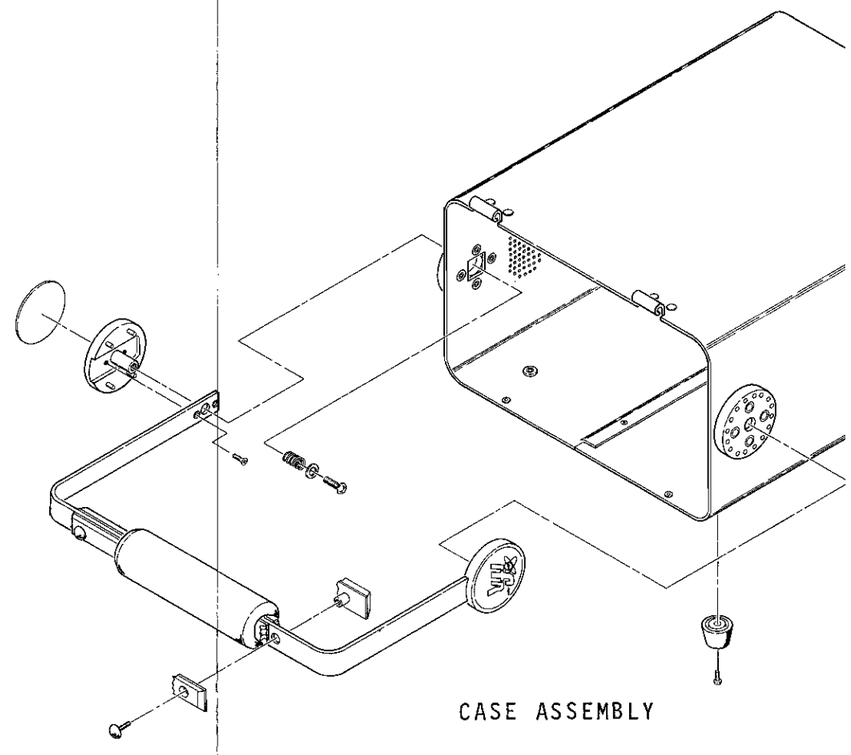
Front	Rear
Front Panel CRT Keyboard	Power Supply Rear Panel
Top	**Bottom**
VCO Filter Module Interface PC Board Control Processor PC Board Video Processor PC Board Sweep Digitizer PC Board Battery (Option) Quasi-Peak (Option) GPIB Interface PC Board (Option) RS-232 Interface PC Board (Option) Digital Extender Board (Option)	Receive IF 2nd LO Summing Loop 1350-2350 MHz VCO 0-60 dB Input Attenuator Digital Mother Board Tracking Generator (Option) 0-75 dB Attenuator (Option)
Right Side	
Log Amp Analyzer IF 10.7 MHz Receiver (Option) Synthesizer #1 Synthesizer #2 1st LO Sampling Loop Reference Oscillator RF Mother Board RF Extender Board (Option)	

Table 1-2 A-7550 Mechanical Groups


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ITEM	NOMENCLATURE
1.	Rear Panel
2.	Power Supply
3.	Receive IF Module
4.	2nd LO Summing Loop Module
5.	VCO Filter Module
6.	1350-2350 MHz VCO Module
7.	RF Extender Board (Option 09)
8.	LOG AMP Module
9.	Reference Oscillator Module
10.	1st LO Sampling Loop Module
11.	Synthesizer #2 Module
12.	Synthesizer #1 Module
13.	10.7 MHz Receiver (Option 04)
14.	Analyzer IF Module
15.	RF Mother Board
16.	Digital Mother Board
17.	Tracking Generator/0-75 dB Attenuator (Option 02)
18.	Input Attenuator Module
19.	Keyboard
20.	20 dB External Amplifier Module (Option 03)
21.	Front Panel
22.	CRT
23.	Quasi-Peak Module (Option 08)
24.	Digital Extender Board (Option 09)
25.	Interface PC Board
26.	Sweep Digitizer PC Board
27.	Video Processor PC Board
28.	Control Processor PC Board
29.	GPIB Interface PC Board (Option 05)
30.	RS-232 Interface PC Board (Option 06)
31.	Battery (Option 01)

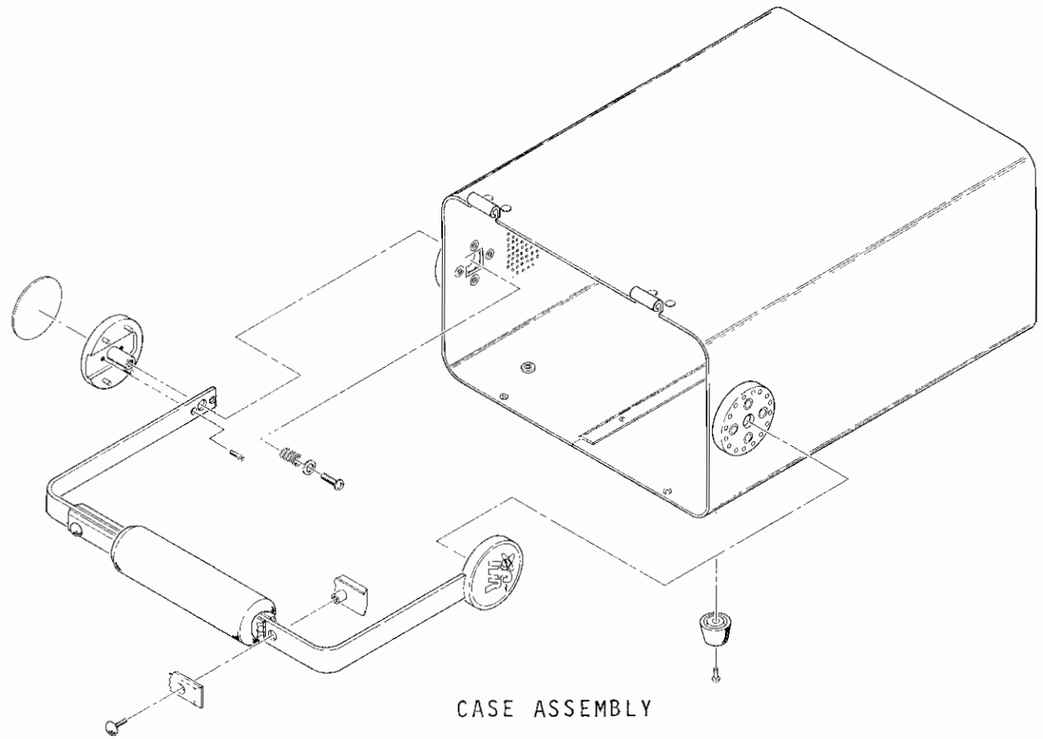


CASE ASSEMBLY

Figure 1-1 A-7550 C
w/Module

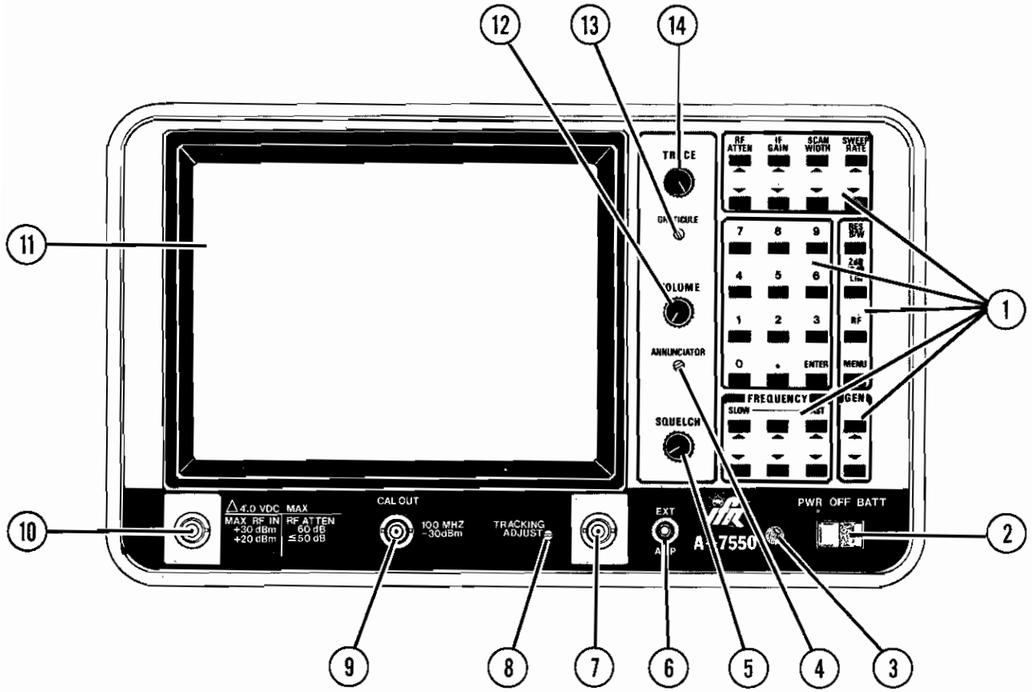
NOMENCLATURE

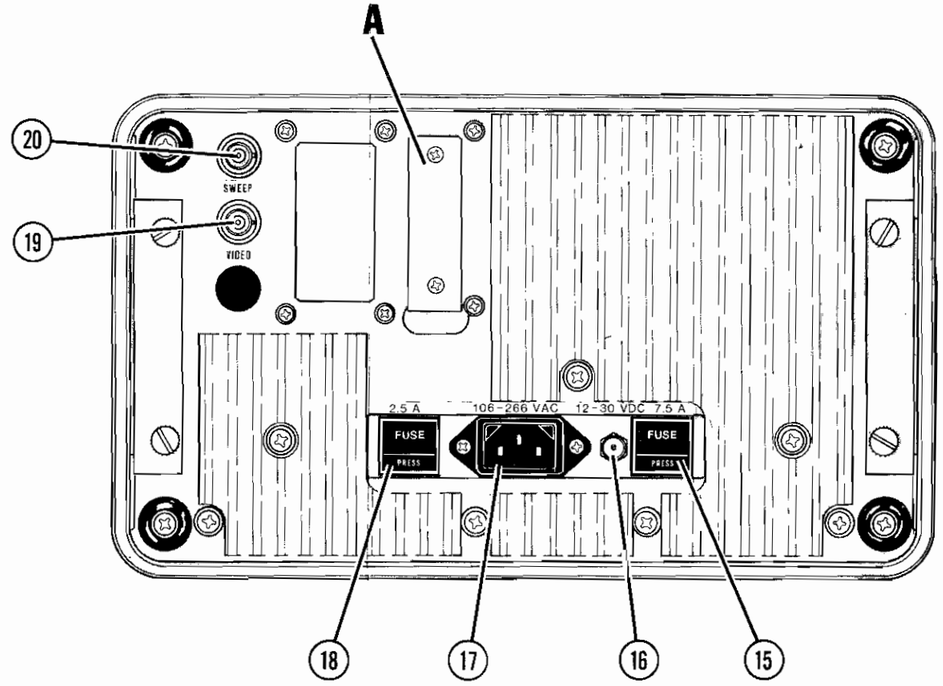
Rear Panel
Power Supply
Receive IF Module
2nd LO Summing Loop Module
VCO Filter Module
1350-2350 MHz VCO Module
RF Extender Board (Option 09)
LOG AMP Module
Reference Oscillator Module
1st LO Sampling Loop Module
Synthesizer #2 Module
Synthesizer #1 Module
10.7 MHz Receiver (Option 04)
Analyzer IF Module
RF Mother Board
Digital Mother Board
Tracking Generator/0-75 dB Attenuator (Option 02)
Input Attenuator Module
Keyboard
20 dB External Amplifier Module (Option 03)
Front Panel
CRT
Quasi-Peak Module (Option 08)
Digital Extender Board (Option 09)
Interface PC Board
Sweep Digitizer PC Board
Video Processor PC Board
Control Processor PC Board
GPIB Interface PC Board (Option 05)
RS-232 Interface PC Board (Option 06)
Battery (Option 01)

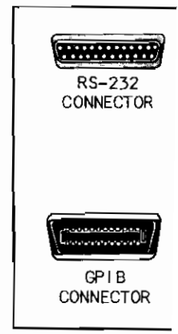


CASE ASSEMBLY

Figure 1-1 A-7550 Composite Assembly w/Module Identification





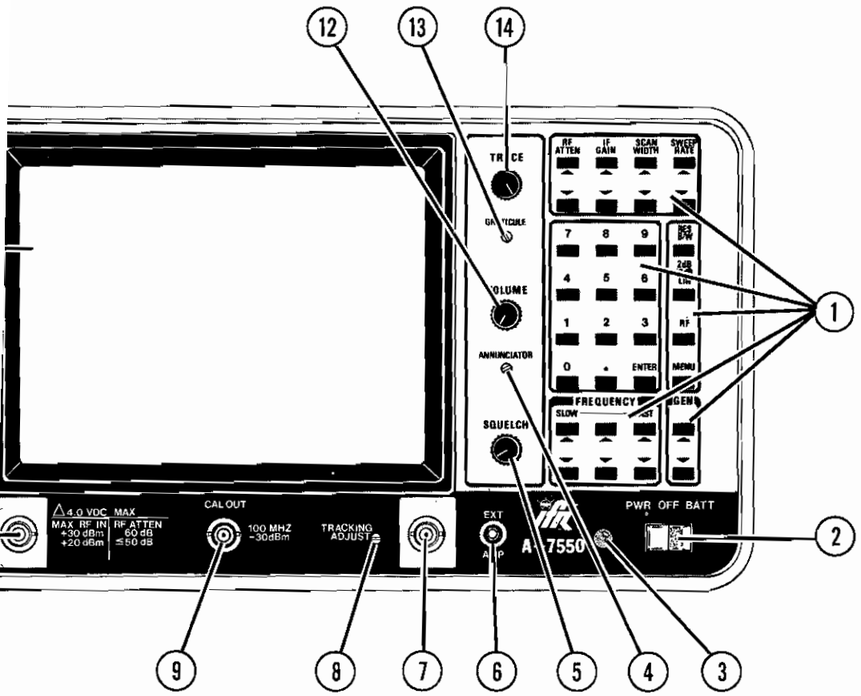


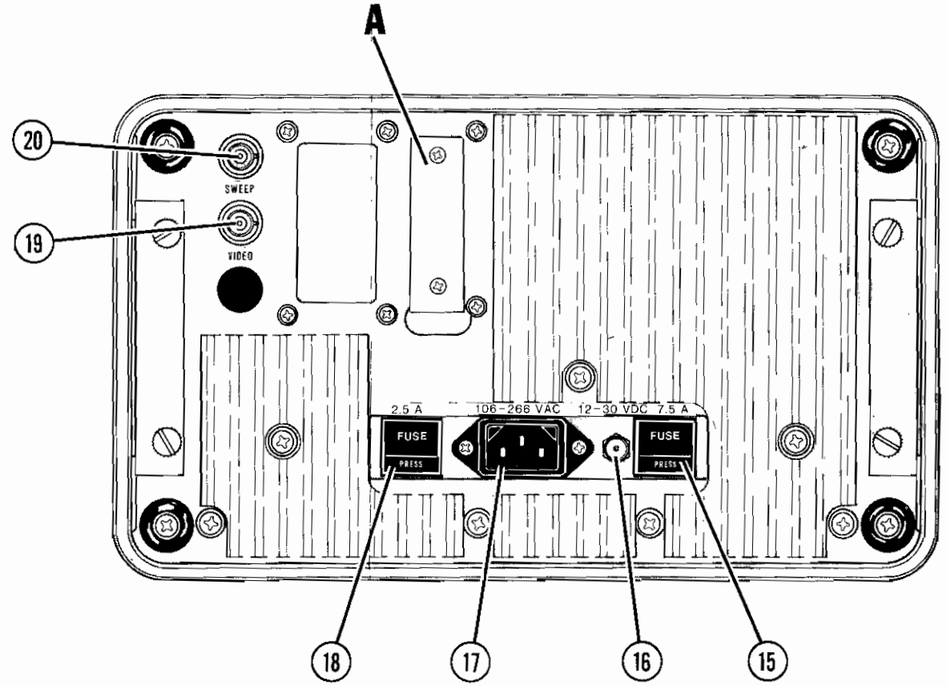
DETAIL **A**

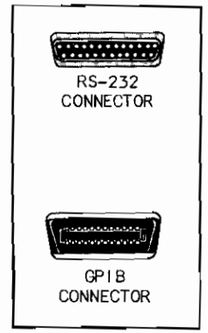
1. Keyboard
2. PWR/OFF/BATT Switch
3. POWER ON Indicator Lamp
4. ANNUNCIATOR Volume Adjust
5. SQUELCH Control
6. EXT AMP Connector
7. GENERATE OUTPUT Connector
8. Tracking Adjust
9. CAL OUT Connector
10. ANALYZER INPUT Connector
11. CRT Display
12. VOLUME Control
13. GRATICULE Intensity Adjust
14. TRACE Intensity Adjust

15. DC Fuse
16. DC Power Input Connector
17. AC Power Input Connector
18. AC Line Fuse
19. ANALOG VIDEO Out Connector
20. SWEEP Out Connector

DESCRIPTION OF CONTROLS, CONNECTORS AND INDICATORS







DETAIL **A**

1. Keyboard
2. PWR/OFF/BATT Switch
3. POWER ON Indicator Lamp
4. ANNUNCIATOR Volume Adjust
5. SQUELCH Control
6. EXT AMP Connector
7. GENERATE OUTPUT Connector
8. Tracking Adjust
9. CAL OUT Connector
10. ANALYZER INPUT Connector
11. CRT Display
12. VOLUME Control
13. GRATICULE Intensity Adjust
14. TRACE Intensity Adjust
15. DC Fuse
16. DC Power Input Connector
17. AC Power Input Connector
18. AC Line Fuse
19. ANALOG VIDEO Out Connector
20. SWEEP Out Connector

DESCRIPTION OF CONTROLS, CONNECTORS AND INDICATORS

SECTION 2 - THEORY OF OPERATION

2-1 GENERAL

This section contains three levels of Theory of Operation and is organized as follows:

1. System Theory of Operation

   Paragraph 2-2 provides a simplified description of signal flow through the A-7550. A System Block Diagram, Figure 2-1, illustrates the signal flow.

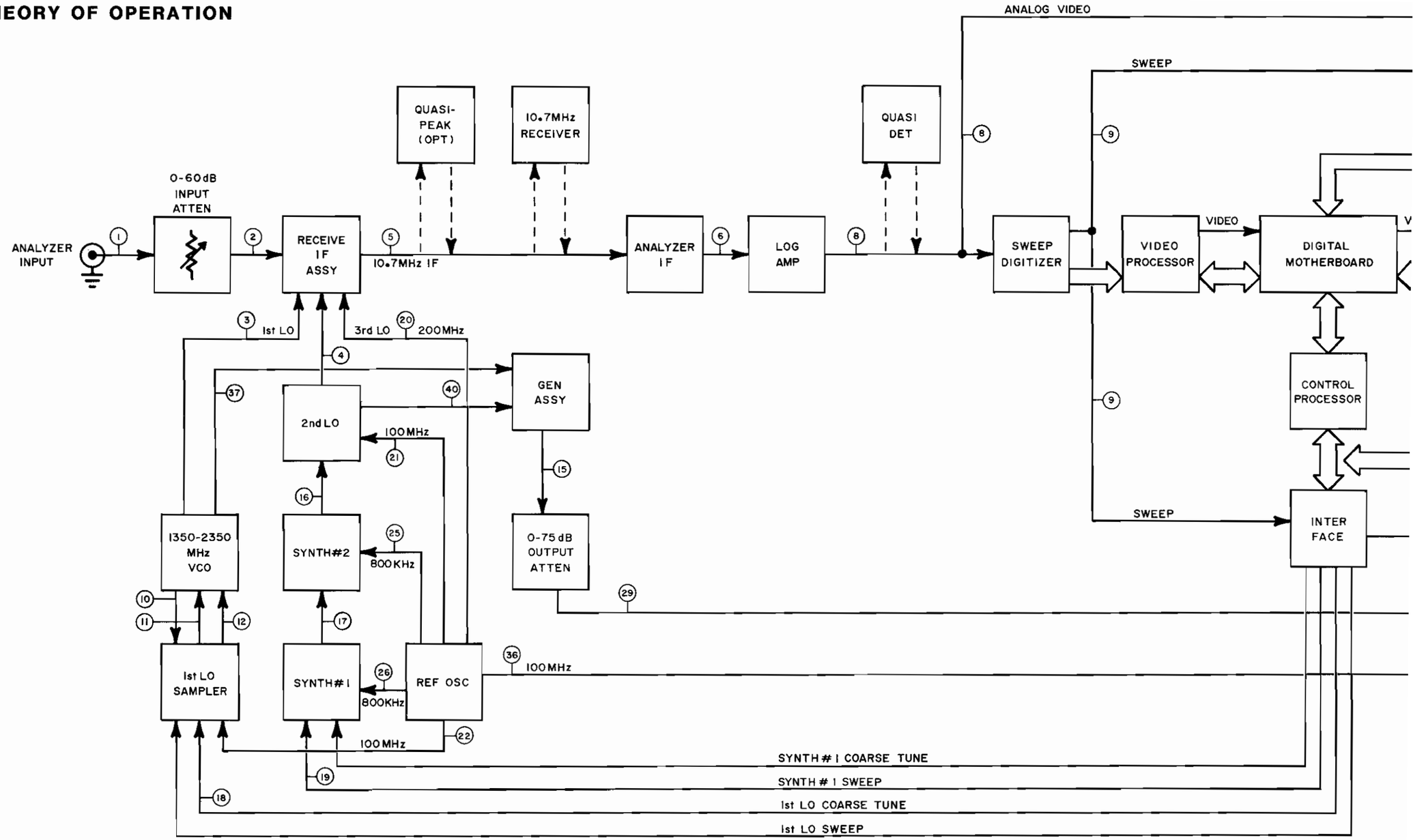
2. Functional Theory of Operation

   Paragraph 2-3 describes the major functional groupings. The description is based upon the accompanying diagram shown for each group.

3. Detailed Theory of Operation

   Paragraph 2-4 provides the detailed theory of operation for each module or assembly. Operation and signal flow description is based upon the accompanying block diagrams.

2-2 SYSTEM THEORY OF OPERATION



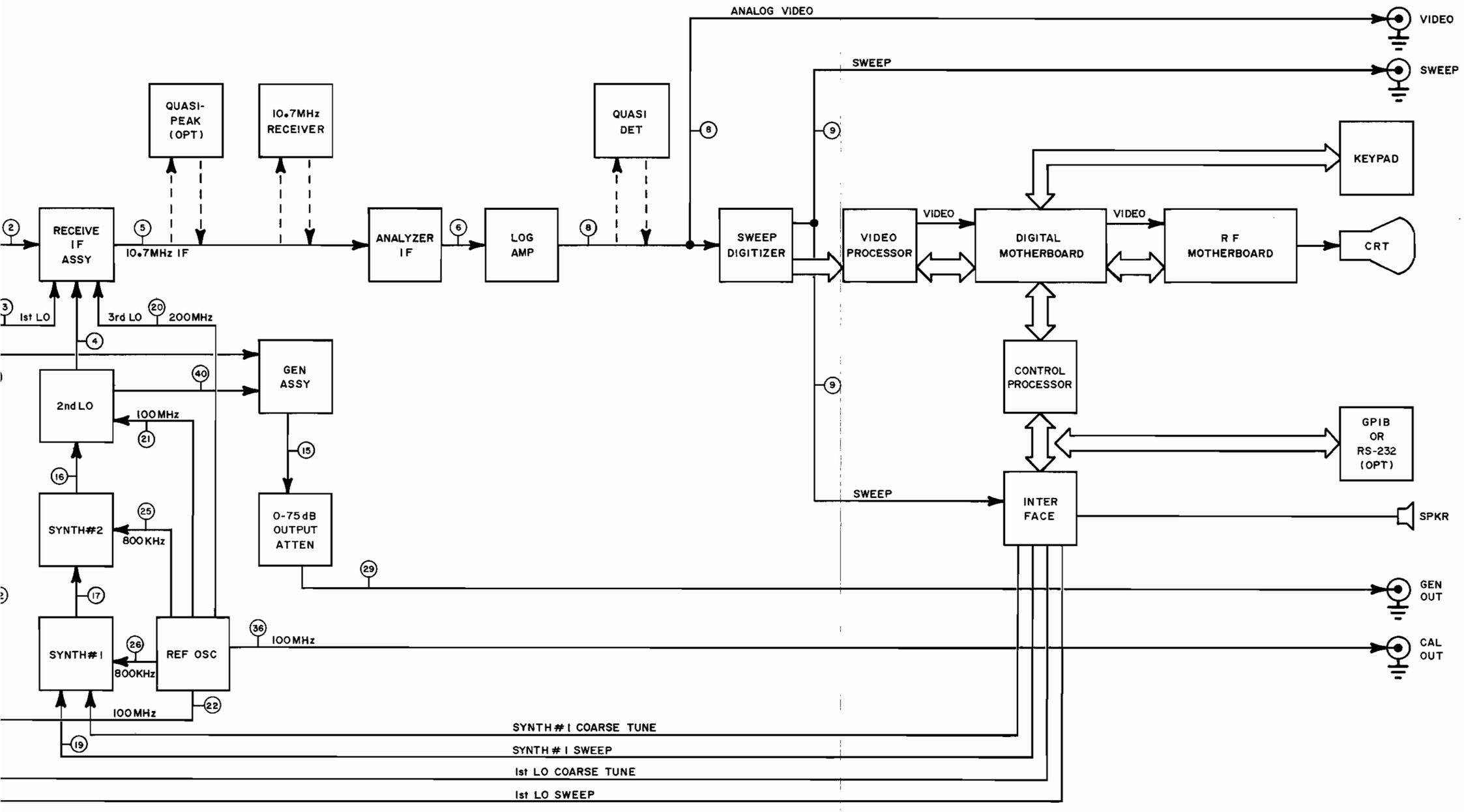


Figure 2-1 System Block Diagram

The A-7550 is an RF Spectrum Analyzer that is processor controlled and menu driven. It uses a CRT display system with a digital Vertical Raster Scan (VRS™) and can be powered by external AC or DC source. Internal battery power is optional.

The microprocessor system automatically selects and optimizes the scan width, sweep rate, display resolution and rate of the slew keys. Frequencies from 100 kHz to 999.9999 MHz can be directly entered through a numeric keyboard. Amplitude references are made using scales in 2 dB/DIV, 10 dB/DIV or in linear scale. They may be referenced in dBm, dBmV or dBμV.

All functions of the A-7550 that are selected from menus are concurrently displayed with graticule and trace information. Signals can be live or stored for comparison purposes. Table 2-1 lists the expanded analyzer options.

Option	Description
01	Internal Rechargeable Battery
02	Tracking Generator with 0 to 70 dB, 1 dB Step Attenuator
04	FM/AM/SSB Receiver
05*	IEEE-488 Interface Bus
06*	RS-232 Interface Bus
07	Selectable 50Ω/75Ω Adapter
08	Quasi-Peak Detector
*Options 05 and 06 cannot both be ordered on the same unit.	

Table 2-1 A-7550 Analyzer Options

The input signal is processed by the Receiver Group consisting of an attenuator, receive IF module, analyzer IF module and log amp. The Video Processor Group digitizes the signal and combines it with graticule and sweep information for display purposes. The Control Processor Group consists of a motherboard, CPU, interface PC board, CRT and keyboard. The Frequency Synthesis Group provides the frequency steering and phase lock function for the Receiver and Generator Groups.

2-3 FUNCTIONAL THEORY OF OPERATION

2-3-1 RECEIVER SECTION OPERATION

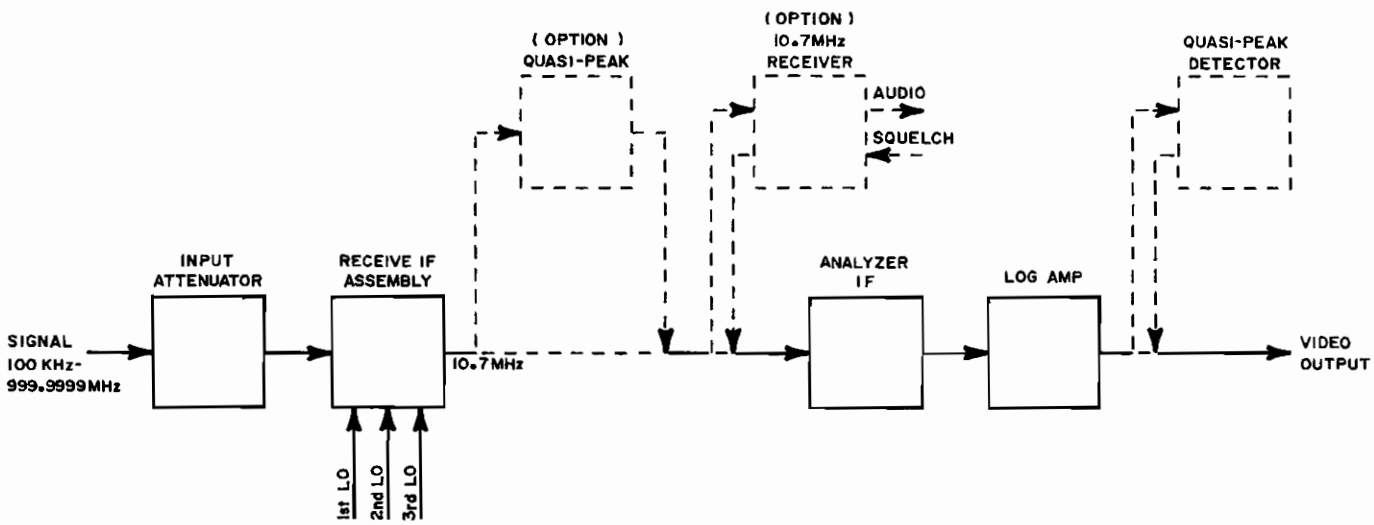


Figure 2-2 Receiver Group Block Diagram

The input signal is sent to the Receiver group. The Input Attenuator provides up to 60 dB of attenuation in 10 dB steps. The Receive IF Assembly receives the signal, triple converts it by mixing with signals from the Frequency Synthesis Group, and produces an IF of 10.7 MHz with 3 MHz bandwidth. The Analyzer IF assembly provides filtering of 300 kHz, 30 kHz, 3 kHz or 300 Hz. This signal is sent to the Log Amp module, where it is logarithmically or linearly amplified for video processing. IF gain of up to 65 dB is also provided in this assembly. If the 10.7 MHz Receiver (Option) is installed, the IF signal is tapped for selective filtering and demodulation. The Quasi-Peak (option) adds the selected bandwidths of 200 Hz, 9 kHz and 120 kHz to meet EMC testing standards.

2-3-2 VIDEO PROCESSOR OPERATION

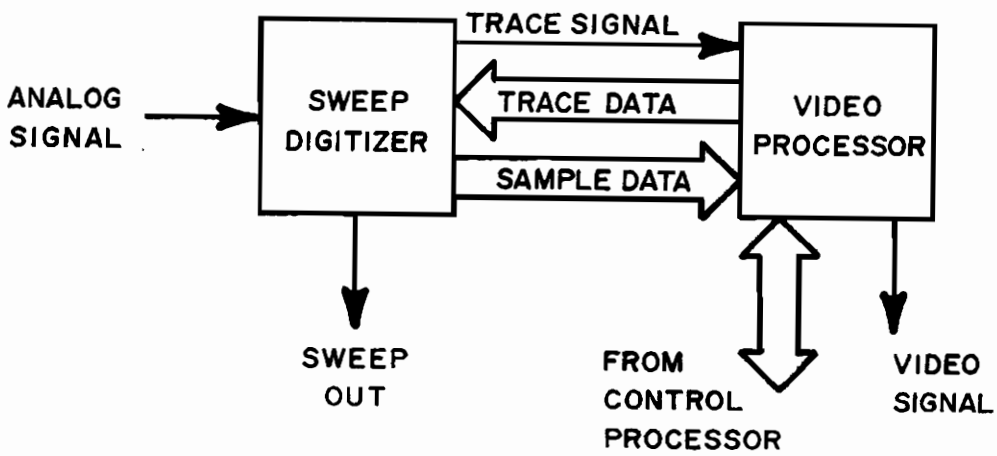


Figure 2-3 Video Processor Functional Block Diagram

The Video Processor group:

- Digitizes the Analog Signal from the Receiver group.
- Processes and stores data samples as required.
- Generates a video signal of alphanumeric (AN), graticule and trace information. This signal is passed to the CRT and displayed.
- Provides sweep information for the frequency synthesizer group.

2-3-3 CONTROL PROCESSOR OPERATION

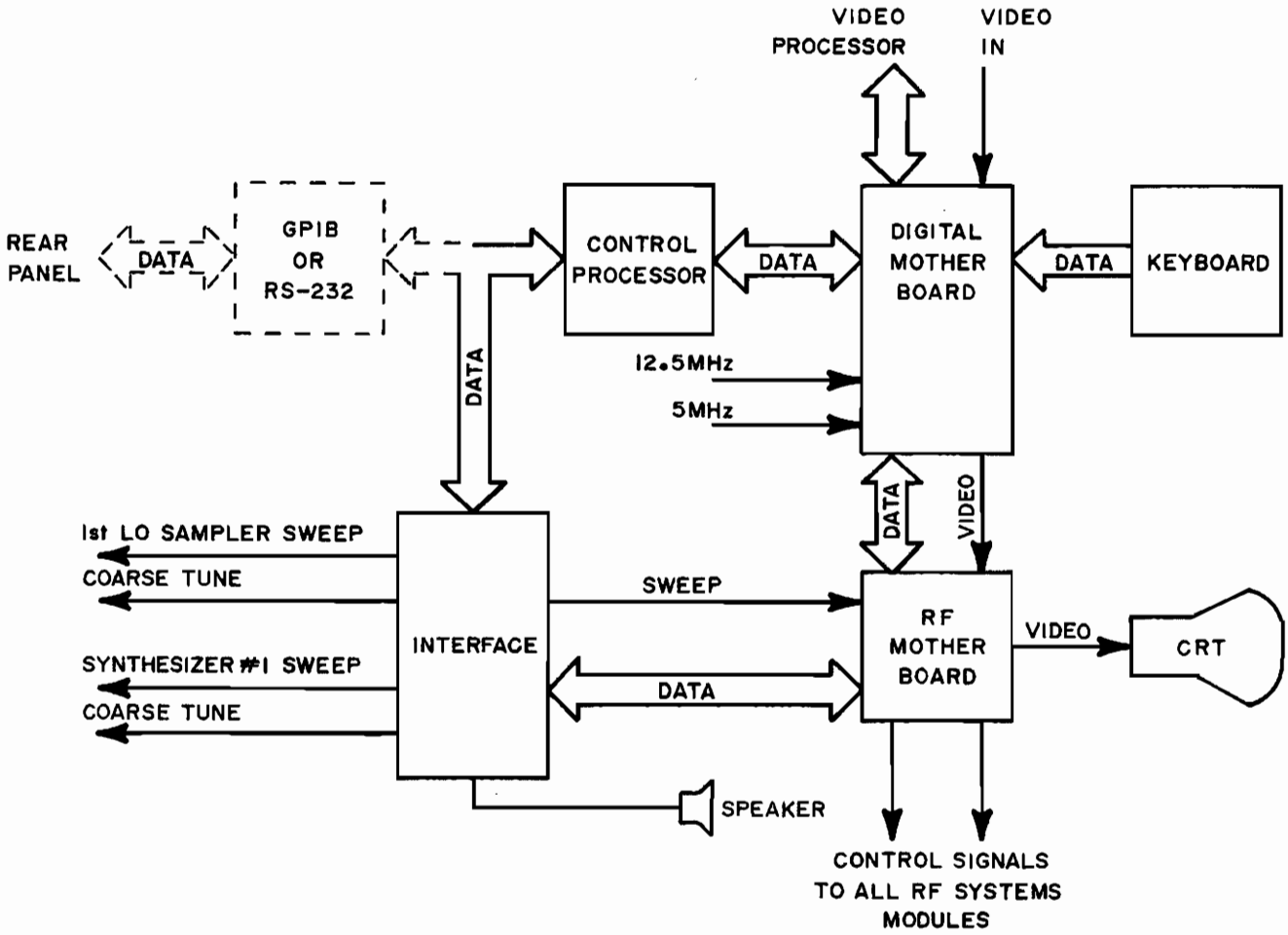


Figure 2-4 Control Processor Functional Block Diagram

The Control Processor group consists of a Digital Motherboard, Control Processor, Interface Board, Keyboard and CRT. Digital information from the keyboard, video processor and CPU are communicated through the motherboards. The Interface Board generates digital and analog signals to control the operation of the RF system.

2-3-4 FREQUENCY SYNTHESIS OPERATION

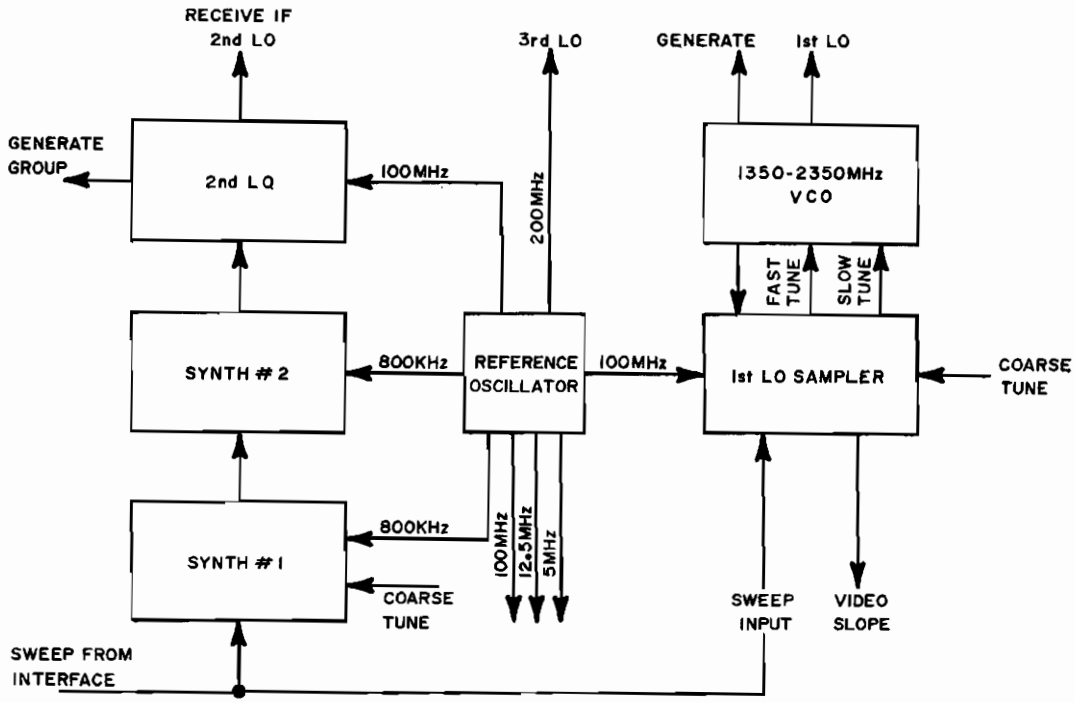


Figure 2-5 Frequency Synthesis Group Block Diagram

The Frequency Synthesis Functional Block consists of the Reference Oscillator, 1st L.O. Sampling Loop Module, the 1350-2350 MHz VCO Module, the Synthesizer #1 Module, the Synthesizer #2 Module, and the 2nd L.O. Module. The modules that make up this functional grouping perform the frequency steering and phase-lock functions for both the Receive IF and the Generator modules. To do this, reference frequencies from the Reference Oscillator and control signals from the Interface PC Board are used. The 1st L.O. Sampling Loop Module steers the 1350-2350 MHz VCO which drives the 1st Mixer in the Receive IF Module and the 2nd Mixer in the Generate Module. The Synthesizer #1 Module, the Synthesizer #2 Module and the 2nd L.O. Module act together to drive the 2nd Mixer in the Receive IF Module and the 1st Mixer in the Generator Module.

The frequencies developed in the frequency synthesis section are dependent on the center frequency and the scan width entered by the operator.

NOTE

THE LOCK FREQUENCY FOR THE START OF THE SWEEP IS THE FREQUENCY AT THE LEFT EDGE OF THE DISPLAY.

NOTE

Synthesizer #1 sweeps 1 kHz/DIV to 1 MHz/DIV. The 1st LO Sampler sweeps at 2 MHz/DIV and above.

EXAMPLES:

Left Lock Frequency:

Center Frequency = 500 MHz
Scan Width = 1 kHz/DIV
Left Lock Frequency = (Center Frequency) - (5 X Scan Width)
Left Lock Frequency = (500 MHz) - (5 X 1 kHz) = 499.995 MHz

1st LO Output Frequency:

1st LO Frequency = (1350 MHz IF) + (Largest multiple of 50 MHz frequency below left lock frequency)*
1st LO Frequency = 1350 MHz + 450 MHz = 1800 MHz

* i.e., (MOD 50 X 50 MHz)

1st Receive IF Output Frequency:

1st Receive IF Frequency = (1st LO Frequency) - (Left Lock Frequency)
1st Receive IF Frequency = (1800 MHz) - (499.995 MHz) = 1300.005 MHz

2nd LO Signals

2nd LO Output Frequency:

NOTE

2nd Receive IF Frequency always equals 189.3 MHz.

2nd LO Output Frequency = (1st Receive IF frequency) - (2nd Receive IF frequency)
2nd LO Output Frequency = (1300.005 MHz) - (189.3 MHz) = 1110.705 MHz

Synth #2 Output Frequency:

NOTE

Synth #2 output frequency is the same as the Summing Loop frequency.

Synth #2 Output Frequency = (2nd LO Frequency) - (1000 MHz)
Synth #2 Output Frequency = (1110.705 MHz) - (1000 MHz) = 110.705 MHz

Synth #2 VCO Frequency:

Calculated Synth #2 Frequency = (Synth #1 Minimum Effective Range Frequency) + (Synth #2 Output Frequency)

Calculated Synth #2 VCO Frequency = (200 kHz) + (110.705 MHz) = 110.905 MHz

Synth #2 VCO Frequency = Calculated Synth #2 raised to the next 100 kHz increment (i.e., MOD 100 X 100 kHz)

Synth #2 VCO Frequency = 111.0 MHz

Synth #1 Output Frequency:

Synth #1 Output Frequency = (Synth #2 VCO Frequency) - (Synth #2 Output Frequency)

Synth #1 Output Frequency = (111.0 MHz) - (110.705 MHz) = 295 kHz

NOTE

Synthesizer #1 starts the sweep at 295 kHz and stops the sweep at 305 kHz.

Table 2-2 is a chart of frequency synthesis calculations for each sweep range.

	CENTER FREQUENCY ENTERED	SCAN/DIV RANGE	LEFT LOCK FREQUENCY	1ST LO OUTPUT (AT 1350-2350 MHz VCO OUT)	1ST RECEIVE IF	2ND RECEIVE IF	2ND LO OUTPUT	SUMMING LOOP VCO	SYNTH #2 VCO	SYNTH #1 MINIMUM EFFECTIVE RANGE	SYNTH #1 OUTPUT
A	500.0000	ZERO	500.0000 FIXED	1850 MHz	1350 MHz	189.3 MHz	1160.7 MHz	160.7 MHz	160.9 MHz	200 kHz	200 kHz
A	500.0000	1 kHz THRU 10 kHz	499.9950	1800 MHz	1300.005 MHz	189.3 MHz	1110.705 MHz START	110.705 MHz START	111.0 MHz	200 kHz	295 kHz START SWEEP
B	500.000	20 kHz THRU 100 kHz	499.900	1800 MHz	1300.10 MHz	189.3 MHz	1110.80 MHz START	110.80 MHz START	112.8 MHz	2.00 MHz	2.0 MHz START SWEEP
C	500.00	200 kHz THRU 1 MHz	499.00	1800 MHz	1301 MHz	189.3 MHz	1111.7 MHz START	111.7 MHz START	131.7 MHz	20 MHz	2 MHz START SWEEP (X 10)
D	500.0	2 MHz THRU 10 MHz	490.0	1800 MHz START SWEEP	1310 MHz	189.3 MHz	1120.7 MHz	120.7 MHz	140.7 MHz	20 MHz	2.0 MHz NO SWEEP (X10)
D	500.0	20 MHz THRU 100 MHz	400.0	1750 MHz START SWEEP (X10)	(	SAME AS D ABOVE					)

Table 2-2 Frequency Synthesis Calculation

2-3-5 GENERATOR SECTION OPERATION

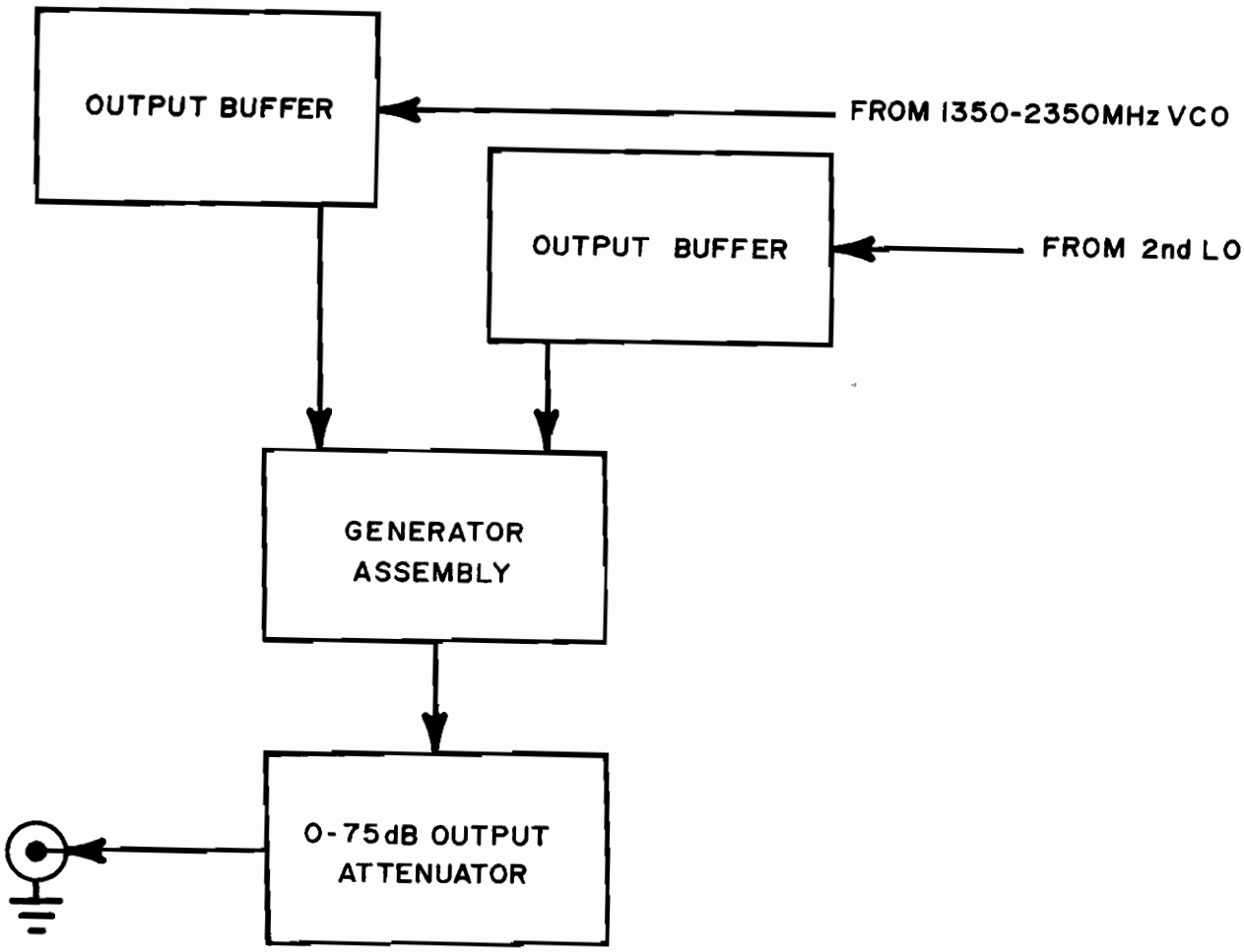


Figure 2-6 Generator Functional Block Diagram

The Generator group performs a tracking generator function. It uses selected outputs of the frequency synthesis group and an internal reference oscillator to create a tracking signal.

2-4 DETAILED THEORY OF OPERATION

The Theory of Operations in the remainder of this section gives supplementary information to the technician concerning the operation of each module in the A-7550. A block diagram accompanies the theory of most modules to assist the technician in following the functional flow of the schematics supplied in Section 5.

2-4-1 POWER SUPPLY MODULE

The Power Supply Module can operate on AC or DC. The AC input can be 106 to 266 VAC and 50 to 400 Hz. The DC input is an external +12 to +30 VDC source or optional internal battery. When the front panel PWR/OFF/BATT switch is set to PWR or to BATT, +12, -12, +5 and +40 VDC voltages are sent to the RF motherboard where they are distributed throughout the set.

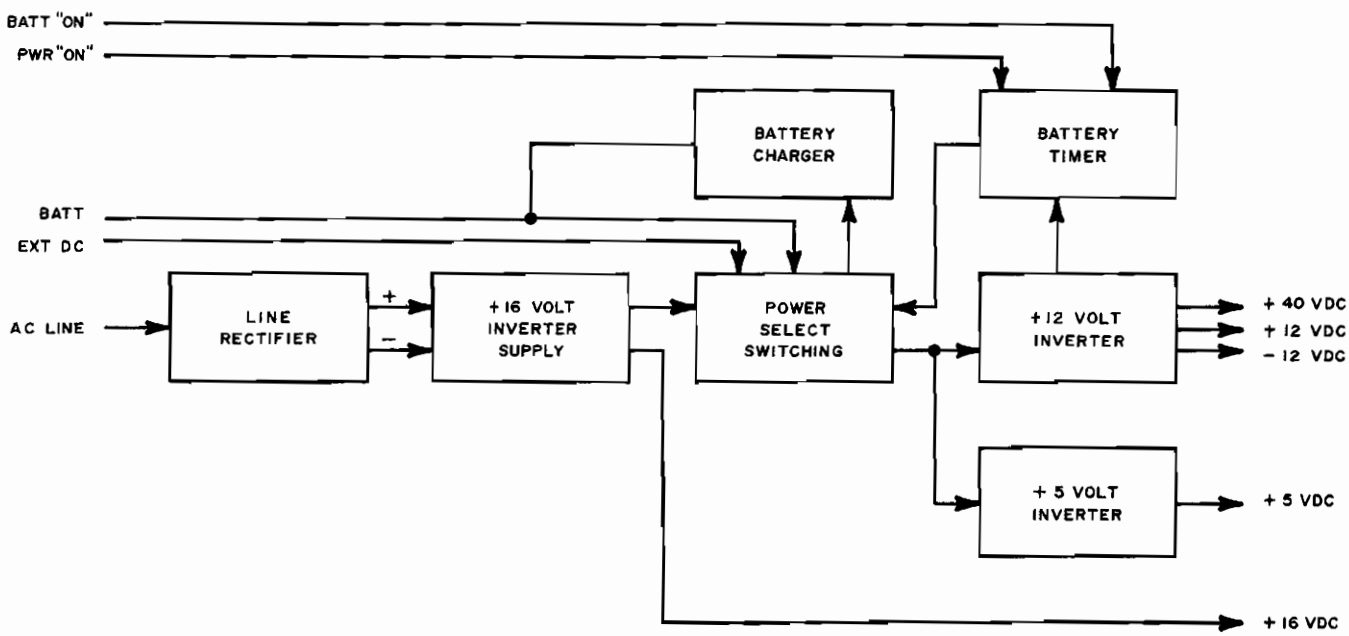


Figure 2-7 Power Supply Module Block Diagram

A. AC Line Voltage

The AC line voltage is filtered and rectified by T16001 and BR16001 on the Line Rectifier PC Board. The output of the rectifier, several hundred volts DC, is filtered by C16001 and C16002. The negative output of the line rectifier is used as a floating ground.

WARNING

THE DIFFERENCE OF POTENTIAL BETWEEN THE FLOATING GROUND AND CIRCUIT OR CHASSIS GROUND CAN EXCEED 300 V. THIS POTENTIAL CAN CAUSE SERIOUS INJURY OR EVEN DEATH. ALWAYS USE AN ISOLATION TRANSFORMER AND TAKE EXTREME CARE WHEN WORKING WITH AC VOLTAGES INSIDE THE POWER SUPPLY MODULE.

The DC output of the rectifier is applied to the Power Supply PC Board, where it is sent to the step-down transformer (T17002) and to the 15.8 V floating regulator. Q17018, Q17019 and CR17027 form a sub-regulator that reduces the rectified DC voltage to approximately 15 V. The regulated DC is supplied to U17011 to produce a sawtooth waveform, which is applied to the positive side of comparator U17012. Opto-coupler (U17013) couples in a controlled DC level, which is applied to the negative side of U17012 and outputs a rectangular wave with a duty cycle controlled by the DC output of the opto-coupler.

This rectangular wave is applied to Q17020 and Q17021, which provides the necessary drive current to give the metal oxide semiconductor switch (Q17022) fast turn-on and turn-off characteristics. Q17023, Q17024 and Q17025 act as current limiters. Q17022 essentially grounds one side of T17002 during the time that the rectangular wave from U17012, pin 3, is higher than pin 2. The output of T17002 is rectified by CR17024 and is fed back, through U17010, to the opto-coupler to provide +16 V regulation. Trimpot R17068 (+16V ADJUST) is provided to tune this feedback.

B. Battery Charger Circuit

The Battery Charger circuit operates on either +16 VDC derived from external AC or on +15 to +30 VDC external DC, whichever source is used. Q17001 supplies the current through CR17006. Q17002 controls the conduction of Q17001 from voltage supplied by comparator U17001. Adjust trimpot R17006 to produce 14.4 V at Q17001 with a minimum current of 0.3 A. If the battery is in low charge state, the voltage output at Q17001 drops and lowers the output voltage divider, R17004, R17005 and R17006, to pin 3 of U17001. Reducing the output at U17001 causes Q17002 to conduct, which increases the conduction of Q17001. R17001 limits the maximum current which Q17001 can draw to approximately 1.5 A.

C. Battery Timer/Enable Circuit

The battery enable circuit consists of flip-flop U17002A and associated components. When the PWR/OFF/BATT switch is toggled to BATT, the resulting ground discharges C17003 through R17014. This forces pin 11 of U17002A to a low condition.

As C17003 charges, the increasing voltage clocks U17002A, pin 13, to high output, which turns on Q17005 to enable the DC regulation circuits. Depressing the switch a second time clocks U17002A output to a low condition. If U17002A is not clocked a second time, the timer circuit will reset U17002A approximately ten minutes later.

Programmable timer U17003 starts counting as it receives +12 V output. A terminal count is set by highs on pins 9 through 12 and the on-chip oscillator frequency is established by R17022, R17023, and C17006 to allow approximately 10 minutes of battery operation. After this time period, U17003 provides a high output to reset U17002A output to a low condition, terminating battery operation only.

A low-voltage battery cutoff circuit stops battery operation if the battery voltage drops below approximately +11.4 VDC. Regulated +12 VDC is applied to the emitter of Q17006 and battery voltage is applied to the base. When battery voltage drops to approximately +11.4 VDC, Q17006 turns on and applies +12 VDC to the SET pin of U17003. This sets the timer to terminal count and causes U17002A to go to a low condition, terminating battery operation.

External power operation is enabled by depressing the PWR/OFF/BATT switch to PWR. This applies a ground to the base of Q17004, turning it on, and causing Q17005 to turn on. Q17003 is provided for fast circuit shutdown if external power is lost.

D. +12V Regulation

Q17005 provides a ground for the enable line if either battery or external power is selected. This turns on Q17007 and turns off Q17012. When Q17007 is on, Zener diode CR17013 sets a +10 VDC level which is applied to U17004, U17005, U17006, U17007, U17008 and U17009. When Q17012 is off, U17004 produces a sawtooth wave that is applied to the non-inverting input of integrator U17005. Zener diode (CR17013) produces 6.9 VDC that is used as a reference source for the +12 VDC and +5 VDC voltage regulator circuits. U17005 compares the oscillator output level with the reference level from U17008 and produces a pulsed output with a duty cycle that decreases as the reference level increases. R17035 and R17037 set a minimum reference to allow a maximum duty cycle of 50%.

The high output of U17005 turns on Q17008, applying voltage to the gates of Q17010 and Q17011. When Q17010 and Q17011 conduct, current flows through the primary winding of T17011. When the output of U17005 is low, Q17008 is turned off, blocking voltage to Q17010 and Q17011, while turning on Q17009. This turns off Q17010 and Q17011; which builds and collapses the magnetic field from the primary winding of T17001 proportionately to the duty cycle of U17005. The -12 VDC and +40 VDC outputs track the +12 VDC output.

If the +12 VDC output is low, the voltage output of divider R17055, R17056 and R17057 falls below the reference voltage level at pin 2 of U17008. This causes U17008 to integrate towards 0 V and increase the duty cycle output to U17005. More power is then supplied to T17001, which increases the +12 V output. If the +12 VDC output is too high, the voltage at pin 3 of U17008 will be above the reference voltage at pin 2 of U17008, causing the output of U17008 to integrate towards +10 V. This decreases the duty cycle from pin 6 of U17005 and reduces the power supplied to T17001, which brings the +12 VDC output within regulation. Trimpot R17056 sets the +12 VDC output.

E. +5V Regulation

R17041 charges C17017 when Q output at U17006 is high. When Q output is low, C17017 is discharged through CR17015.

The ramp produced by R17041 and R17017 is applied to pin 3 of U17007. The voltage at pin 2 of U17007 sets the duty cycle at pin 6 of U17007 and is controlled by the output U17009. If the +5 VDC output is low, voltage divider, R17060, R17061 and R17062, causes pin 3 of U17009 to drop below the reference level at pin 2 of U17009. This causes the output at U17009 to integrate towards 0 V, which increases the duty cycle at pin 6 of U17007 and increases the +5 VDC output to the proper level, should the +5 VDC output be high. The voltage at pin 3 of U17009 will then be above the voltage at pin 2 of U17009, causing the output of U17009 to integrate towards +10 VDC, decreasing the duty cycle and decreasing the +5 V output regulation.

When the output of U17007 is high, Q17013 turns on, dropping the emitter of Q17015 low and allowing Q17016 and Q17017 to conduct. In this state, Q17014 is off. When U17017 output is low, Q17013 is off and Q17014 conducts, forcing emitter Q17017 to go high. The high voltage of gates Q17016 and Q17017 turns them off. L17008, L17009 and C17023 form a filter to produce +5 V output for the system. Trimpot R17062 sets the +5 VDC output.

2-4-2 0-60 dB INPUT ATTENUATOR MODULE

When 0 dB is selected, control lines to relays K35001A and K35002A are at 0 V, allowing the signal to be routed through contacts K35001A and K35002A. These contacts are normally closed. Pin 1 of J34003 supplies -12 V, which turns on diodes CR35002A and CR35003A, and bypasses the 30 dB attenuator.

When 10 dB is selected, pin 3 of J34003 goes high (+12 V) and energizes relay K35001A, which routes the signal through the 10 dB attenuator, R35001A, R35002A, R35003A and C35003A. When 20 dB is selected, pin 2 of J34003 goes high and routes the signal through the 20 dB attenuator, R35017A, R35006A, R35005A, and C35007A. When 30 dB is selected, pin 1 of J34003 goes to +12 V, allowing conduction of CR35001A and CR35004A; which sends the input signal through the 30 dB attenuators. When 50 dB is selected, the signal is routed through the 20 dB and 30 dB attenuators. When 60 dB is selected, the signal is routed through the 10 dB, 20 dB and 30 dB attenuators.

2-4-3 RECEIVE IF MODULE

The Receive IF Module receives the attenuated RF input signal and, through interaction with the frequency synthesis modules, converts it three times to give a 10.7 MHz IF output.

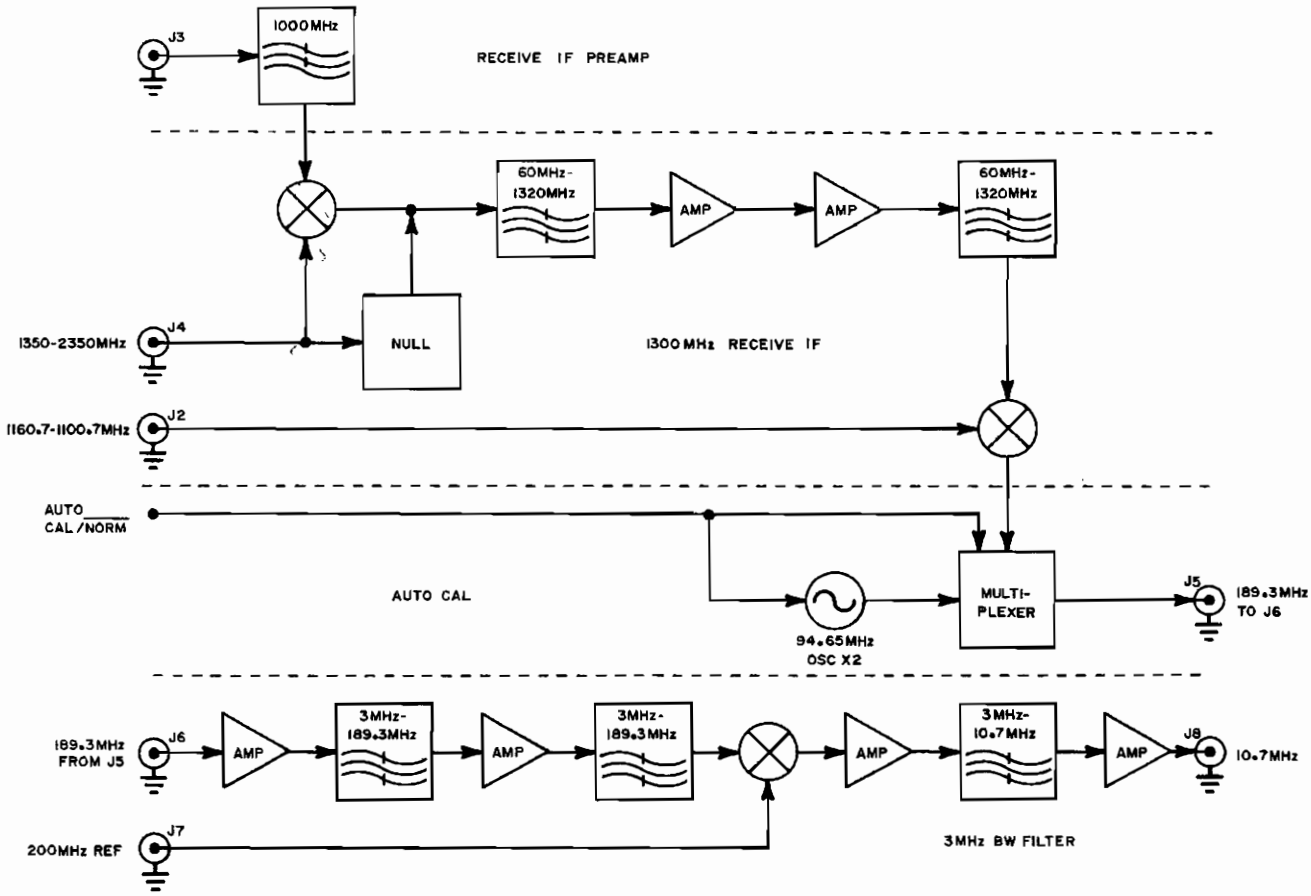


Figure 2-8 Receive IF Module Block Diagram

A. Input Low-Pass Filter PC Board

The input signal passes through a low-pass filter before it is passed to the first mixer.

B. 1300 MHz Rec IF PC Board

MXR41001 mixes the input signal with a signal from the 1350 to 2350 MHz VCO to up-convert it to a 1290 to 1350 MHz IF signal. A null circuit nulls the 0 frequency, which, if the LO signal overdrives the IF amplifiers, could desensitize the 0-10 MHz band. U45001 and U45002 amplify the mixed signal and send it through the 1290-1350 MHz bandpass filters to MXR41002. On later sets, Q45001 and U45001 provide the necessary amplification. MXR41002 down-converts the IF signal to 189.3 MHz by mixing it with an 1160.7 to 1100.71 MHz signal from the 2nd LO block.

C. Auto Cal PC Board

The A-7550 microprocessor normally has the AUTO CAL/$\overline{\text{NORM}}$ line set to about -10 V. This forward biases CR43001 and CR43002 to allow the received signal to pass. Periodically, the microprocessor sets the AUTO CAL/$\overline{\text{NORM}}$ line high (about +10 V). This forward biases CR43003 to power up a 94.65 MHz calibrated oscillator circuit, while shutting off the received signal. The oscillator then drives CR43007, resulting in a high level of second harmonic (189.3 MHz). The 189.3 MHz harmonic is then used as a calibrated reference level.

The microprocessor uses the calibrated output level of the oscillator to adjust the IF gain and maintain the amplitude calibration of the A-7550. The A-7550 performs an auto cal cycle every 600 sweeps.

Q43001, Y42001 and associated components form the oscillator circuit. L43006 is an adjustment for tuning the oscillator. CR43005 is a level detector that biases Q43002 and Q43003 to maintain constant amplitude. CR43006 is used for temperature compensation. The RF output goes through CR43007, trimpot R43010 and R43011. R43010 is used to set the Auto Cal reference level.

D. 3 MHz BW Filter PC Board

The 189.3 MHz signal is passed through Q42001 to the first 189.3 MHz bandpass filter. The output of this filter is buffered and amplified by Q42002 and passed through the second bandpass filter. The output of the second filter is applied to MXR42001, where it is mixed with 200 MHz from the reference module to produce 10.7 MHz IF. Q42003 amplifies the 10.7 MHz IF, which is then filtered and amplified by Q42004. Trimpot R42029 is adjusted to match the 10.7 MHz output level at J41008 with the RF Analyzer input level. J41008 sends the 10.7 MHz signal to the ANAL IF Module.

NOTE

If the Quasi-Peak Filter Module or the Receiver Module is installed, the 10.7 MHz signal is routed through each of the installed modules.

2-4-4 ANALYZER IF MODULE

The Spectrum Analyzer IF module selects the resolution bandwidths for the analyzer display. Available bandwidths are 3 MHz, 300 kHz, 30 kHz, 3 kHz and 300 Hz.

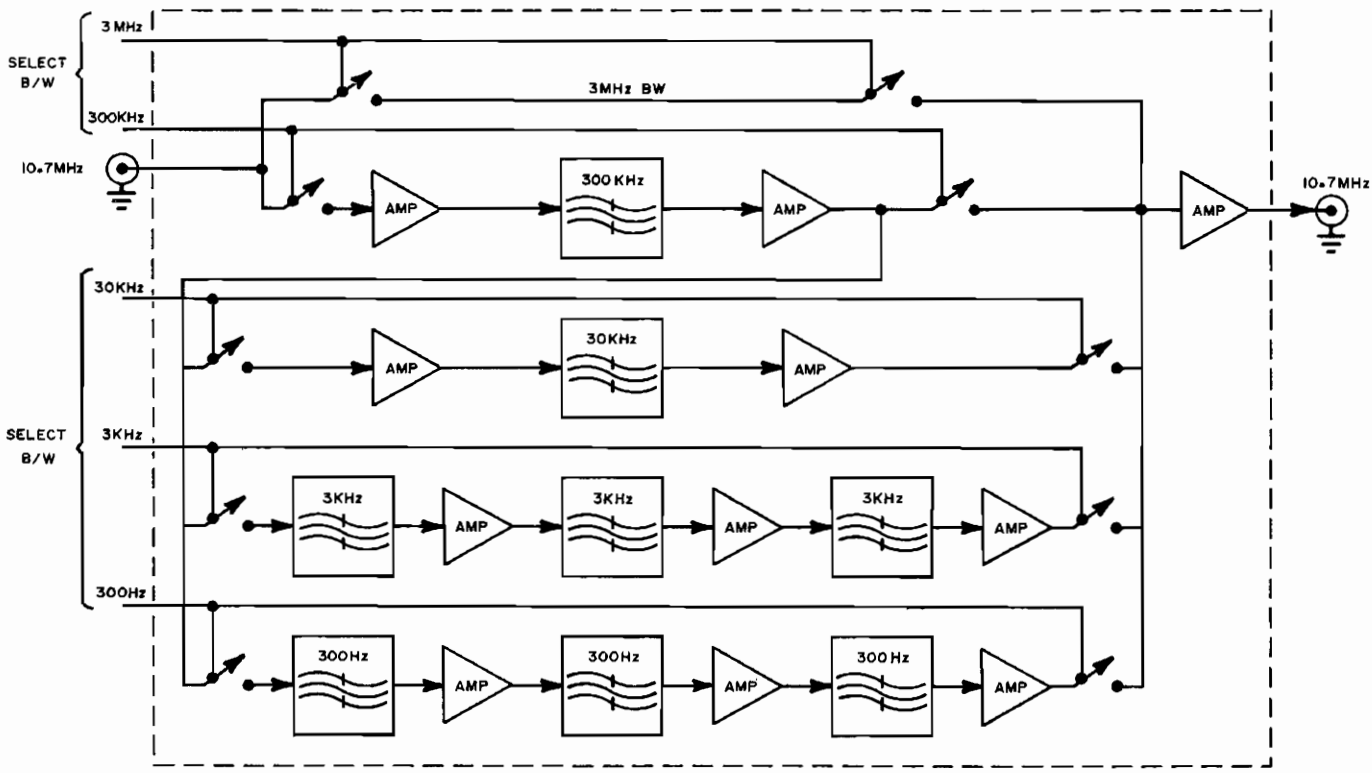


Figure 2-9 Analyzer IF Module Block Diagram

When any one of the bandwidth select lines goes high, its appropriate signal path is selected. For instance, if pin 3 of P21001 goes high, CR22008, CR22005, CR22002 and CR22014 are forward biased to allow the 10.7 MHz signal to pass through the 300 kHz bandwidth path, then through the 3 kHz bandwidth path. Except for 3 MHz bandwidth selection, which bypasses any filtering on this board, all signals flow through the 300 kHz filter. 300 kHz, 30 kHz, 3 kHz and 300 Hz bandwidths have tunable elements and level adjusting pots. For whichever bandwidth is selected, Q22003 amplifies the IF level. Trimpot R22020 (IF LEVEL GAIN) is provided to adjust the IF gain to the Analyzer output level. The output of the Analyzer IF Module is sent to the Analyzer Log Amp.

2-4-5 LOG AMP MODULE

The 10.7 MHz IF signal from the Analyzer IF Module is input at J25003. The microprocessor on the Control Processor board sets the control lines as selected through the keyboard and by menu operation, and also compensates for Auto Cal gain and temperature changes.

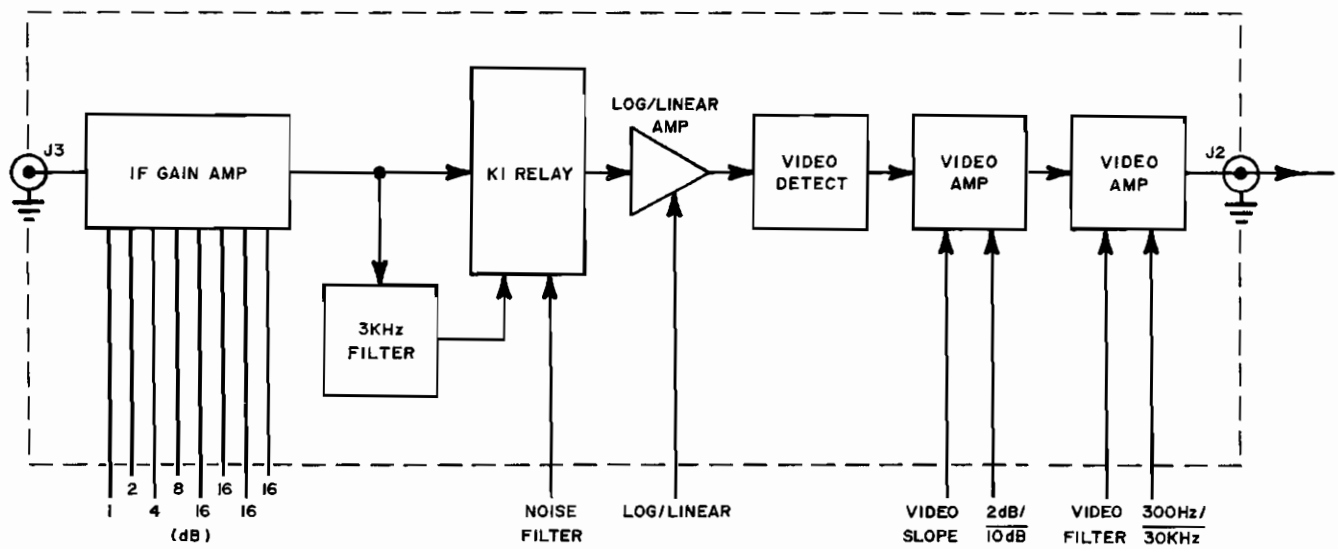


Figure 2-10 Log Amp Module Block Diagram

A. IF Gain

Q26001 through Q26017 and associated components form the IF Gain stages. A maximum total of 65 dB is available through the keyboard.

The eight control signals for gain selection come from the Interface Board, as selected by the microprocessor. The first four control lines select IF gain of 1, 2, 4 and 8 dB, respectively. Each of the next four control lines selects an independent 16 dB gain stage. When the microprocessor selects 1 dB of IF gain, pin 1 of J25001 is pulled high. This turns on Q26002 which parallels R26005 with emitter resistor R26004 of Q26001. Each gain stage operates similarly.

Relay K26001 powers up when the noise filter line, pin 19 of P25001, goes high. Because of the noise from the IF Gain Amplifier, YFL26001 then switches into the gain circuit to further filter the signal. This occurs whenever 300 Hz or 3 kHz is selected as resolution bandwidth.

B. LOG/LIN Amplifiers

The voltage applied to pin 21 of J25001 selects either LOG or LIN mode. When the voltage applied goes low, the LOG amplifier mode is selected. When the voltage applied goes high, the LIN Amplifier Mode is selected.

1. Log Amplifier Operation

When the voltage applied to pin 21 of P25001 goes low, +12 V is selected on pin 14 of U26005A and +5 V is selected on pin 15 of U26005B. This sets the amplifier stages of Q26018 through Q26029 to LOG mode. The first four stages, Q26018 through Q26025 operate similarly and are explained below using the stage consisting of Q26018 and Q26019.

Forward biasing of diodes CR26003 and CR26004 puts R26064 and C26035 in parallel with R26061 and R26063. The gain stage becomes logarithmic as the transistor emitter current overcomes the diode conduction current. Trimpot R26066 (REF LINE COMPRESSOR) sets a voltage limiting level for top of screen display.

2. LIN Amplifier Operation

When the voltage applied to pin 21 of P25001 goes high, -5 V is selected on pin 14 of U26005A and +12 V is selected on pin 15 of U26005B. This sets the amplifier stages of Q26018 through Q26029 to the LIN mode. The log diodes in each stage are reverse biased, which isolates them from the circuit. Each of the first four stages then have a single resistor to ground. In the fifth stage, CR26013 and CR26014 are forward biased, putting R26111 in parallel with R26110. In the sixth stage, CR26018 and CR26019 are forward biased putting R26124 and R26123 in parallel with R26122. Trimpot R26123 (LINEAR GAIN ADJ) is provided in one parallel leg to match the LIN level with the log level.

C. Video Detect

C26067 couples the 10.7 MHz signal into a discrete differential amplifier circuit consisting of Q26030, Q26031 and Q26032. C26022 couples the signal from the collector of Q26032 to full-wave detector (CR26021 and CR26022). C26076, C26077 and L26010 then filter the signal before sending it to U26003.

D. Video Amp

U26003 is an inverting video amplifier. The 2 dB/10 dB line selects the gain of the first half of the video amplifier (U26003A). R25156 (2 dB OFFSET) and R26151 (10 dB OFFSET) set their respective offset reference levels. (On PC board 7010-5337-100, R26195 (LINEAR OFFSET) has been added for a linear voltage reference. This adjustment is switched in through U26005C when the linear mode is selected.) R26159 (2 dB GAIN) and R26161 (10 dB GAIN) set their respective gain levels for trace display. To compensate for amplitude loss at high frequencies, a DC voltage is input from the frequency-to-voltage converter of the first LO SAMPLER to pin 3 of U26003A.

E. Video Filters

The output of U26003A feeds U26001B which switches capacitors in either the 30 kHz or 300 kHz video filter as selected from the A-7550 filter menu. U26001C switches between the capacitors or NONE SELECTED. When the 300 Hz filter is selected, U26001B connects C26082, 0.1 µF capacitor in parallel with R26164. When the 30 kHz filter is selected, C26081, 1000 pF capacitor, is connected in parallel with R26164. The output of the video amp (U26003B), which acts as a buffer, is sent to the sweep digitizer board and to the ANALOG VIDEO OUT connector on the rear panel.

2-4-6 10.7 MHz RECEIVER MODULE (OPTION)

The 10.7 MHz Receiver Module receives a 10.7 MHz signal from the Receive IF Module and directly sends it to the ANAL IF Module. The tapped signal is filtered, demodulated and routed to the speaker via the Interface PC Board.

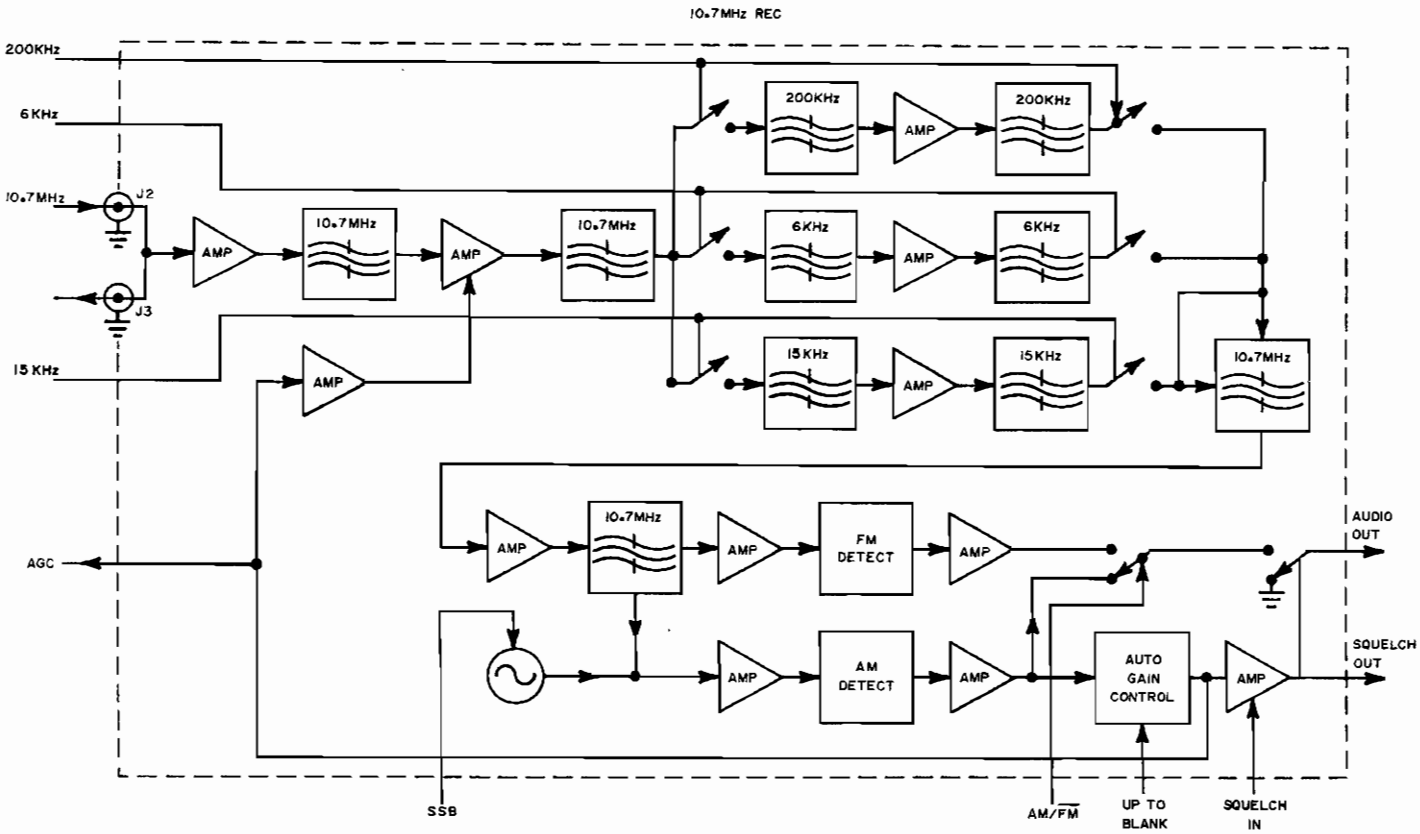


Figure 2-11 10.7 MHz Receiver Module Block Diagram

A. Bandwidth Selection

Bandwidth selection is controlled by the microprocessor, via the RCVR menu. Table 2-3 shows the action of the control lines as selections are made on the RCVR menu.

RCVR Selection	Control Lines				
	6K	15K	200K	SSB	FM/$\overline{\text{AM}}$
FM1 (NAR)	0	1	0	0	1
FM2 (Wide)	0	0	1	0	1
SSB	1	0	0	1	0
AM1 (NAR)	1	0	0	0	0
AM2 (Wide)	0	1	0	0	0

Table 2-3 Receiver Audio Bandwidth Selection

B. Bandpass Amplifier Circuit

Q58001 amplifies the signal received from the Receive IF and routes it to FL58001. FL58001 (pin 1) output is applied to pin 2 of FET Q580003. Pin 3 is controlled by the AGC (Automatic Gain Control) signal from Q58007 and Q58008. Filter FL58003 tunes the drain of Q58003 to 10.7 MHz. From FL58003, the signal is split and filtered for 6K, 15K or 200K bandwidths.

Each filter consists of (in signal flow order) a blocking diode, a crystal filter, a transistor amplifier, a second crystal filter, and a second blocking diode. To select any of the three filters, a +12 V bias is applied to the blocking diodes and to the transistor of the selected filter circuit.

C. FM Detector Circuit

Q58009 receives the filtered 10.7 MHz signal at pin 2 and amplifies it. Pin 3 of Q58003 is controlled by the AGC signal from Q58007 and Q58008. The output at pin 6 of FL58005 is amplified by Q58010. Diodes CR58008 and CR58009 limit the FM envelope. U58001 is an FM detector. The components connected to pins 2, 10 and 12 of U58001 form a tune circuit for the detector at 10.7 MHz. The detected FM audio output at pin 1 is amplified by U58002B and switched through U58003C to U58003B if the FM select line is high.

D. AM Detector Circuit

The output tap, pin 3 of FL58005, is coupled to the base of Q58013. When SSB is selected on the RCVR menu, pin 2 of J57001A goes high, causing Q58011 to conduct. This allows Q58012 to oscillate at 10.7 MHz. SSB injection level, R58077, is a level adjustment for the 10.7 MHz input to Q58013. The output at the collector of Q58013 is tuned by FL58006. CR58011 and C58076 form an AM detector. U58002A amplifies the detected AM and applies the audio to pin 12 of U58003C.

For FM/AM operation, the 10.7 MHz level detected by CR58011 and C58076 is fed to pin 15 of U58003A through R58087 (47 K). For SSB operation, Q58014 is turned on. Q58014 routes the 10.7 MHz level detected by CR58011 and C58076 through R58086 and CR58012 to pin 15 of U58003A.

When TSR1 (Time Share Receiver) is selected on the RCVR menu, Q58015 is turned off during RF sweep retrace. This allows R58090 to enable U58003A, which passes the AGC (Automatic Gain Control) signal to reverse bias CR58014. This, in turn, allows squelch audio gate, U58003C, to operate normally. U58004A is the AGC amplifier and U58005A provides AGC positive limiting.

In FM operation, the extra capacitance of C58079 is switched in through U58006C. U58004B is a differential amplifier which sets the squelch threshold and controls the audio output of the selected mode, switched through U58003B. Q58007 and Q58008 are the AGC gain transistors whose current is controlled by the AGC amplifier (U58004A).

R58088 and R58089 send +1.1 V on pin 3 of U58004A, causing the output of U58004A to go positive. When the output of U58005A to pin 2 of U58004A reaches the voltage level at pin 3 of U58004A, pin 1 of U58004A maintains a positive voltage and maximum receiver gain.

When the signal level detected from pin 1 of U58002A exceeds the voltage level at pin 3 of U58004A, the output of U58004A integrates toward -12 V. The negative voltage from pin 1 of U58004A activates the AGC system through transistors Q58007 and Q58008. This reduces receiver gain. When voltage at pin 1 of U58002A equals voltage at pin 3 of U58004A, U58004A maintains a negative output voltage.

As U58004A pulls down emitter Q58008, it first conducts and reduces its collector voltage and gain at Q58009. As the collector of Q58008 pulls down the emitter of Q58007, it conducts and reduces its collector voltage and gain at Q58003. U58004A output also goes to pin 6 of U58004B (squelch gate). While pin 5 of U58004B is more negative than the squelch, Q58015 is off, allowing U58003B to pass an audio signal.

2-4-7 QUASI-PEAK FILTER MODULE (OPTION)

The Quasi-Peak Filter module is an optional module which selects the bandwidths required for Quasi-Peak operation.

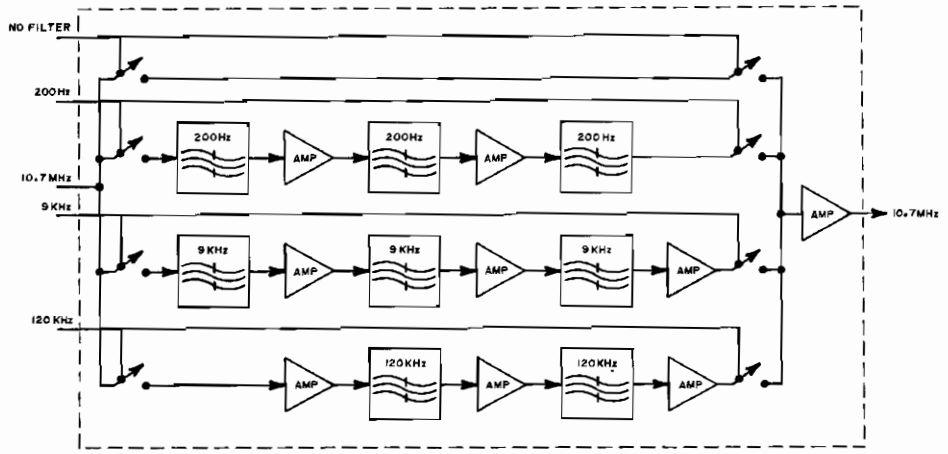


Figure 2-12 Quasi-Peak Module Block Diagram

A. Bandwidth Selection

Pins 4 and 5 of J62001 are, respectively, TC MSB and TC LSB. These lines are controlled by the Control Processor Board, through the Interface Board. The time constant desired can be selected through the QUASI-PEAK menu, as shown in Table 2-4.

Time Constant	MSB	LSB	Bandwidth
None	0	0	Normal Anal
TC1	0	1	200 Hz
TC2	1	0	9 kHz
TC3	1	1	120 kHz

NOTE Time constants and bandwidths are paired and cannot be split. Bandwidth is not available in normal analyzer functions.

Table 2-4 Quasi-Peak Bandwidth Selection

B. Quasi-Peak IF Filter

Q36009 through Q63012 conduct forward bias CR63001 through CR63008, respectively, depending on the selected bandwidth. For example, if the 200 Hz bandwidth is selected, Q63010 conducts. CR63001 and CR63002 are forward biased, allowing the incoming signal to pass through the 200 Hz filter. If Quasi-Peak bandwidths are not selected, Q63009 conducts forward bias (CR63003 and CR63004). This allows the 10.7 MHz signal to pass through the Quasi-Peak assembly. Gain pots are provided in each path to set the necessary output level for each filter circuit.

2-4-8 SWEEP DIGITIZER PC BOARD

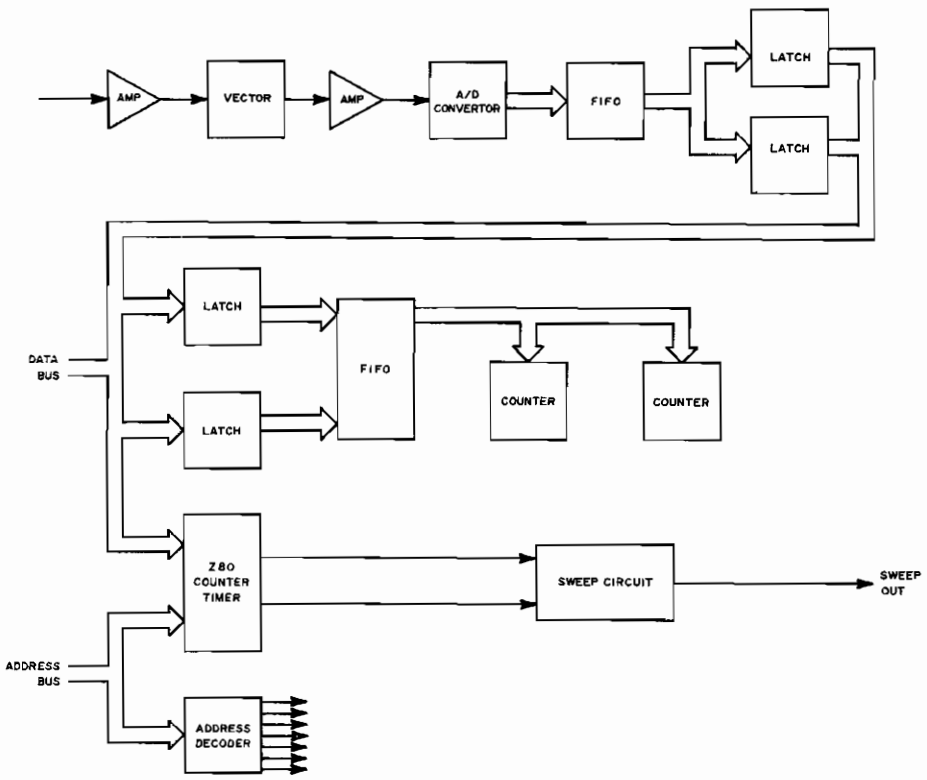


Figure 2-13 Sweep Digitizer PC Board Block Diagram

The Sweep Digitizer PC Board has three functions:

1. Taking digital samples;
2. Generating the sweep waveform for the RF system; and
3. Producing traces for the CRT display.

Timing diagrams are included in Figure 5-8.

A. Sample Circuit

Video from the Log Amp Module enters the Sweep Digitizer PC Board through J32003, where it is low-pass filtered by C32019. U32028 charges C32025 through CR32003 and R32003 to the positive signal peak occurring in each sample interval. This peak is sampled by C32021. After sampling, Q32001 discharges C32025 to about -0.7 VDC. (Q32001 is driven by a negative-going pulse on the base of Q32002.) U32017 output is fed to ten-bit analog-to-digital converter (ADC) U35010. The data is fed into a 512 x 9-bit First-in First-out memory (Sample FIFO), U32005. The sample FIFO is written at the sample interval rate. This allows the Microprocessor PC Board to read the data as time permits. U32023B operates as two monostable multi-vibrators to properly sequence the peak holding and digitizing processes.

B. Sweep Circuit

When a sweep is required, the Trace Microprocessor sends a "start" command to the Sweep Digitizer PC Board. U32006 decodes the command and sets a flip-flop consisting of U32018A and U32018B. U32018B releases the clear pin (11) of U32024, a 12-bit counter. The counter increments on negative edges of the ramp clock pulse provided at pin 9 of U32011. U32024 is incremented twice per sample interval, producing a digitized ramp. U32025, a ten-bit digital-to-analog converter (DAC), produces a ramp current that feeds U32026A, a current-to-voltage converter. After low-pass filtering, the sweep ramp is output through J35002 to the Interface PC Board in the Control Processor Group. The Trace Microprocessor generates a "stop" command which holds U32024 reset until the next "start" command is received. (The "Stop" command can be generated at any indefinite time after the last sample is taken).

C. Trace Circuit

Trace Circuit display consists of a series of vertical line segments. Each segment is produced by turning the electron beam on and off at particular times. The Trace Microprocessor batch loads 9-bit digital values into U32008, a 512 x 9 First-in First-out memory (Display FIFO) in an on-off-on-off sequence. The BCUR signal from the Video Processor PC Board generates an interrupt to the Trace Microprocessor at the end of each displayed field. The Trace Microprocessor then loads all values for the next field to be displayed.

U32009A generates the interrupt (reset by $\overline{3CW}$) and U32009A tells the Trace Microprocessor which field to load. U32003 and U32004 converts 8-bit data into 9-bit words. U32014/U32015 and U32020/U32021 are configured as 9-bit down counters.

The counters operate as follows:

The first counter to reach zero stops counting and turns on trace. When the other counter reaches zero, it stops counting and turns off trace. U32012A and U32012B stop their respective counters. U32013 and U32027 provide the timing signals for loading and enabling the counters. U32022 delays the U32014/U32015 count by one clock pulse and delays the U32020/U32021 count by five clock pulses. (The counters are loaded at different times.) U32018C and U32019A generate the trace from the signal produced by the counters and delay elements. The trace is a TTL-level signal that is sent to the Video Processor PC Board for gating and analog level adjustment.

2-4-9 VIDEO PROCESSOR PC BOARD

The Video Processor PC Board communicates with the Control Processor PC Board and Sweep Digitizer PC Board to develop display video.

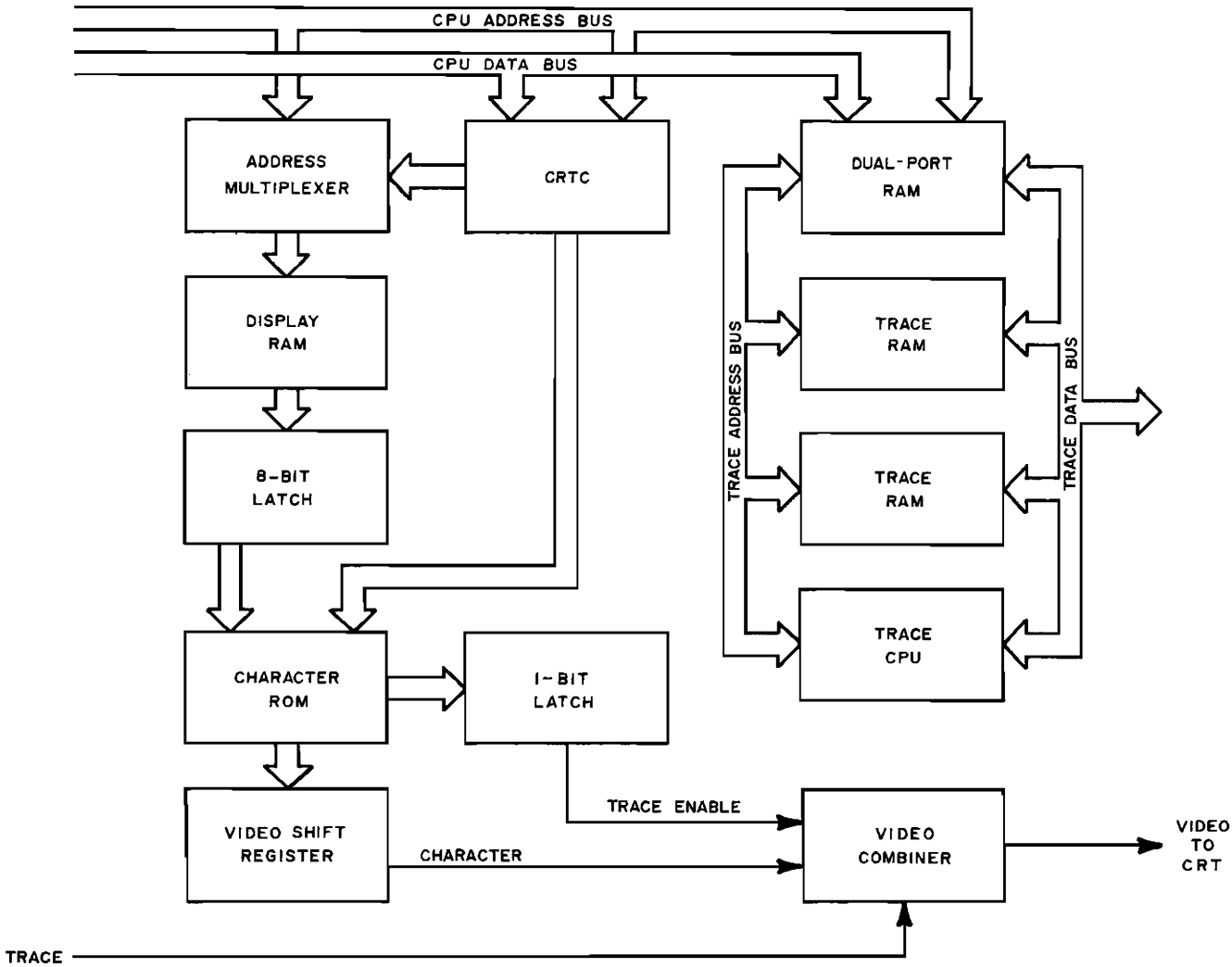


Figure 2-14 Video Processor PC Board Block Diagram

A. A-7550 Display

The A-7550 uses interlaced Vertical Raster Scan (VRS$^{T.M.}$) with a 7-inch electromagnetic-deflection monochrome CRT. The display operates in a manner similar to, but not compatible with, standard broadcast video. The deflection yoke in the CRT is rotated 90° counter-clockwise from standard video, and scanning frequencies are higher. In interlaced scan, alternate fields (even/odd) produce video, timed to position the lines of one display field midway between the lines of the other display field.

B. Character Display

The Character Display Section of the Video Processor PC Board displays alphabetic and numeric characters. The graticules are special display characters. The CRT controller (U31007) is the heart of the Display section. It provides address information during Display RAM read and synchronizes CRT and trace section signals.

U31001, U31002 and U31003 address Display RAM. When the control processor (U20004) is writing information into Display RAM, U20004 supplies memory addresses to the Display RAM; otherwise, the U31007 supplies memory addresses to Display RAM. U31032 latches Display RAM output and selects the appropriate character from character ROM. Character ROM output is seven bits. Six bits are input to video shift register (U31010) and output to the Video Combiner. The other bit identifies a graticule character and is output to U31012B.

U31011, U31021C, U31021D and U31022B provide timing signals for Display RAM, latches and shift registers. The Display Enable (DE) signal from the CRT Controller is delayed in U31029 for Sweep Digitizer PC Board use. Characters are arranged in U31008 as 6 x 13 pixels.

C. Trace Display

Most of the Trace Display Section is on the Sweep Digitizer PC Board. The trace uses its own microprocessor system (U31004, U31009, U31017, U31018, U31019 and U31020). U31017 is also used for temporary storage of trace information. U31019 is a dual-port RAM. This device buffers commands and information between the trace microprocessor system and Control Processor.

D. Video Combiner and Video Output Section

Traces cannot appear over characters without the graticule bit set. The circuitry that controls this section is U31027, U31021A, U31021B and U31026E.

Q31001, Q31002 and associated components, form a differential amplifier for graticule video. The graticule pot on the front panel adjusts current flow, which adjusts the gain of the graticule video amplifier. Q31003 and Q31004 operate similarly for the trace and non-graticule characters. The collectors of Q31002 and Q31004 have a common load resistor which superimposes or combines the dual output. U31012A, U31022A, and Q31005 are microprocessor controlled and serve to shunt part of the video signal to ground. Otherwise, the display would be too bright to view comfortably in some display modes.

U31025 buffers the clock and synchronizing signals for the Sweep Digitizer PC Board, CRT Module and CRT Controller (U31007).

2-4-10 CONTROL PROCESSOR PC BOARD

The Control Processor Board serves as the master controller of the A-7550. It controls communication between the Interface PC Board and the Video Processor PC Board, the Keyboard and either the GPIB or RS-232 option (if either is installed). Circuitry has also been included on the Control Processor PC Board that allows the unit to be expanded with a plug-in ROM Pack Module.

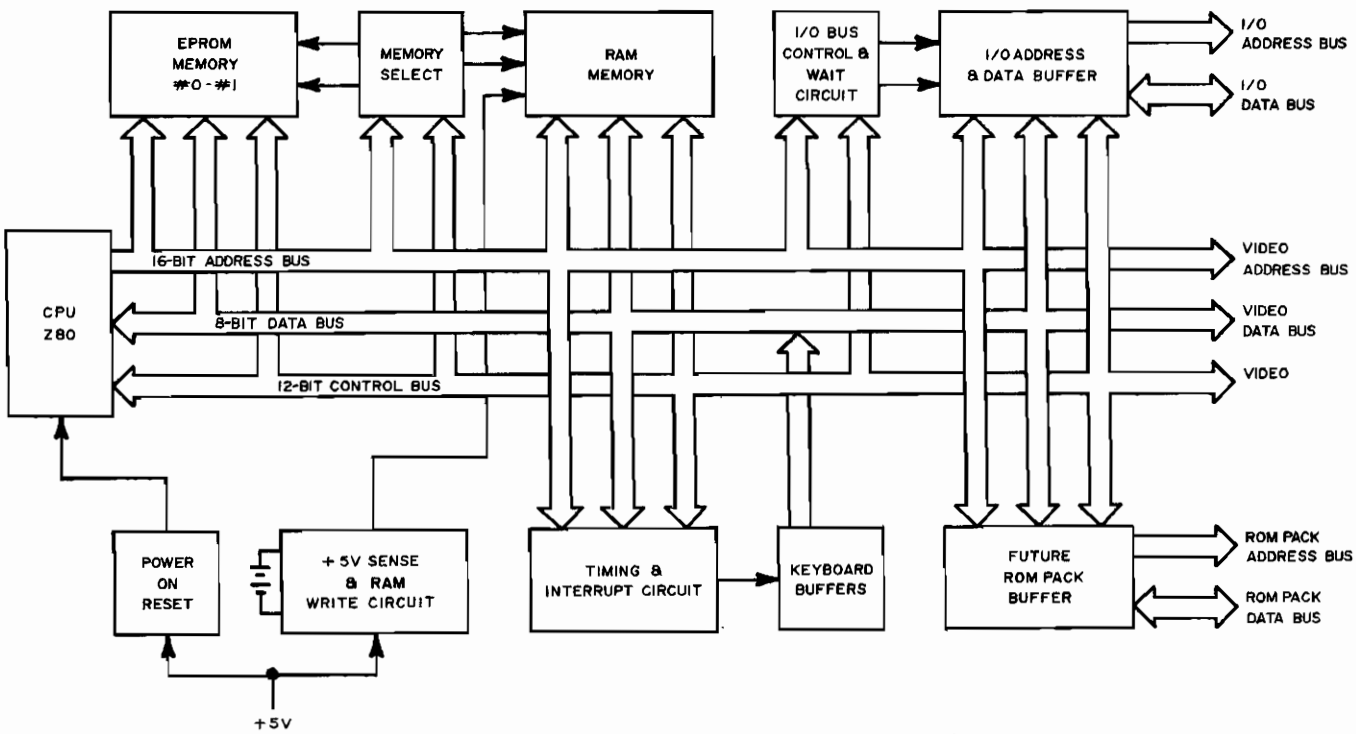


Figure 2-15 Control Processor PC Board Block Diagram

A. CPU

The three buses used for communication are an 8-bit data bus, a 16-bit address bus and a 12-bit control bus. U20005 through U20008 are the bus buffers for the CPU. U20023C and U20023D control the direction of the data bus. A 5 MHz system clock is input at pin 27B of P20001. U20025C and Q20025B buffer the clock, which is then referred to as Φ_1. Φ_1 is further buffered through U20008 to become Φ_2. Φ_2 is used to clock the CPU and CTC.

B. Memory

PROMs U20009 and U20011 are the processor's memory. U20012 is the RAM which holds data in memory after the A-7550 is turned off, so that it is available upon power-up. The lithium battery, BT20001, provides approximately +3V, which is sufficient to hold the contents of the RAM valid, even though +3V is not sufficient for reading and writing.

C. +5V Sense and RAM Write Circuit

Q20002 and Q20003 form a differential amplifier to detect a power-off condition by monitoring the +5V line. When the output of Q20002 goes below approximately +4.7V, Q20004 and Q20005 turn off. This prevents the active low signal from pin 12 of U20010 from reaching U20012, and thus prevents any data in the RAM from being inadvertently changed. When the +5V line drops below approximately +3V, CR20002 becomes reverse biased and CR20003 becomes forward biased. Then the RAM is powered by the lithium battery. This is the standby or power-off mode. The +5V line is also monitored by two gates of U20025 for power-on reset. When the set is first powered-up, the gates change states to activate the $\overline{\text{RESET}}$ line. When the set is powered-down, or when C20001 is fully charged, the $\overline{\text{RESET}}$ line is inactive high. The $\overline{\text{RESET}}$ line resets the CPU and the CTC.

D. Memory Select

U20010 is the memory select IC. When $\overline{\text{MREQ}}$ is active and $\overline{\text{RFSH}}$ is inactive, U20010 selects one of the memory devices according to address lines A13 - A15.

E. Timing and Interrupt Circuit

The timing and interrupt circuit consists of CTC U20017, decoder U20014 and the interrupt lines. U20014 decodes six address lines and $\overline{\text{M1}}$ and $\overline{\text{IORQ}}$ control lines. The decoded outputs can enable U20015, U20016, U20017 or the Interface Bus Control Circuit. When U20015 is enabled, data corresponding to the eight horizontal rows on the keyboard is read onto the data bus. When U20016 is enabled, data corresponding to the four vertical columns on the keyboard is read onto the data bus. The interrupt signals sent to the CTC tell which device has been interrupted.

F. Interface Bus Control and Wait Circuit

U20021 and U20022 buffer the interface address lines for output to interface devices. U20019 and U20020 are bi-directional buffers which control the data flow to or from the interface devices. A wait circuit is provided because devices on the buffered buses require longer set-up times than devices tied directly to the Z-80 bus. U20013, two gates of U20024 and three gates of U20026 form the wait circuit, which has a 3 µs time-out period. After the wait circuit times out, the Z-80 finishes its current machine cycle and tristates U20014. On the first rising edge of the clock signal after U20014 is tristated, U20018 is set, tristating the interface data bus. The interface address bus is tristated when U20014 is not selected.

2-4-11 GPIB PC BOARD

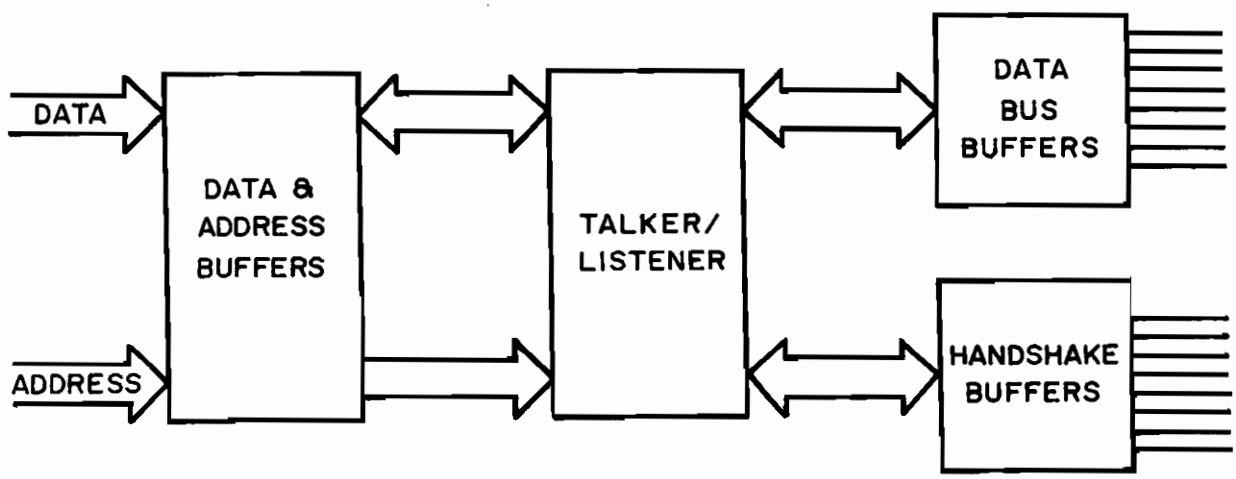


Figure 2-16 GPIB PC Board Block Diagram

The GPIB PC Board is the means of communication between an external GPIB controller and the A-7550. U56001 is a bi-directional buffer for data sent to and from the CPU. U56002 is an input buffer for address and control lines from the CPU. U56003 is a decoder used to control data transmission and the enable line of U56006. U56006 performs the "housekeeping" chores on the GPIB bus. U56007 through U56010 are bi-directional buffers.

2-4-12 RS-232 INTERFACE PC BOARD

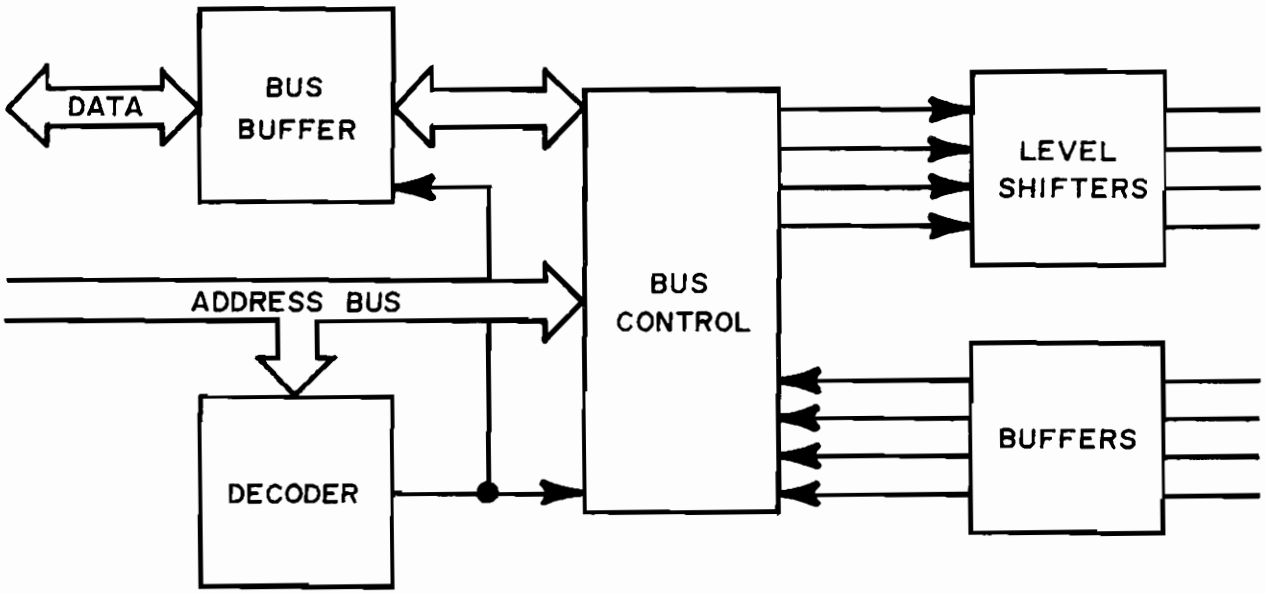


Figure 2-17 RS-232 Interface PC Board Block Diagram

The RS-232 Interface Board is the means of communication between an external RS-232 controller and the A-7550. U55001 is a bi-directional buffer for data sent to and from the CPU. U55002 is a decoder used to control data transmission. U55004 is an asynchronous interface adapter used to convert data from a parallel format to a serial format in the transmitting mode. It converts data from the serial format to parallel format in the receiving mode. U55005 and U55007 perform level shifting.

2-4-13a INTERFACE PC BOARD (Serial Numbers 1001 Thru 1476)

The Interface PC Board distributes analog and digital information throughout the set. Discrete lines which control the RF Section are routed to the RF Motherboard. Sweep adjustments and discrete digital input to the Control Processor are also located on this board.

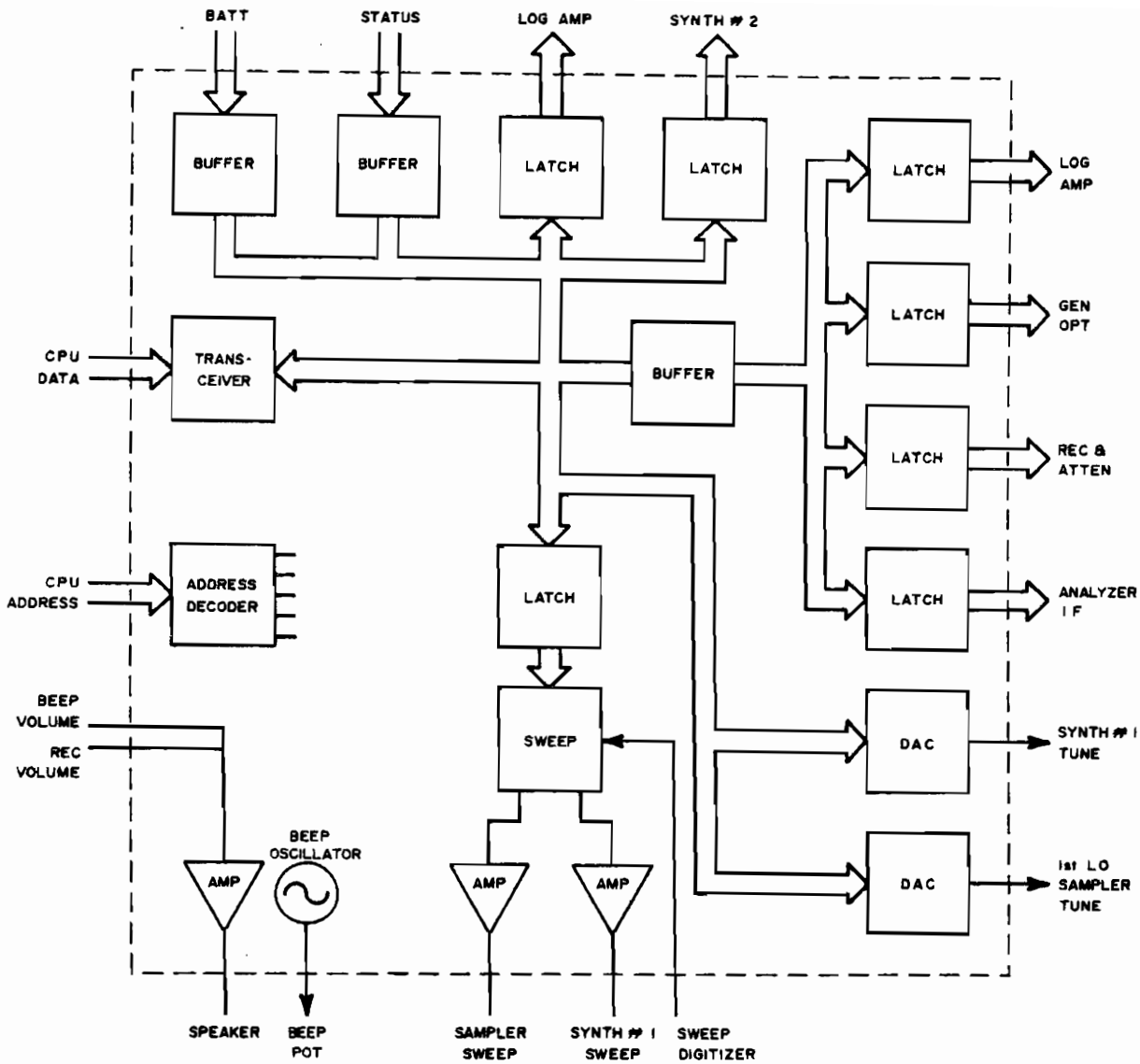


Figure 2-18 Interface PC Board Block Diagram (S/N 1001 thru 1476)

U19002 and U19003 are TTL PROMs used at lookup tables that translate address lines from the Control Processor Board into enable lines for the Interface Board. U19001 is a tristate transceiver that reads from or writes to the processor board. U19013 and U19024 are read buffers. U19013 is for status and option detect while U19024 reads battery voltage only. U19014 and U19015 are the D/A converters which develop the coarse tune voltages sent to Synthesizer #1 and the 1st L.O. Sampling Loop, respectively. U19021 (and associated resistor network) is configured to divide by 1, 2, 5, or 10. The sweep input at J19005 comes from the Sweep Digitizer Board. When the scan range is 1 kHz/DIV to 1 MHz/DIV, the Synth #1 Sweep En and Unlock are active. Above 2 MHz/DIV, the Sampler Sweep En and Hold are active. U19027 and U19004 form a tone oscillator which functions when an entry from the keyboard is accepted. U19005 is the speaker amplifier which is driven whenever an entry from the keyboard is accepted or when audio is received from the installed 10.7 MHz Receiver Option. Jumper block JTB19001 is provided to disable Auto Cal when calibrating the A-7550.

2-4-13b INTERFACE PC BOARD (Serial Number 1477 and On)

The Interface PC Board distributes analog and digital information throughout the set. Discrete lines which control the RF Section are routed to the RF Motherboard. Sweep adjustments and discrete digital input to the Control Processor are also located on this board.

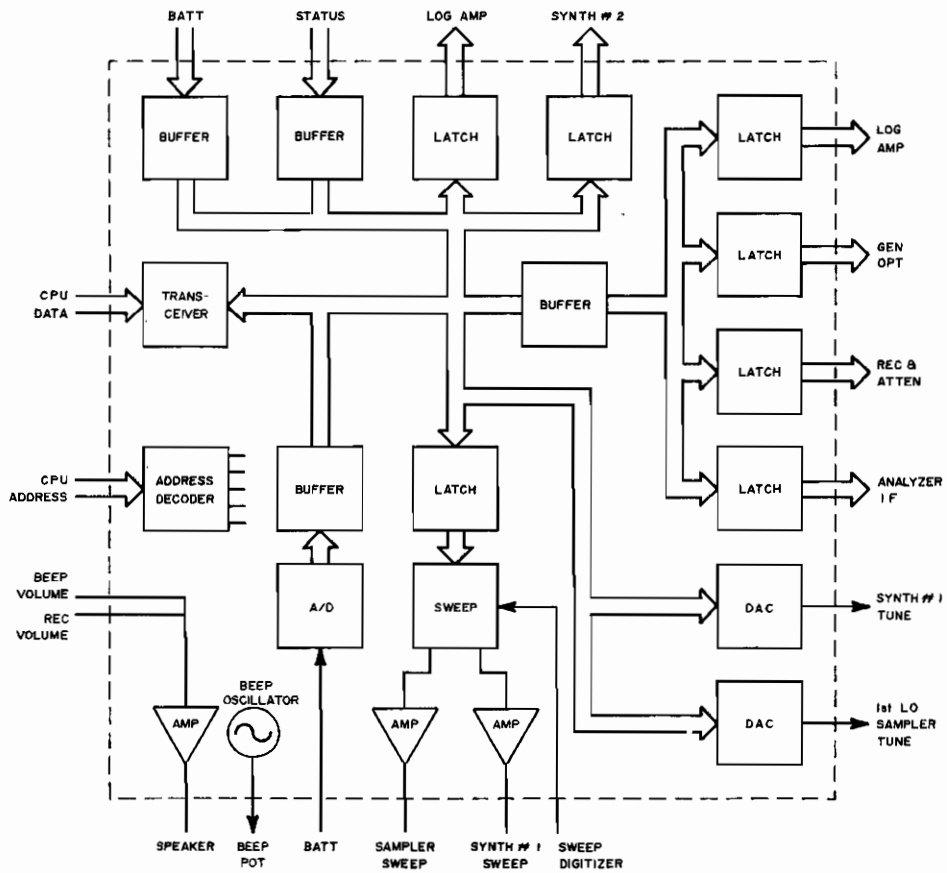


Figure 2-19 Interface PC Board Block Diagram (S/N 1477 and On)

U19011 and U19012 are TTL PROMs used at lookup tables that translate address lines from the Control Processor Board into enable lines for the Interface Board. U19013 is a tristate transceiver that reads from or writes to the processor bus. Notice that U19001 and U19008 are read buffers. U19002 and U19003 are digital-to-analog converters which develop the coarse tune voltages sent to the 1st LO Sampling Loop and to Synthesizer #1, respectively. U19004A (and associated resistor network), is configured to divide by 1, 2, 5 or 10. The sweep input at J19005 comes from the Sweep Digitizer Board. When the scan range is 1 kHz/DIV to 1 MHz/DIV, the Synth #1 Sweep En and Unlock are active. Above 2 MHz/DIV, the Sampler Sweep En and $\overline{\text{HOLD}}$ are active. U19018 and U19019 form a tone oscillator which is driven whenever an entry from the keyboard is accepted. U19023 is the speaker amplifier which is driven whenever an entry from the keyboard is accepted, or when audio from the 10.7 MHz Receiver is present. Jumper block JTB19001 is provided to disable Auto Cal when calibrating the A-7550. U19017 is an A/D converter which reads the battery voltage.

2-4-14 REFERENCE OSCILLATOR MODULE

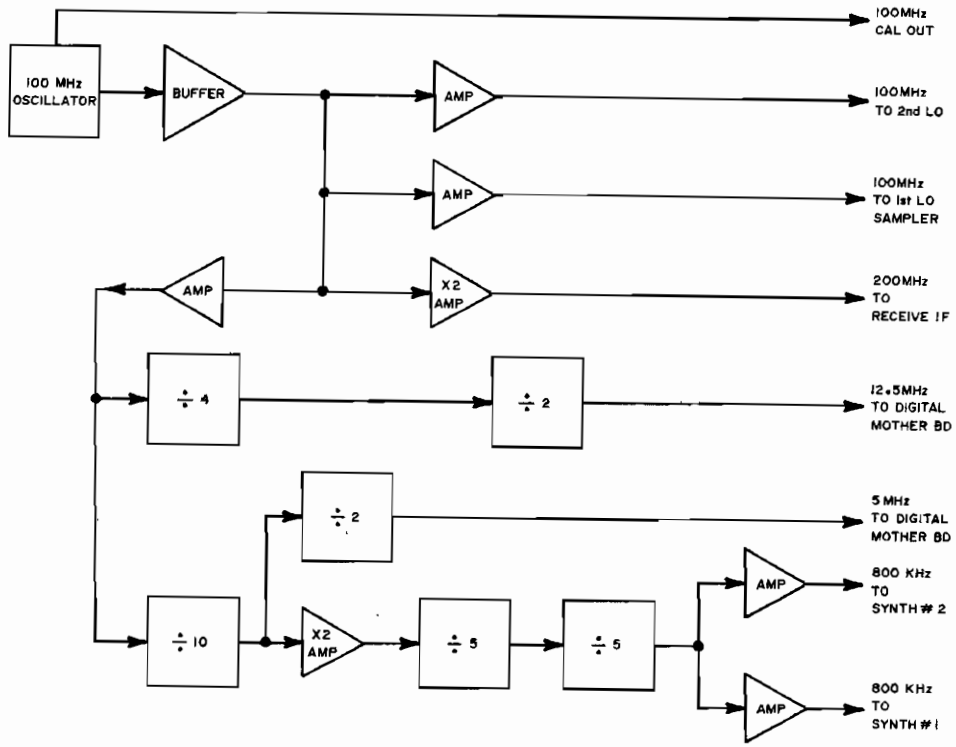


Figure 2-20 Reference Oscillator Module Block Diagram

Q47001, Y47001 and associated components, form the 100 MHz Oscillator. Coil L47002 sets the frequency of the 100 MHz time base. CR47001 and C47002 form a peak detector for differential amps Q47002 and Q47003, which acts as a level control for the oscillator. CR47002 is needed for temperature compensation for CR47001.

If the detected peak voltage on Q47002 is less than the bias voltage of 1.3 VDC on Q47003, then Q47002 is turned off, increasing the bias voltage which increases AC Gain of Q47001. When the detected peak voltage is greater than the bias voltage of 1.3 V at Q47003, then Q47002 is turned on, reducing the AC Gain of Q47001.

The oscillator output going through trimpot R47023 adjusts the 100 MHz CAL OUTPUT level to the front panel. R47024 and R47025 form the proper output impedance at REF CAL OUT.

Q47004 isolates the 100 MHz oscillator from the output buffers. Q47005 buffers the 100 MHz output to the 2nd LO block. Q47006 buffers the 100 MHz output to the 1st LO SAMPLER. Q47007 multiplies the output to 200 MHz for the 3rd Mixer in the RECEIVE IF. Q47008 and Q47012 buffer the 100 MHz to the reference divider circuits.

U47002 is a divide-by-4 ECL device. To convert the signal to TTL, C47030 couples the 25 MHz output to R47029 and R47030. U47003A divides the 25 MHz by 2 for the 12.5 MHz clock to the video processor.

U47001 is a divide-by-ten device with 10 MHz TTL output. U47003B divides the 10 MHz by 2 forming a 5 MHz clock to the Video and Control Processors. Q47004 doubles the 10 MHz output of U47001 to 20 MHz. Next, U47004 divides the output from U47001 by 5 and sends the 4 MHz signal to U47005, which divides the signal again by 5, forming an 800 kHz reference signal. The output of Q47010 drives Synthesizer #2 and the output from Q47011 drives Synthesizer #1.

2-4-15 1ST LO SAMPLER LOOP MODULE

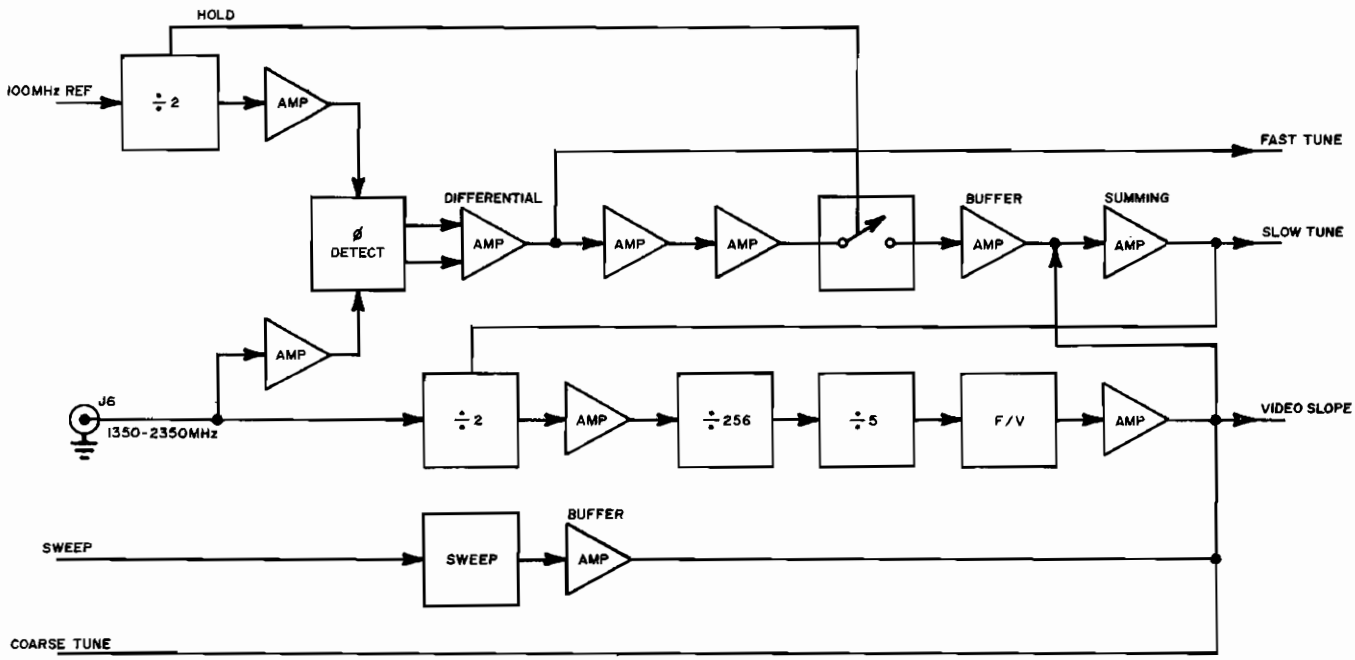


Figure 2-21 1st LO Sampler Loop Module Block Diagram

The 1st LO Sampler Loop Module uses frequency-to-voltage conversion, coarse tune sweep and phase lock voltages to develop a slow tune voltage used to steer the 1350 to 2350 MHz VCO Module. It also uses the VCO frequency and a reference frequency to develop a fast tune voltage which is used for phase correction of the VCO.

A. Fast Tune Voltage

The frequency from the VCO enters at J3ØØØ6 for high-speed sampling creating the Fast Tune Voltage. The 100 MHz reference frequency is input at J29003 and passed to U29011 where it is divided by 2. If the HOLD line is low, output at U29011 will be disabled. Otherwise, Q29020 amplifies the 50 MHz reference signal from U29011 to drive CR29012, which produces 50 MHz Harmonics. The harmonics are mixed through CR29010 and CR29011 to sample the VCO phase. Differential amplifier, Q29015 through Q29018, amplifies the sampled DC phase lock voltages. The Q29017 collector drives U29012A and fast tune output to clean the VCO signal.

B. Slow Tune Voltage

The fast tune voltage is passed through integrator U29013B and switch U29008B to buffer U29012B. It is summed at U29010A to create the VCO slow tune voltage. During sweep mode, the HOLD line is low to open switch U29008B and the slow tune phase lock voltage is held by C29072. If the VCO signal is not locked on a multiple of 50 MHz, U29012A oscillates at about 100 Hz. The VCO voltage varies ±20 MHz so the sampler can find the 50 MHz step-to-phase lock.

The voltage summation point for the slow tune line is pin 2 of U30010A. U29012B output, the frequency-to-voltage (F/V) Converter, the coarse tune and sweep signals are summed to create the slow tune voltage. Sweep input enters at pin 3 of P29001 and is divided by 10 if the scan range is 10 MHz or less per division. The microprocessor controls the sweep to ensure its presence only after the synthesizers have been locked at the left-lock frequency and the scan range is at least 2 MHz/DIV.

The digital-to-analog conversion performed on the Interface PC Board, determines the coarse tune voltage entered at J29002. The frequency from the VCO enters at J30006 and goes through a regenerative divide-by-two circuit. This circuit contains MXR30001, series resonant circuit CR30001, L30001, C30005 and Amplifier U30001. The series resonant circuit produces a 90° phase shift signal, which is fed into the Mixer IF Port at one-half the input frequency. CR30001 and the slow-tune circuit form a tracking filter that steers the mixed frequency output to one-half the input frequency.

Next, the VCO signal is divided by 1280 across a series of divider chips. Q30006 and Q30008 transform the signal into a sharply defined square wave. C30029 and R30022 transform the square wave into pulses. The negative-going pulse is limited by Zener diode CR30017; the positive-going pulse turns on Q30009, causing a current through R30024. R30110, R30111, C30033, C30079 and C30034 form a low-pass filter to average the voltage developed across R30024. The frequency-to-voltage converter output is summed at pin 2 of U30010A. The F/V converter output is also sent to the Log Amp where it supplies compensation to the video amp.

The resultant tune voltage from U30010A is sent through integrator U30009B. U30009B output pulls down on emitter Q30013 which conducts to vary the slow tune line output (0 to +30 V). Q30010 operates as a current limiter on the +40 V tune supply. Trimpots R30045 (HIGH LIMIT) and R30049 (LOW LIMIT) set the maximum and minimum slow tune voltages, respectively, for the VCO. The summed tune voltage is fed back through U30009A and adjusted by trimpots R30032 (DIVIDER TUNE OFFSET) and R30034 (DIVIDER TUNE GAIN), which sets the amplifier level for tuning the regenerative mixer divider circuit.

2-4-16 1350-2350 MHz VCO MODULE

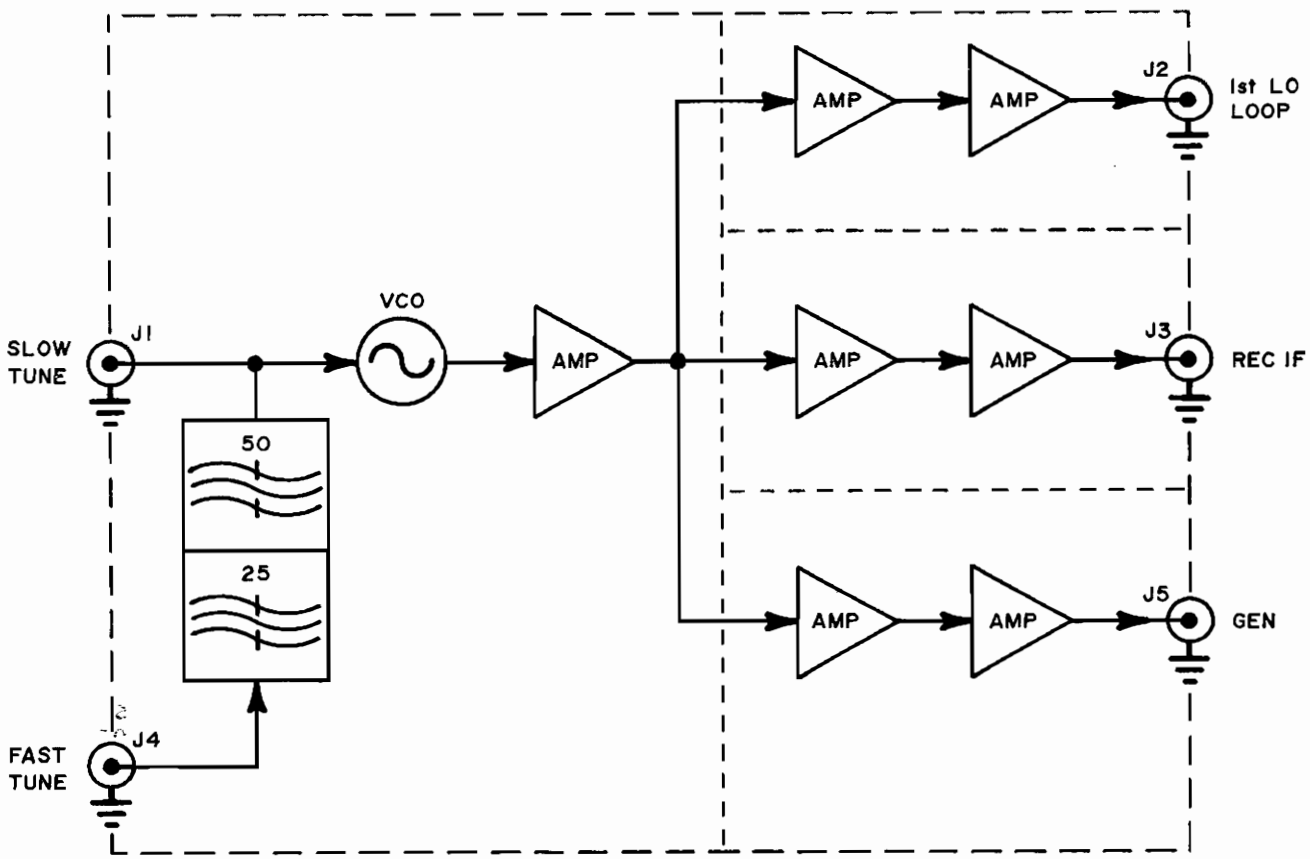


Figure 2-22 1350-2350 MHz VCO Module Block Diagram

The VCO Module develops the RF signal source for the LO Mixers and 1st LO Sampler Loop Module. J39001 and J39004 are, respectively, the slow tune and fast tune voltages developed by the 1st LO Sampler Loop Module. U40001 is a varactor-tuned oscillator with a frequency range of 1300 to 2350 MHz. The oscillator frequency is amplified and sent to three output stages for amplification. The output at J39002 is sent to the 1st LO Sampler Loop Module to phase lock the VCO Module. Output at J39003 and J39005 are, respectively, sent to the Receive IF Module and Generator Module (if installed) for frequency conversion. A Notch Filter, input at J39004, suppresses modulation of the VCO at 25 and 50 MHz.

2-4-17 SYNTHESIZER #1 MODULE

Synthesizer #1 uses coarse tune and sweep voltages from the Interface PC Board and an 800 kHz reference frequency to develop a phase-locked VCO output frequency.

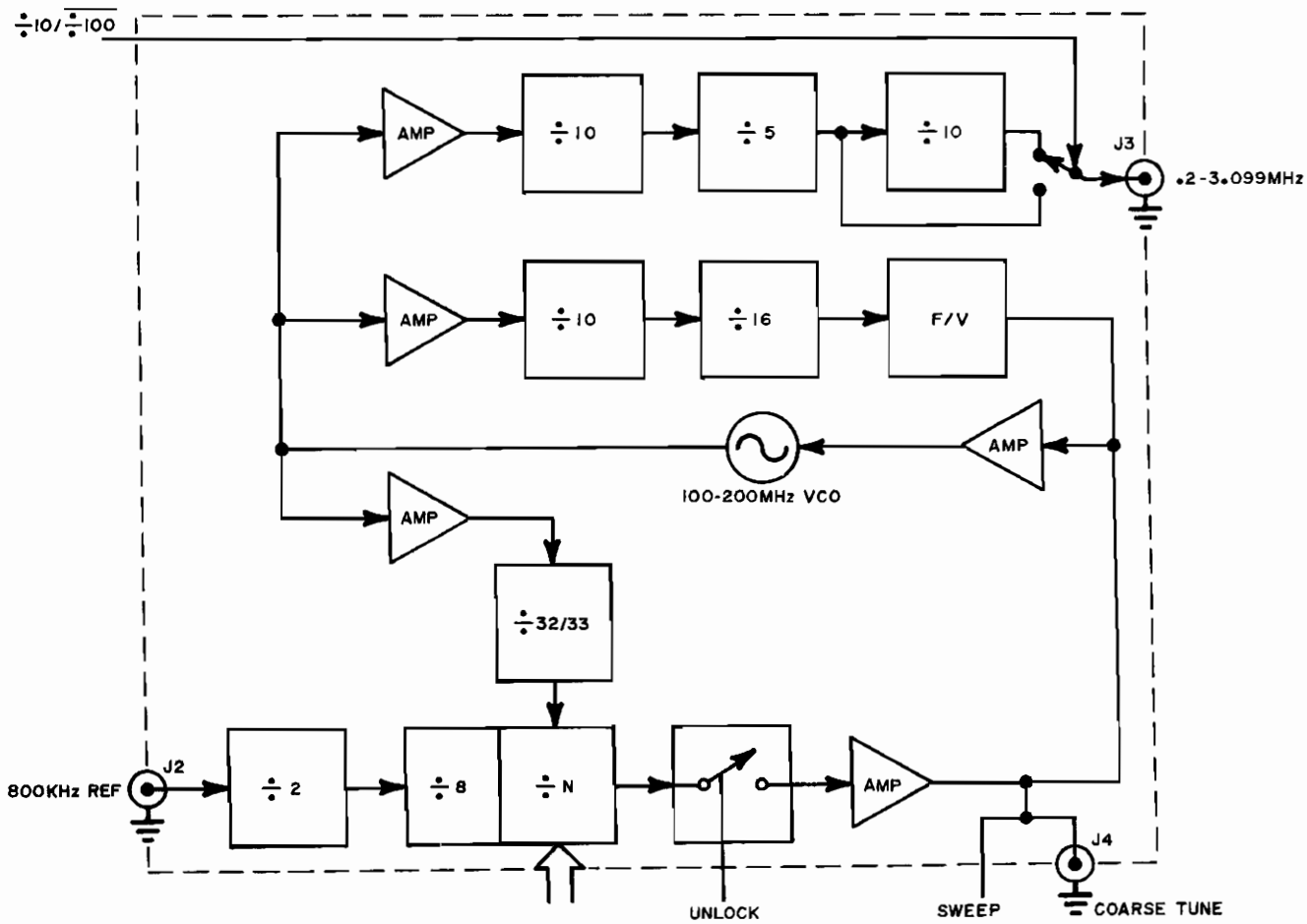


Figure 2-23 Synthesizer #1 Module Block Diagram

A. 50 kHz Loop

U24010 is a phase comparator used to phase lock the 100 to 200 MHz on-board VCO with a 50 kHz reference signal using serial data from the microprocessor. U24008 divides the 800 kHz reference signal from the Reference Oscillator Module in half before passing it to U24010. U24010 then divides the 400 kHz signal by eight, resulting in the 50 kHz reference signal.

U24009 is a dual modular prescaler controlled by U24010 that divides the VCO frequency by 32 or 33. Pins 3 and 4 of U24010 are the phase detector outputs that charge or discharge C24042 through CR24010 and CR24011 according to the phase difference between the signals. If U24010 is unlocked, pin 9 goes low, causing DS24001 to illuminate. The unlock line, pin 20 of P23001, is microprocessor controlled and is low for sweep and high for switching phase lock tune voltage on C24042 to integrator U24013B. The phase lock signal from U24013B is summed with the sweep and coarse tune signals at the input to amplifier U24007B. The summed tune voltage controls the 100 to 200 MHz VCO frequency.

B. Frequency-to-Voltage Converter

U24004 and U24005 divide the VCO frequency by 10 and 16, respectively. Q24006 and Q24007 transform the signal into a sharply defined square wave. C24022 and R24028 transform the square wave into pulses. The negative-going pulse is limited by Q24008; the positive-going pulse turns on Q24009, causing a current through R24033. R24061, R24035, C24025, C24026 and C24014 form a low-pass filter to average the voltage developed across R24033. The frequency-to-voltage (F/V) converter output from U24007B is then summed at pin 2 of U24007A.

Coarse tune voltage (DAC voltage) and sweep voltage, both from the Interface PC Board, are also summed with the frequency-to-voltage correction and phase lock signal at U24007A. The microprocessor controls the sweep input so it is present only after the synthesizers have been locked at the left-lock frequency and the scan range is between 1 kHz/DIV and 1 MHz/DIV, inclusively.

The VCO output is divided by ten in U24001 and by 5 in U24002. Within dispersion range A (see Figure 5-1), the output is further divided by ten (in U24006). The resultant output is sent to Synthesizer #2 Module.

2-4-18 SYNTHESIZER #2 MODULE

Synthesizer #2 uses synthesizer #1 output and an 800 kHz reference frequency to develop a phase locked VCO frequency output as part of the 2nd LO Source.

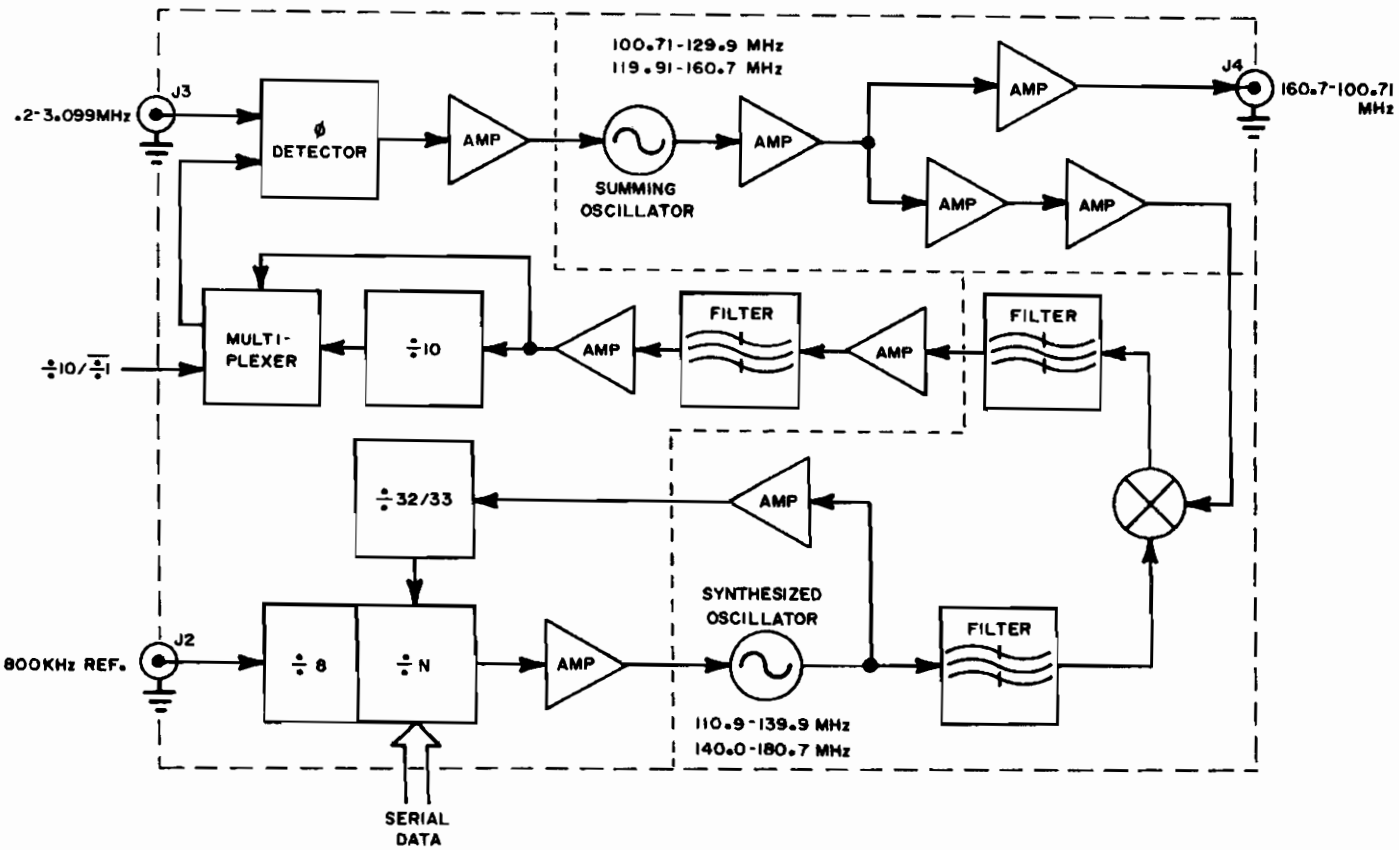


Figure 2-24 Synthesizer #2 Module Block Diagram

A. Synthesized Oscillator

U28007 is a phase comparator used to lock the on-board VCO with a 100 kHz reference signal using serial data from the microprocessor. The 800 kHz reference frequency from the Reference Oscillator Module is divided by eight in U28007. Pins 3 and 4 of U28007 form the phase detector output that charges and discharges C28065 through CR28015 and CR28016, depending on the phase difference. If the loop is unlocked, DS28002 illuminates when pin 9 goes low. The phase lock tune voltage on C28064 integrates at U28010. The output controls the synthesized VCO frequency.

Q28003, Q28018 and associated components, form the synthesized VCO circuit. The VCO is switched between low and high ranges by data bit 19 and Q28017. High range results from Q28017 pulling current through CR28018 and putting L28018 and L28019 in parallel with L28012. Q28019 buffers VCO output to drive mixer MXR28001 and Q28020. Q28020 drives dual modular prescalar U28009, which is controlled by U28007. U28009 divides the VCO frequency by 32 or 33.

B. Summing Oscillator

The summing oscillator circuit generates the output frequency for Synthesizer #2. The synthesizer-VCO difference signal and input signal from Synthesizer #1 are phase locked to control Synthesizer #2 output frequency. Q28002, Q28007 and associated components form the 100.71 MHz to 160.7 MHz Summing VCO Circuit. The VCO is switched between low and high ranges by data bit 18 and Q28006. High range occurs when Q28006 pulls current through CR28009, putting L28003 in parallel with L28004. Q28008 buffers the VCO output to drive Q28009 and Q28010. Q28009 provides the output signal from 100.71 to 160.7 MHz to J27004. Q28010 and Q28011 provide the Summing VCO signal to drive mixer MXR28001.

The frequency difference from MXR28001 between the Summing Oscillator and Synthesizer Oscillator is low-pass filtered to become the phase lock reference signal for the Summing VCO Circuit. When scan range C or D is selected, pin 7 of P27001 goes high. When P27001 goes high, U28006A selects the divide-by-ten difference signal from U28005.

U28003 operates as a charge pump phase comparator between the oscillator difference signal and Synthesizer #1 input signal. If the signals are not in phase, the charge on C28011 increases or decreases according to their phase difference. C28011 voltage integrates at U28004. The output from U28004 controls the 100.71 to 160.7 MHz Summing VCO signal. U28001A operates when phase lock is lost and the charge on C28011 is too high. The integrator direction is reversed to reduce the Summing VCO to its lowest frequency and scans for phase lock again. Pin 6 of U28002B pulls high when an unlocked condition is sensed, forcing Q28001 to conduct and illuminating DS28001.

2-4-19 2ND LO SUMMING LOOP MODULE

The 2nd LO Summing Loop Module uses a 100 MHz reference signal and the VCO input from Synthesizer #2 to phase lock an internal VCO.

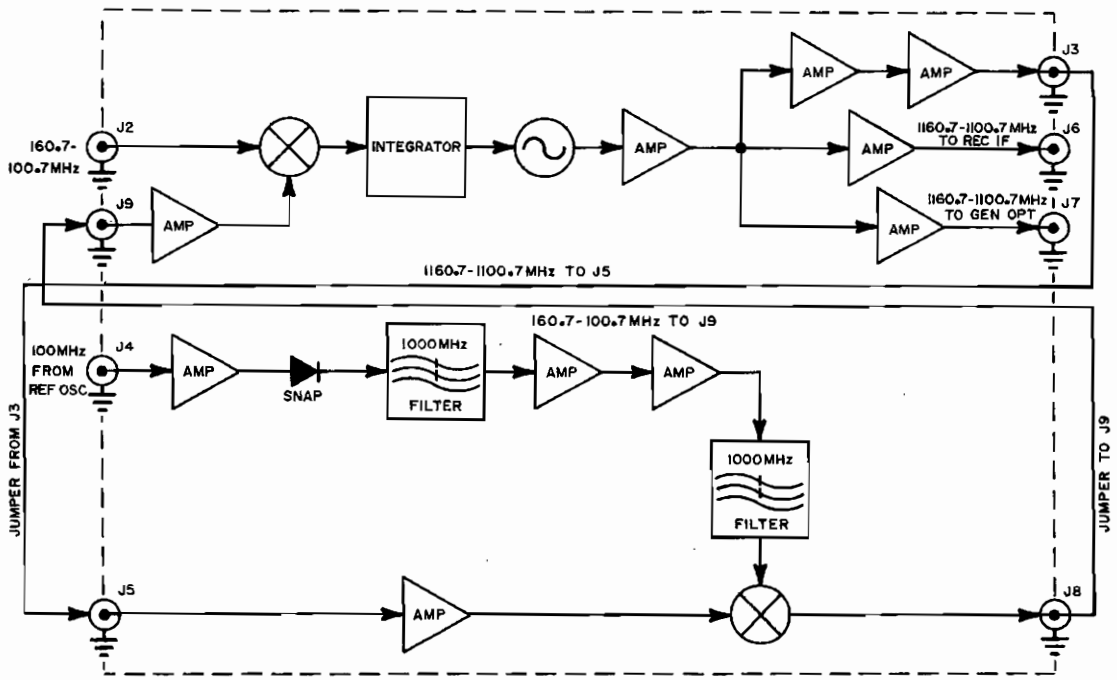


Figure 2-25 2nd LO Summing Loop Module Block Diagram

A. 1000 MHz Multiplier PC Board

A 100 MHz reference signal is input at J36004 and amplified by Q37002. Q37002 drives snap diode (CR37002) to produce 100 MHz harmonics. The 1000 MHz harmonic is bandpass filtered before it is amplified by Q37003 and Q37004, to drive the 2nd LO Mixer Circuit.

B. 2nd LO Mixer PC Board

The 1000 MHz signal is input to MXR18001 through a 1000 MHz bandpass filter. MXR18001 mixes this signal with an 1160.7 to 1100.71 VCO signal to produce 160.7 to 100.71 MHz signal for the 1160 MHz VCO board.

C. 1160 MHz VCO PC Board

The 160.7 to 100.71 Hz signal from the 2nd LO Mixer board is mixed with the 160.7 to 100.71 MHz signal from Synthesizer #2 at MXR 38001 to obtain a desired zero beat. If the input signals are out of phase, U38001 produces a DC output which is the tune voltage for the onboard VCO. Q38001 and associated components form an 1160.7 to 1100.71 MHz VCO, the output of which is buffered and sent to the Receiver IF Module, the 2nd LO Mixer board, and to the optional Generator Module, if installed.

2-4-20 TRACKING GENERATOR MODULE (OPTION)

The Tracking Generator Module is an optional module that performs a tracking generator function, if desired. It uses the 1160.7 to 1100.71 MHz output of the 2nd LO Module and the 1350 to 2350 MHz output of the 1350 to 2350 MHz VCO Module to mix with a 189.3 MHz source and develop a tracking signal.

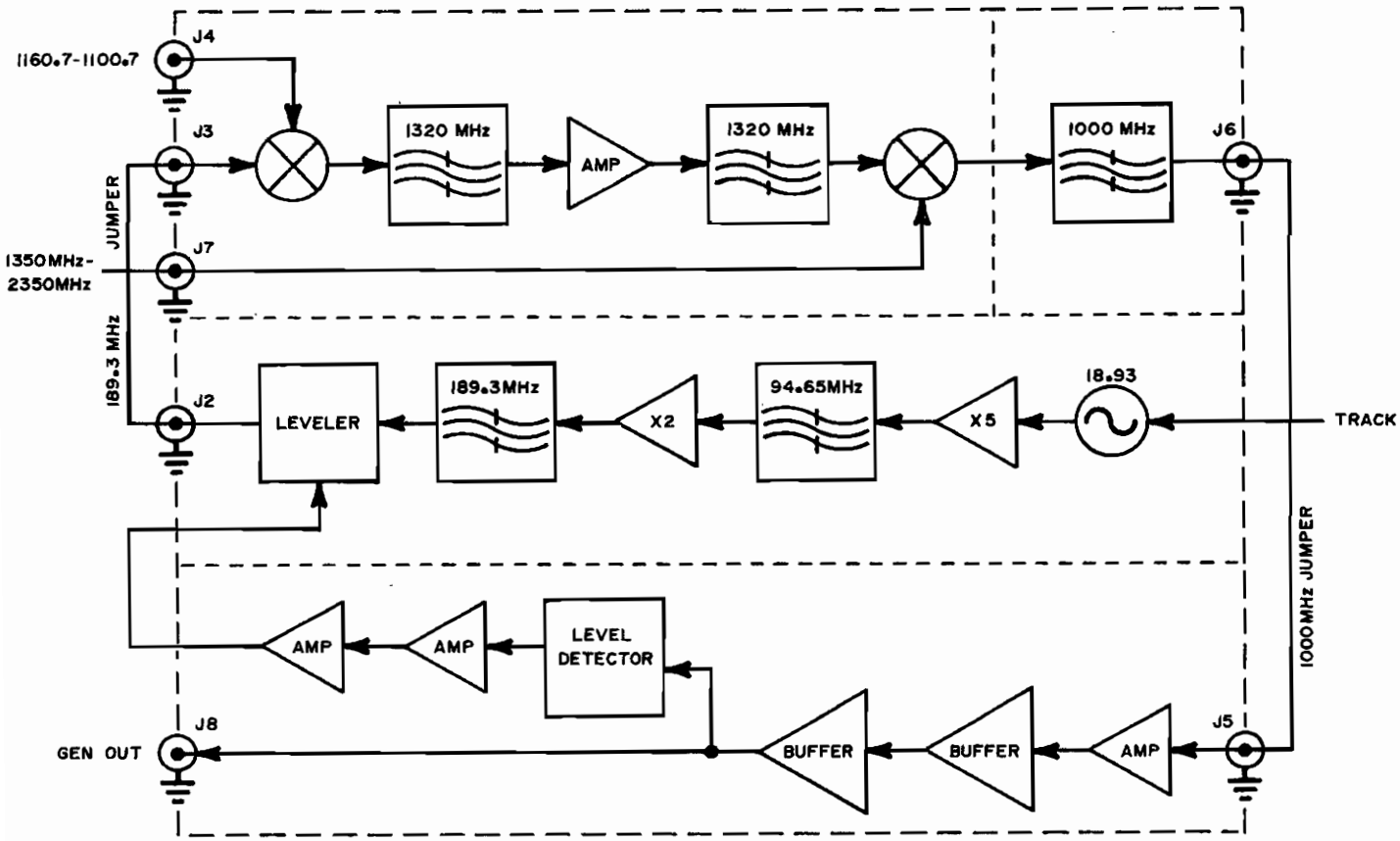


Figure 2-26 Tracking Generator Module Block Diagram

A. Generate Source PC Board

When the tracking generator function is selected on the SETUP menu, pins 4 and 5 of J50001 go high to enable the module. The 18.93 MHz oscillator consists of Y51001, Q51001 and associated components. Q51002 and its filtered tank circuit is used as a times-5 multiplier to 94.65 MHz. Q51003 and Q51004 and the associated tank circuit are used as a times-2 multiplier to 189.3 MHz. The TRACKING ADJUST control on the front panel is used to adjust the oscillator frequency each side of 189.3 MHz. A positive leveler input voltage forward biases CR51002 and CR51003 to allow the 189.3 MHz source signal level to be controlled at J50002.

B. 1300 MHz GEN IF PC Board

The 189.3 MHz input at J50003 and the 1st LO input at J50004 are mixed in MXR53001 to produce a 1290 to 1350 MHz IF, which is filtered in a 1290 to 1350 MHz bandpass filter. U53001 and U53002 amplify the IF signal before it passes through another 1290 to 1350 MHz bandpass filter. MXR53002 mixes the IF signal with a 1350 to 2350 MHz VCO source (J50007) to produce a 0 to 1000 MHz low-pass filter board and output at J50006 to the GEN AMP PC Board.

C. GEN AMP PC Board

U54001 and Q54001 amplify the 0 to 1000 MHz Tracking Signal input (J50005) to drive amplifier Q54002. Q54002 can drive a 50 ohm load at J54008. Q54003 controls the current to Q54002 for operating over a wide frequency range. CR54002 and CR54003 detect the RF output level at J50008. The DC signal is filtered and integrated (U54002B) to control the 189.3 MHz output signal generated at J50002. Trimpot R54022 (OUTPUT LEVEL ADJ) sets the generated output RF level at the GENERATE OUTPUT Jack (on the front panel).

2-4-21 0-75 dB OUTPUT ATTENUATOR MODULE (OPTION)

The Output Attenuator contains both a 0-60 dB PC Board and a 0-15 dB PC Board, and steps in 1 dB increments. Theory of Operation for the 0-60 dB PC board is the same as the 0-60 dB PC Board in the Input Attenuator. (Refer to Paragraph 2-4-2)

2-4-22 0-15 dB PC BOARD

When its respective control line goes high, one of the relays is activated, putting its attenuation network into the circuit. For instance, when the signal at FL49004 goes high, K49001 is energized to put R49001, R49002 and R49003 into the circuit. These three resistors provide 1 dB of attenuation. If more attenuation is selected, the CPU selected control lines go high. This activates K-relays for cumulative attenuation. Selection of the control lines is controlled by the Control Processor board through the Interface PC Board.

SECTION 3 - PERFORMANCE EVALUATION

3-1 GENERAL

This section contains step-by-step test procedures for assessing the performance of the A-7550. These procedures should be performed as the first step in the troubleshooting/maintenance process. Appendix A contains performance specifications and variations. Test setups are shown in the figures provided in this section. Allow ten minutes to warm up the A-7550 to ensure its stable operation. All procedures in this section are performed using the A-7550 front and rear panels and do not require removing the case.

The following performance evaluation tests are included in this manual:

Test Number	Title	Page
3-2	CAL OUT Performance Evaluation	3-5
3-3	Scan Width Linearity Performance Evaluation	3-7
3-4	Noise Sidebands Performance Evaluation	3-8
3-5	Amplitude Scale Linearity Performance Evaluation	3-9
3-6	Frequency Response Performance Evaluation	3-11
3-7	Resolution Bandwidth Accuracy Performance Evaluation	3-13
3-8	Variance Between Bandwidth Filters Performance Evaluation	3-14
3-9	IF Gain Performance Evaluation	3-15
3-10	Input Attenuator Performance Evaluation	3-17
3-11	Tracking Generator Performance Evaluation (Option)	3-19
3-12	10.7 MHz Receiver Performance Evaluation (Option)	3-21
3-13	Quasi-Peak Performance Evaluation (Option)	(To Be Supplied)

A Performance Evaluation Record sheet is provided for recording data from each test.

NOTE

Numbers within parenthesis following an A-7550 control, connector, or indicator pertain to item number shown in Figure 1-2.

3-1-1 TEST EQUIPMENT REQUIREMENTS

Appendix B contains a comprehensive list of test equipment suitable for performing any of the procedures in this Section. Any other equipment meeting the specifications listed in Appendix B may be substituted for the recommended equipment.

3-1-2 CORRECTIVE MAINTENANCE PROCEDURES

The performance tests in this section are aids to operators and technicians when determining whether or not the A-7550 functions properly. A failure condition is normally reflected as either a calibration error or a malfunction. A calibration error is defined as a measurement or reading (relating to the unit being tested) that is not within prescribed tolerances. In this condition, the set may outwardly appear to be functioning properly. A malfunction denotes a defective condition where a signal may be totally absent, grossly out of tolerance or that the unit (or any part thereof) is not working properly.

If a failure condition is confirmed, the technician should take appropriate corrective maintenance action to return the set to its prescribed operating condition.

TABLE 3-1: A-7550 PERFORMANCE EVALUATION RECORD

Technician: _____ S/N: _____

Para.	Test	Min	Results Actual	Max
3-2	Calibrator			
	Frequency	99.9975 MHz	_____	100.0025 MHz
	Amplitude	-31 dBm	_____	-29 dBm
3-4	Noise Sidebands			
	Noise level		_____	65 dBc
3-5	Amplitude Scale Linearity			
	10 dB/DIV Log			
	10 dB step	-0.15 dB/DIV	_____	+0.15 dB/DIV
	Total	-2.5 dB	_____	+2.5 dB
	2 dB/DIV Log			
	2 dB step	-0.4/2 dB DIV	_____	+0.4/2dB DIV
	Total	-1.5 dB	_____	+1.5 dB
	Linear (demod)	-10%	_____	+10%
3-6	Frequency Response	-2 dB	_____	+2 dB
3-7	Resolution Bandwidth Accuracy			
	3 MHz	2.1 MHz	_____	3.9 MHz
	300 kHz	210 kHz	_____	390 kHz
	30 kHz	21 kHz	_____	39 kHz
	3 kHz	2.1 kHz	_____	3.9 kHz
	300 Hz	210 Hz	_____	390 Hz
3-8	Amplitude Variation			
	3 MHz	-2 dB	_____	+2 dB
	300 kHz	-2 dB	_____	+2 dB
	30 kHz	-2 dB	_____	+2 dB
	3 kHz	-2 dB	_____	+2 dB
	300 Hz	-4 dB	_____	+4 dB
3-9	IF Gain (0 to 20 dB)	-2 dB	_____	+2 dB
3-10	Input Attenuator			
	0 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	10 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	20 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	30 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	40 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	50 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB
	60 dB	-0.5 dB/10 dB	_____	+0.5 dB/10 dB

TABLE 3-1 (CONTINUED): A-7550 PERFORMANCE EVALUATION RECORD

Para.	Test	Min	Results Actual	Max
3-11	Tracking Generator (Option)			
	Frequency Range	100 kHz	_____	1 GHz
	Output Level	-75 dBm	_____	0 dBm
	Flatness	-2 dB	_____	+2 dB
	Residual FM (RMS peak)		_____	100 Hz
	Spurious:			
	Harmonics		_____	20 dBc
	Non-harmonics		_____	40 dBc
3-12	10.7 MHz Receiver (Option)			
	Range	100 kHz	_____	1 GHz
	Center Freq. Resolution	100 Hz	_____	
	Sensitivity (typical)	2 µV	_____	
	Selectivity (3 dB):			
	FM2	200 kHz	_____	
	FM1	15 kHz	_____	
	SSB	6 kHz	_____	
	AM1	6 kHz	_____	
	AM2	15 kHz	_____	
	Adjacent Channel Reject.:			
	200 kHz Filter		_____	<40 dB at
			_____	±300 Hz
	15 kHz Filter		_____	<40 dB at
			_____	±27 kHz
	6 kHz Filter		_____	<40 dB at
			_____	±12 kHz
3-13	Quasi-Peak Detector (Option)			
	(To Be Supplied)			

3-2 CAL OUT PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D:

1 Spectrum Analyzer

1 Frequency Counter

1 RF Signal Generator

1 Power Meter w/Thermistor Mount

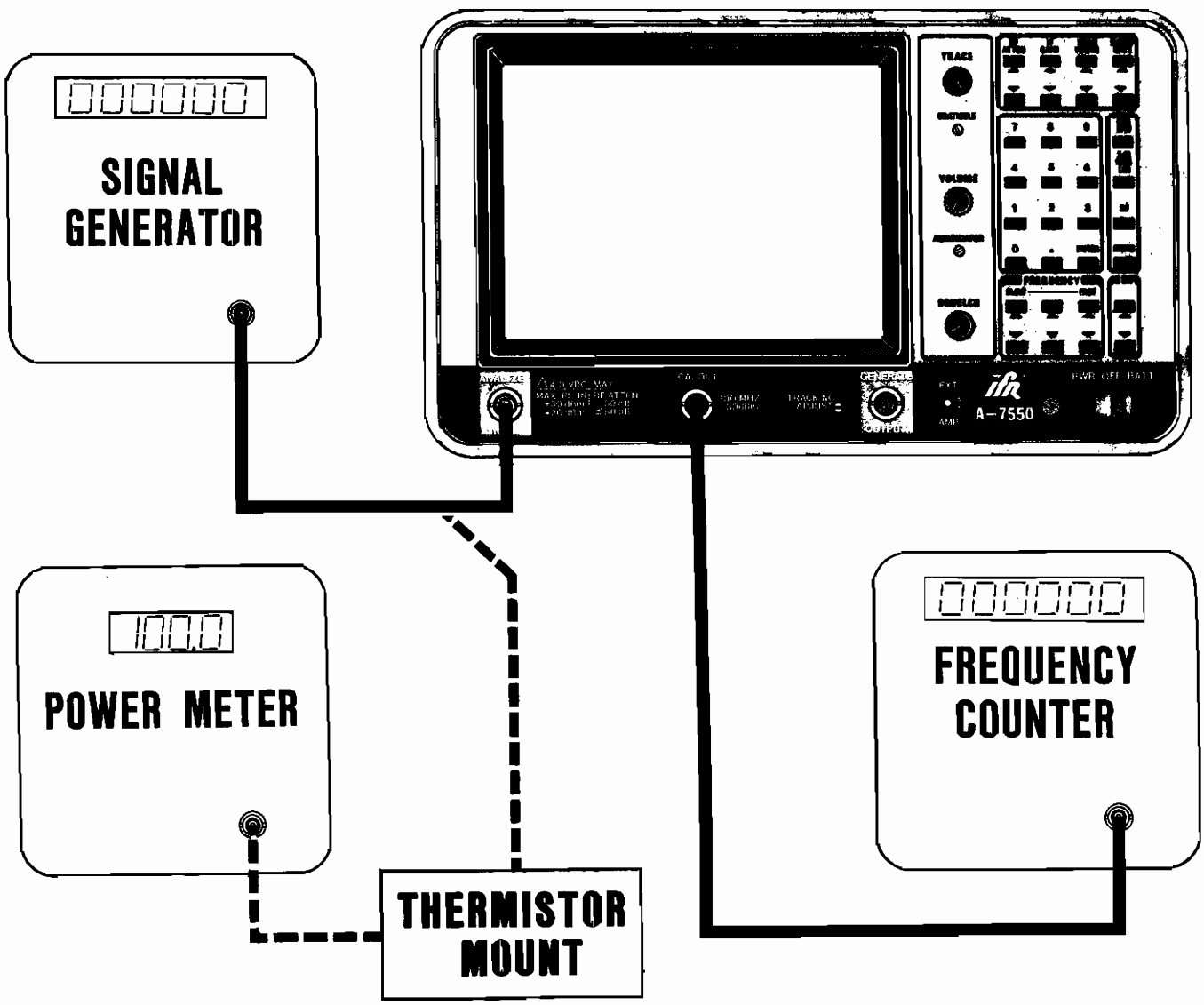


Figure 3-1 CAL OUT Test Setup

STEP	PROCEDURE

1. Set A-7550 controls as follows:

   Center Frequency ..... 100 MHz
   RF ATTEN ..... 10 dB
   IF GAIN 0
   Scan Width ..... 1 kHz/DIV

2. Using Frequency Counter, measure the reference frequency at the A-7550 CAL OUT Connector (9). Verify frequency is 100 MHz (±2500 Hz) at room temperature.

3. Disconnect Frequency Counter. Set RF Signal Generator to 100 MHz at -30 dBm and verify the output with a power meter.

4. Connect RF Signal Generator to A-7550 ANALYZER INPUT Connector (10). Note level on CRT Display (11) or store in memory using STORE function and COMP Mode.

5. Disconnect RF Signal Generator. Connect A-7550 Analyzer CAL OUT Connector (9) to A-7550 ANALYZER INPUT Connector (10) with the same coax cable used in Step 4. Verify the signal level is the same (±1 dBm) as noted in Step 3.

3-3 SCAN WIDTH LINEARITY PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Standard 50Ω Coax Cable

STEP PROCEDURE

1. Connect A-7550 CAL OUT Connector (9) to ANALYZER INPUT Connector (10).

2. Set A-7550 controls as follows:

Center Frequency	(RF, ENTER) (See Note)
SCANWIDTH	100 MHz/DIV
2 dB/10 dB/LIN	10 dB
IF GAIN	0
RF ATTN	10 dB

NOTE

Pressing ([RF] , [ENTER]) sets the CF to 500 MHz and the SCANWIDTH to 100 MHz/DIV.

3. Verify the 1000 MHz signal peak is on the far right major graticule (-½ minor division). Verify remaining harmonic peaks are centered on major graticules (±1 minor division).

4. Using center graticule as a reference, decrease SCAN WIDTH entire range. Verify harmonic response peak remains centered (±1.25 minor divisions).

3-4 NOISE SIDEBANDS PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D:

1 RF Signal Generator

STEP PROCEDURE

1. Set A-7550 controls as follows:

Filters Menu	300 Hz
Center Frequency	10 MHz
SCAN WIDTH	10 kHz/DIV
RF ATTEN	0 dB
IF GAIN	0
2 dB/10 dB/LIN	10 dB

2. Set RF Signal Generator to 10 MHz at -30 dBm. Connect RF Signal Generator to A-7550 ANALYZER INPUT connector (10). Verify noise sidebands are lower than 65 dBc at left and right edge of display.

3-5 AMPLITUDE SCALE LINEARITY PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D:

1 RF Signal Generator

1 Power Meter w/Thermistor Mount

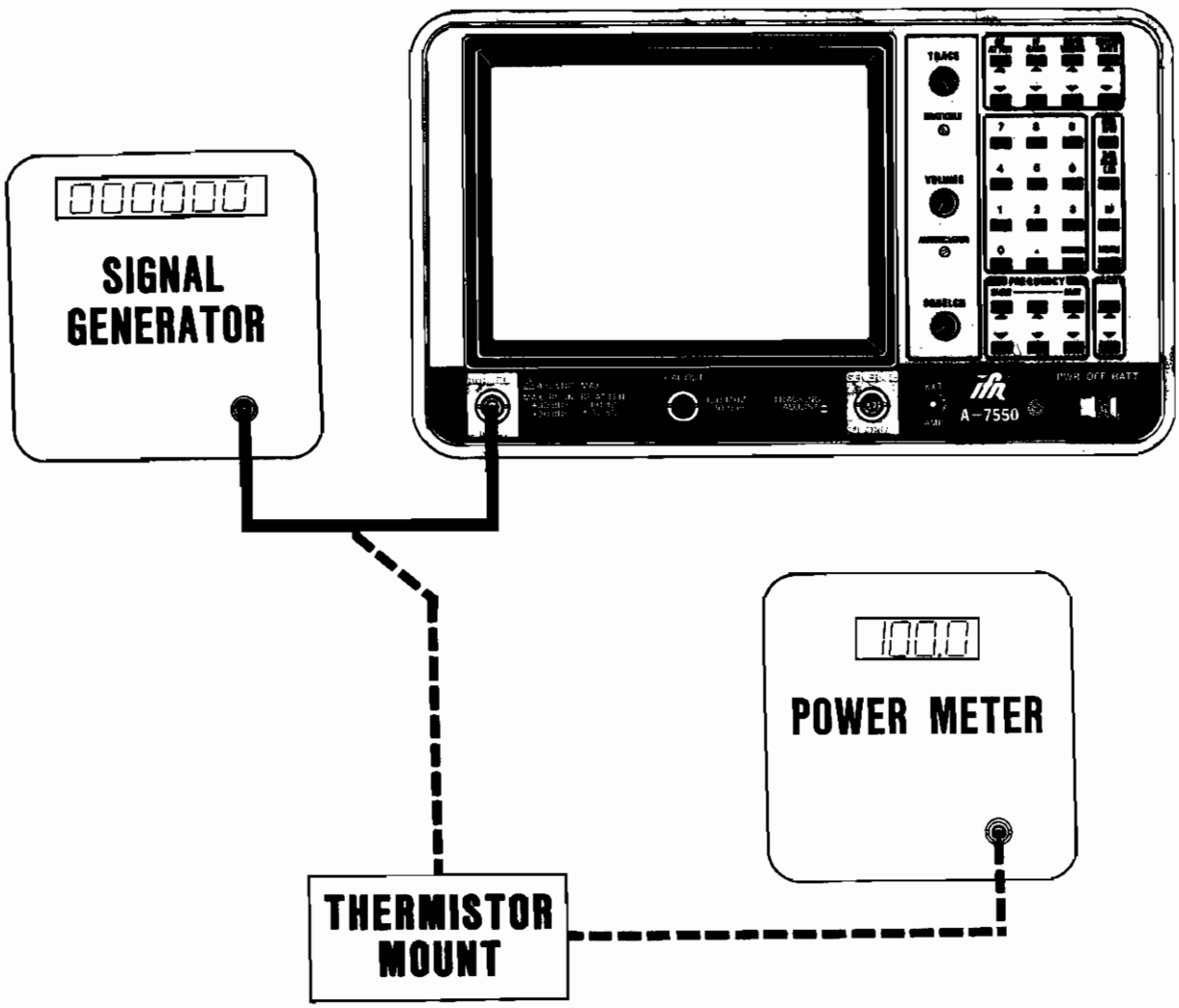


Figure 3-2 Amplitude Scale Linearity Test Setup

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	10 MHz
SCAN WIDTH	1 MHz/DIV
RF ATTEN	0 dB
2 dB/10 dB/LIN	10 dB LOG

STEP PROCEDURE

2. Set RF Generator on 10 MHz at -30 dBm. Connect RF Signal Generator output connector to A-7550 ANALYZER INPUT Connector (10).

3. Step RF ATTEN to 60 dB in 10 dB steps. At each step, record deviation from graticule. Above the graticule would be a positive deviation. Below the graticule would be a negative deviation.

RF ATTEN	Deviation
0 dB	_____
10 dB	_____
20 dB	_____
30 dB	_____
40 dB	_____
50 dB	_____
60 dB	_____

Add the greatest positive deviation to the greatest negative deviation to give total deviation. Verify total deviation (at 60 dB) does not exceed 2.5 dB.

4. Set A-7550 Control 2 dB/10 dB/LIN to 2 dB. Set RF ATTEN to Ø. Step RF Signal Generator from -30 dBm down to -42 dBm in 2 dB steps. At each step, verify output level with a Power Meter. Record deviation seen on A-7550 at each step. Above the respective graticule would be a positive deviation. Below the respective graticule would be a negative deviation.

RF Signal Generator	Deviation
-30 dBm	_____
-32 dBm	_____
-34 dBm	_____
-36 dBm	_____
-38 dBm	_____
-40 dBm	_____
-42 dBm	_____
Total =	_____

Add the greatest positive deviation to the greatest negative deviation to give total deviation. Verify total deviation does not exceed 1.5 dB.

5. Set A-7550 controls IF GAIN, 2 dB/10 dB/LIN to LIN and RF ATTN to 0. Adjust trace to top display graticule, if necessary. Decrease RF Signal Generator output 6 dBm. Verify trace is at middle display graticule (±0.4 major division).

3-6 FREQUENCY RESPONSE PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator---(8656) step programmable

1 Power Meter w/Thermistor Mount

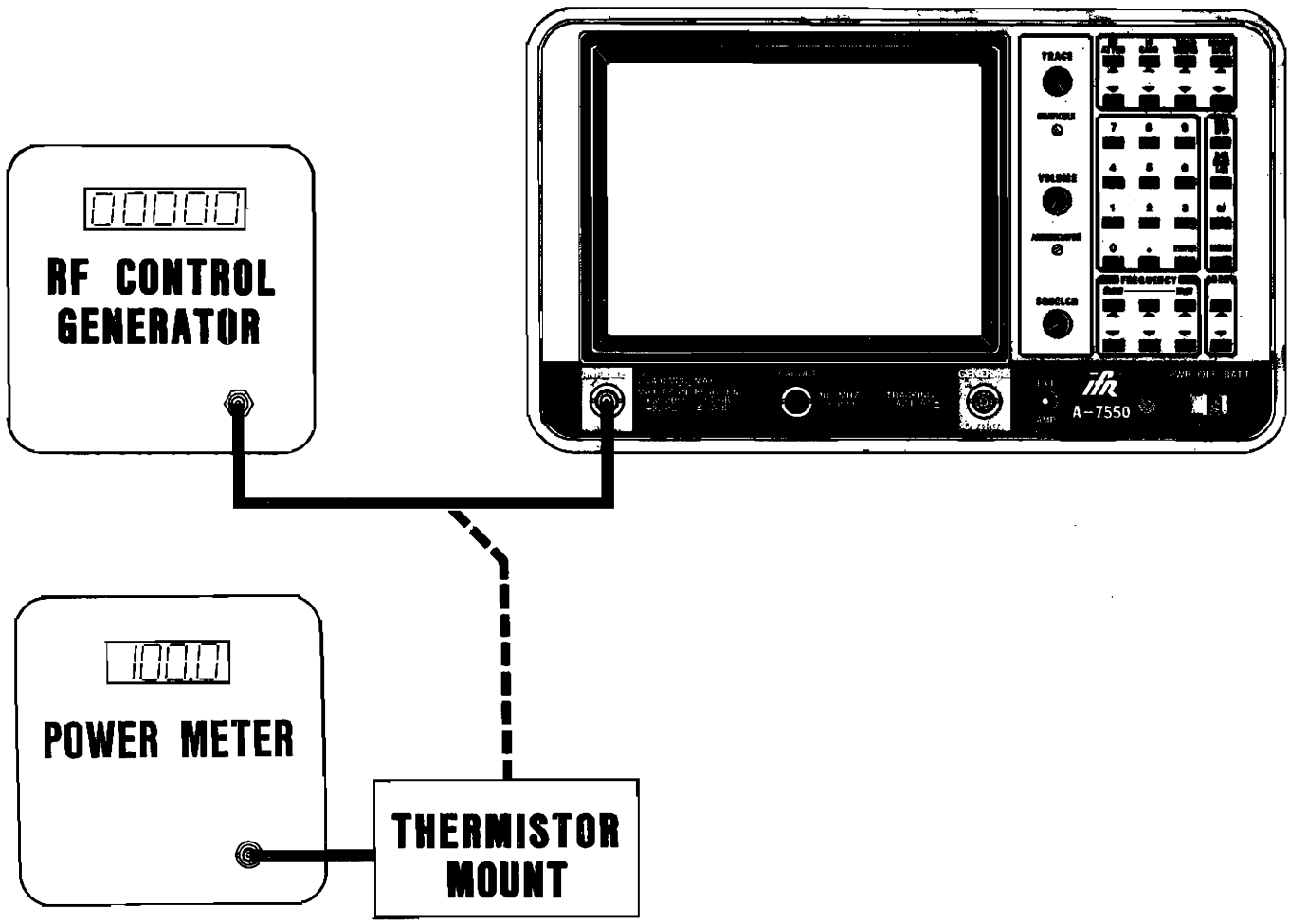


Figure 3-3 Frequency Response Test Setup

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	(RF,ENTER) (See Note)
RF ATTEN	0 dB
IF GAIN	0
2 dB/10 dB/LIN	2 dB
Filters Menu	None
SCANWIDTH	100 MHz/DIV

NOTE

Pressing (RF , ENTER) sets the CF to 500 MHz and the SCANWIDTH to 100 MHz/DIV.

2. Set RF Signal Generator to step from 10 MHz to 1000 MHz in 10 MHz steps. Set output level to -34 dBm.

3. Connect RF Signal Generator to A-7550 ANALYZER INPUT connector (10). As RF Signal Generator steps, observe the maximum positive and negative deviation from the -34 dBm reference. Verify deviation of -34 dBm does not exceed 4 dB.

NOTE

If RF Signal Generator output level is consistent throughout frequency range, eliminate following power meter check.

4. At the points noted in Step 3, check output level of RF Signal Generator with a Power Meter and adjust output level to exactly -34 dBm. Reconnect RF Signal Generator to A-7550 ANALYZER INPUT connector and observe deviation from reference at these points. Add the maximum positive and negative deviations. Verify flatness does not exceed 4 dB total at noted points.

3-7 RESOLUTION BANDWIDTH ACCURACY PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	10 MHz
SCAN WIDTH	1 MHz/DIV
RES BW	3 MHz
2 dB/10 dB/LIN	2 dB LOG
RF ATTEN	10 dB
IF GAIN	5 dB

2. Set RF Signal Generator to 10 MHz at -30 dBm. Connect RF Signal Generator output to A-7550 ANALYZER INPUT (10). Adjust frequency and amplitude to center peak of signal at center and top of CRT display.

3. Verify A-7550 3 MHz bandwidth is between 2.1 MHz and 3.9 MHz wide at 3 dB below peak level.

4. Set A-7550 SCAN WIDTH to 100 kHz/DIV and RES BW to 300 kHz. Verify 300 kHz bandwidth is between 210 kHz and 390 kHz wide at 3 dB below peak level.

5. Set A-7550 SCAN WIDTH to 10 kHz/DIV and RES BW to 30 kHz. Verify 30 kHz bandwidth is between 21 kHz and 39 kHz wide at 3 dB below peak level.

6. Set A-7550 SCAN WIDTH to 1 kHz/DIV and RES BW to 3 kHz. Verify 3 kHz bandwidth is between 2.1 kHz and 3.9 kHz wide at 3 dB below peak level.

7. Set A-7550 RES BW to 300 Hz and leave SCAN WIDTH at 1 kHz/DIV. Verify 300 Hz bandwidth is between 210 Hz and 390 Hz wide at 3 dB below peak level.

3-8 VARIANCE BETWEEN BANDWIDTH FILTERS PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Standard 50Ω Coax Cable

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	100 MHz
RF ATTEN	0 dB
IF GAIN	0 dB
2 dB/10 dB/LIN	2 dB
RES B/W	1 kHz/DIV
Mode Menu	Live, 3 MHz B/W

2. Adjust signal to position peak of 100 MHz signal at mid-scale graticule with no modulation. Use the -30 dB graticule as a reference (±2 dB). Connect A-7550 CAL OUT connector (9) to ANALYZER INPUT connector (10).

3. Note that the amplitude level at each bandwidth setting listed below is within the prescribed variance at each step.

Resolution Bandwidth	Variance	Actual Bandwidth
3 MHz	±2 dB	_____
300 kHz	±2 dB	_____
30 kHz	±2 dB	_____
3 kHz	±2 dB	_____
300 Hz	±4 dB	_____

3-9 IF GAIN PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D:

1 RF Signal Generator

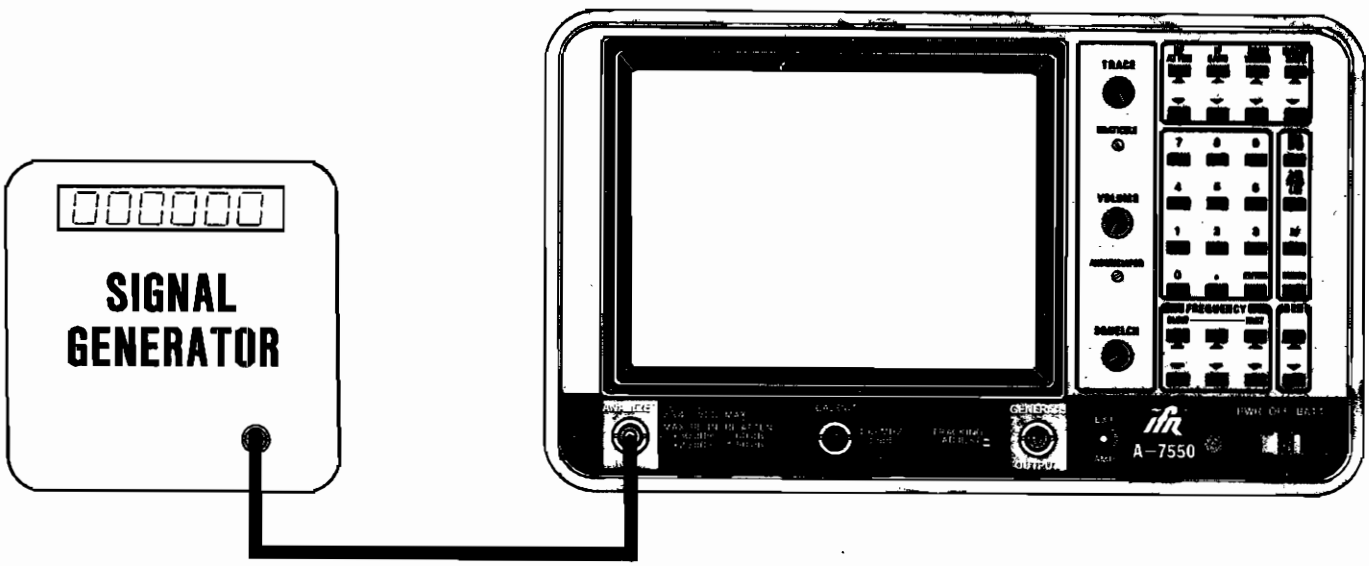


Figure 3-4 IF Gain Test Setup

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	225 MHz
SCAN WIDTH	5 kHz/DIV
RF ATTEN	Ø dB
IF GAIN	0
2 dB/10 dB/LIN	2 dB

2. Set RF Signal Generator to 225 MHz at -34 dBm. Connect RF Generator output to ANALYZER INPUT.

3. Adjust RF Signal Generator to peak the signal on the -34 dB graticule (second graticule from the top). Use this graticule as a reference.

STEP	PROCEDURE
4.	Lower RF Generator Output 20 dB to -55 dBm and adjust the IF Gain control for 20 dB. Compare the displayed signal level to the signal level in step 3 (±2 dB).
5.	Drop the input level 45 dB using the 10 dB and 1 dB attenuators. Adjust the IF Gain Control for maximum gain. Again, compare the displayed signal to the stored signal in Step 3 (±4 dB).
6.	Set the IF Gain Control to 0 dB.

3-10 INPUT ATTENUATOR PERFORMANCE EVALUATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D:

1 RF Signal Generator

1 10 dB Step Attenuator

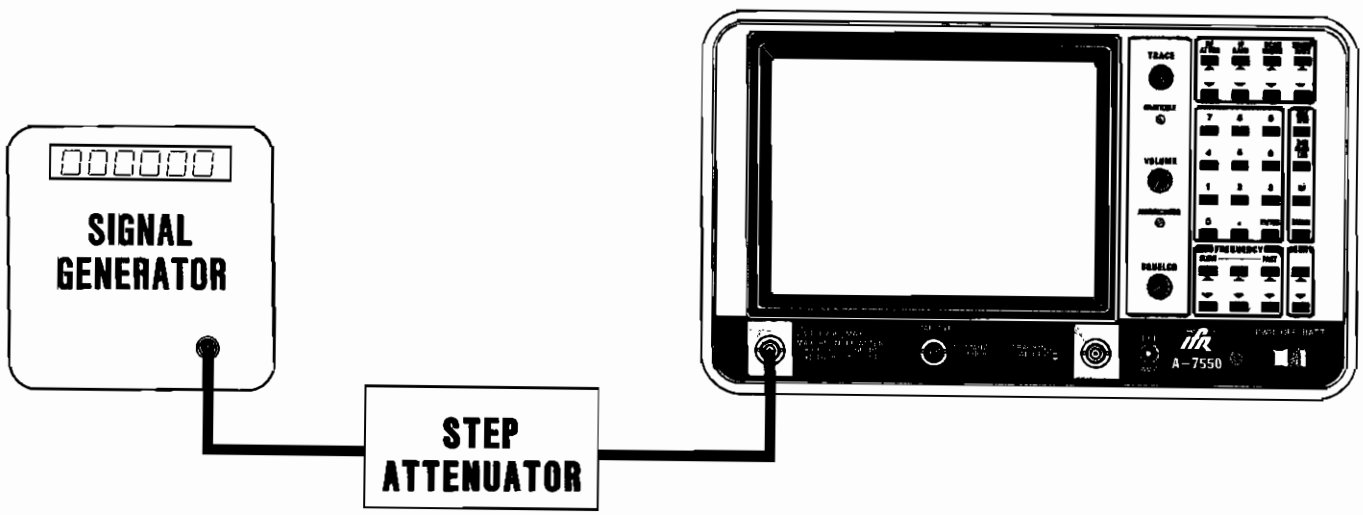


Figure 3-5 Input Attenuator Test Setup

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	225 MHz
SCAN WIDTH	5 kHz/DIV
RF ATTEN	0 dB
IF GAIN	0
2 dB/10 dB/LIN	2 dB

2. Connect equipment as shown in Figure 3-5. Set Step Attenuator to 0. Set RF Signal Generator to 225 MHz at -34 dB (i.e., second graticule from the top of the A-7550 display).

3. Set the Step Attenuator to 10 dB. Adjust the RF Signal Generator to peak the signal on the -34 dB graticule (second graticule from the top). Store this trace signal for use as a reference.

4. Set Step Attenuator to 0 dB. Set RF ATTEN to 10 dB. Compare the displayed signal with the stored signal and record the difference in the space provided below. The amplitude difference should be less than .5 dB at each 10 dB step.

Attenuator	225 MHz RF ATTEN	Deviation
0 dB	10 dB	_____
10 dB	20 dB	_____
20 dB	30 dB	_____
30 dB	40 dB	_____
40 dB	50 dB	_____
50 dB	60 dB	_____

5. Reset the RF on the A-7550 and the Signal Generator to 910 MHz. Reset the IF Gain to -50 dB.

6. Set the Step Attenuator to 20 dB and store the trace signal as stated in Step 3. Use this signal as a reference.

7. Repeat Step 4 beginning at 10 dB Step Attenuator setting and 20 dB RF ATTEN setting.

Attenuator	910 MHz RF ATTEN	Deviation
10 dB	20 dB	_____
20 dB	30 dB	_____
30 dB	40 dB	_____
40 dB	50 dB	_____
50 dB	60 dB	_____
60 dB	70 dB	_____

3-11 TRACKING GENERATOR & OUTPUT ATTENUATOR PERFORMANCE EVALUATION (OPTION)

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Spectrum Analyzer

1 Modulation Meter

1 Power Meter

1 Frequency Counter

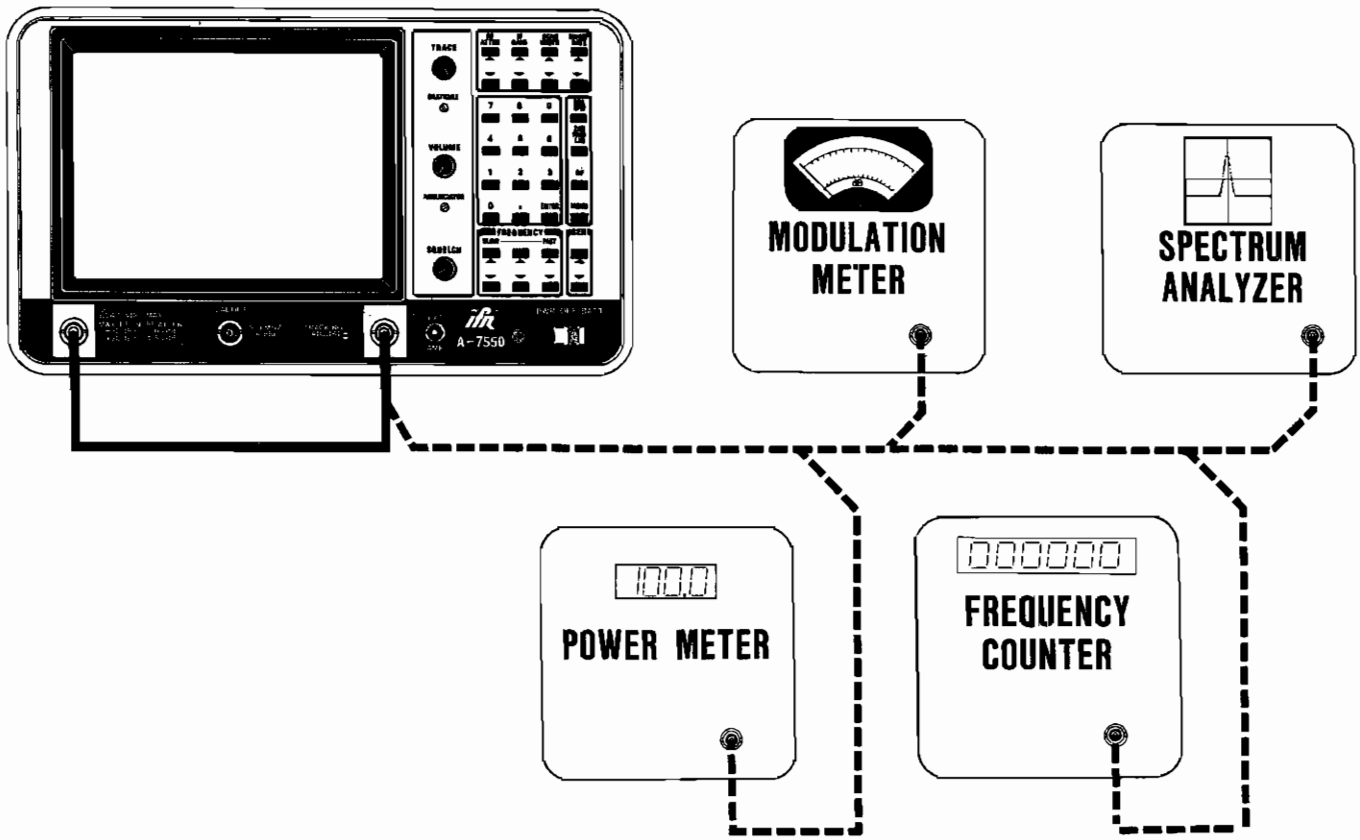


Figure 3-6 Tracking Generator Test Setup

STEP PROCEDURE

1. Connect power meter to A-7550 GENERATE OUTPUT (7).

2. Set A-7550 controls as follows:

Center Frequency	10 MHz
Scan Width	0
Setup Menu	50Ω, dBm, Gen 1
Gen	-20 dBm

STEP PROCEDURE

3. Step FREQUENCY in 10 MHz steps, from 10 through 990 MHz. Verify Generate Output is -20 dB (±2 dB) of each increase.

4. Disconnect power meter.

5. Connect the frequency counter to GENERATE OUTPUT.

6. Use TRACKING ADJUST pot to verify generator output frequency varies from ≥3 kHz below 10 MHz to ≥6 kHz above 10 MHz (i.e., ≤9.997 MHz to ≥10.006 MHz).

7. Set TRACKING ADJUST to 10 MHz before disconnecting the frequency counter.

8. Set A-7550 controls as follows:

Center Frequency	100 MHz
Scan Width	0
Gen	0

9. Connect Modulation Meter to the A-7550 GENERATE OUTPUT Connector (7). Verify residual FM is less than 100 Hz (RMS PEAK). Disconnect modulation meter.

10. Connect an external Spectrum Analyzer to the A-7550 GENERATE OUTPUT Connector (7). Verify the following:

    a. Harmonics are less than 20 dBc.

    b. Non-harmonics are less than 40 dBc.

11. Connect GENERATE OUTPUT to ANALYZER INPUT on the A-7550 to test the 0-60 dB Output Attenuator.

12. Set A-7550 controls as follows:

RF ATTEN	30 dB
RES BW	300 Hz
Center Frequency	225 MHz
10 dB/2 dB/LIN	10 dB
SCAN WIDTH	1 kHz/DIV

13. Step the Generator Attenuator from 0 to -75 dB in -1 dB steps. Verify the trace signal (±1.5 dB) at each division of generator output.

NOTE

TRACKING ADJUST pot may need adjustment at the maximum signal level.

3-12 10.7 MHz RECEIVER PERFORMANCE EVALUATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator

STEP PROCEDURE

1. Set A-7550 controls as follows:

Center Frequency	225 MHz
SCAN WIDTH	0
RF ATTEN	0 dB
IF GAIN	0
2 dB/10 dB/LIN	10 dB LOG
RCVR Menu	FM1
SETUP Menu	"50Ω, dBm"

2. Adjust SQUELCH Control to threshold where receiver noise is squelched.

3. Sensitivity
   Set RF Signal Generator to 225 MHz at -120 dBm.

4. Connect RF Signal Generator output to A-7550 ANALYZER INPUT (10). Increase RF Signal Generator output level until squelch is broken on the A-7550. Verify this level is -101 dBm (2 µV) or lower.

5. Adjacent Channel Rejection
   Set RF Signal Generator and A-7550 SETUP menu as shown in Table 3-2. For each setting, check the sensitivity level and then verify that the RF Signal Generator output level can be increased 40 dB from the sensitivity level before squelch is broken.

RF Signal Generator (MHz)	A-7550 Frequency (MHz)	SETUP Menu
225.3000	225.0000	FM2
224.7000	225.0000	FM2
225.0270	225.0000	FM1
224.9730	225.0000	FM1
225.0120	225.0000	AM1
225.9880	225.0000	AM1

Table 3-2 Adjacent Channel Rejection Settings

6. Selectivity

Set RF Signal Generator to -80 dBm at frequencies shown in Table 3-3 and set A-7550 to corresponding settings. Quiet A-7550 with SQUELCH Control at each setting. At each setting, increase RF Signal Generator output level until squelch is broken. Verify at each setting that level can be increased $\geq$3 dB.

RF Signal Generator (MHz)	A-7550 Frequency (MHz)	SETUP Menu
225.1000	225.0000	FM2
224.9000	225.0000	FM2
225.0075	225.0000	FM1
224.9925	225.0000	FM1
225.0030	225.0000	AM1
224.9970	225.0000	AM1

Table 3-3 Selectivity Settings

3-13 QUASI-PEAK PERFORMANCE EVALUATION (OPTION)

(TO BE SUPPLIED)

SECTION 4 - CALIBRATION

4-1 GENERAL

This section contains the following calibration procedures:

Calibration Procedure	Title	Page
4-2	Power Supply Calibration	4-9
4-3	Display Calibration	4-13
4-4	CRT Calibration	4-15
4-5	Reference Oscillator Calibration	4-21
4-6	RF Control Calibration	4-23
4-7	Amplitude Calibration	4-27
4-8	Tracking Generator Calibration (Option)	4-35
4-9	10.7 MHz Receiver Calibration (Option)	4-37
4-10	Quasi-Peak Filter Calibration (Option)	(To Be Supplied)

Paragraphs 4-2 through 4-7 comprise the normal calibration procedure. A calibration record sheet is provided for recording data from these procedures. Paragraphs 4-8 and on are performed only if the particular option is installed, as necessary. The normal calibration procedures should be performed when one or more of the following conditions are met:

1. If, during the course of normal operation, the A-7550 or any major function thereof fails to meet the performance specifications as provided in "SECTION 3 - PERFORMANCE EVALUATION".

2. If a module is found to be defective and requires replacement (see Table 4-1, MODULE REPLACEMENT & ALIGNMENT REQUIREMENTS).

3. If the recommended 12-month calibration interval is due.

The A-7550 Calibration Record on pages 4-5 through 4-8 can be used to keep track of calibration procedures performed and measurements obtained. You may want to duplicate these pages for future use. Reference numbers (callouts) in parentheses refer to Front/Rear Panel designators. These correspond to the designators used in Figure 1-2.

4-1-1 SAFETY PRECAUTIONS

As with any piece of electronic equipment, extreme caution should be taken when working on "live" circuits. Certain circuits and/or components within the A-7550 contain extremely high voltage potentials, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. When performing the calibration procedures, be sure to observe the following WARNINGS:

WARNING

WHEN WORKING WITH "LIVE" CIRCUITS OF HIGH POTENTIAL:

KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERIOUS SHOCK HAZARD.

REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL.

USE ONLY INSULATED TROUBLESHOOTING TOOLS.

FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AND A RUBBER FLOOR MAT UNDERNEATH TECHNICIAN'S CHAIR.

HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS.

4-1-2 CALIBRATION EQUIPMENT REQUIREMENTS

Appendix B contains a list of test equipment suitable for performing any of the procedures listed in this manual. Any other equipment meeting the specifications listed in Appendix B may be substituted for the recommended models. Allow Analyzer 10 minutes to warm-up to insure electrical stability.

NOTE

For certain procedures in this section, the equipment listed in Appendix B may exceed the minimum required specifications; for this reason, minimum use specifications appear with all calibration procedures where accessory test equipment is required.

4-1-3 DISASSEMBLY REQUIREMENTS

To perform any calibration procedure in this section, the case must be removed from the A-7550.

MODULES BEING REPLACED OR REPAIRED ↓ / CALIBRATION PROCEDURE(S) PERFORMED →	POWER SUPPLY (4-2)	DISPLAY (4-3)	CRT (4-4)	REFERENCE OSCILLATOR (4-5)	RF CONTROL (4-6)	AMPLITUDE (4-7)	TRACKING GENERATOR (4-8)	10.7 MHz RECEIVER (4-9)	QUASI PEAK FILTER (4-10)
POWER SUPPLY	●				●		●		
REFERENCE OSCILLATOR				●					
I/P ATTENUATOR						●			
RECIEVE IF					●	●			
10.7 MHz RECIEVER								●	
ANALYZER IF						●			
QUASI PEAK						●			●
LOG AMP						●			
SWEEP DIGITIZER BOARD		●			●				
VIDEO PROCESSOR BOARD		●							
CRT		●	●			●			
1st L.O. SAMPLING LOOP					●				
2nd L.O. SAMPLING LOOP					●				
SYNTHESIZER #1					●				
SYNTHESIZER #2					●				
INTERFACE BOARD					●	●			
TRACKING GENERATOR							●		
[1] O/P ATTENUATOR							●		
[1] EXTERNAL AMPLIFIER									
1350-2350 MHz VCO									
[2] RF MOTHERBOARD	[2]								
[2] CONTROL PROCESSOR BOARD	[2]								

[1] Perform only if Tracking Generator is installed
[2] Check operation only: Select different frequencies and amplitudes

Table 4-1 Module Replacement and Calibration Requirements

TABLE 4-2: A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

	Para (Step)	Value/Checked
1. Power Supply:	4-2	
Power Supply Lines:		
+16V, ±0.5V	(1,2,3)	_____
+5.2V, ±0.05V	(1,2,3)	_____
+12V, ±0.2V	(1,2,3)	_____
-12V, ±0.5V	(1,2,3)	_____
+40V, +32V to +45V	(1,2,3)	_____
Batt Charge: +14.5V at 0.3A	(4)	_____
Current Limit: 1.1A to 1.7A	(5)	_____
Batt Monitor:		
Low: 5.0V, ±0.1V	(6)	_____
High: 7.5V, ±0.1V	(7)	_____
Low Voltage Cutoff: 11.0V to 11.8V	(10)	_____
Batt Timer: 10 min ± 2 min	(11)	_____
Line Interrupt: 2 sec. minimum	(12,13)	_____
External DC: +12V to 30 VDC (operates)	(14)	Yes/No
2. Display:	4-3	
Reset to LOGO on Power-up	(2)	_____
Grid Display Alignment	(3)	_____
Alpha Display	(4)	_____
Keyboard Operation	(5)	_____
Keyboard Annunciator Adj.	(6)	_____
Graticule Intensity	(7)	_____
Trace Intensity Adj.	(8)	_____
3. CRT:	4-4	
Preset Pots (check only):	(4a-h)	_____
Reset Power	(5)	_____
Vertical	(7)	_____
Width	(8)	_____
Interlace	(9,10)	_____
Master Brightness (VR105)	(6)	_____
or (R71012)	(6)	_____
Focus	(11)	_____
Trace	(12)	_____
Graticule	(12)	_____
Yoke	(13-22)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

	Para (Step)	Value/Checked
4. Oscillator:	4-5	
Frequency: 100 MHz, ±2500 Hz	(1)	_____
Amplitude: -30 dB, ±.1 dBm	(2,3)	_____
5. RF Control:	4-6	
Syn #1		
Tune offset cal @ 50.0000 MHz: 0V, ±1V	(3)	_____
Tune offset cal @ 50.0999 MHz: 0V, ±1V	(4)	_____
Regenerative divider: smooth operation	(5,6,7)	_____
Sampler offset: 0 V, ±5 mV	(8-9)	_____
VCO:		
Low limit: 1325 MHz	(12)	_____
High limit: 2390 MHz	(13)	_____
VCO Sampler DAC:		
Tune offset @ 1350 MHz: 0V, ±1V	(15)	_____
Tune gain @ 2300 MHz: 0V, ±1V	(16)	_____
Sampler Loop/Syn #1 disp. gain:		_____
Centered	(20)	_____
Sampler DAC tune dispersion gain:		
Centered	(21)	_____
RF null cal: -45 dBm < RF < -35 dBm	(22)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

	Para (Step)	Value/Checked
6. Amplitude:	4-7	
Auto cal OFF	(1)	_____
Receive IF level cal @ -10 dBm:		
10.7 MHz	(4,5)	_____
Resolution BW levels		
3 MHz	(6)	_____
300 kHz	(8)	_____
30 kHz	(9)	_____
3 kHz	(10)	_____
300 Hz	(11)	_____
10 dB LOG cal: ±0.5 dB	(12-20)	_____
2 dB LOG cal: ±0.1 dB	(21-23)	_____
LINEAR: Within 10%	(24-26)	_____
Auto Cal OFF Level: -10 dB ±0.5 dB		
@ 225 MHz	(29)	_____
Auto Cal ON level: -10 dB ±0.5 dB		
@ 225 MHz	(30-31)	_____
IF Gain linearity: ±2 dB	(32)	_____
RF Attenuation linearity ±0.5 dB	(33)	_____
Sweep flatness: ±2 dB	(35)	_____
IF filter flatness: ±2 dB	(36-37)	_____
Noise floor: -125 dBm	(38)	_____
Sidebands: <65 dBc	(39)	_____
Video filter: 300 Hz	(40-42)	_____
Base Line Rise: -70 dBc max, ±5 kHz	(43)	_____
Spurious Signal Level	(44)	_____
75Ω Test: level rises 6 dB	(45)	_____
7. Tracking Generator (Option):	4-8	
Tracking Adjust: -3 kHz to +6 kHz from CF	(1)	_____
Output level adjust: (-10 dB)	(2)	_____
Gen Keys: 0 to -75 dB Atten	(5)	_____
75Ω test display level: Decreases 6 dB	(6)	_____
Harmonics less than 20 dBc	(7)	
Non-harmonics less than 40 dBc	(7)	
Frequency Deviation (Residual FM): ±100 Hz (RMS PEAK) @ 100 MHz	(9)	_____
External Amp: +11.7V, ±0.2V	(10)	_____

TABLE 4-2 (CONTINUED): A-7550 CALIBRATION RECORD

Technician: _____ S/N: _____

	Para (Step)	Value/Checked
8. 10.7 MHz Receiver (Option):	4-9	
Bandpass on RCVR Menu: FM2 (200 kHz bandpass)	(5)	_____
Bandpass on FM1: 15 kHz bandpass	(7)	_____
Bandpass on AM1: 6 kHz bandpass		
Distortion:		
FM2 Audio: 6V p-p, <5% distortion	(10)	_____
FM1: 6V p-p, <3 distortion	(11)	
AM1 & AM2: <1% distortion	(12)	_____
Sensitivity: 10 dB SINAD, -71 dBm or less	(13)	_____
SSB Injection: 1V p-p	(14)	_____
Squelch: Audio present	(15)	_____
Audio Blanking: Audio present TSR	(16)	_____
9. Quasi-Peak (Option):	TO BE SUPPLIED	

4-2 POWER SUPPLY CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 DC Voltmeter--Any

1 Insulated Tuning Tool

1 Battery Load Simulator (IFR Part No. 1003-9801-600)--See Appendix D

1 DC Power Supply--Variable from +10.9V to +30V Current--5A (Surges to 15A)

FIGURE REFERENCES: Figure 5-7 Power Supply Module
Figure 4-13 Composite and Adjustments

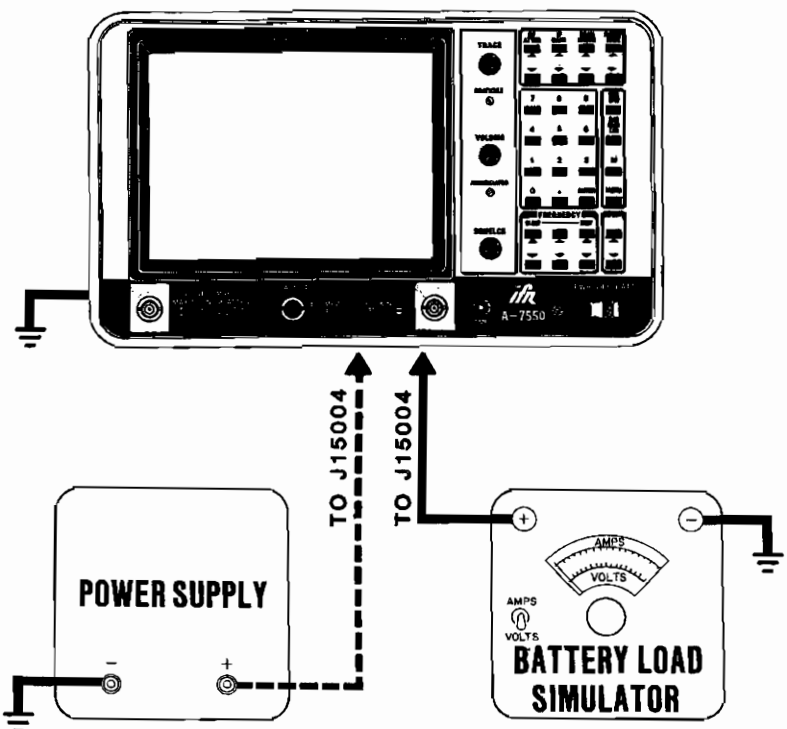


Figure 4-1 Power Supply Calibration Test Setup

STEP PROCEDURE

NOTE

On units with Serial Numbers 1001 through 1476, the Power Supply lines are most easily accessed where they connect into the RF Motherboard. Locate the RF Motherboard in the Bottom View of Figure 4-13. The Power Supply lines will be soldered into the RF Motherboard at the bottom edge.

STEP PROCEDURE

1. Power Supply Lines

Test resistance between Power Supply lines and chassis ground as follows:

Line	Pin # of J15003	Resistance
+12V (red)	1,2	>20Ω
+5V (orange)	4,5	>100Ω
-12V (yellow)	7	>300Ω
+40V (green)	12	>15 KΩ

2. Connect AC power cord to A-7550 and place PWR/OFF/BATT switch to "PWR".

3. Verify Power Supply output voltage on Power Supply lines as shown on chart below. If necessary, adjust indicated trimpot to desired voltage level.

Line	Tolerance	Adjustment
+16 V (blue)	±0.5 V	R17068
+12 V (red)	±0.2 V	R17056
+5.2 V (orange)	±0.05 V	R17062
-12 V (yellow)	±0.5 V	None (tracks +12 V line)
+40 V (green)	+32 V to +45 V	None (tracks +12 V line)

NOTE

To gain access to the adjustment holes in the Power Supply, the Receive IF Module must be moved. Leave hard-wire connections attached to these modules if they are moved.

NOTE

The +16V line is only used in the Power Supply. If other lines are within tolerance, checking the +16V line is not necessary.

4. Batt Charge

Remove bracket covering battery to gain access to battery connector (J15004). Disconnect J15004 from the battery. Connect the Battery Load Simulator to J15004 (Figure 4-1). Verify a battery charge voltage of +14.5V at a 0.3A load. If necessary, adjust R17006 (BATT CHARGE) to desired level.

STEP PROCEDURE

CAUTION

IN STEP 5, DO NOT LEAVE BATTERY LOAD SIMULATOR SET TO MAXIMUM CURRENT LOAD FOR AN APPRECIABLE LENGTH OF TIME. A QUICK GLANCE IS ALL THAT IS NECESSARY. THIS PREVENTS POSSIBLE DAMAGE TO THE SET.

5. Current Limit

Set Battery Load Simulator to give a maximum current load. Verify that battery charge current limit is between 1.1A and 1.7A. Disconnect Battery Load Simulator from J15004.

6. Batt Monitor (SN 1001 through 1476)

Measure the voltage at the junction of R33009 and trimpot R33008 on the RF motherboard. If the voltage is not +5 V (±0.1 V), adjust R33007 (BATT REF ADJ) to the desired voltage level.

7. Measure the voltage at the junction of trimpots R33007 and R33008 on the RF motherboard. If the voltage is not +7.5 V (±0.1 V), adjust R33008 (BATT CAL) to the desired voltage level.

6. Batt Monitor (SN 1477 and on)

Measure the voltage at pin 4 of U19007 (IC) on the Interface PC Board. If the voltage is not +5 V (±0.1 V), adjust R19029 (BATT REF ADJ), as necessary, to the desired voltage.

7. Measure the voltage at pin 8 of U19007 (IC) on the Interface PC Board. If the voltage is not +7.5 V (±0.1 V), adjust R19030 (BATT CAL), as necessary, to the desired voltage.

8. Battery Operation (All Units)

Turn set OFF. Disconnect AC power cord from A-7550. Connect variable DC power supply, set at +14.2 VDC, to J15004 (battery connector - Figure 4-1). Turn set on to "BATT".

9. Voltage Display

Select TEST menu on the A-7550. Vary the DC Power Supply in half-volt increments from +11.5V to +15V. At each increment, select "5" on the TEST menu to measure battery charging voltage. Verify that BATT voltage changes for each half-volt increment on CRT.

10. Low Voltage Cutoff

Slowly decrease DC power supply voltage and verify that the set turns off between +11.0V and +11.8V.

NOTE

On units with Serial Numbers 1477 and on, Power Supply lines should be checked at pin 96 on the Motherboard.

11. Batt Timer

Increase DC power supply to approximately +14V. Toggle the PWR/OFF/BATT Switch to "BATT" to turn on the battery power. Verify battery timer operation by observing that A-7550 shuts off in 10 minutes (±2 minutes).

12. Line Interrupt

Disconnect DC power supply. Connect J15004 to battery and connect AC power to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

13. Remove AC power cord and verify the A-7550 continues to operate for at least 2 seconds. This is not a critical time period. Merely verify there is some delay.

14. External DC

Connect DC power supply, set at +12 to +30 VDC, to DC input connector on A-7550. Set PWR/OFF/BATT Switch (2) to "PWR". Verify A-7550 operates with +12 to +30 VDC input.

4-3 DISPLAY CALIBRATION

SPECIAL ACCESSORY
EQUIPMENT REQ'D: 1 Insulated Tuning Tool--w/Common Tip

FIGURE REFERENCES: Figure 5-4 Front Panel
Figure 5-5 Keyboard

STEP PROCEDURE

NOTE

If the CRT display is skewed, rolling or tilted in the following steps, go to paragraph 4-4, CRT Calibration.

1. Connect AC power cord to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

2. Reset to LOGO

   Verify IFR logo is present on CRT display. Press any key on the keyboard and verify analyzer grid is present on CRT display or grid appears within 8 seconds.

3. Grid Display Alignment

   Verify grid is correct in size and shape (straight lines and square corners).

4. Alpha Display

   Verify alpha display (letters and numbers) is clear and legible.

5. Keyboard Operation

   Verify keyboard controls alpha display.

6. Keyboard Annunciator Adjustment

   Verify "beep" is audible when keys are pressed. Adjust ANNUNCIATOR pot on front panel for desired audible level.

7. Graticule Intensity Adjustment

   NOTE

   If the brightness intensity is too low in the following steps, go to step 6-8 of Paragraph 4-4 to adjust master brightness level.

   Verify grid display brightness is variable. Adjust GRATICULE Intensity Adjust (IA) (13) on front panel for desired brightness (see NOTE above).

STEP	PROCEDURE

8. Trace Intensity Adjustment

Verify alpha display brightness is variable. Adjust TRACE Intensity Adjust (IA) (14) on front panel for desired brightness (see NOTE in Step 7, above).

4-4 CRT CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Insulated Tuning Tool

1 Insulated Hex (0.100) Tuning Tool

FIGURE REFERENCES: Figure 4-13 Composite and Adjustments
Figure 5-6 Computron CRT Display Module

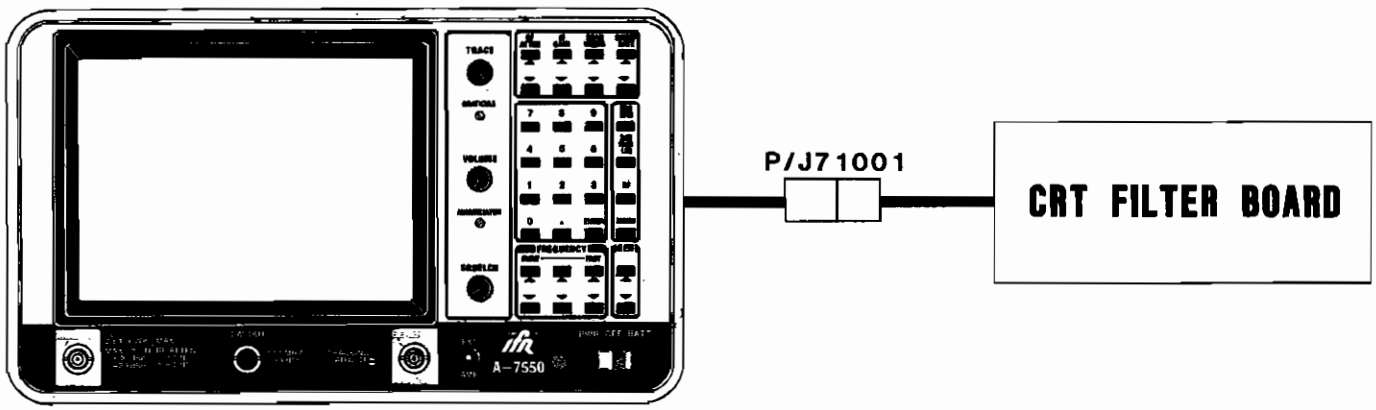


Figure 4-2 CRT Calibration Test Setup

NOTE

This procedure is performed only as needed.

STEP PROCEDURE

CAUTION

HIGH VOLTAGES ARE PRESENT ON THE CRT MODULE DURING OPERATION. DO NOT TOUCH ANY METAL PARTS ON THE CRT SATELLITE PC BOARD. KEEP HANDS AWAY FROM METAL CONNECTIONS ON TOP AND BOTTOM OF YOKE.

1. Disconnect J71001 on the CRT Filter Board and remove CRT Module from A-7550.

2. Remove Figure 4-3 from manual. Cut on outside of line as indicated. Carefully center the cut line within the white viewing area of the CRT and, using transparent tape, tape overlay onto face of the CRT. The dimensions of the cut line are the dimensions of the CRT bezel when the CRT is mounted in the set. The cut edge of the overlay will be approximately the same as the white part of the CRT.

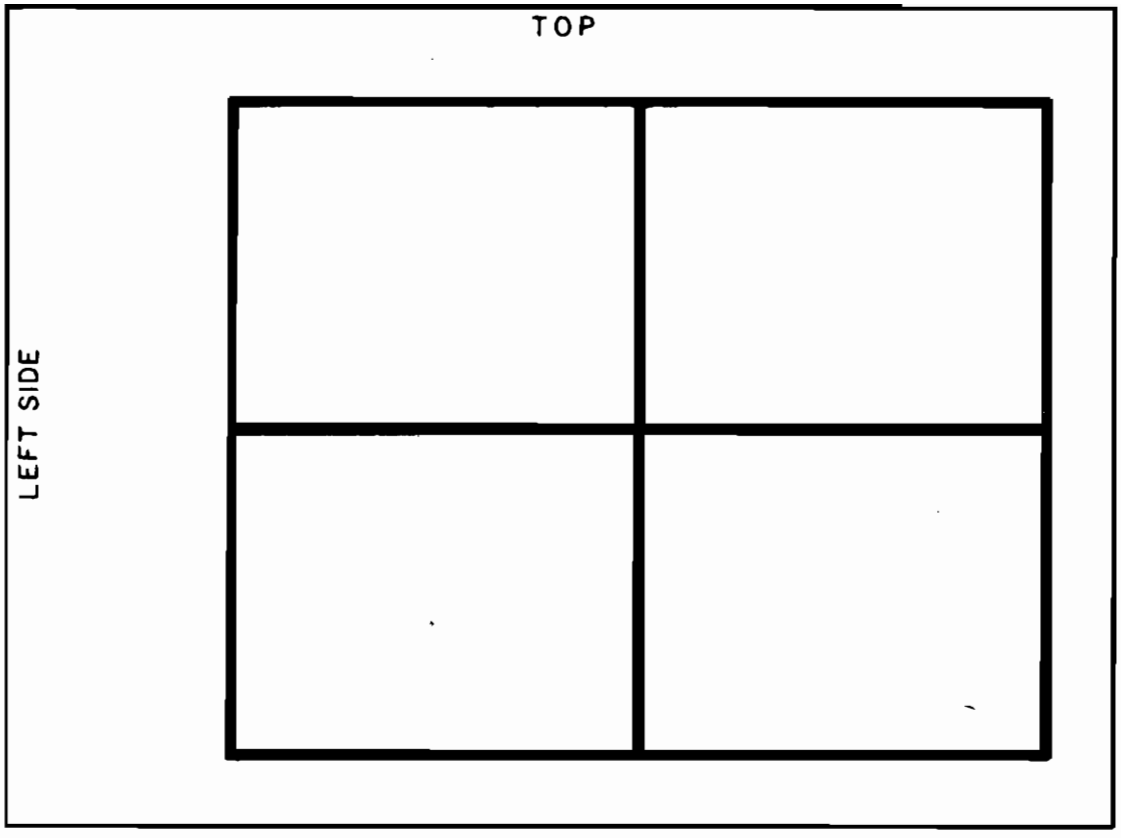


Figure 4-3 Overlay For CRT Calibration.

STEP PROCEDURE

NOTE

At all times during this procedure, keep the CRT Module oriented so that the display faces magnetic North or South. This will keep any earth magnetic effects from distorting the display after reinstallation of the mu-metal shield.

3. Connect J71001 on the CRT Filter Board to P71001. (Fabricating an extender cable may be necessary.)

4. Preset pots to the following specifications:

   A. R71006 (VERT) on CRT Filter Bd. - midrange

   B. R71004 (WIDTH) on CRT Filter Bd. - midrange

   C. R71005 (INTERLACE) on CRT Filter Bd. - midrange

   D. VR103 (VIDEO) on CRT Main Bd. - fully CW

   E. VR105 (MASTER BRIGHT) on CRT Main Bd. - midrange
      R71012 (MASTER BRIGHT) is on CRT Filter Bd for later sets.

   F. VR200 (FOCUS) on CRT Satellite Bd. - midrange

   G. TRACE Intensity Adjust on Front Panel - fully CW

   H. GRATICULE Intensity Adjust on Front Panel - fully CW

5. Set PWR/OFF/BATT Switch (2) to "PWR". Wait 30 seconds for warmup.

6. IFR logo should appear, but may be unstable. Adjust VR105 (R71012) (MASTER BRIGHT) until the green background just disappears.

7. Adjust R71006 (VERT) until the image stops rolling vertically. Adjust in one direction if image rolls up, adjust in the other direction if image rolls down. Adjust midway between rolls.

8. Adjust R71004 (WIDTH) until logo covers about 3/4 of screen width.

9. Adjust R71005 (INTERLACE) until the display is stable horizontally.

10. Using eyepiece (jeweler's loupe), adjust R71005 (INTERLACE) until the lines are evenly spaced in the top center of the border.

STEP PROCEDURE

11. Press any key on the KEYBOARD (1). The graticules should then be displayed. Using eyepiece, adjust VR200 (FOCUS) until the lettering at the top edge is at its sharpest.

12. Set TRACE Intensity Adjust (14) and GRATICULE Intensity Adjust (13) for comfortable viewing.

13. Observe graticules (horizontal and vertical) to see if the yoke is properly positioned. If both horizontal and vertical graticules seem to be turned slightly in the same direction, rotate the yoke as described in Step 14. Otherwise, go to Step 15.

14. Loosen Phillips-head screw on back of yoke. Carefully cut into putty on front of tube so wires are not cut or broken. Twist gently to break the putty bond, holding the yoke to the tube. Rotate yoke until the center horizontal graticule line is perfectly horizontal. Tighten Phillips-head screw.

NOTE

There are eight evenly-spaced square magnets at the front of the deflection yoke. One edge of the magnets is identified with a color code indicating magnetic strength as follows:

Small White - Weakest
Yellow
Green
Red
Blue
Large White - Strongest

The magnets should not need adjustment unless they have been moved or if the yoke and/or CRT have been replaced.

The magnets affect the display as shown in Figures 4-4 and 4-6. Avoid rotating magnets unless abnormal effects result, as shown in Figures 4-4 and 4-6.

If alignment cannot be accomplished, a weaker or stronger magnet may have to be substituted for any of the existing magnets.

15. Rotate each of the corner magnets (see Figure 4-4) in turn, to square up the corners.

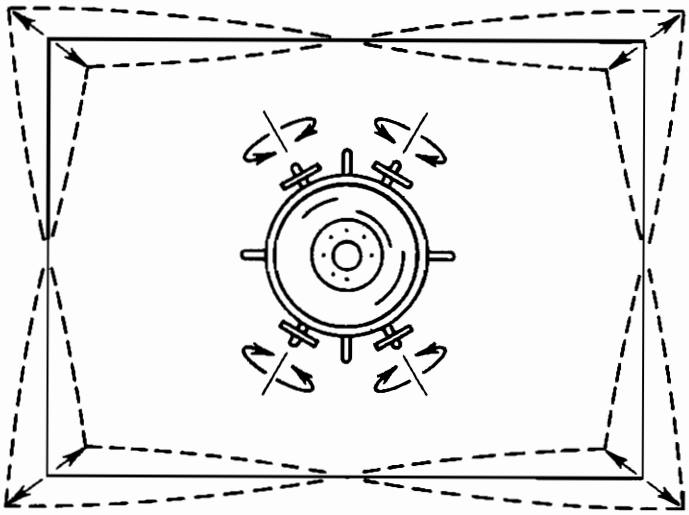


Figure 4-4 Trapezoidal Adjustments

STEP PROCEDURE

16. There are two black centering tabs toward the back of the yoke (see Figure 4-5). These center the display. Adjust the tabs to align the graticules with the furnished overlay.

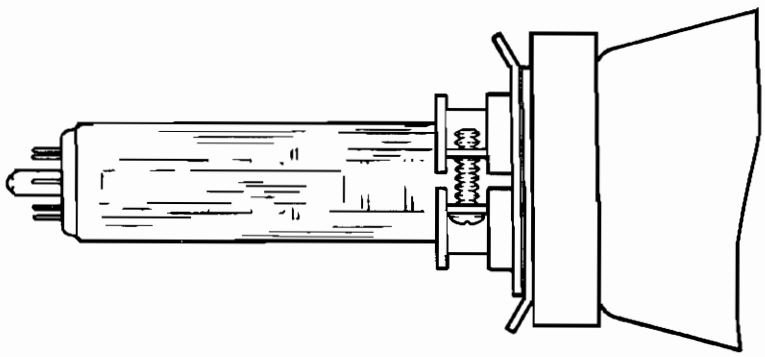


Figure 4-5 Partial View of CRT Neck/Deflection Yoke

17. Adjust the two side magnets and the two top magnets (see Figure 4-6) to align the sides of the display.

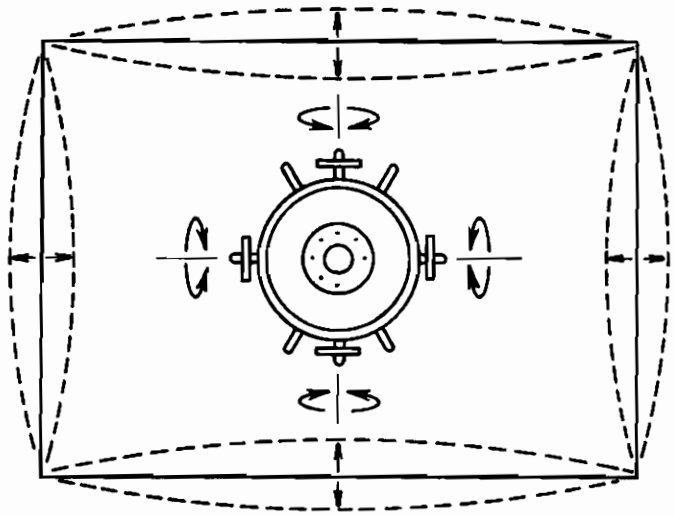


Figure 4-6 Pincushion/Barrel Adjustments

STEP PROCEDURE

18. If necessary, readjust the black centering tabs.

NOTE

R71004 (WIDTH) may have to be adjusted to align the width of the display with the furnished overlay.

19. Repeat Steps 13 through 18 until display is aligned.

20. Install mu-metal shield and observe display. Adjust R71004 (WIDTH) pot and L101 (HEIGHT) coil on CRT Main PC board to align display. It may also be necessary to adjust the magnets and centering tabs to align the display. If so, slide the mu-metal off and make adjustments. Reinstall mu-metal and observe display. Continue until display is aligned.

21. If the yoke was rotated in Step 14, apply putty to the front of the yoke to secure the yoke to the glass tube. Keep the putty away from the wires in the yoke.

22. Install CRT Module in set and observe display. If display is acceptable, this procedure is complete; otherwise, repeat Steps 13 through 21.

4-5 REFERENCE OSCILLATOR CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Spectrum Analyzer

1 Frequency Counter

1 RF Signal Generator

1 Power Meter w/Thermistor Mount

FIGURE REFERENCES: Figure 5-17 Reference Oscillator Module
Figure 4-13 Composite and Adjustments

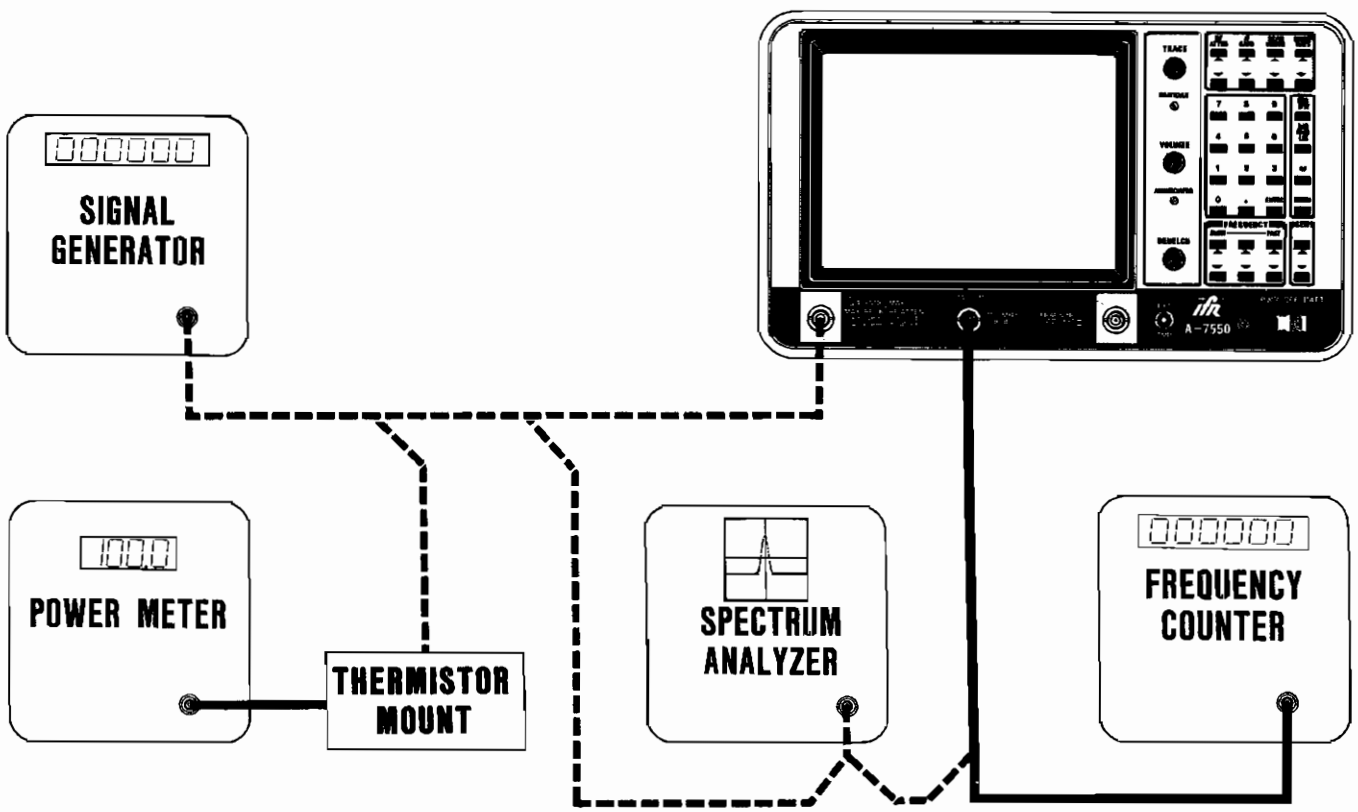


Figure 4-7 Reference Oscillator Calibration Test Setup

STEP	PROCEDURE

1. Frequency

Using Frequency Counter, measure the reference frequency at CAL OUT Connector on A-7550. Verify frequency is 100 MHz (± 2500 Hz) at room temperature. Adjust L47002 (REF FREQ) on Reference Oscillator module.

STEP	PROCEDURE

2. Amplitude

   Disconnect Frequency Counter. Set RF Signal Generator to 100 MHz at -30 dBm and verify level with Power Meter. Connect RF Signal Generator to an external Spectrum Analyzer and note signal level.

3. Disconnect RF Signal Generator. Then, using the same coax cable used in Step 2, connect CAL OUT (9) to external Spectrum Analyzer. Verify signal level is the same as noted in Step 2 (±0.1 dB). If necessary, adjust R47023 (CAL ADJ) on Reference Oscillator Module.

NOTE

Reference Frequency and CAL ADJ interact, sometimes as much as 2 dB and/or 500 kHz. Repeat Step 1 after adjusting R47023 or L47002.

4-6 RF CONTROL CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope

1 DC Power Supply

1 Digital Voltmeter

1 Tune Control Pot--Appendix D

1 Spectrum Analyzer

FIGURE REFERENCES: Figure 4-13 Composite and Adjustments

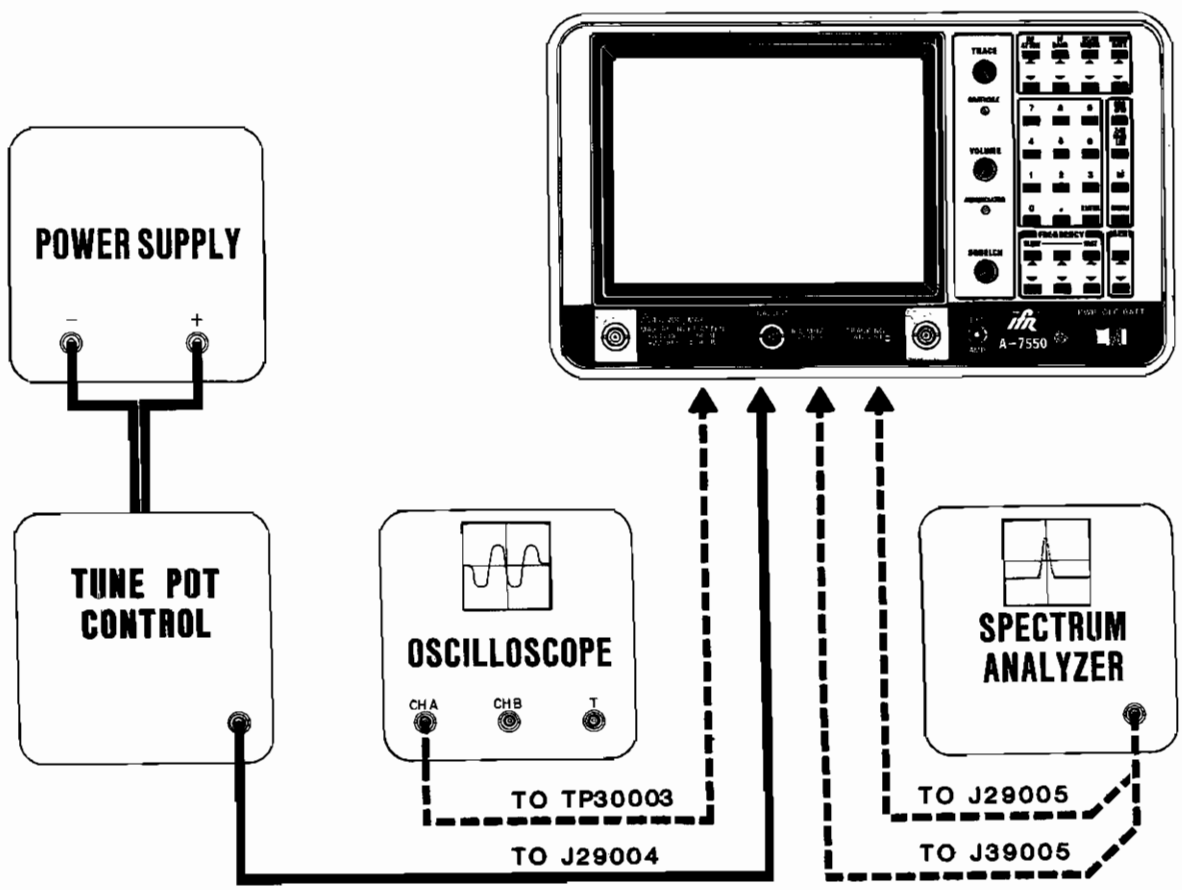


Figure 4-8 RF Control Calibration Test Setup

STEP PROCEDURE

1. Connect test equipment (Figure 4-8) and AC power cord to A-7550. Place PWR/OFF/BATT Switch (2) to "PWR".

2. Set SCAN WIDTH to 0 kHz/DIV and center frequency to 50.0000 MHz. (Press: RF 50. ENTER)

3. Syn. #1 Tune Offset

Verify 0 VDC (±1 V) is present at TP23001 on Synthesizer #1 module If necessary, adjust R19047 (SYN #1 OFFSET) (R19013 on Serial Numbers 1477 and on) on Interface Board to desired voltage level.

4. Syn. #1 Tune Gain

Select 50.0999 MHz as center frequency. (Press: RF 50.0999 ENTER). Verify 0 V (±1 V) at TP23001. If necessary, adjust R19043 (SYN #1 GAIN) (R19007 on SN 1477 and on) on Interface Board to desired voltage level.

5. Regenerative Divider

Remove jumper from JTB30001 on 1st L.O. Sampling Loop Module. Disconnect coax #11 from J29004 on 1st L.O. Sampling Loop Module. Put a tee on J29004 and connect coax #11 on one side of tee. Connect Tune Control Pot to other side of tee.

6. Connect an external Spectrum Analyzer to J39005 on 1350-2350 MHz VCO Module. (Disconnect coax #13 from J39005 if Tracking Generator option is installed.) Manually tune the VCO from 1325 to 2450 MHz with the Tune Control Pot to verify manual control of the VCO frequency.

7. Connect an Oscilloscope to TP30003 on the 1st L.O. Sampling Loop module. While manually tuning the VCO between 1325 MHz and 2450 MHz, verify a smooth voltage change on the Oscilloscope (i.e., -2 to -4 V). If necessary, adjust R30033 (DIVIDER TUNE GAIN) on 1st LO Sampling Loop Module to desired voltage level (i.e., -2 to -4 V).

NOTE

On some sets, TP30003 is not accessible through the top of the 1st L.O. Sampling Loop module. A test wire (insulated, 22 AWG) must be soldered to TP30003 after removing and disassembling the module. The test wire may then be fed through one of the adjustment holes for this cal procedure. The test wire must be removed after this procedure is completed.

8. Sampler Offset

Manually tune the VCO for a 1500 MHz signal display on the external Spectrum Analyzer. Disconnect external Spectrum Analyzer from J39005, and connect it to J29005 on the 1st L.O. Sampling Loop module. Adjust external Spectrum Analyzer until signal is centered on 0 MHz with 5 MHz/DIV. Adjust Tune Control Pot until the tallest spurs are within 5 MHz from the signal center.

STEP PROCEDURE

9. Using digital voltmeter, measure DC voltage at TP30004 on 1st L.O. Sampling Loop Module. If the voltage is not 0 VDC (±5 mV), adjust R30070 (SAMPLER OFFSET) to the desired voltage level.

10. Disconnect external Spectrum Analyzer from J29005 and connect it to J39005 on the 1350-2350 MHz VCO Module. Connect coax #12 to J29005. Disconnect tee from J29004 and connect coax #11 to J29004. Install jumper on JTB30001.

CAUTION

HEREON, DO NOT ALLOW THE DC POWER SUPPLY TO EXCEED +5 VDC. IT SHOULD BE SET TO 0 VDC BEFORE CONNECTING TO J29002.

11. Low Limit Cal

Disconnect coax #18 from J29002 on the 1st L.O. Sampling Loop Module. Connect Tune Control Pot to J29002 for manual tuning. Verify manual control from 1325 MHz to 2450 MHz as seen on external Spectrum Analyzer.

12. Manually tune VCO below 1350 MHz as displayed on the external Spectrum Analyzer. Adjust R30049 (LOW LIMIT) on the 1st L.O. Sampling Loop Module to stop VCO frequency at 1325 MHz.

13. High Limit Cal

Manually tune the VCO above 2350 MHz as displayed on the external Spectrum Analyzer. Adjust R30045 (HIGH LIMIT) on the 1st L.O. Sampling Loop module to stop VCO frequency at 2390 MHz.

14. Sampler DAC Tune Offset

Disconnect Tune Control Pot from J29002. Connect coax #18 to J29002. Set SCAN WIDTH to 0 kHz/DIV and set 0.0050 MHz center frequency on A-7550 (Press: RF 0 ENTER).

15. Verify 1350 MHz VCO frequency as read on external Spectrum Analyzer. Verify voltage on TP30007 on 1st L.O. Sampling Loop module is 0V (±1V). If necessary, adjust R19051 (SAMPLER OFFSET) (R19009 on SN 1477 and on) on the Interface PC Board, to desired voltage level.

16. Sampler DAC Tune Gain

Select 950.0 MHz center frequency on A-7550. Verify VCO frequency as read on external Spectrum Analyzer is 2300 MHz. Verify voltage at TP30007 is 0V (±1V). If necessary, adjust R19049 (SAMPLER GAIN) (R19005 on SN 1477 and on) on the Interface PC Board.

STEP	PROCEDURE

17. Repeat Steps 15 and 16 and verify voltage at TP30007 is 0V (±1V).

18. Disconnect External Spectrum Analyzer from J39005 and connect coax #13 (if Tracking Generator is installed) to J39005.

19. Sampler Loop/SYN #1 Dispersion Gain

    Connect COAX from CAL OUT to ANALYZER INPUT. Press key sequence: RF ENTER to select full scan operation.

20. Reset SCANWIDTH to 500 kHz/DIV and adjust R19068 (R19022 for S/N 1477 and on), SYN #1 SWEEP GAIN, to center 500 MHz signal (±1.25 minor divisions) of center graticule. Step down scanwidth to verify 500 MHz signal stays within 1.25 minor divisions of center frequency division.

    NOTE

    T32023 (SWEEP RAMP ADJ) on Sweep Digitizer PC Board may require adjustment if R19068 (R19022 on SN 1477 and on) cannot supply the necessary

21. Reset the unit to full scan (Press: RF ENTER). If necessary, adjust R19066 (SAMPLER SWEEP GAIN) (R19024 on SN 1477 and on) on Interface PC Board until there is one 100 MHz harmonic/DIV aligned on each major division. The 1000 MHz harmonic should be aligned with the right-most graticule.

22. RF Null Cal

    Disconnect CAL OUT (9) from ANALYZER INPUT (10). Select zero Frequency Mode (Press: RF 0 ENTER) and zero SCAN WIDTH (0 kHz/DIV). Remove COAX #34 from J41005 on the Receive IF Module. Connect an External Spectrum Analyzer to J41005. Verify the 189.3 MHz signal level is between -35 and -45 dBm. If necessary, adjust R44002 (1350 MHz NULL #1) and R44003 (1350 MHz NULL #2) in the Receive IF module. Connect Coax #34 to J41005 when finished.

4-7 AMPLITUDE CALIBRATION

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 RF Signal Generator

1 Spectrum Analyzer

1 Power Meter w/Thermistor Mount

FIGURE REFERENCES: Figure 4-13 Composite and Adjustments
Figure 5-15 Interface PC Board

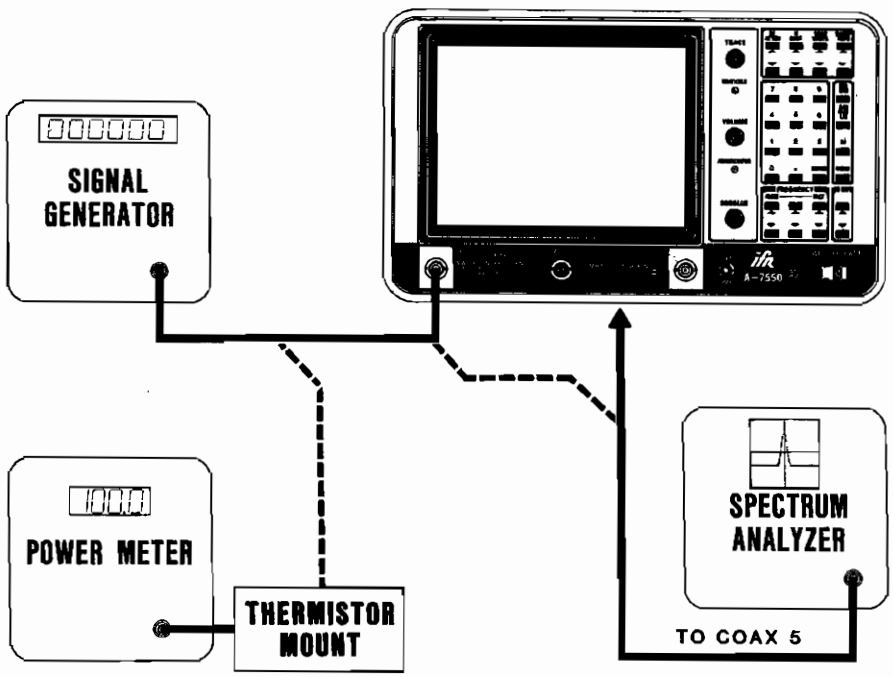


Figure 4-9 Amplitude Calibration Test Setup

STEP PROCEDURE

1. Auto Cal OFF

   Jumper together the two posts of JTB19001 on the Interface PC Board to disable Auto-Cal.

2. Connect AC power cord to A-7550. Set PWR/OFF/BATT Switch (2) to "PWR".

3. Set the following CRT values:

   Center Frequency ..... 225.0000 MHz
   SCAN WIDTH 0
   RES BW ..... 3 MHz
   RF ATTEN ..... 30 dB
   2 dB/10 dB/LIN ..... 2 dB LOG
   FILTERS menu ..... None

STEP	PROCEDURE

4. Connect RF Signal Generator to a power meter and set RF Signal Generator output to 10.7 MHz at -10 dBm. Disconnect power meter and connect external Spectrum Analyzer, set at 10.7 MHz center frequency and 2 dB/DIV, to output of RF Signal Generator. Note or store the calibrated signal level.

5. Receive IF Level Cal

   Disconnect coax #5 from J41008 on the Receive IF Module. Connect an external Spectrum Analyzer to coax #5. Connect RF Signal Generator, set to 225 MHz at -10 dBm as calibrated on a power meter, to ANALYZER INPUT (10) on A-7550. Verify signal is 10.7 MHz at -10 dBm to -14 dBm. (Signal level may be as low as -14 dBm, if the remainder of the steps in this procedure are to be accomplished.) If necessary, adjust R42029 (IF GAIN ADJ) in Receive IF module to set level.

6. 3 MHz BW

   Connect coax #5 to J41008. Disconnect coax #6 from J26003 on LOG AMP module. Connect an external Spectrum Analyzer to coax #6. Verify signal is 10.7 MHz at -10 dBm, ±0.5 dB. If necessary, adjust R22020 (IF LEVEL GAIN) on Analyzer IF module to desired signal level. Connect coax #6 on Log Amp.

7. Press SCANWIDTH pushbutton (up) until scanwidth setting is 2 kHz/DIV. Select the 3 MHz B/W again. Note, or store in memory, the trace level on the CRT display.

8. 300 kHz BW

   Select 300 kHz RES BW. Verify trace level is identical to Note in Step 7. If necessary, adjust R22015 (300 kHz LEVEL ADJ) on Analyzer IF module to desired level.

9. 30 kHz BW

   Select 30 kHz RES BW. Verify trace level is the same as noted in Step 7. If necessary, adjust R22031 (30 kHz LEVEL ADJ) on Analyzer IF module to desired level.

10. 3 kHz BW

    Select 3 kHz RES BW. Verify trace level is the same as noted in Step 7. If necessary, adjust R22052 (3 kHz LEVEL ADJ) on Analyzer IF module to desired level.

11. 300 Hz BW

    Select 300 Hz RES BW. Verify trace level is the same as noted in Step 7. If necessary, adjust R22074 (300 Hz LEVEL ADJ) on Analyzer IF module to desired level.

STEP PROCEDURE

12. 10 dB LOG Cal Linearity

Set the following CRT values:

Center Frequency	225 MHz
SCAN WIDTH	5 kHz/DIV
RES BW	3 kHz
RF ATTEN	30 dB
IF GAIN	0
2 dB/10 dB/LIN	10 dB LOG
FILTERS Menu	None

13. Set RF Signal Generator to 225 MHz at -70 dBm. Connect RF Signal Generator to ANALYZER INPUT Connector. Verify -70 dBm (±0.5 dB) on the CRT. If necessary, adjust R26151 (10 dB OFFSET) on the Log Amp module to the desired level.

14. Recalibrate RF Signal Generator to 225 MHz at -10 dBm. Verify -10 dBm (±0.5 dB) on the CRT. If necessary, adjust R26161 (10 dB GAIN) on the Log Amp module to desired level. If adjustment was necessary, repeat Steps 13 and 14.

15. Recalibrate RF Signal Generator to 225 MHz at 0 dBm. Verify the signal is within 0.5 dB from the top of the screen display. If necessary, adjust R26066 (REF LINE COMPRESSOR) on the Log Amp Module. If adjustment was necessary, repeat Steps 13 and 14.

16. Recalibrate RF Signal Generator to -60 dBm, -50 dBm and -40 dBm. If the corresponding levels on the CRT are within 0.5 dB, go to Step 18. If not, continue at Step 17.

17. Recalibrate RF Signal Generator to -50 dBm. Observe the error on the CRT. If necessary, adjust R26097 (LOG LINEARITY LOW) on the Log Amp Module for twice the error shown. Repeat Steps 13 and 14.

18. Recalibrate RF Signal Generator to -20 dBm, -30 dBm and -40 dBm. If the corresponding levels on the CRT are within 0.5 dB, go to Step 20. If not, continue at Step 19.

19. Recalibrate RF Signal Generator to -30 dBm. Observe the error on the CRT. If necessary, adjust R26074 (LOG LINEARITY HIGH) on the Log Amp Module for twice the error shown. Repeat Steps 13 and 14.

20. Step RF Signal Generator in 10 dB increments from -70 dBm to 0 dBm. Verify at each increment that each corresponding level on the CRT agrees within 0.5 dB.

STEP PROCEDURE

21. 2 dB LOG Cal Linearity

Select 2 dB LOG on 2 dB/10 dB/LIN scale. Recalibrate RF Signal Generator to -10 dBm. Verify a -10 dBm (±0.5 dB) level on the CRT. If necessary, adjust R26156 (2 dB OFFSET) on the Log Amp Module to desired level.

22. Recalibrate RF Signal Generator to 0 dBm. Verify a 0 dBm (±0.5 dB) level on the CRT. If necessary, adjust R26159 (2 dB GAIN) on the Log Amp Module to desired level.

23. Repeat Steps 21 and 22 and verify levels are within 0.5 dB of corresponding inputs.

24. LINEAR

Select LIN on 2 dB/10 dB/LIN scale. Recalibrate RF Signal generator to 0 dBm. Verify the top graticule on the CRT agrees with input. If necessary, adjust R26123 (LINEARITY GAIN ADJUST) on the Log Amp Module to desired level.

25. Disconnect RF Signal Generator. Verify the base line on the CRT is on the bottom graticule. If necessary, adjust R26195 (LINEAR OFFSET) on the Log Amp Module to desired level.

NOTE

R26195 (LINEAR OFFSET) is only installed on Log Amp PC Board 7010-5337-100.

26. Repeat Steps 24 and 25 and verify LIN calibration is within 10%.

27. Repeat 2 dB LOG CAL Linearity (Steps 21 through 23) before Step 28.

28. Set RF Signal Generator to 225 MHz, -10 dBm, and check level with the Power Meter. Reset the following CRT values:

Center Frequency	225.0 MHz
SCAN WIDTH	2 kHz/DIV
RES BW	3 MHz
RF ATTEN	30 dB
IF GAIN	0
2 dB/10 dB/LIN	2 dB

29. Auto Cal OFF Level

Verify trace on CRT is at -10 dB level (± 0.5 dB). If trace is more than 0.5 dB off, restart the calibration procedure from Step 3.

STEP PROCEDURE

30. Auto Cal ON Level

Remove shorting jumper from JTB19001 on the Interface PC Board to enable Auto Cal. Set PWR/OFF/BATT Switch (2) OFF, then back to PWR to cycle the Auto Cal. Verify trace level on CRT of -10 dB. If necessary, adjust R43010 (AUTO CAL LEVEL) in Receive IF Module to desired level. If adjustment was made, set PWR/OFF/BATT Switch (2) OFF, then back to PWR. Repeat this step until trace stays at -10 dB after power cycle.

31. Reset the following CRT values:

Center Frequency	225 MHz
SCAN WIDTH	2 kHz/DIV
RES BW	3 kHz
RF ATTEN	30 dB
IF GAIN	0
FILTERS Menu	none
2 dB/10 dB/LIN	10 dB

32. IF Gain Linearity

Set the RF Signal Generator to 225 MHz at -10 dBm, and check level with Power Meter. Connect RF Signal Generator to ANALYZER INPUT (10) to verify tolerance is met for values shown in Table 4-3. Measure from trace to first graticule down from top.

RF Signal Generator (dBm)	A-7550 IF GAIN (dB)	Tolerance	Actual
-10	0	±2 dB	_____
-20	10	±2 dB	_____
-30	20	±2 dB	_____

Table 4-3 IF GAIN Linearity

33. RF Attenuation Linearity

Select 0 IF GAIN and 0 RF ATTEN. Check RF Signal Generator levels with a Power Meter and make settings as shown in Table 4-4. Measure tolerance from 3rd graticule down from top. If check fails, repair or replace 0-60 dB Input Attenuator.

RF Signal Generator (dBm)	A-7550 RF ATTEN (dB)	Tolerance*	Actual
-60	0	±0.5 dB	_____
-50	10	±0.5 dB	_____
-40	20	±0.5 dB	_____
-30	30	±0.5 dB	_____
-20	40	±1.0 dB	_____
-10	50	±1.0 dB	_____
0	60	±1.5 dB	_____

*Tolerance is cumulative at each stage of the Attenuator up to 1.5 dB total.

Table 4-5 RF Attenuation Linearity

34. Reset the following CRT values:

Center Frequency ..... 500 MHz
SCAN WIDTH ..... 100 MHz/DIV
RES BW ..... 3 MHz
RF ATTEN ..... 30 dB
IF GAIN 0
SWEEP RATE ..... 20 mSec
2 dB/10 dB/LIN ..... 2 dB

35. Sweep Flatness

Step RF Signal generator from 100 kHz to 999 MHz in 50 MHz increments. At each increment, verify a -10 dBm output level with a power meter and then verify A-7550 reads within 2 dB of level.

36. Reset the following CRT values:

SCAN WIDTH ..... 1 kHz/DIV
RES BW ..... 300 kHz
RF ATTEN ..... 30 dB
IF GAIN 0
Center Frequency ..... 100.005 MHz

37. IF Filter Flatness

Set RF Signal Generator to 100.005 MHz at -5 dBm. Connect RF Signal Generator into A-7550 and note, or save, level. Change A-7550 to 100.004 MHz center frequency. Press Slow Scan (-1 step). Verify level is the same (±2 dB), as previously noted. If check fails, repair or replace Receive IF Module.

STEP PROCEDURE

38. Noise Floor

Reset the following CRT values:

Scanwidth	1 kHz/DIV
Center Frequency	225 MHz
RES BW	300 Hz
MODE Menu	Average
RF ATTEN	0 dB
Video Filter	300 Hz

Disconnect RF Signal Generator. Verify the trace baseline on the CRT is lower than -125 dBm by raising IF Gain. When check is complete, return IF Gain to 0.

39. Sidebands

Connect CAL OUT (9) to ANALYZER INPUT (10). Reset the following CRT values:

Center Frequency	100 MHz
SCAN WIDTH	10 kHz/DIV
RES BW	3 kHz

Verify sidebands, at five times the resolution BW, are more than 65 dB below the carrier.

40. Video Filter

Disconnect CAL OUT (9) from ANALYZER INPUT (10). Set RF Signal Generator to 100 MHz at -10 dBm, and check level with a Power Meter. Modulate the Generator signal with a 1 kHz signal to 80% AM.

41. Connect RF Signal Generator into ANALYZER INPUT Connector. Reset the following CRT values:

Center Frequency	100 MHz
SCAN WIDTH	0
RES BW	3 MHz
2 dB/10 dB/LIN	LIN
FILTERS Menu	None
RF ATTEN	30 dB

42. Reset the following CRT value:

FILTERS Menu	300 Hz

Verify an approximate 60% drop in detected modulation. If no drop is detected in the video, repair the 300 Hz filter in the Log Amp Module.

STEP PROCEDURE

43. Base Line Rise

Set RF Signal Generator to 50 MHz at 0 dBm, with no modulation. Reset the following CRT values:

Center Frequency	50 MHz
SCAN WIDTH	1 kHz/DIV
RES BW	300 Hz
RF ATTEN	30 dB
FILTERS Menu	300 Hz

Vary the RF Signal Generator frequency slowly across the 50 MHz point. Verify the base line floor at ±5 kHz is not greater than -70 dBc.

44. Spurious Signal at 100 MHz

Set RF Signal Generator to 100 MHz at 0 dBm. Reset the following CRT values:

Center Frequency	100 MHz
SCAN WIDTH	20 kHz/DIV

Record the level of the spurious signal, if any, about 30 kHz above 100 MHz on the CRT.

45. 75Ω Test

Select 75Ω on the SETUP menu. Verify signal level on the CRT rises 6 dB. When test is complete, select 50Ω on the SETUP menu.

4-8 TRACKING GENERATOR CALIBRATION (OPTION)

PREREQUISITE: RF Control Calibration (paragraph 4-5)
Amplitude Calibration (paragraph 4-6)

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Boonton Modulation Meter
1 Spectrum Analyzer
1 Frequency Counter

FIGURE REFERENCES: Figure 4-13 Composite and Adjustments
Figure 5-24 Generate Module

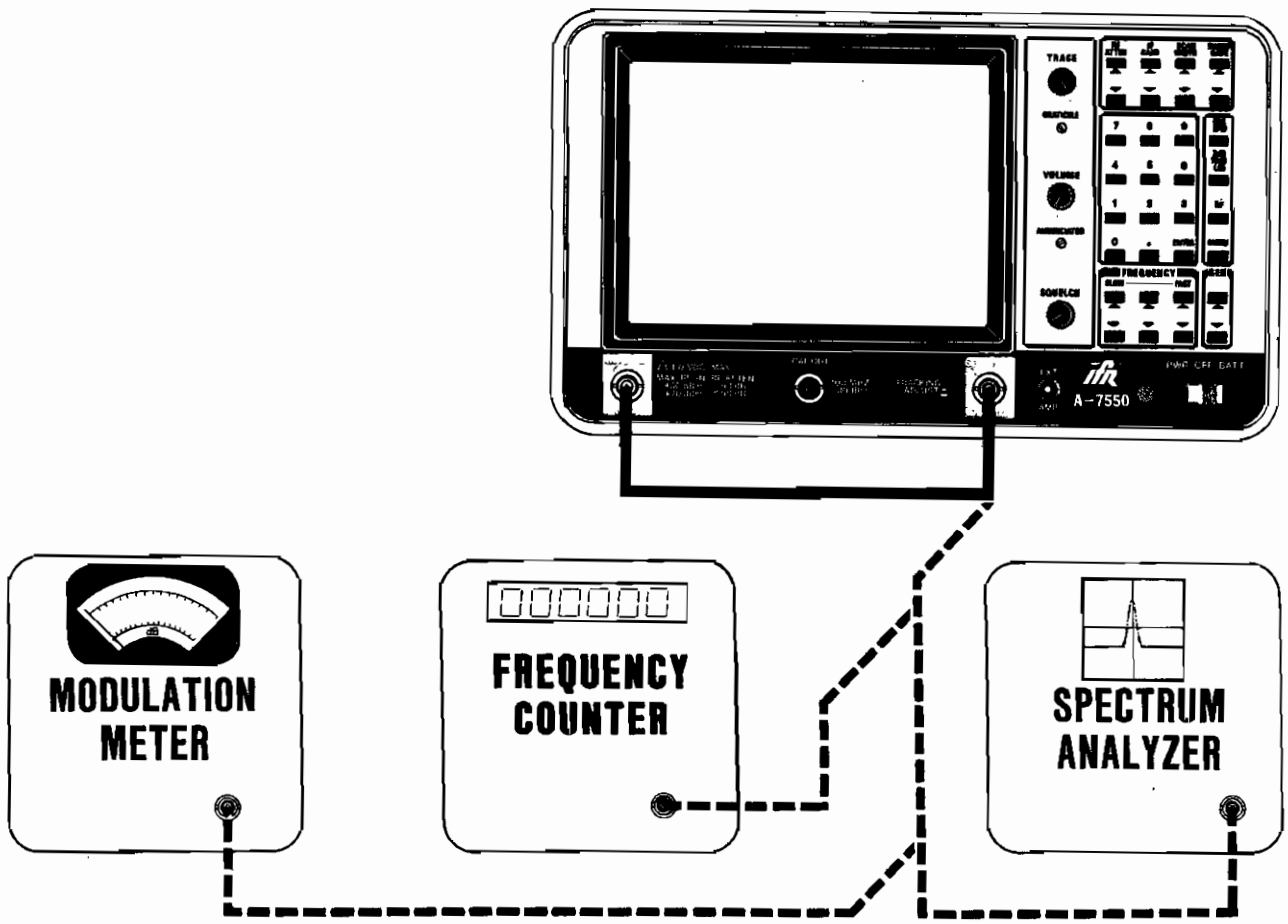


Figure 4-10 Tracking Generator Calibration Test Setup

STEP PROCEDURE

1. Set the following CRT values:

SETUP Menu	5 GEN 1
Center Frequency	1.0000 MHz
SCAN WIDTH	0
GEN	-20 dBm

Using a frequency counter, verify the range of TRACKING ADJUST (8) on the front panel is at least -3 kHz and +6 kHz from the selected RF Frequency. When test is complete, return generate frequency to the selected frequency. Disconnect frequency counter.

2. Reset the following CRT values:

SETUP Menu	GEN 1, 50Ω, dBm
Center Frequency	500 MHz
SCAN WIDTH	100 MHz/DIV
RES BW	3 MHz
RF ATTEN	30 dB
GEN	-10 dB
2 dB/10 dB/LIN	2 dB LOG

3. Connect A-7550, GENERATE OUTPUT (7) to A-7550 ANALYZER INPUT. Verify generate output level on display is centered on -10 dB graticule. If necessary, adjust R51022 (OUTPUT LEVEL ADJ) on Generate Module to desired level.

4. Reset the following CRT values:

RF ATTEN	0 dB
GEN	0 dB

5. Verify 0 dB attenuation. Then, using GEN keys, step output attenuation from 0 to -75 dB. Verify that output level is within 2 dB of each selection. Step output attenuation up to 10 dB (-10 dB Gen Output).

6. Select 75Ω on SETUP menu. Verify IF Gain increases 6 dB and generator display level decreases 6 dB. Select 50Ω on the SETUP menu when test is complete.

7. Connect an external Spectrum Analyzer to the GENERATE OUTPUT (7). Verify that for Generate Output signals at a sweep rate of 2 Sec/Div, harmonics are lower than 20 dBc and non-harmonics are lower than 40 dBc.

8. Reset the following CRT values:

Center Frequency	100 MHz
SCAN WIDTH	0

9. Connect modulation meter to A-7550 GENERATE OUTPUT (7). Verify frequency deviation (Residual FM) <100 Hz (RMS PEAK).

10. External Amp

If the Generate Option is installed, select "Gen 1" in the SETUP menu. Verify voltage on EXT AMP Connector (EXT AC) (6) is +11.7 VDC (±0.2 V).

4-9 10.7 MHz RECEIVER CALIBRATION (OPTION)

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope

1 RF Signal Generator

1 Distortion Analyzer

1 Spectrum Analyzer

FIGURE REFERENCES: Figure 4-13 Composite and Adjustments
Figure 5-25 10.7 MHz Receiver Module

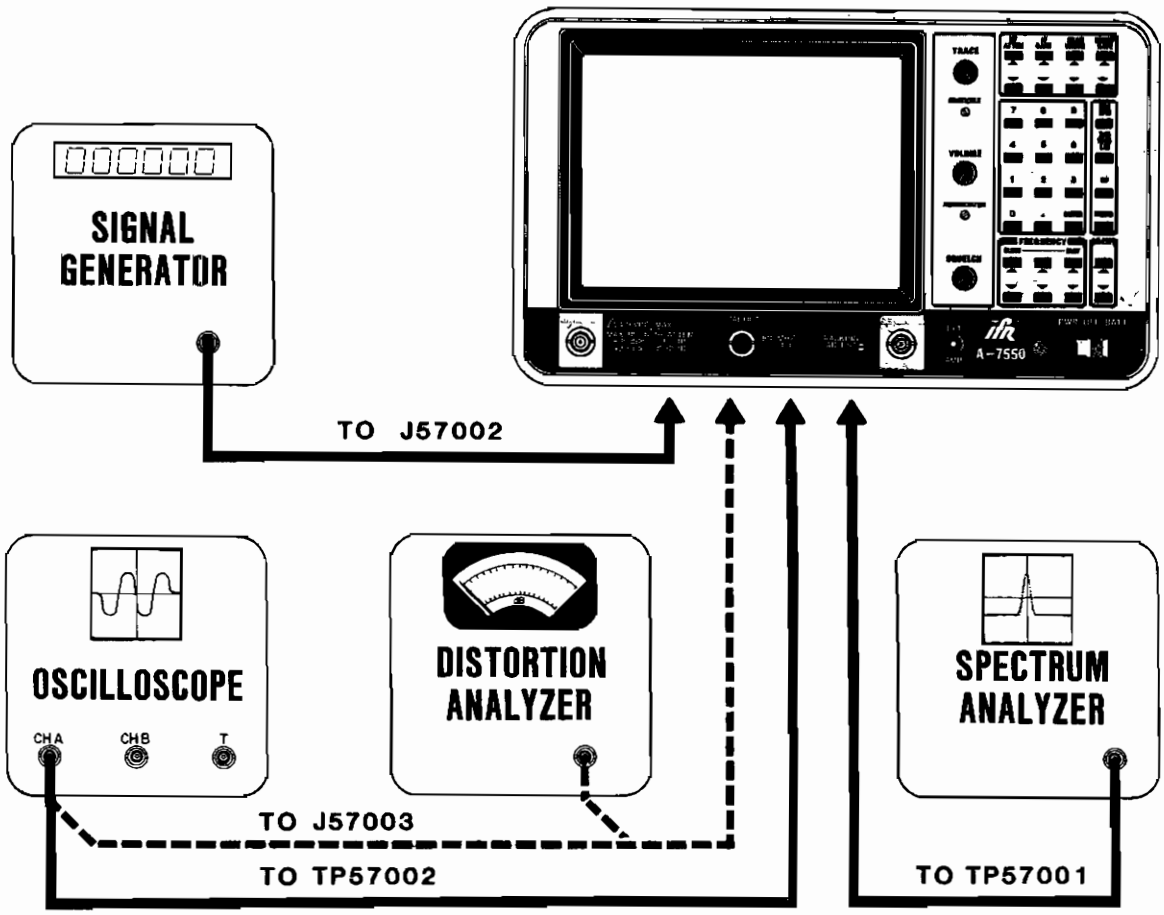


Figure 4-11 10.7 MHz Receiver Calibration Test Setup

STEP PROCEDURE

1. Remove coax cable from 10.7 MHz Receiver and 10.7 MHz Receiver Module from its slot. Remove 10.7 MHz Receiver PC Board from can. Using extender board, reinstall 10.7 MHz Receiver PC Board. Do not connect coaxes.

2. Set the CRT to the following values:

   SCAN WIDTH 0
   RCVR Menu FM2

3. Terminate J57003 on 10.7 MHz Receiver PC Board with a 50Ω termination.

4. Connect RF Signal Generator output, set at 10.7 MHz at -60 dBm, to J57002.

5. Connect external Spectrum Analyzer input to TP57001 on 10.7 MHz Receiver Module. Center external Spectrum Analyzer on 10.7 MHz at 50 kHz/DIV. Adjust 200 kHz bandpass for maximum and best shape using FL58001, FL58003, FL58004 and FL58005.

6. Connect Oscilloscope to TP58002 on 10.7 MHz Receiver PC Board. Adjust FL58006 for maximum AGC as shown on Oscilloscope.

7. Select "FM1" in RCVR menu. Set external Spectrum Analyzer to 5 kHz/DIV. Adjust 15 kHz bandpass for maximum and best shape using C58029, C58030, C58034 and C58035.

8. Select "AM1" in RCVR menu. Set external Spectrum Analyzer to 2 kHz/DIV. Adjust 6 kHz bandpass for maximum and best shape using C58019, C58020, C58024 and C58025. Disconnect external Spectrum Analyzer.

9. Distortion
   Select "FM2" on RCVR menu. Set an RF Signal Generator for 0 dBm and a 1 kHz tone with 50 kHz deviation.

10. Connect the Oscilloscope to pin 23 of P57001. Verify audio is about 6 V peak-to-peak. Disconnect Oscilloscope. Connect Distortion Analyzer to pin 23 of P57001 using the Distortion Meter setting. Verify distortion is less than 0.5%. If necessary, adjust L58019 to lower distortion level.

11. Select "FM1" on RCVR menu. Set RF Signal Generator to 5 kHz deviation. Verify less than 3% distortion.

12. Set RF Signal Generator to 10.7 MHz at -10 dBm with 50% AM. Select "AM1" and then "AM2" on RCVR menu and verify less than 1% distortion for both selections.

13. Sensitivity
    Reset Distortion Analyzer to SINAD setting. Set RF Signal Generator to 10.7 MHz at -10 dBm with 5 kHz deviation. Select "FM1" on RCVR menu. Verify 10 dB SINAD is typically -71 dBm or less. Disconnect Distortion Analyzer.

STEP	PROCEDURE

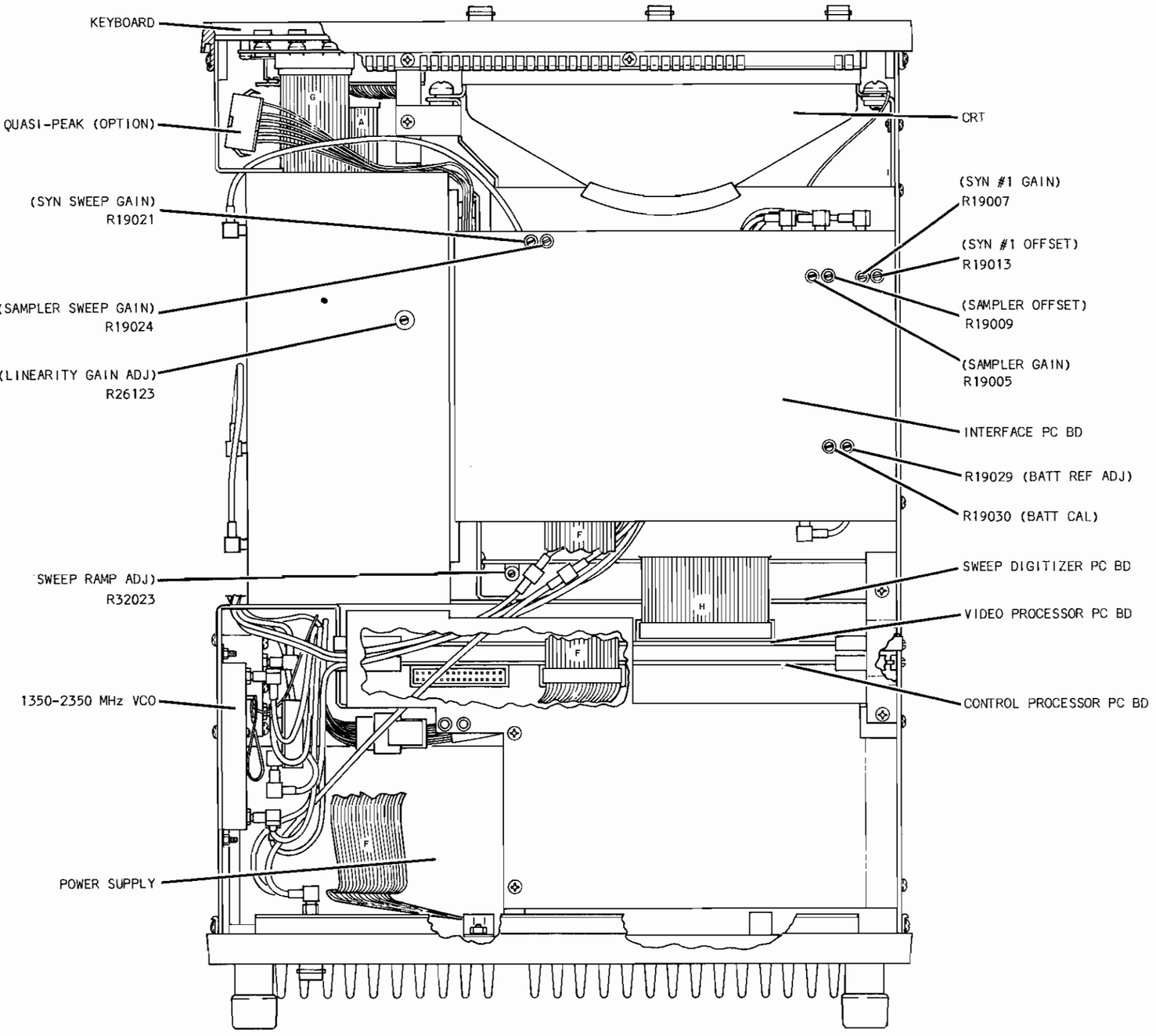
14. SSB Injection
Select "SSB" on RCVR menu. Set RF Signal Generator to 10.7 MHz at -70 dBm with no modulation. Connect Oscilloscope to pin 23 of P57001. Adjust R58077 (SSB INJECTION LEVEL) for a 1 V peak-to-peak beat-frequency level.

15. Squelch
Rotate SQUELCH Control (5) on A-7550 and verify audio switches on and off.

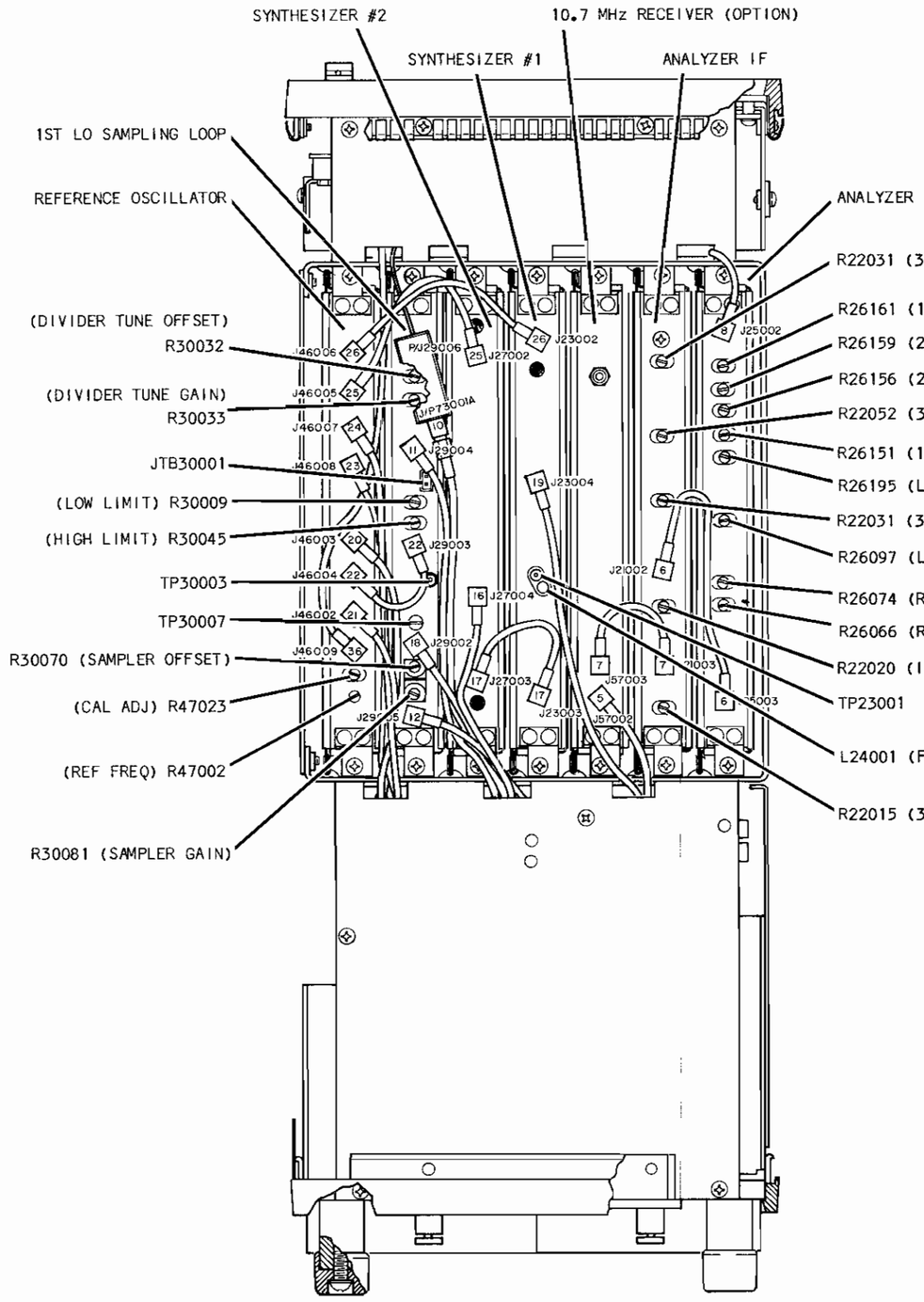
16. Audio Blanking
Select "TSR" on RCVR menu and verify audio switches on and off when SCANWIDTH is >0 kHz/DIV. Turn off TSR on RCVR menu when finished with test.

4-10 QUASI-PEAK FILTER CALIBRATION (OPTION)

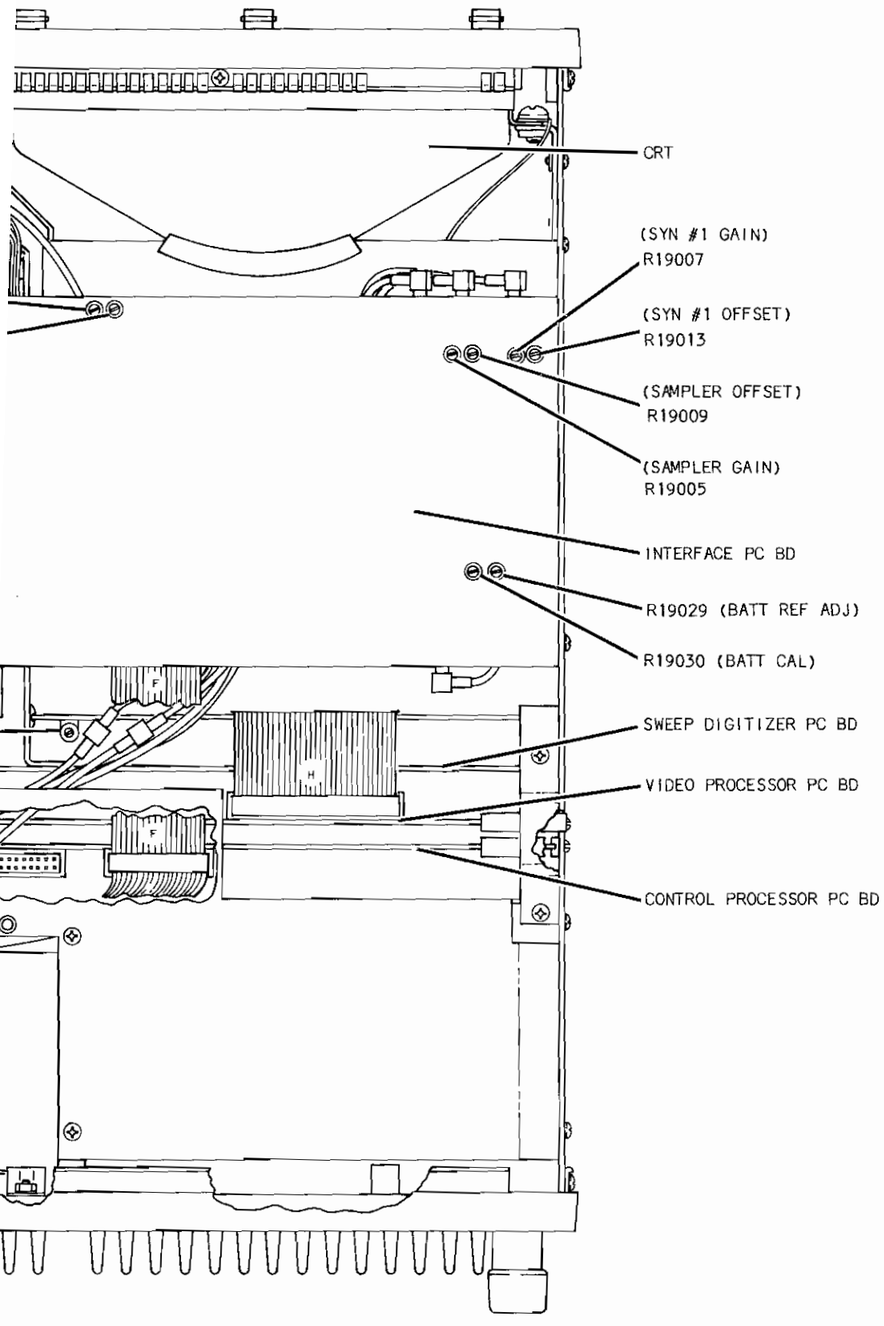
(To Be Supplied)



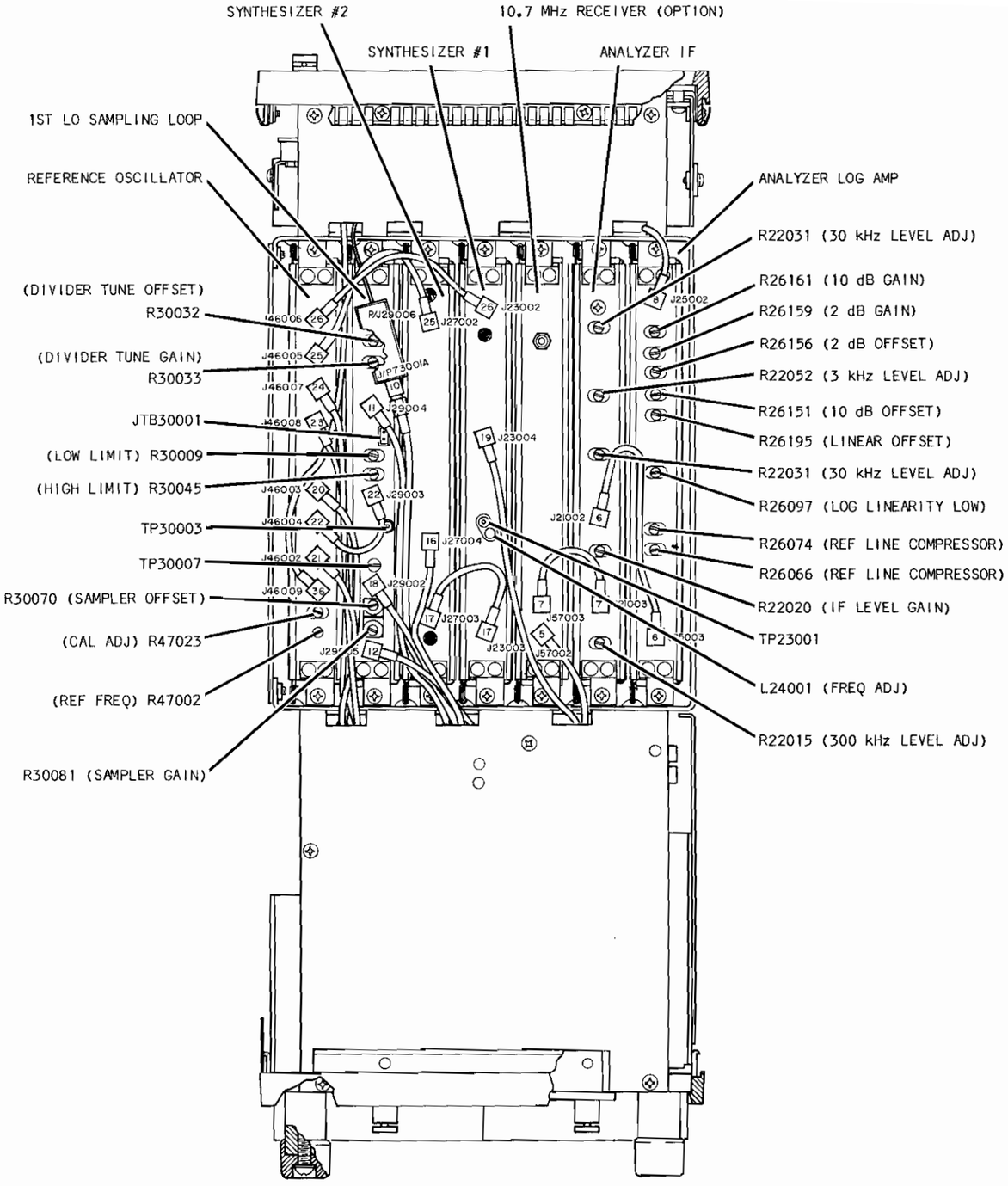
TOP VIEW



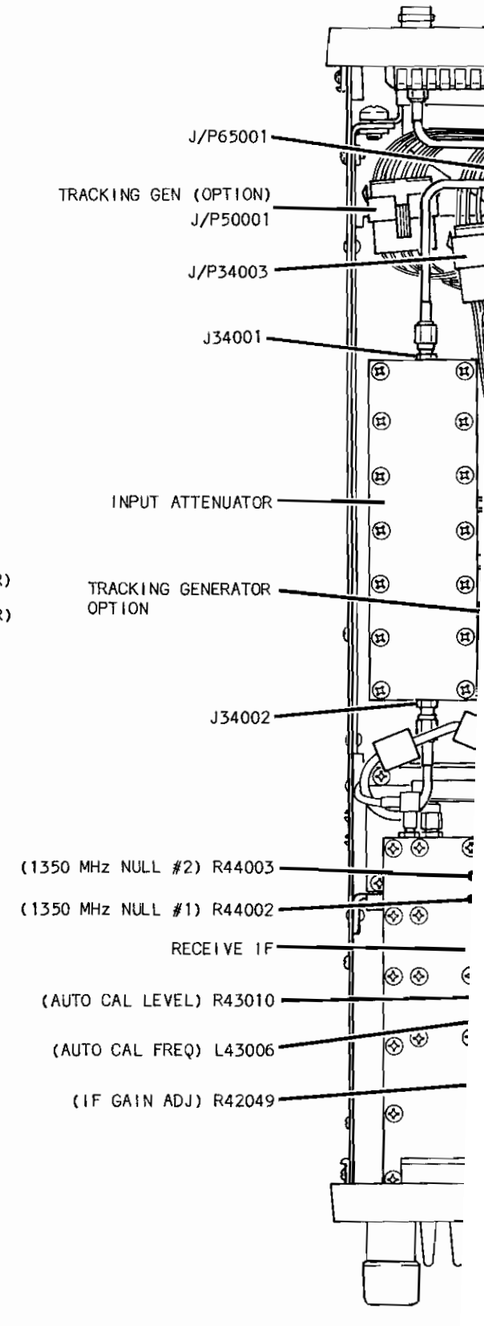
RIGHT SIDE VIEW



TOP VIEW



RIGHT SIDE VIEW



EL ADJ)

)

T)

L ADJ)

ET)

SET)

EL ADJ)

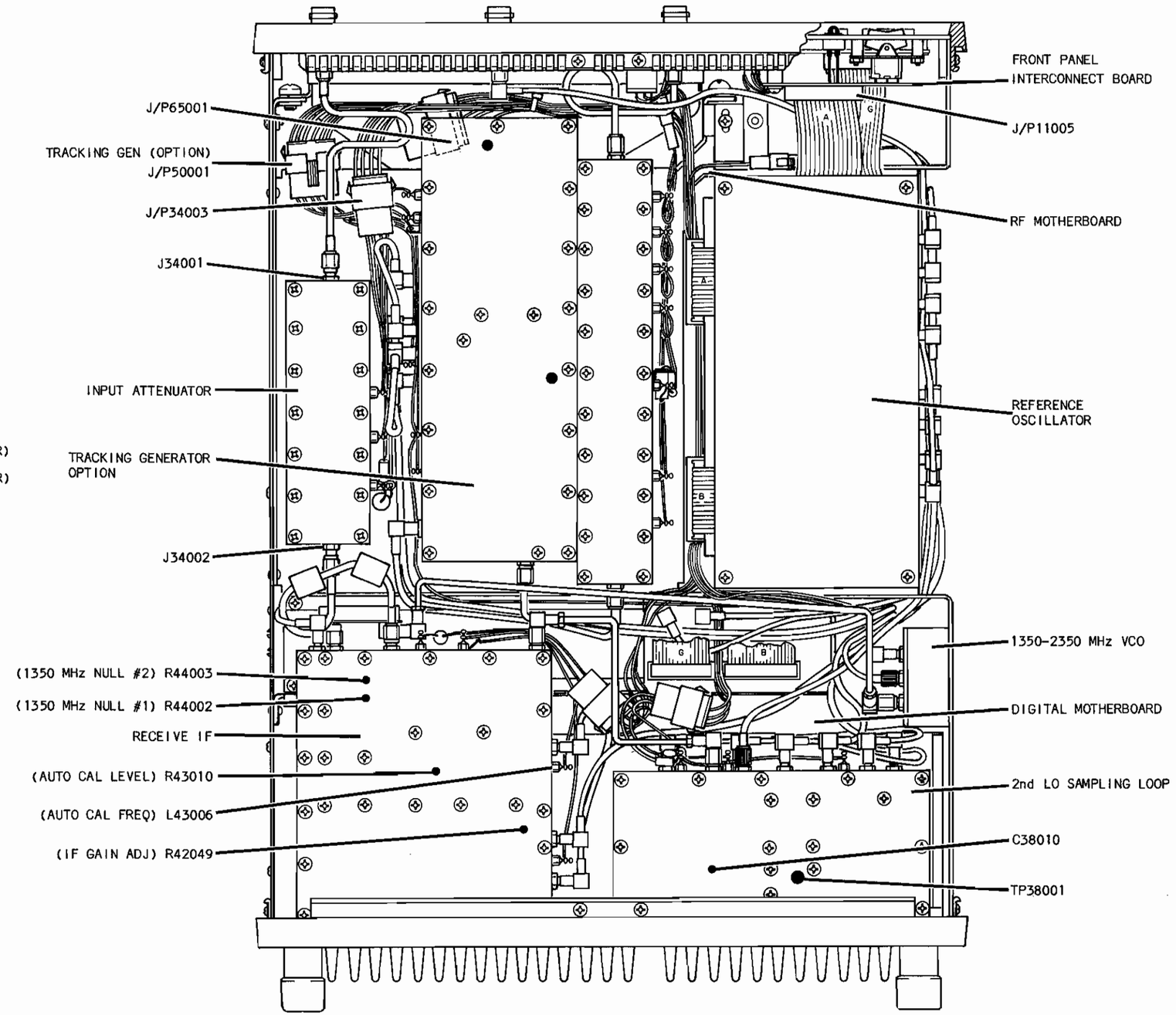
ITY LOW)

OMPRESSOR)

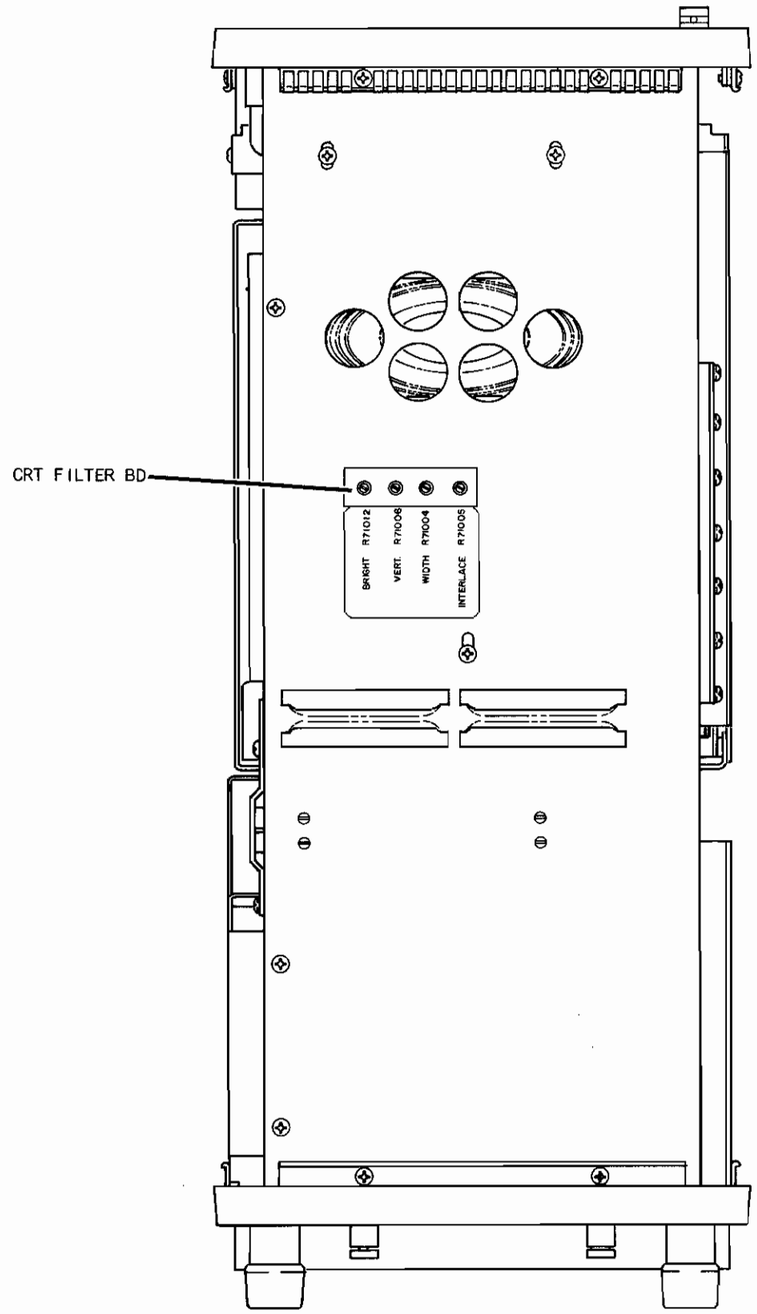
OMPRESSOR)

AIN)

VEL ADJ)



BOTTOM VIEW



LEFT SIDE VIEW

Figure 4-13 Composite and Adjustments

SECTION 5 - TECHNICAL DATA

5-1 GENERAL

This section contains mechanical assemblies, PC Board layouts and schematics for all modules in the A-7550. The data sheets are approximately sequenced in the order of discussion in Section 2 (Theory of Operation).* An index of all data sheets is contained in paragraph 5-3.

5-2 HOW TO USE SCHEMATICS

To trace coaxial cable conductors from one schematic to another, follow the procedures outlined in paragraph 5-2-1. To trace conductors for multiple pin connectors, refer to paragraph 5-2-2.

5-2-1 COAXIAL CABLES

A. Locate desired module on the Interconnect Diagram (Figure 5-2).

B. Locate the desired coaxial cable on Interconnect Diagram. (Coaxial connectors are identified by reference designators and by a circled number which corresponds to a physically affixed tag on the coaxial cable.)

C. Follow coaxial cable on Interconnect Drawing to locate opposite end of connector. Note module reference designator on destination end of coaxial cable.

D. Locate schematic of desired module or index of technical data in paragraph 5-3.

E. Locate reference designator of coaxial connector and continue tracing circuit.

5-2-2 MULTIPLE PIN CONNECTORS

A. Locate desired module on Interconnect Diagram (Figure 5-2).

B. Locate desired multiple pin connector on Interconnect Diagram. Note reference designator of the mating connector.

C. Note module or wire harness on which the connector is mounted or grouped.

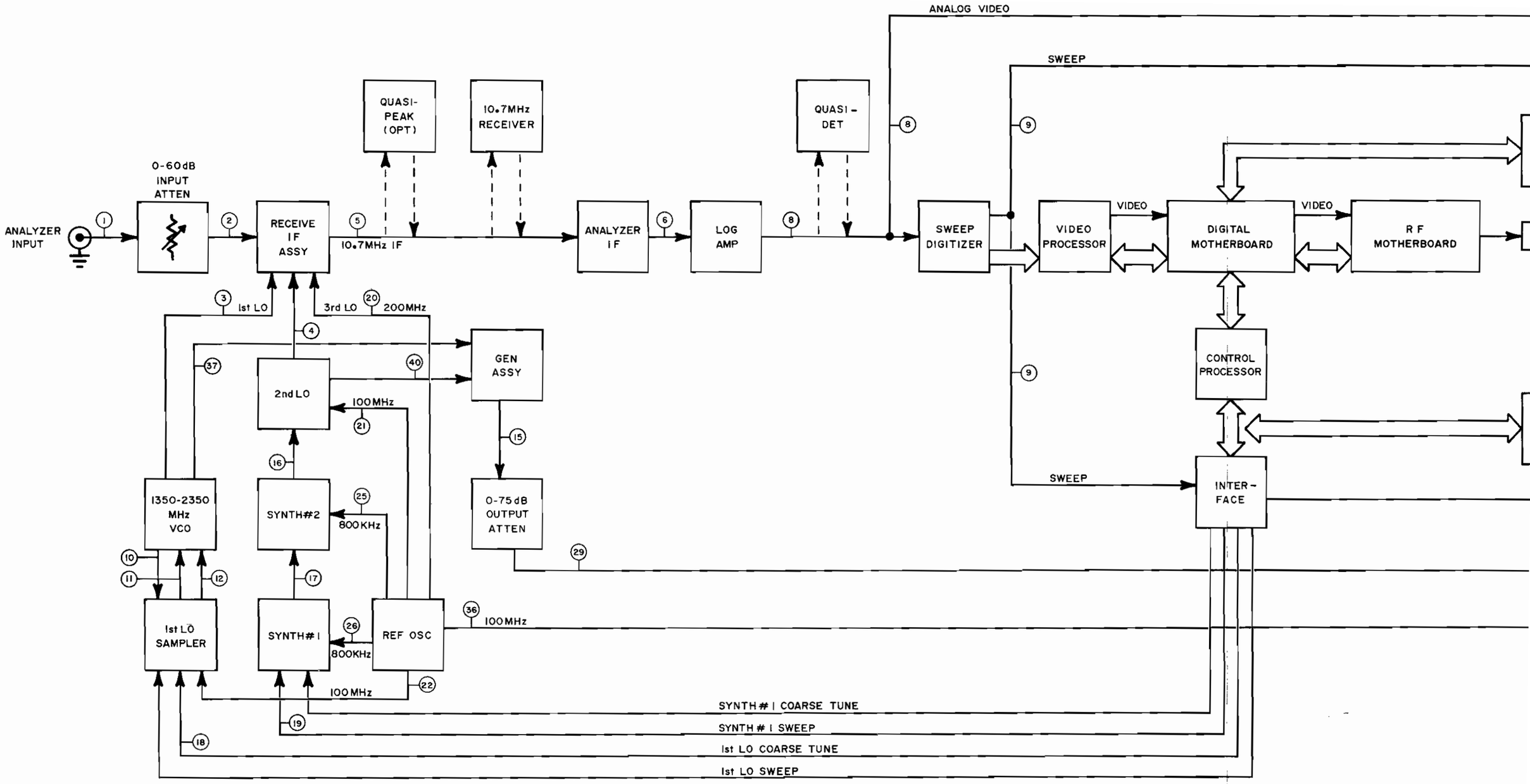
D. Locate schematic of desired module on index of technical data in paragraph 5-3.

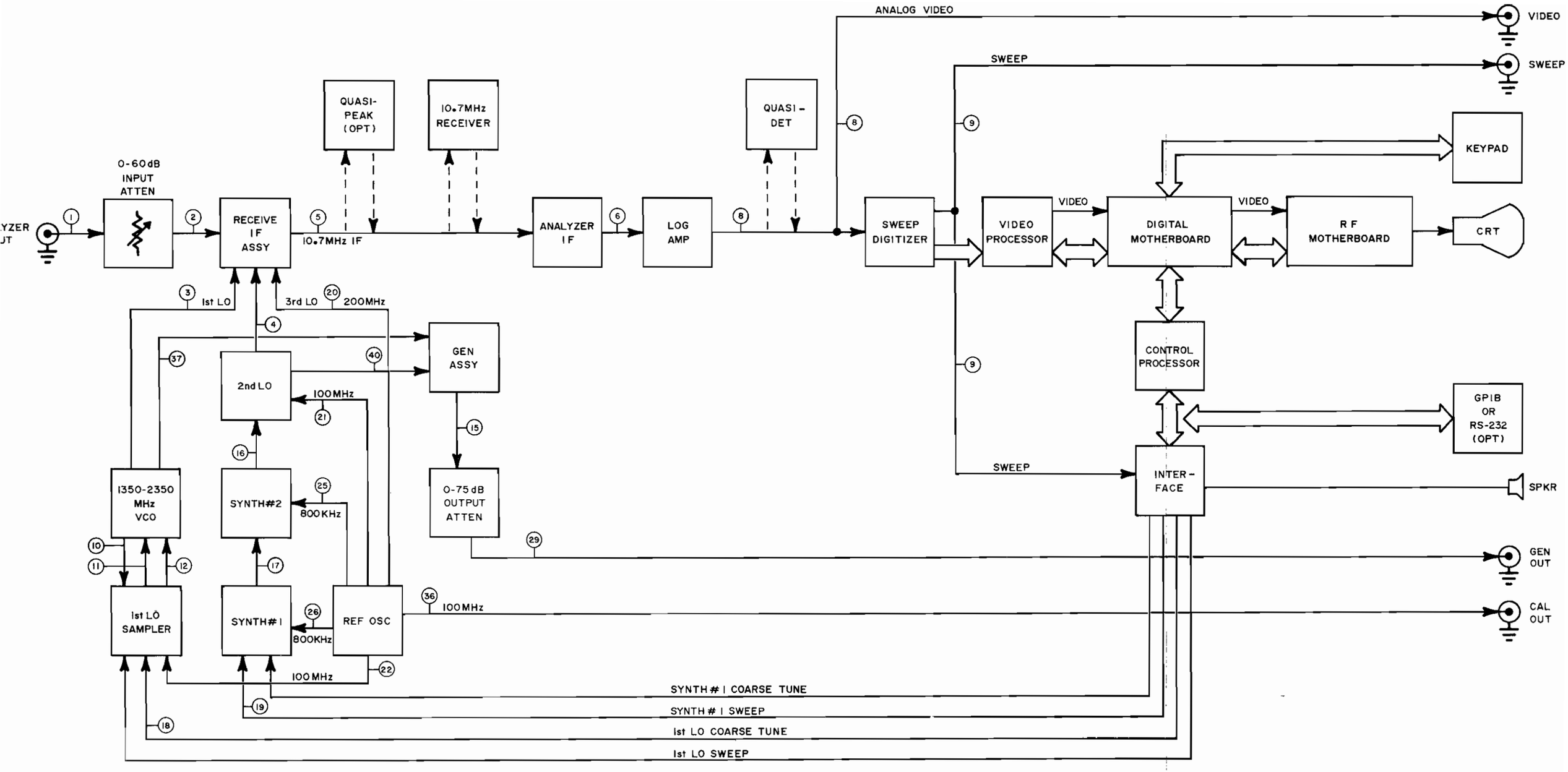
* Several multiple page data sheets may be sequenced out of order. Also, data sheets for optional modules are sequenced numerically after all standard modules.

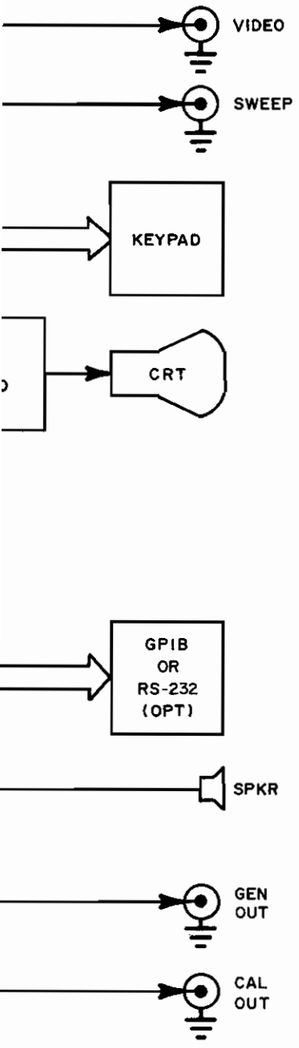
E. Using module schematic, locate reference designator of connector and corresponding pin number. Continue tracing circuit.

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ANALOG VIDEO
SWEEP
QUASI-PEAK (OPT)
10.7MHz RECEIVER
QUASI-DET
0-60dB INPUT ATTEN
ANALYZER INPUT
RECEIVE IF ASSY
10.7MHz IF
ANALYZER IF
LOG AMP
SWEEP DIGITIZER
VIDEO PROCESSOR
VIDEO
DIGITAL MOTHERBOARD
R F MOTHERBOARD
CONTROL PROCESSOR
INTER-FACE
1st LO
3rd LO
200MHz
GEN ASSY
2nd LO
100MHz
1350-2350 MHz VCO
SYNTH#2
800KHz
0-75dB OUTPUT ATTEN
1st LO SAMPLER
SYNTH#1
REF OSC
SYNTH # 1 COARSE TUNE
SYNTH # 1 SWEEP
1st LO COARSE TUNE
1st LO SWEEP


ANALOG VIDEO
VIDEO
SWEEP
SWEEP
QUASI-
PEAK
(OPT)
10.7MHz
RECEIVER
QUASI-
DET
0-60dB
INPUT
ATTEN
RECEIVE
IF
ASSY
10.7MHz IF
ANALYZER
IF
LOG
AMP
SWEEP
DIGITIZER
VIDEO
PROCESSOR
VIDEO
DIGITAL
MOTHERBOARD
VIDEO
R F
MOTHERBOARD
KEYPAD
CRT
1st LO
3rd LO
200MHz
GEN
ASSY
2nd LO
100MHz
CONTROL
PROCESSOR
GPIB
OR
RS-232
(OPT)
1350-2350
MHz
VCO
SYNTH#2
800KHz
0-75dB
OUTPUT
ATTEN
SWEEP
INTER-
FACE
SPKR
GEN
OUT
1st LO
SAMPLER
SYNTH#1
800KHz
REF OSC
100MHz
CAL
OUT
100MHz
SYNTH#1 COARSE TUNE
SYNTH#1 SWEEP
1st LO COARSE TUNE
1st LO SWEEP



COAX	ITEM	DPN	FROM	TO	SIGNAL	LEVEL
1	45	6042-5382-500	J11001/J11006 (FRONT PANEL)	J34001 (0-60 dB ATTENUATOR)	100 kHz to 1 GHz	-120 to 30 dBm
2	46	6042-5382-600	J34002 (0-60 dB ATTENUATOR)	J41003 (REC IF)	100 kHz to 1 GHZ	-120 to 30 dBm
3	47	6042-5383-600	J39003 (VCO)	J73001B (REC IF *VIA BUFFER AMP*)	1350 to 2350 MHz	+5 dBm
4	48	6042-5383-500	J36006 (2ND LO)	J41002 (REC IF)	1100.7 to 1160.7 MHz	+5 dBm
5	49	6050-0041-450	J41008 (REC IF)	J21003 (ANAL IF) OR J57002 (OPTION #4 10.7 MHz REC)	10.7 MHz	0 dBm REF
# 6	50	6050-0040-300	J21002 (ANAL IF)	J25003 (ANAL. LOG AMP)	10.7 MHz	0 dBm REF
* 7	*	6050-0040-250	J57003 (10.7 MHz REC) OPTION #4	J21003 (ANAL. IF)	10.7 MHz	0 dBM REF
8	51	6050-9900-401	J25002 (LOG AMP)	J32003 & J10003/J10005 (SWEEP DIGITIZER/R PANEL) (ANALOG VIDEO OUT)	VIDEO	0-.8V (VALID VIDEO)
9	52	6050-9900-402	J32002 (SWEEP DIGITIZER)	J19005 & J10001/J10004 (INTERFACE/REAR PANEL (SWEEP OUT))	SWEEP (RAMP)	+5 V 50 mS
10	53	6055-0040-800	J39002 (VCO)	J73001A (1ST LO SAMPLING LOOP) VIA BUFFER AMP	1350 TO 2350 MHz	+5 dBm
11	54	6050-0040-950	J78001 (1ST LO SAMPLING LOOP	J78001 (VCO) - VIA VCO FILTER	SLOW TUNE	0 - 20 VDC
12	55	6050-0040-500	J29005 (1ST LO SAMPLING LOOP	J39004 (VCO)	FAST TUNE	0 - 5 VDC
*15	*	6042-5382-700	J50008 (GEN ASSY) OPTION #2	J48001 (OUTPUT ATTEN) OPTION #2	0-1000 MHz	0 dBm
16	56	6050-0040-750	J27004 (SYNTH #2)	J36002 (2ND LO)	100.7 TO 160.7 MHz	+5 dBm
17	57	6050-0040-200	J23003 (SYNTH #1)	J27003 (SYNTH #2)	.2 to 3.099 MHz	TTL
18	58	6050-0041-920	J19006 (INTERFACE)	J29002 (1ST LO SAMPLING LOOP)	COARSE TUNE	0 - 5 VDC
19	59	6050-0041-920	J19007 (INTERFACE)	J23004 (SYNTH #1)	COARSE TUNE	0 - 2.5 VDC
20	60	6050-0041-550	J46003 (REF OSC)	J41007 (REC IF)	200 MHz	+5 dBm
21	66	6050-0040-700	J46002 (REF OSC)	J36004 (2ND LO)	100 MHz	+5 dBm
22	57	6050-0040-200	J46004 (REF OSC)	J29003 (1ST LO SAMPLING LOOP)	100 MHz	+5 dBm
23	54	6050-0040-950	J46008 (REF OSC)	J14004 (DIGITAL MOTHER BOARD)	12.5 MHz	TTL
24	54	6050-0040-950	J46007 (REF OSC)	J14003 (DIGITAL MOTHER BOARD)	5 MHz	TTL
25	61	6050-0040-250	J46005 (REF OSC)	J27002 (SYNTH #2)	800 kHz	TTL
26	62	6050-0040-350	J46006 (REF OSC)	J23002 (SYNTH #1)	800 kHz	TTL
27	REF	6050-0040-550	J36008 (2ND LO)	J36009 (2ND LO)	100.7 TO 160.7 MHz	-19 dBm
28	REF	6050-1050-850	J19008 (INTERFACE)	SPEAKER (CRT ASSY)	DEMOD AUDIO	
*29	*	6042-5382-600	J48002 (OUTPUT ATTEN.)	J11002/J11007 (FRONT PNL) (GEN OUT)	0 - 1000 MHz	-60 to 0 dBm
*30	*	6050-0040-950	J21002 (ANALYZER IF)	J62002 (QUASI-PEAK FILT.) OPTION #8	10.7 MHz	0 dBm REF
*31	*	6050-0041-220	J62003 (QUASI-PEAK FILT) OPTION #8	J25003 (LOG AMP)	10.7 MHz	0 dBm REF
32	REF	6050-0040-250	J50002 (GEN ASSY) OPTION #2	J50003 (GEN ASSY) OPTION #2	189.3 MHz	-20 dBm
33	REF	6050-0040-250	J50006 (GEN ASSY) OPTION #2	J50005 (GEN ASSY) OPTION #2	0 - 1000 MHz	-30 dBm
34	REF	6050-0040-450	J41005 (REC IF)	J41006 (REC IF)	189.3 MHz	INPUT @ J41003
35	REF	6050-0040-250	J36005 (2ND LO)	J36003 (2ND LO)	1100.7 TO 1160.7 MHz	+5 dBm
36	63	6050-0561-300	J49009 (REF OSC)	J11003/J11008 (FRT PNL) CAL OUTPUT	100 MHz	-30 dBm
*37	*	6050-0050-925	J39005 (VCO)	J6801A (OUTPUT BUFFER) OPTION #2	1350 TO 2350 MHz	+5 dBm
*38	*	6050-0041-600	J6802A (OUTPUT BUFFER) OPTION #2	J50007 (GEN ASSY) OPTION #2	1350 TO 2350 MHz	+5 dBm
*39	*	6050-0042-020	J6802B (OUTPUT BUFFER) OPTION #2	J50004 (GEN ASSY) OPTION #2	1100.7 TO 1160.7 MHz	+5 dBm
*40	*	6050-0051-250	J36007 (2ND LO)	J6801B (OUTPUT BUFFER) OPTION #2	1100.7 TO 1160.7 MHz	+5 dBm

#COAX NOT USED IF QUASI-PEAK FILTER IS INSTALLED

*COAX USED IF OPTION IS INSTALLED.

Figure 5-1 A-7550 System Block Diagram With Coax Numbers and Signal Flow

LO SAMPLING LOOP
0000-5314-600
(29000)

SYNTHESIZER #1
0000-5313-500
(23000)

SYNTHESIZER #2
0000-5313-300
(27000)

REFERENCE OSCILLATOR
0000-5311-300
(46000)

ANALYZER IF
0000-5317-000
(21000)

ANALYZER LOG AMP
0000-5314-100
(25000)

10.7 MHz RECEIVER
0000-5310-600
(57000)

P29001 J29001
P23001 J23001
P27001 J27001
P46001 J46001
P21001 J21001
P25001 J25001
P57001 J57001

RF MOTHERBOARD/WIRE HARNESS
0000-5315-300
(33000)

J19002 P19002
J33001
J33005

INTERFACE
0000-5315-200
(19000)

J19001 P19001

P34003 J34003
P48003 J48003
P50001 J50001
P73002A J73002A

INPUT ATTENUATOR
0000-5310-100
(34000)

OUTPUT ATTENUATOR
0000-5310-201
(48000)

GENERATOR BLOCK
0000-5311-000
(50000)

FL50004

RED

FL6901A

OUTPUT BUFFER
0000-5016-801
(6900A)

BUFFER AMP
0000-5315-500
(73000A)

P/O 6045-5381-900

SWEEP DIGITIZER
0000-5314-300
(32000)

J32001 P32001

6045-5382-100

P11005 J11005

FRONT PANEL
0000-5312-200
(11000)

KEYBOARD
0000-5311-200
(12000)

J12001 P12001

6045-5382-200

P36001 J36001
P41001 J41001
P39006 J39006

259 LO SUMMING LOOP
0000-5314-800
(36000)

RECEIVE IF
0000-5312-300
(41000)

1350-2350 MHz VCO
0000-5315-600
(39000)

RED

FL69018

OUTPUT BUFFER
0000-5016-800
(6900B)

P/O 6045-5381-900

P20002 J20002
J20003

CONTROL PROCESSOR
0000-5316-600
(20000)

P31001 J31001

VIDEO PROCESSOR
0000-5316-500
(31000)

P20001 J20001
P14002 J14002
P31002 J31002
P14001 J14001

DIGITAL MOTHERBOARD
0000-5314-000
(14000)

P62001 J62001
P65001 J65001
P15003 J15003

QUASI-PEAK FILTER
0000-5311-800
(62000)

CRT MODULE
0000-5314-900
(65000)

BATTERY
(59000)

POWER SUPPLY
0000-5313-400
(15000)

J15001
J15002
J15004 P15004

REAR PANEL

J10002

SEE DETAILS A & B

P56001 J56001

GPIB INTERFACE
0000-5312-700
(56000)

J56002

DETAIL A

P55001 J55001

RS-232 INTERFACE
0000-5312-500
(55000)

J55002

DETAIL B

SWEEP DIGITIZER
0000-5314-300
(32000)

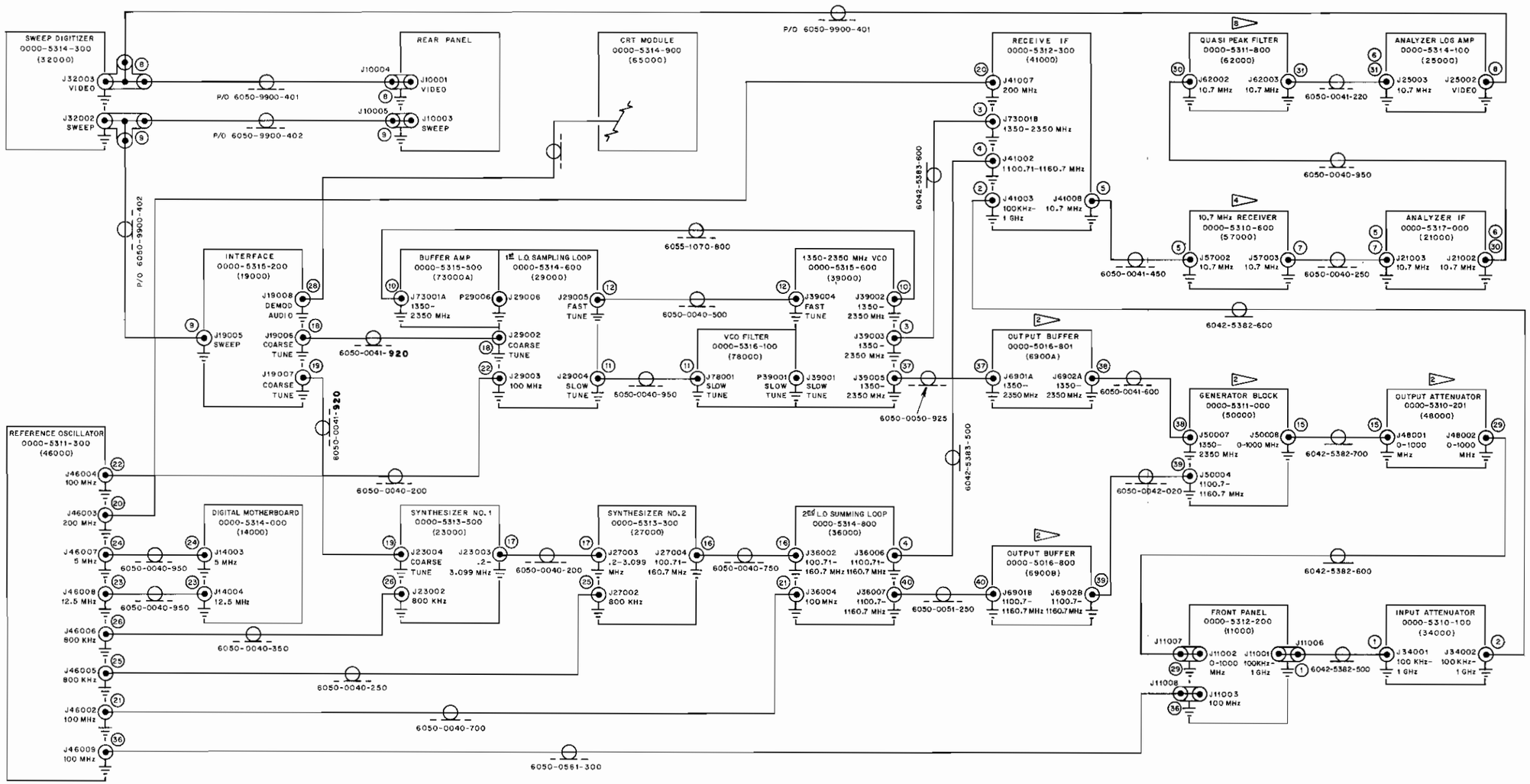
J32003 VIDEO
J32002 SWEEP

P/O 6050-9900-402

REFERENCE OSCILLATOR
0000-5311-300
(46000)

J46004 100 MHz
J46003 200 MHz
J46007 5 MHz
J46008 12.5 MHz
J46006 800 KHz
J46005 800 KHz
J46002 100 MHz
J46009 100 MHz

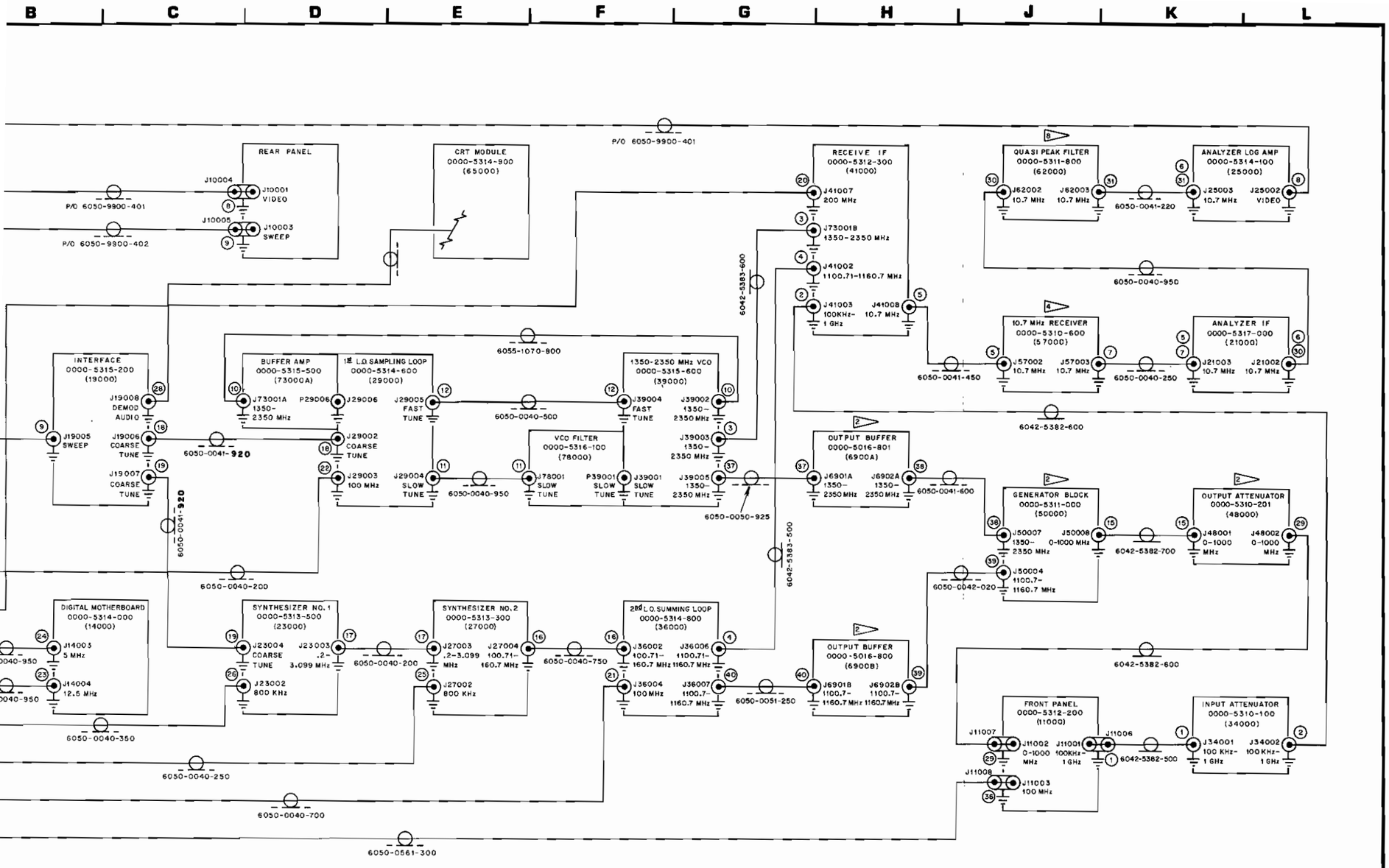
6050-9900-401



NOTE

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9.

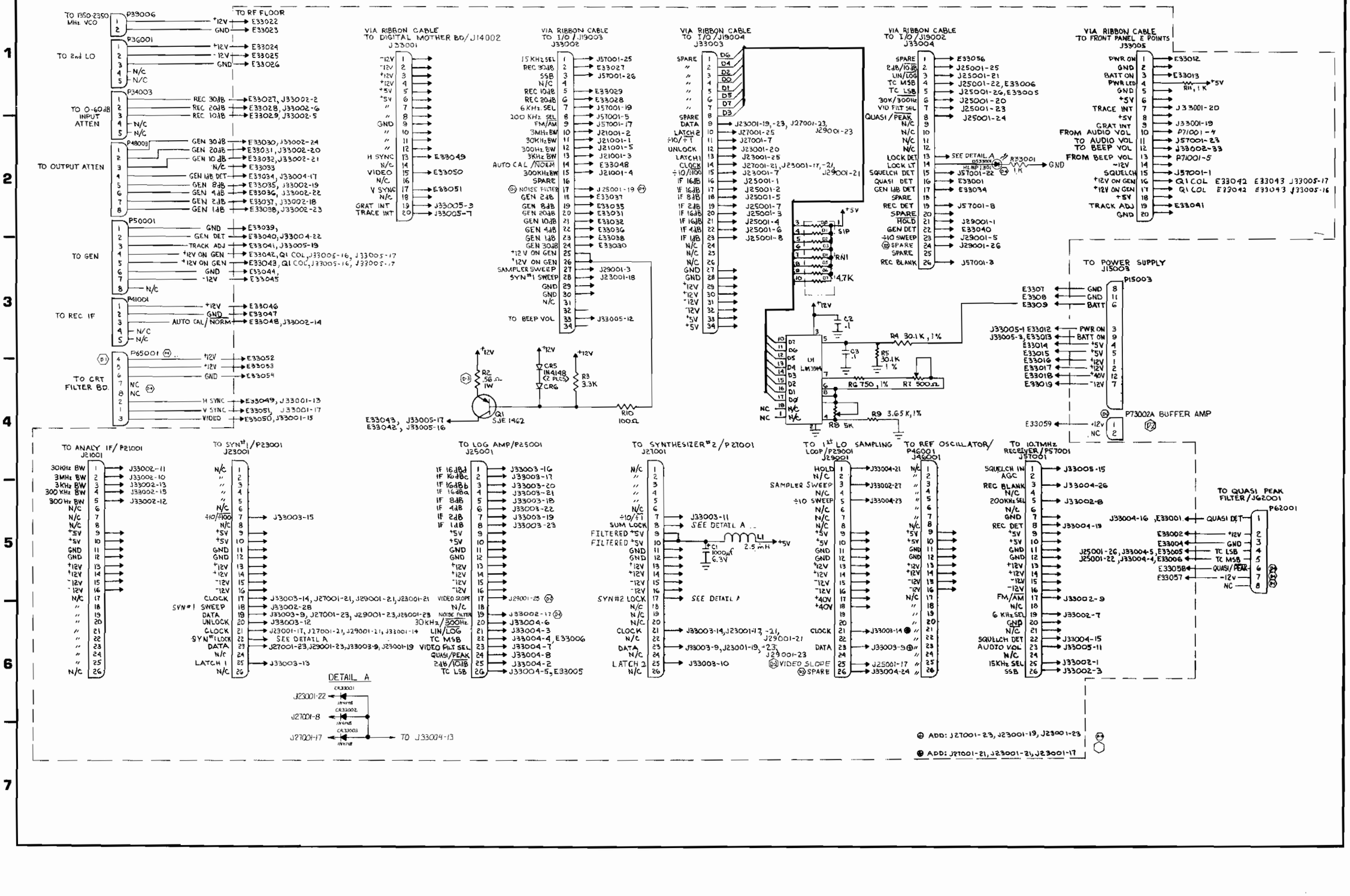
Figure 5-2 Intercor
(D-0000-

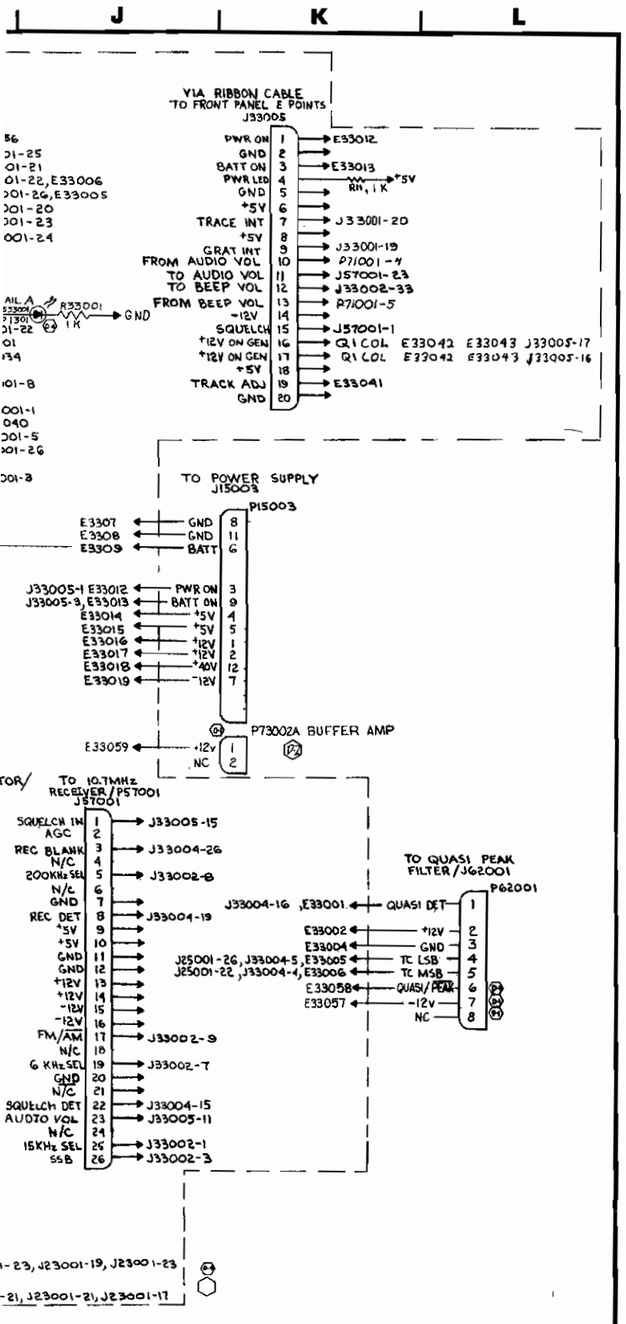


NOTES:

1. OPTION (1): RECHARGEABLE BATTERY.
2. OPTION (2): TRACKING GENERATOR (INCLUDES GEN. BLOCK, OUTPUT ATTENUATOR, TWO OUTPUT BUFFERS, COAX CABLES AND ATTACHING PARTS).
3. OPTION (5) OR OPTION (6) MAY BE INSTALLED, BUT NOT ON THE SAME UNIT.
4. OPTION (4): 10.7 MHz RECEIVER. (IF THIS OPTION IS NOT INSTALLED, USE COAX NO. 5, D/P/N 6050-0041-450 BETWEEN J41008 AND J21003.)
5. OPTION (5): GPIB INTERFACE PC BD.
6. OPTION (6): RS-232 INTERFACE PC BD.
7. J10002 BECOMES P56001 WHEN GPIB IS INSTALLED OR P55001 WHEN RS-232 IS INSTALLED.
8. OPTION (8): QUASI-PEAK FILTER. (IF THIS OPTION IS NOT INSTALLED, USE COAX NO. 6, D/P/N 6050-0040-300 IN PLACE OF COAXES 30 AND 31 BETWEEN J25003 AND J21002.)
9. PART OF MOTHERBOARD/WIRE HARN, (SEE 0000-5315-300).

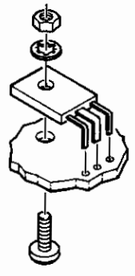
Figure 5-2 Interconnect Diagram (D-0000-5310-000-W)


TO RF FLOOR
P33006
TO 1350-2350 MHz VCO
+12V → E33022
GND → E33023
P36001
TO 2nd LO
+12V → E33024
-12V → E33025
GND → E33026
N/C
P34003
TO 0-60dB INPUT ATTEN
REC 30dB → E33027, J33002-2
REC 20dB → E33028, J33002-6
REC 10dB → E33029, J33002-5
P48003
TO OUTPUT ATTEN
GEN 30dB → E33030, J33002-24
GEN 20dB → E33031, J33002-20
GEN 10dB → E33032, J33002-21
N/C → E33033
GEN 1dB DET → E33034, J33004-17
GEN 8dB → E33035, J33002-19
GEN 4dB → E33036, J33002-22
GEN 2dB → E33037, J33002-18
GEN 1dB → E33038, J33002-23
P50001
TO GEN
GND → E33039,
GEN DET → E33040, J33004-22
TRACK ADJ → E33041, J33005-19
+12V ON GEN → E33042, Q1 COL, J33005-16, J33005-17
+12V ON GEN → E33043, Q1 COL, J33005-16, J33005-17
GND → E33044,
-12V → E33045
P41001
TO REC IF
+12V → E33046
GND → E33047
AUTO CAL/NORM → E33048, J33002-14
P65001
TO CRT FILTER BD.
+12V → E33052
+12V → E33053
GND → E33054
H SYNC → E33049, J33001-13
V SYNC → E33051, J33001-17
VIDEO → E33050, J33001-15
VIA RIBBON CABLE TO DIGITAL MOTHER BD/J14002 J33001
-12V 1
-12V 2
+12V 3
+12V 4
+5V 5
+5V 6
" 7
" 8
GND 9
" 10
" 11
" 12
H SYNC 13 → E33049
N/C 14
VIDEO 15 → E33050
N/C
V SYNC 17 → E33051
N/C 18
GRAT INT 19 → J33005-3
TRACE INT 20 → J33005-7
VIA RIBBON CABLE TO I/O J19003 J33002
15 KHz SEL 1 → J57001-25
REC 30dB 2 → E33027
SSB 3 → J57001-26
N/C 4
REC 10dB 5 → E33029
REC 20dB 6 → E33028
6 KHz SEL 7 → J57001-19
200 KHz SEL 8 → J57001-5
FM/AM 9 → J57001-17
3MHz BW 10 → J21001-2
30KHz BW 11 → J21001-1
300Hz BW 12 → J21001-5
3KHz BW 13 → J21001-3
AUTO CAL/NORM 14 → E33048
300KHz BW 15 → J21001-4
SPARE 16
NOISE FILTER 17 → J25001-19
GEN 2dB 18 → E33037
GEN 8dB 19 → E33035
GEN 20dB 20 → E33031
GEN 10dB 21 → E33032
GEN 4dB 22 → E33036
GEN 1dB 23 → E33038
GEN 30dB 24 → E33030
+12 V ON GEN 25
+12V ON GEN 26
SAMPLER SWEEP 27 → J29001-3
SYN#1 SWEEP 28 → J23001-18
GND 29
GND 30
N/C 31
32
TO BEEP VOL 33 → J33005-12
34
VIA RIBBON CABLE TO I/O J19004 J33003
SPARE 1 D6
" 2 D4
" 3 D2
" 4 D0
" 5 D1
" 6 D5
" 7 D7
" 8 D3
SPARE DATA 9 → J23001-19, -23, J27001-23, J29001-23
LATCH 2 10 → J27001-25
÷10/÷1 11 → J27001-7
UNLOCK 12 → J23001-20
LATCH 1 13 → J23001-25
CLOCK 14 → J27001-21, J23001-17, -21, J29001-21
÷10/100 15 → J23001-7
IF 16dB 16 → J25001-1
IF 16dB 17 → J25001-2
IF 8dB 18 → J25001-5
IF 2dB 19 → J25001-7
IF 16dB 20 → J25001-3
IF 16dB 21 → J25001-4
IF 4dB 22 → J25001-6
IF 1dB 23 → J25001-8
N/C 24
N/C 25
N/C 26
GND 27
GND 28
+12V 29
+12V 30
-12V 31
-12V 32
+5V 33
+5V 34
VIA RIBBON CABLE TO I/O J19002 J33004
SPARE 1 → E33056
8dB/10dB 2 → J25001-25
LIN/LOG 3 → J25001-21
TC MSB 4 → J25001-22, E33006
TC LSB 5 → J25001-26, E33005
30K/300Hz 6 → J25001-20
VID FILT SEL 7 → J25001-23
QUASI/PEAK 8 → J25001-24
N/C 9
N/C 10
N/C 11
N/C 12
LOCK DET 13 → SEE DETAIL A
LOCK LT 14
SQUELCH DET 15 → J57001-22
QUASI DET 16 → E33001
GEN 1dB DET 17 → E33034
SPARE 18
REC DET 19 → J57001-8
SPARE 20
HOLD 21 → J29001-1
GEN DET 22 → E33040
÷10 SWEEP 23 → J29001-5
SPARE 24 → J29001-26
SPARE 25
REC BLANK 26 → J57001-3
R33001 1K
GND
VIA RIBBON CABLE TO FRONT PANEL E POINTS J33005
PWR ON 1 → E33012
GND 2 → J25001-25
BATT ON 3 → E33013
PWR LED 4 → +5V, RH, 1K
GND 5
+5V 6
TRACE INT 7 → J33001-20
+5V 8
GRAT INT 9 → J33001-19
FROM AUDIO VOL 10 → P71001-4
TO AUDIO VOL 11 → J57001-23
TO BEEP VOL 12 → J33002-33
FROM BEEP VOL 13 → P71001-5
-12V 14
SQUELCH 15 → J57001-1
+12V ON GEN 16 → Q1 COL E33042 E33043 J33005-17
+12V ON GEN 17 → Q1 COL E33042 E33043 J33005-16
+5V 18
TRACK ADJ 19 → E33041
GND 20
SIP RN1 4.7K
+5V
+12V
C2 .1
C3 .1
R4 30.1K, 1%
R5 30.1K 1%
RG 750, 1%
R7 500Ω
R9 3.65K, 1%
R8 5K
LH LM394
NC
NC
TO POWER SUPPLY J15003
P15003
E33307 GND 8
E33308 GND 11
E33309 BATT 6
J33005-4 E33012 PWR ON 3
J33005-3, E33013 BATT ON 9
E33014 +5V 4
E33015 +5V 5
E33016 +12V 1
E33017 +12V 2
E33018 +40V 12
E33019 -12V 7
P73002A BUFFER AMP
E33059 +12V 1
NC 2
TO 10.7MHz RECEIVER/PS7001 J57001
SQUELCH IN 1 → J33005-15
AGC 2
REC BLANK 3 → J33004-26
N/C 4
200KHz SEL 5 → J33002-8
N/C 6
GND 7 → J33004-16, E33001
REC DET 8 → J33004-19
+5V 9
+5V 10 → E33002
GND 11 → E33004
GND 12 → J25001-26, J33004-5, E33005
+12V 13 → J25001-22, J33004-4, E33006
+12V 14 → E33058
-12V 15 → E33057
-12V 16
FM/AM 17 → J33002-9
N/C 18
6 KHz SEL 19 → J33002-7
GND 20
N/C 21
SQUELCH DET 22 → J33004-15
AUDIO VOL 23 → J33005-11
N/C 24
15KHz SEL 25 → J33002-1
SSB 26 → J33002-3
TO QUASI PEAK FILTER/J62001
P62001
QUASI DET 1
+12V 2
GND 3
TC LSB 4
TC MSB 5
QUASI PEAK 6
-12V 7
NC 8
TO LOG AMP/P25001 J25001
IF 16dBd 1 → J33003-16
IF 16dBc 2 → J33003-17
IF 16dBb 3 → J33003-20
IF 16dBa 4 → J33003-21
IF 8dB 5 → J33003-18
IF 4dB 6 → J33003-22
IF 2dB 7 → J33003-19
IF 1dB 8 → J33003-23
+5V 9
+5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
VIDEO SLOPE 17 → J29001-25
N/C 18
NOISE FILTER 19 → J33002-17
30kHz/300Hz 20 → J33004-6
LIN/LOG 21 → J33004-3
TC MSB 22 → J33004-4, E33006
VIDEO FILT SEL 23 → J33004-7
QUASI/PEAK 24 → J33004-8
24dB/10dB 25 → J33004-2
TC LSB 26 → J33004-5, E33005
TO SYN#1/P23001 J23001
N/C 1
" 2
" 3
" 4
" 5
N/C 6
÷10/÷100 7 → J33003-15
N/C 8
+5V 9
+5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
CLOCK 17 → J33003-14, J27001-21, J29001-21, J23001-21
SYN#1 SWEEP 18 → J33002-28
DATA 19 → J33003-9, J27001-23, J29001-23, J23001-23
UNLOCK 20 → J33003-12
CLOCK 21 → J23001-17, J27001-21, J29001-21, J33001-14
SYN#1 LOCK 22 → SEE DETAIL A
DATA 23 → J27001-23, J29001-23, J33003-9, J23001-19
N/C 24
LATCH 1 25 → J33003-13
N/C 26
TO ANALY IF/P21001 J21001
30kHz BW 1 → J33002-11
3MHz BW 2 → J33002-10
3KHz BW 3 → J33002-13
300 KHz BW 4 → J33002-15
300Hz BW 5 → J33002-12
N/C 6
N/C 7
N/C 8
+5V 9
+5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
N/C 17
" 18
" 19
" 20
" 21
" 22
" 23
" 24
" 25
N/C 26
DETAIL A
CR33001 J23001-22
CR33002 J27001-8
CR33003 J27001-17
TO J33004-13
TO SYNTHESIZER#2/P27001 J27001
N/C 1
" 2
" 3
" 4
" 5
N/C 6
÷10/÷1 7 → J33003-11
SUM LOCK 8 → SEE DETAIL A
FILTERED +5V 9
FILTERED +5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
SYN#2 LOCK 17 → SEE DETAIL A
N/C 18
N/C 19
N/C 20
CLOCK 21 → J33003-14, J23001-17, -21, J29001-21
N/C 22
DATA 23 → J33003-9, J23001-19, -23, J29001-23
N/C 24
LATCH 2 25 → J33003-10
N/C 26
L1 2.5 mH
C1 1000μF 6.3V
+5V
TO 1st LO SAMPLING LOOP/P29001 J29001
HOLD 1 → J33004-21
N/C 2
SAMPLER SWEEP 3 → J33002-27
N/C 4
÷10 SWEEP 5 → J33004-23
N/C 6
N/C 7
N/C 8
+5V 9
+5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
+40V 17
+40V 18
19
20
CLOCK 21 → J33003-14
22
DATA 23 → J33003-9
24
VIDEO SLOPE 25 → J25001-17
SPARE 26 → J33004-24
TO REF OSCILLATOR/P46001 J46001
N/C 1
" 2
" 3
" 4
" 5
" 6
" 7
N/C 8
+5V 9
+5V 10
GND 11
GND 12
+12V 13
+12V 14
-12V 15
-12V 16
N/C 17
" 18
" 19
" 20
" 21
" 22
" 23
" 24
" 25
" 26
⊕ ADD: J27001-23, J23001-19, J29001-23
⊕ ADD: J27001-21, J23001-21, J23001-17
NOTES:
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3.
4.

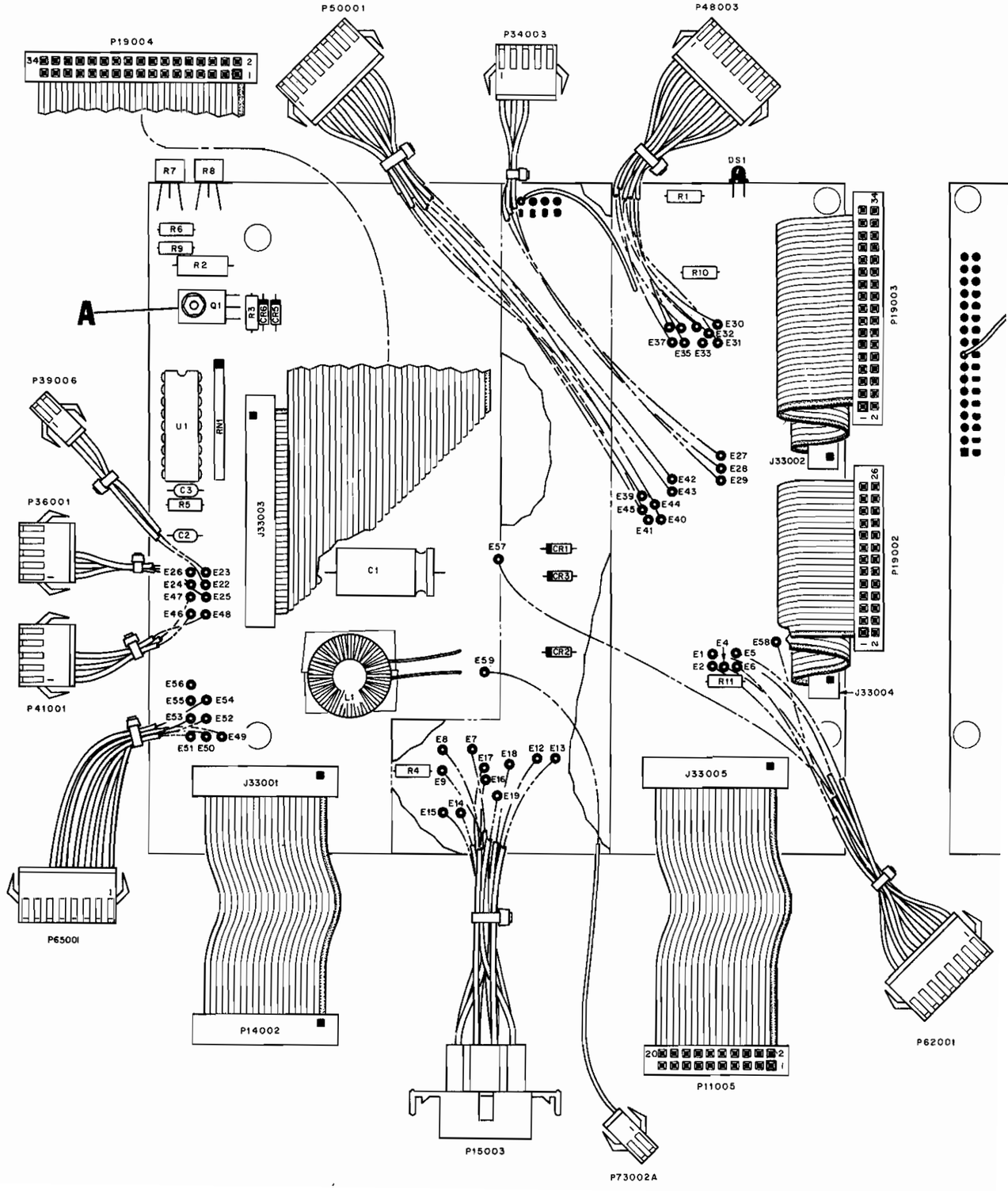


NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 33000 (E.G., R1 IS R33001).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS SPECIFIED).



DETAIL **A**

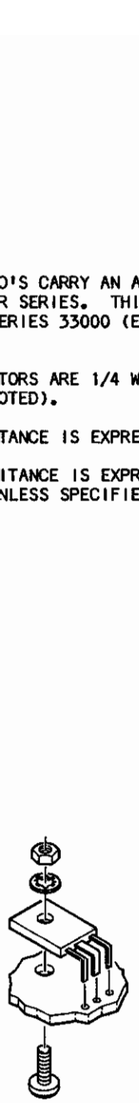


O'S CARRY AN ASSIGNED
R SERIES. THIS SCHEMATIC
ERIES 33000 (E.G., R1 IS

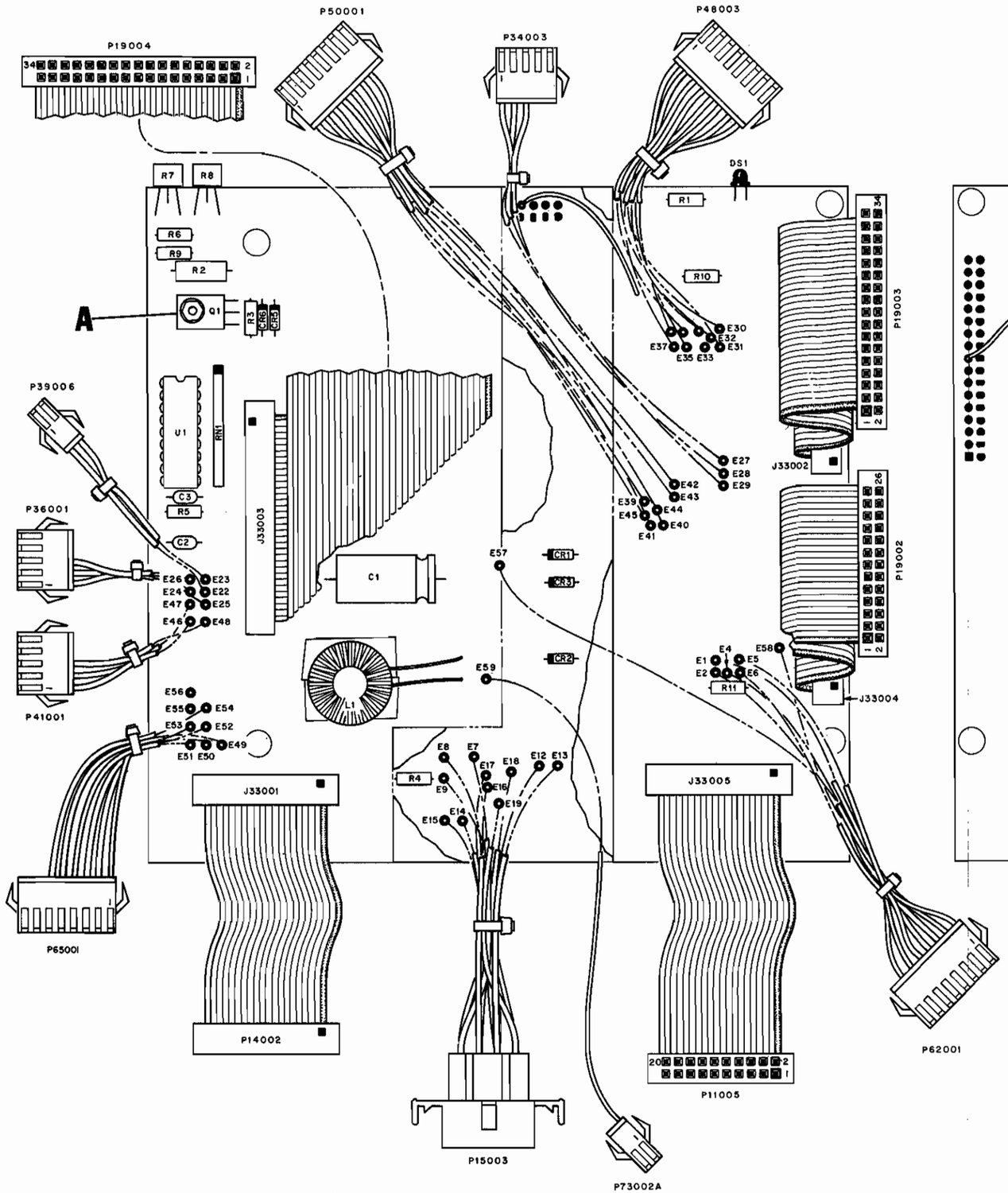
TORS ARE 1/4 W, 5% TOLERANCE
OTED).

TANCE IS EXPRESSED IN OHMS.

ITANCE IS EXPRESSED IN MICRO-
NLESS SPECIFIED).



DETAIL **A**



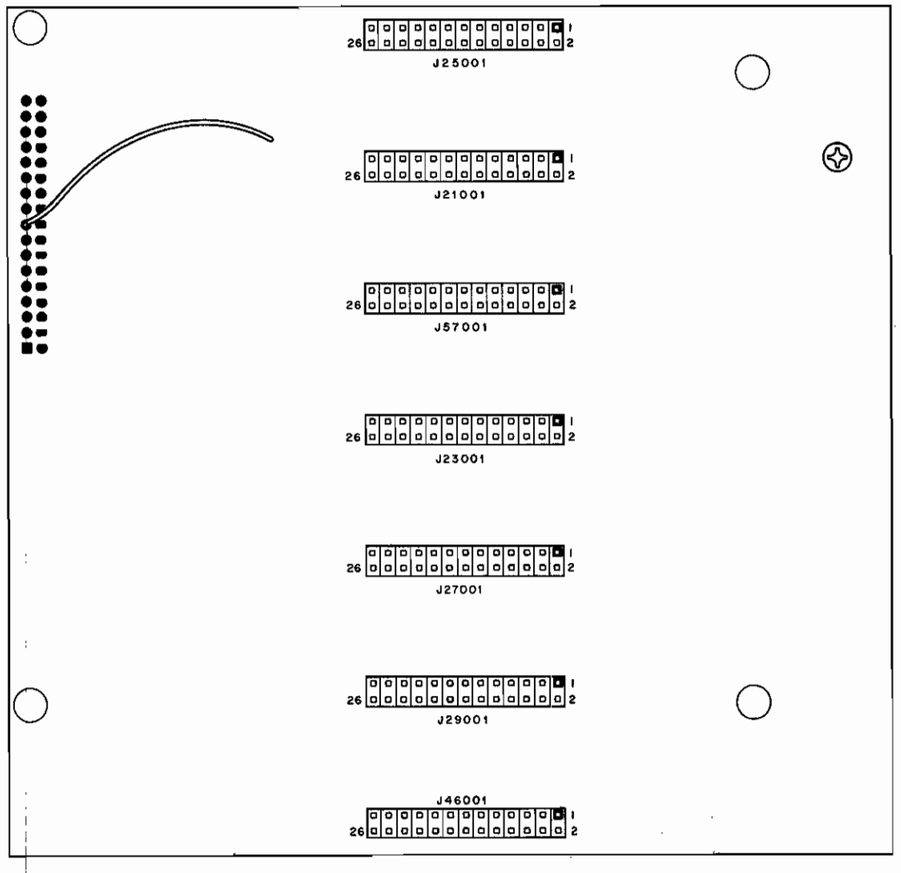
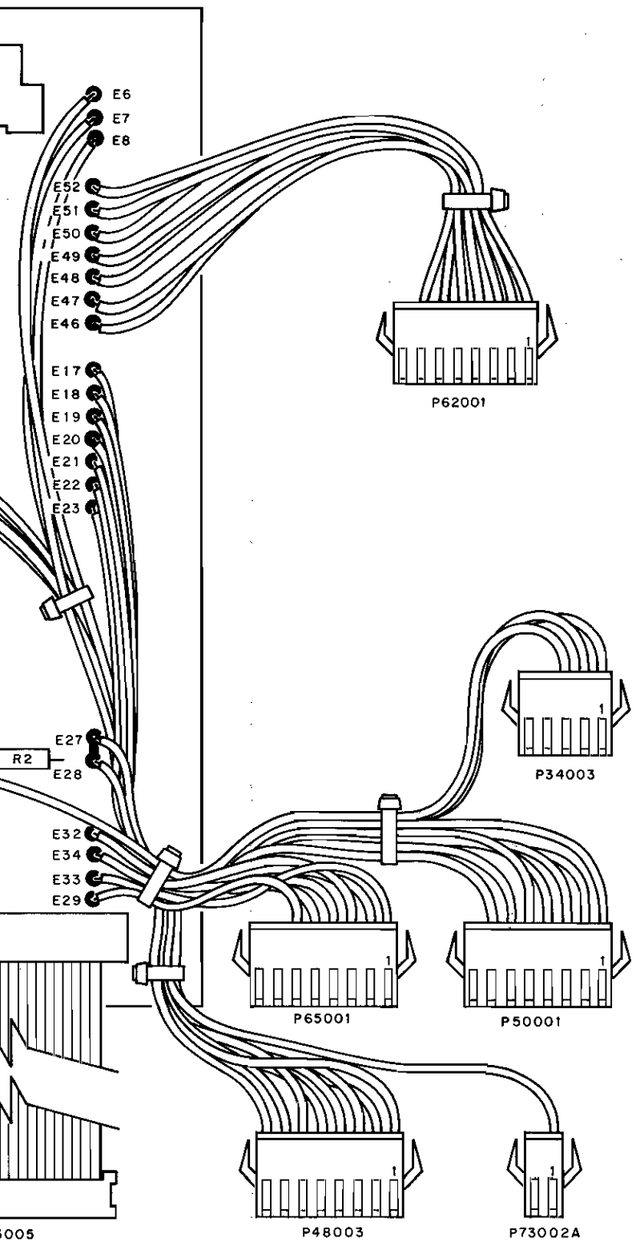


Figure 5-3 RF Motherboard (Sheet 1 of 3)
(S/N 1001 Thru S/N 1476)
(D-00000-5013-000-D4)



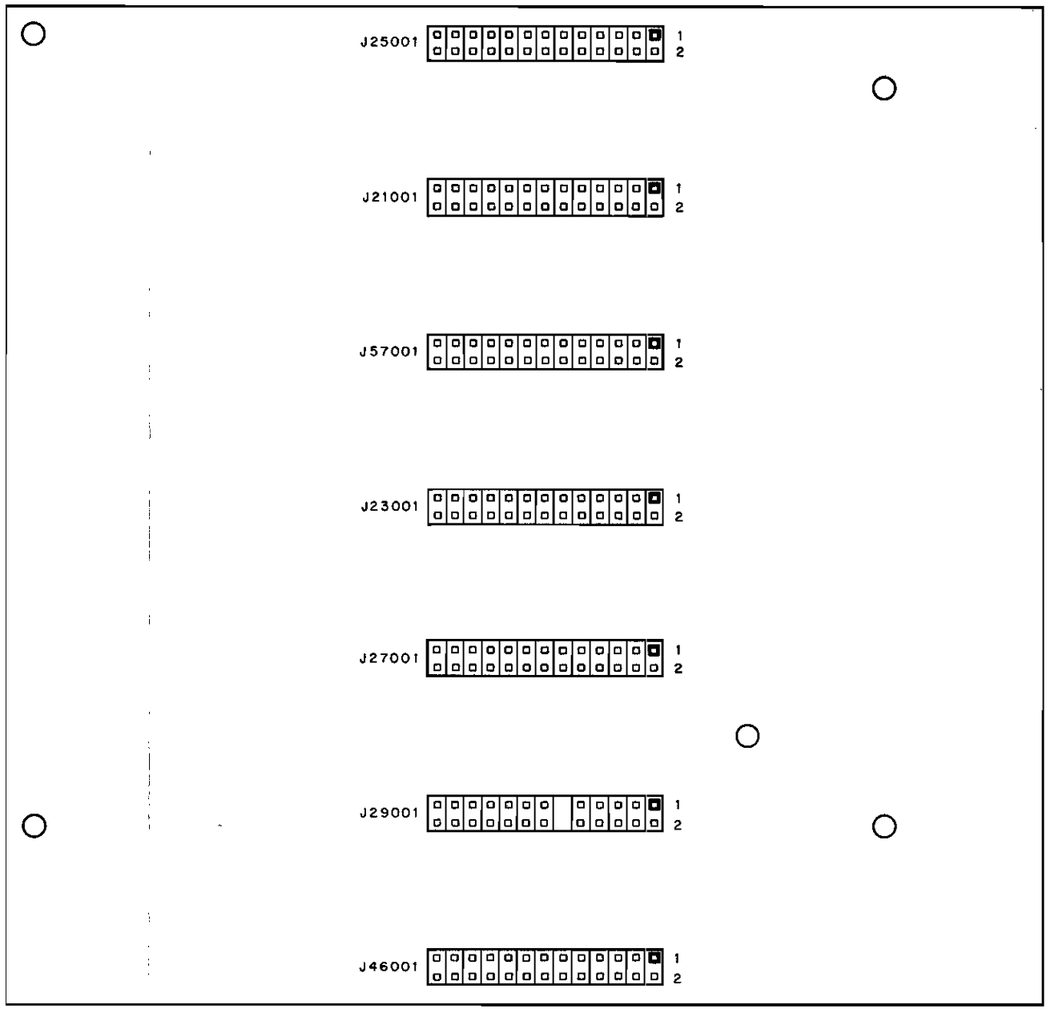
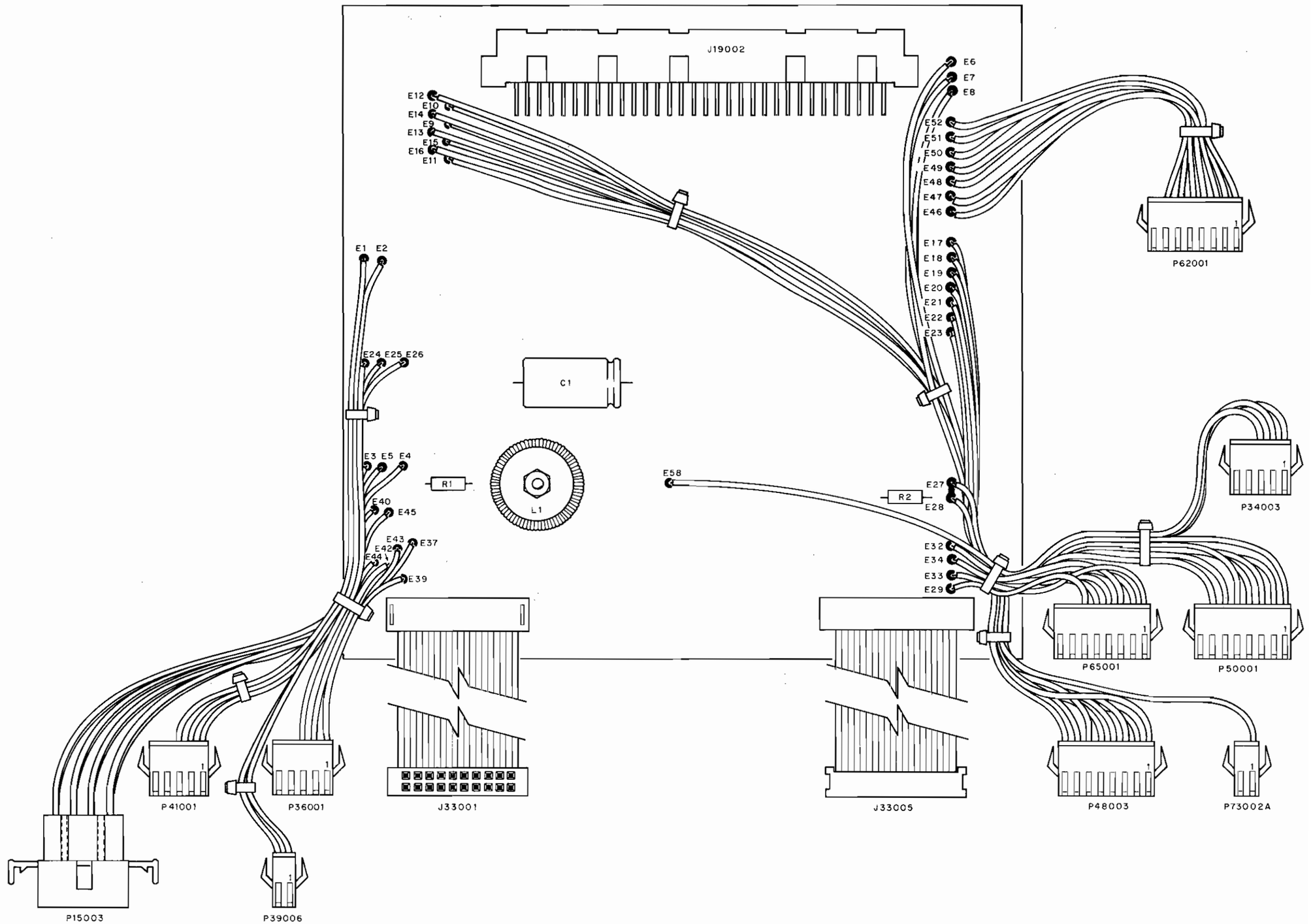


Figure 5-3 RF Motherboard (Sheet 2 of 3)
(S/N 1477 & ON) (D-0000-5315-300-C2)


J19002
E12
E10
E14
E9
E13
E15
E16
E11
E1
E2
E24
E25
E26
E3
E5
E4
E40
E45
E43
E42
E44
E37
E39
C1
R1
L1
E6
E7
E8
E52
E51
E50
E49
E48
E47
E46
P62001
E17
E18
E19
E20
E21
E22
E23
E58
R2
E27
E28
E32
E34
E33
E29
P34003
P65001
P50001
P41001
P36001
J33001
J33005
P48003
P73002A
P15003
P39006

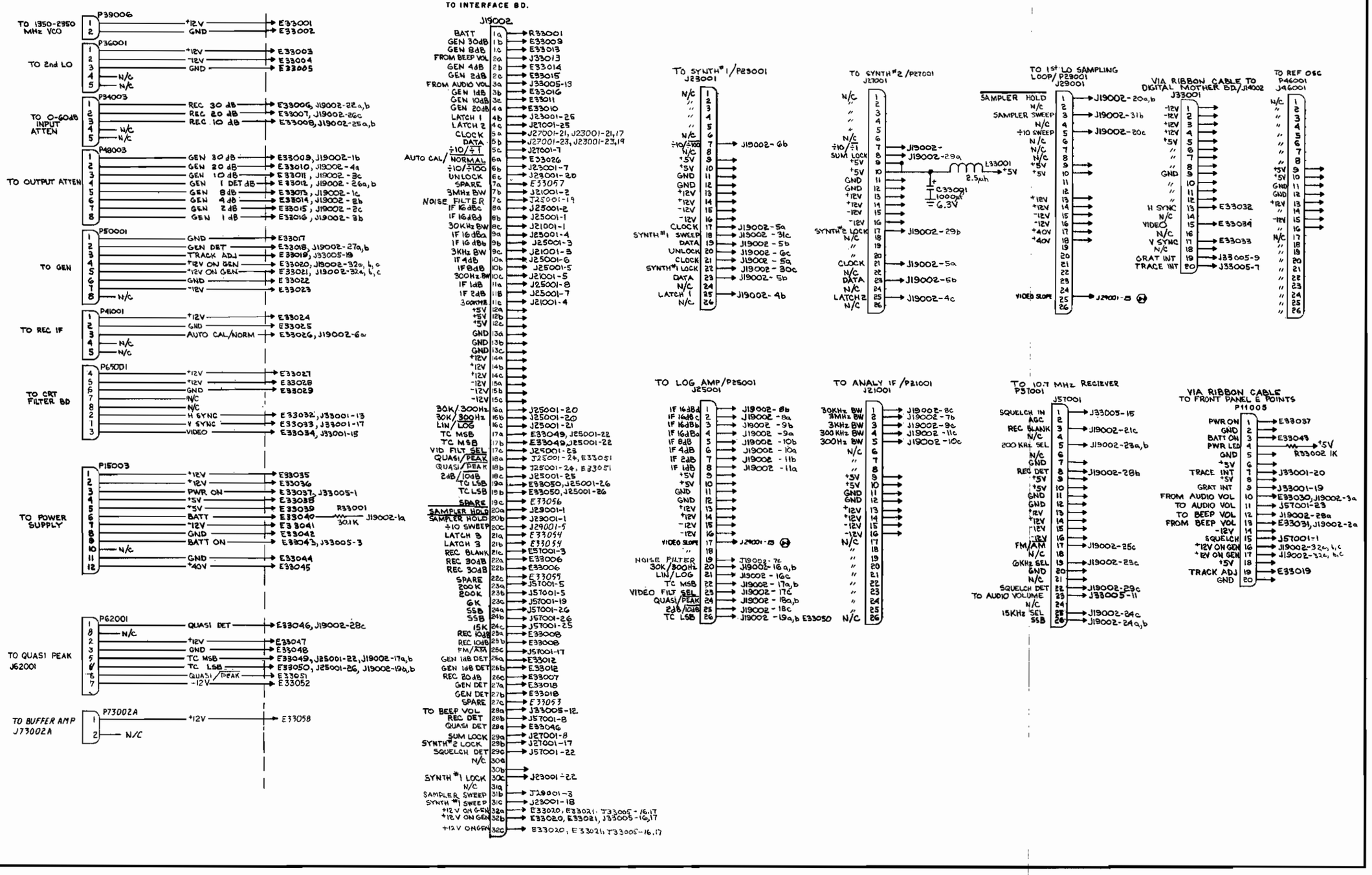


Figure 5-3 RF Motherboard (Sheet 3 of 3)
(S/N 1477 & ON) (D-0000-5315-300-C2)

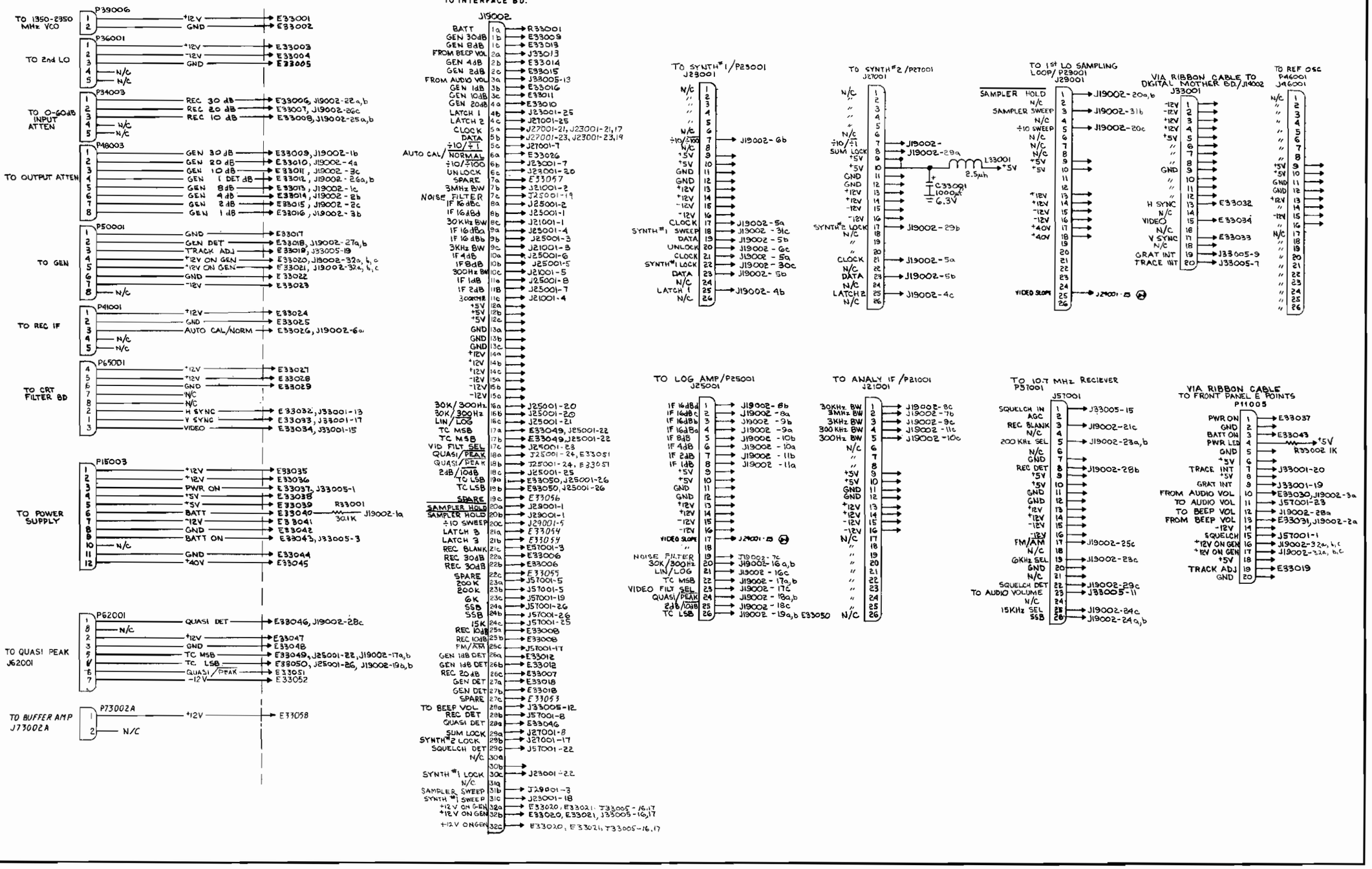
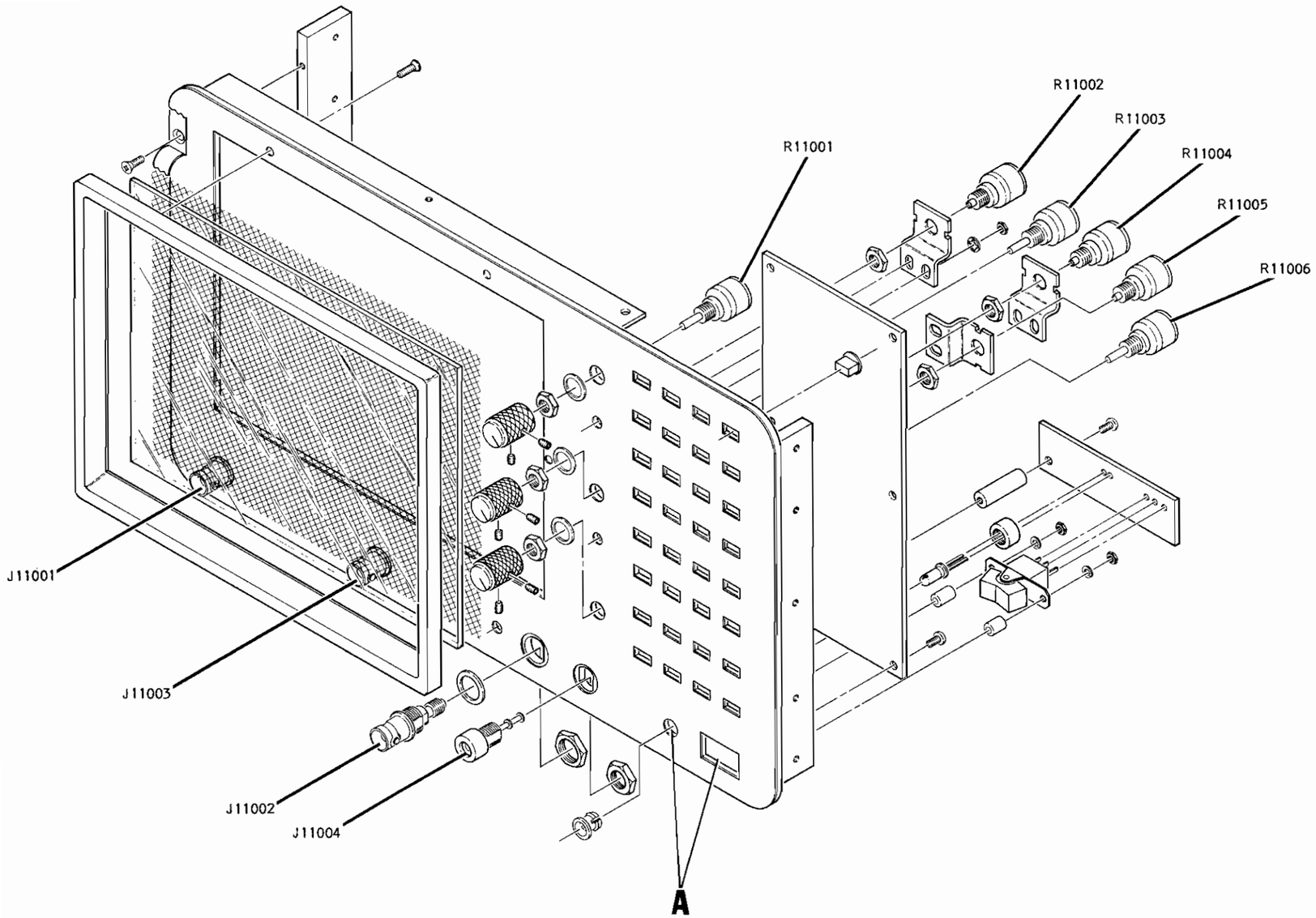
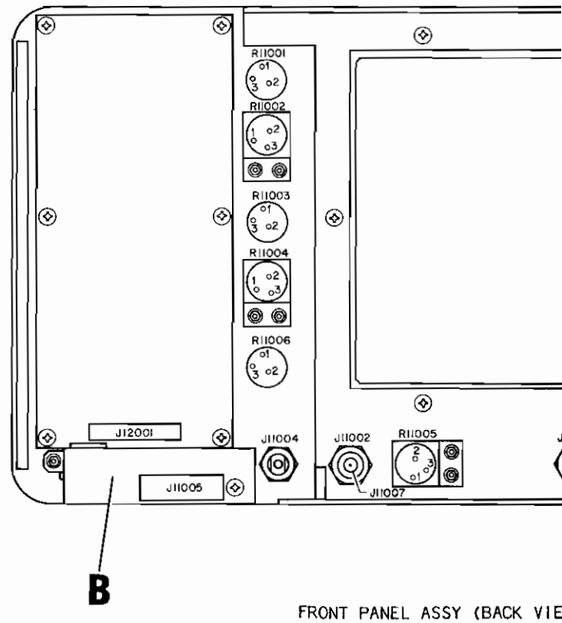


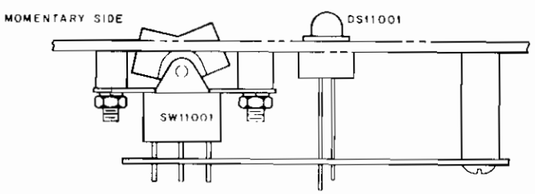
Figure 5-3 RF Motherboard (S
(S/N 1477 & ON)



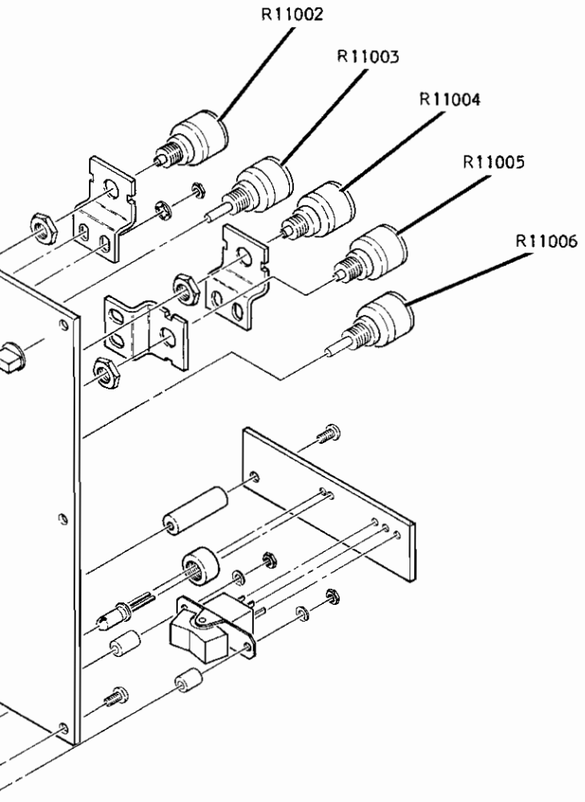
FRONT PANEL ASSY (FRONT VIEW)

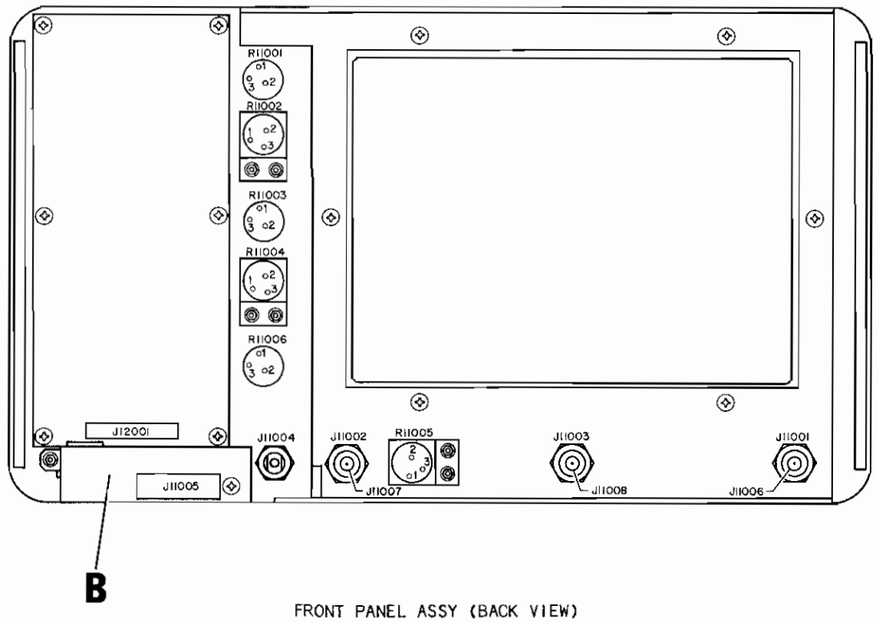


FRONT PANEL ASSY (BACK VIE

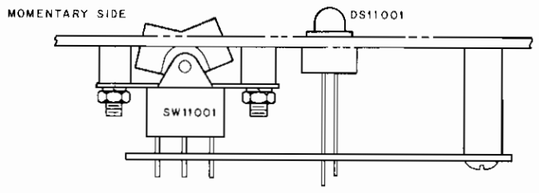


DETAIL **A**

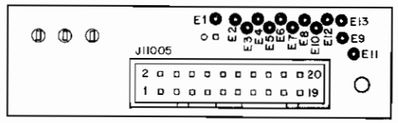




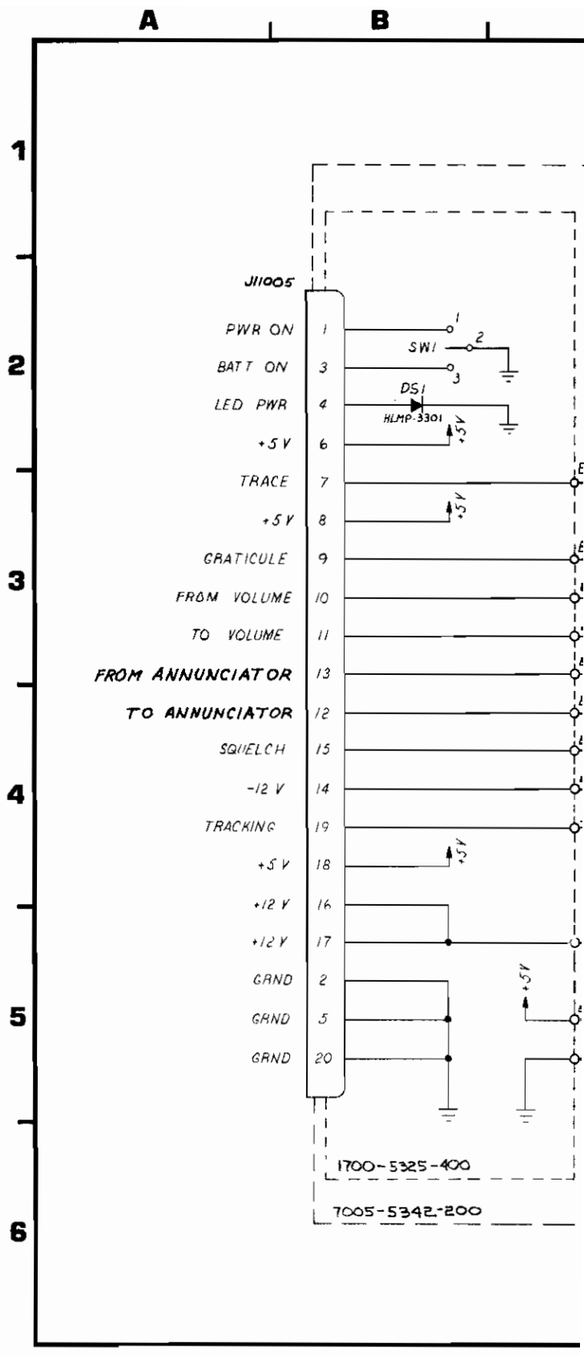
FRONT PANEL ASSY (BACK VIEW)

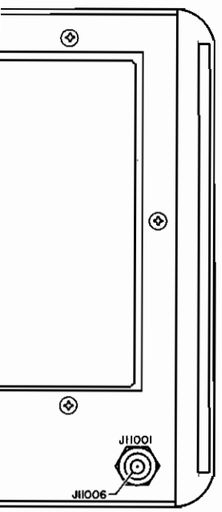


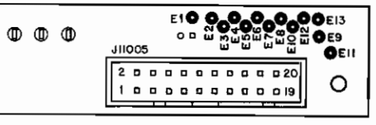
DETAIL **A**



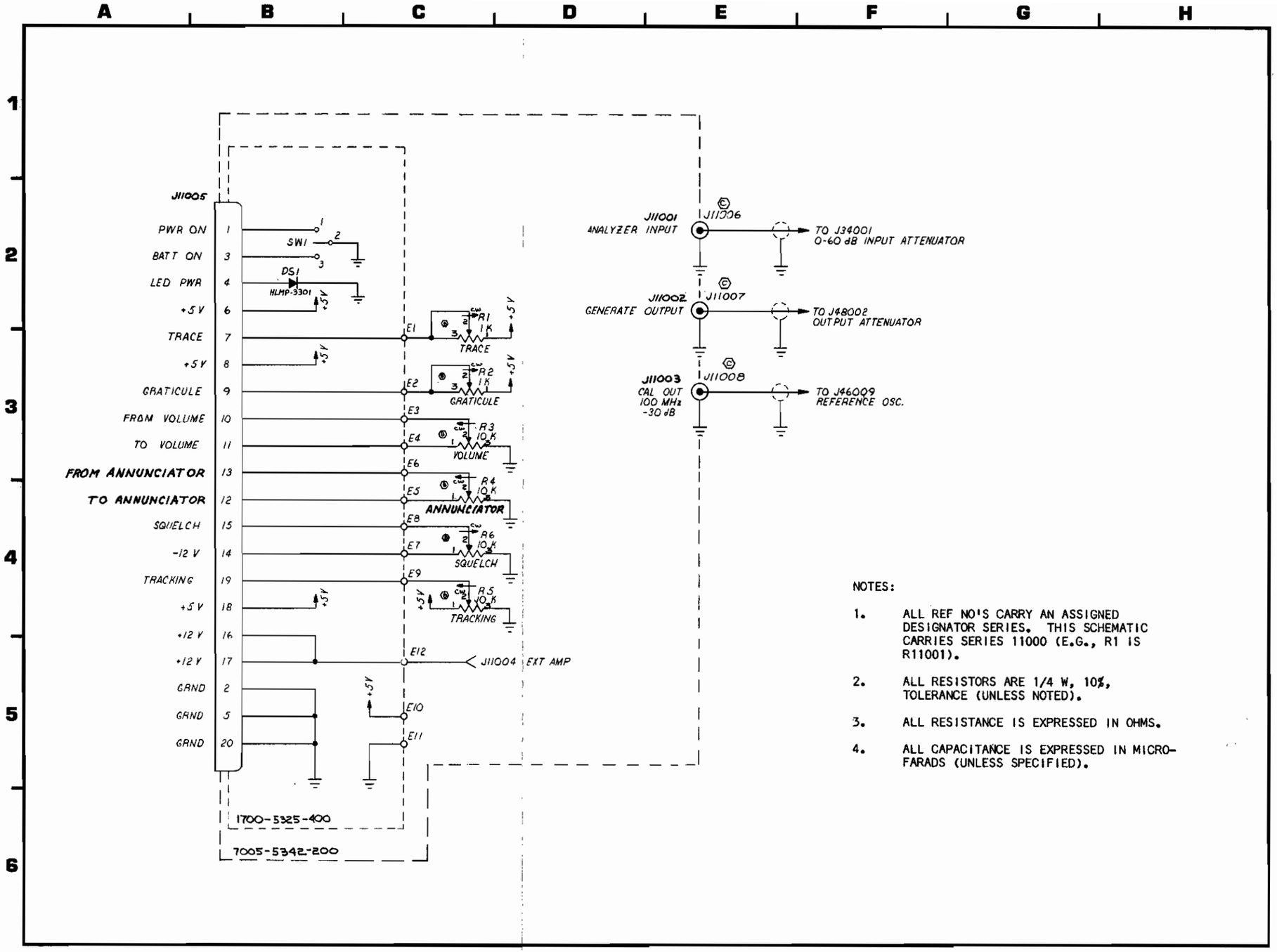
DETAIL **B**







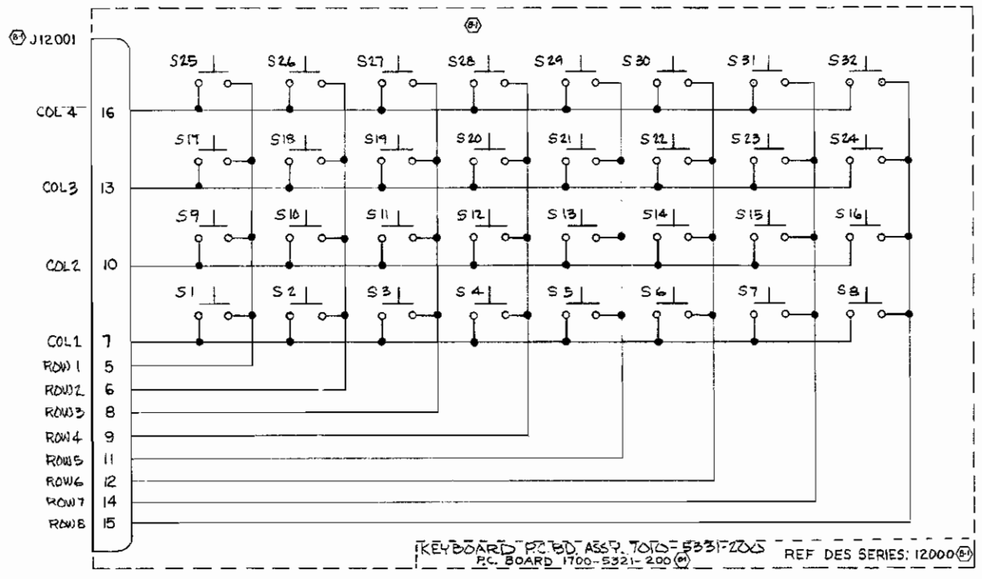
DETAIL **B**



NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 11000 (E.G., R1 IS R11001).
2. ALL RESISTORS ARE 1/4 W, 10%, TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS (UNLESS SPECIFIED).

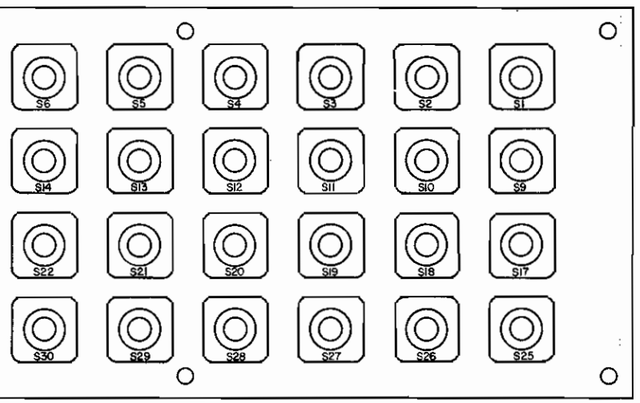
Figure 5-4 Front Panel (D-0000-5312-200-C)

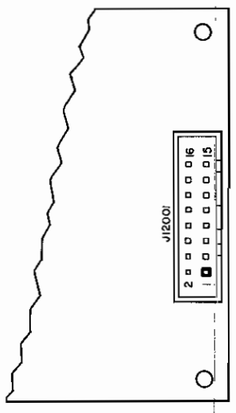


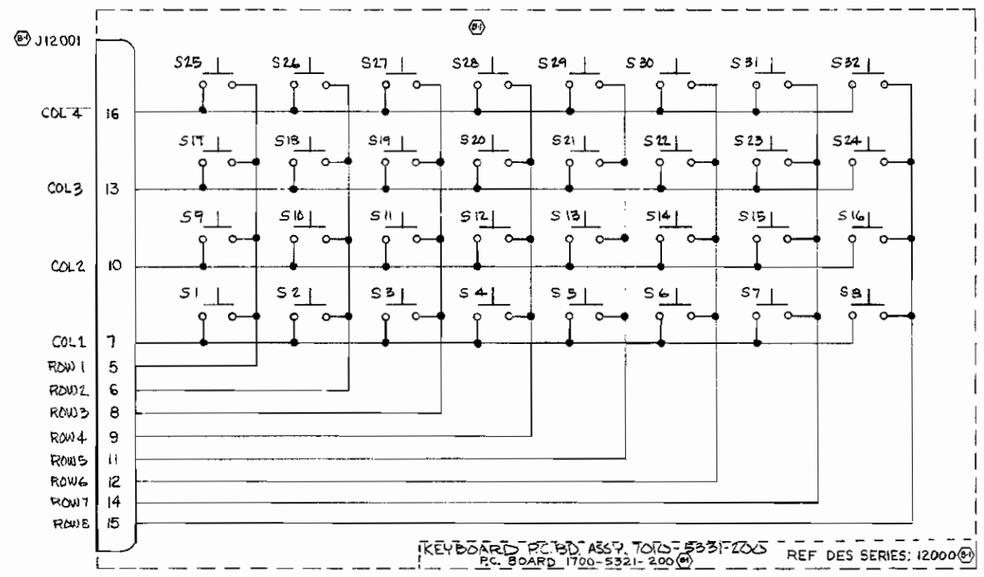
NOTES:

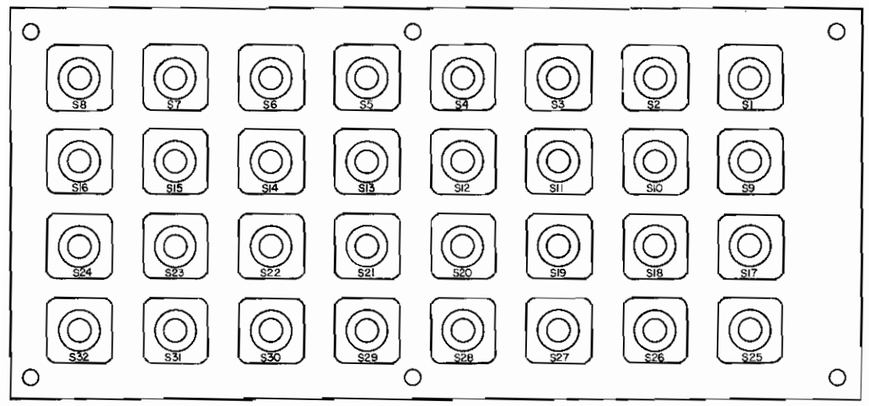
1. ALL REF NOS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 12000 (E.G., S1 IS S12001).

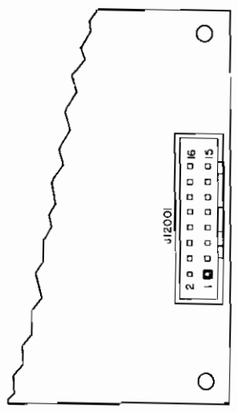
Figure 5-5 Keyboard
(D-0000-5311-200-B1)

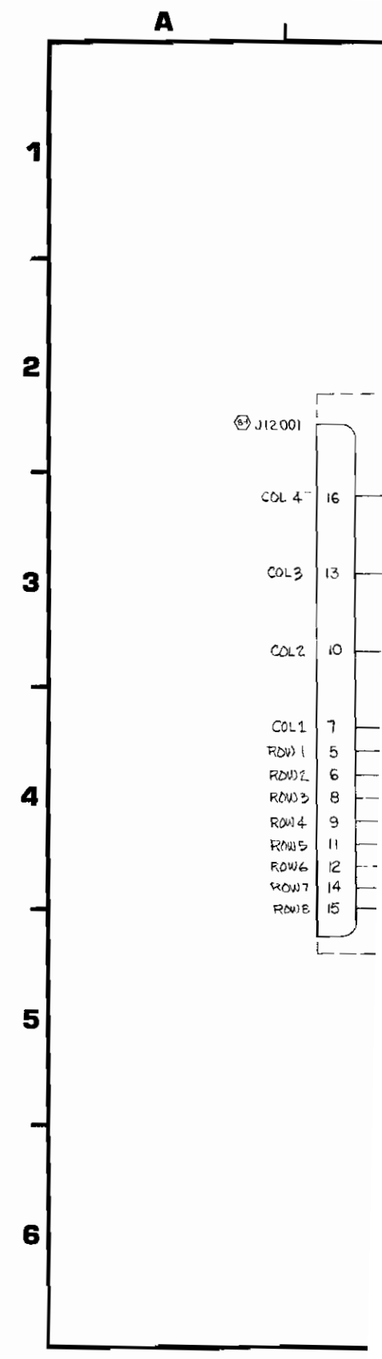

S6
S5
S4
S3
S2
S1
S14
S15
S12
S11
S10
S9
S22
S21
S20
S19
S18
S17
S30
S29
S28
S27
S26
S25

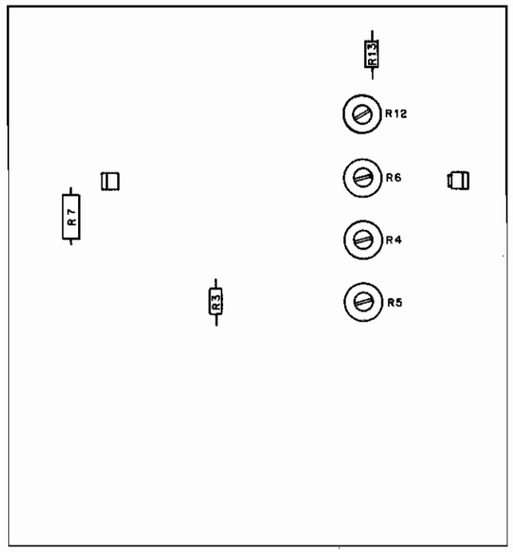

J12001
16
15
2
1


J12001
COL4 16
COL3 13
COL2 10
COL1 7
ROW1 5
ROW2 6
ROW3 8
ROW4 9
ROW5 11
ROW6 12
ROW7 14
ROW8 15
S25 S26 S27 S28 S29 S30 S31 S32
S17 S18 S19 S20 S21 S22 S23 S24
S9 S10 S11 S12 S13 S14 S15 S16
S1 S2 S3 S4 S5 S6 S7 S8
KEYBOARD PC BD ASSY. 7070-5331-2003
PC. BOARD 1700-5321-200
REF DES SERIES: 12000

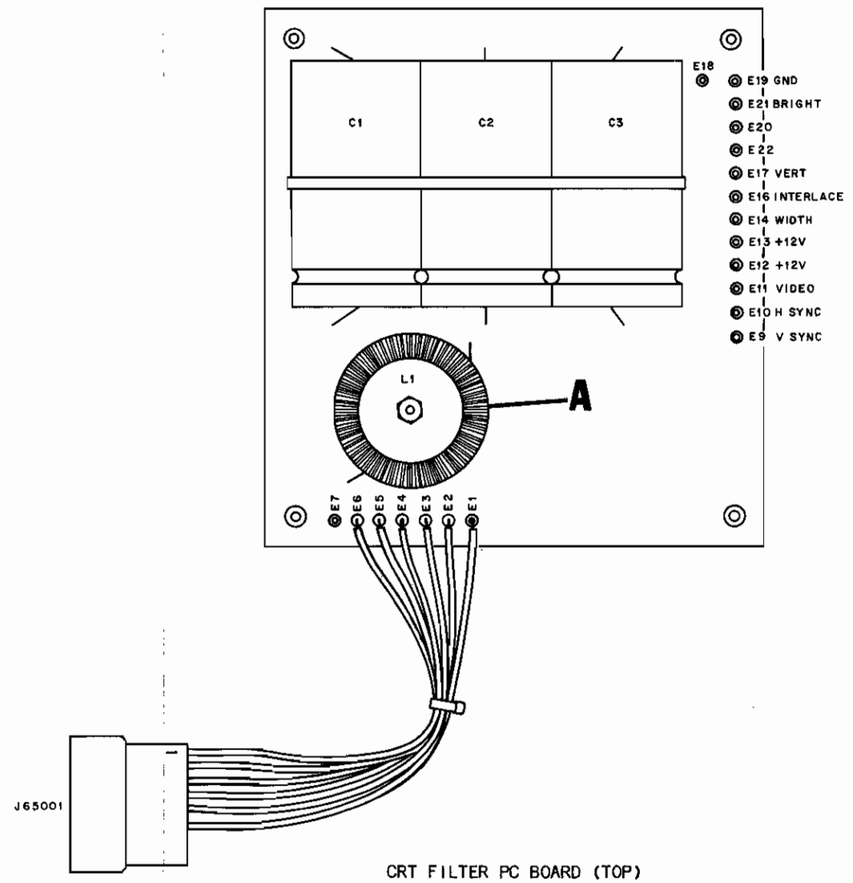

S8
S7
S6
S5
S4
S3
S2
S1
S16
S15
S14
S13
S12
S11
S10
S9
S24
S23
S22
S21
S20
S19
S18
S17
S32
S31
S30
S29
S28
S27
S26
S25


J12001
16
15
2
1

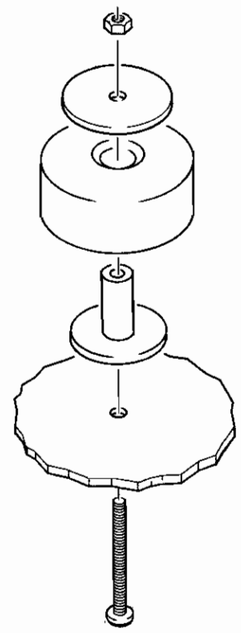

A
1
2
3
4
5
6
J12001
COL 4
16
COL3
13
COL2
10
COL1
7
ROW1
5
ROW2
6
ROW3
8
ROW4
9
ROW5
11
ROW6
12
ROW7
14
ROW8
15



CRT FILTER PC BOARD (BOTTOM)

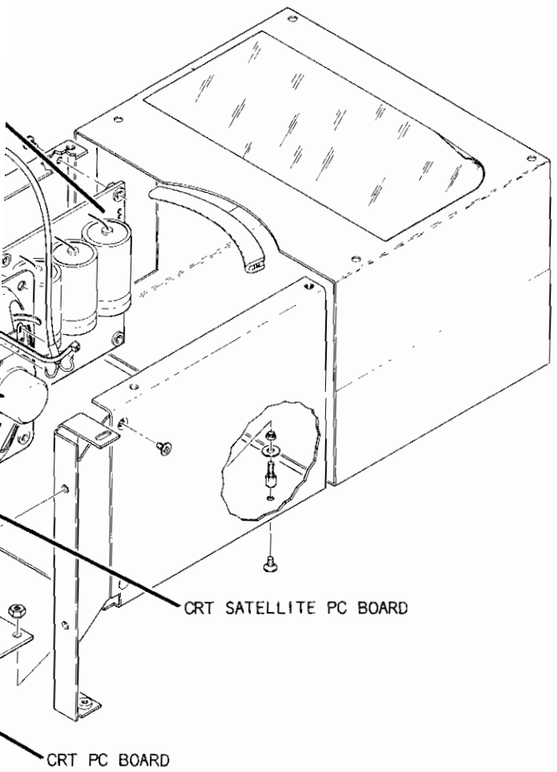


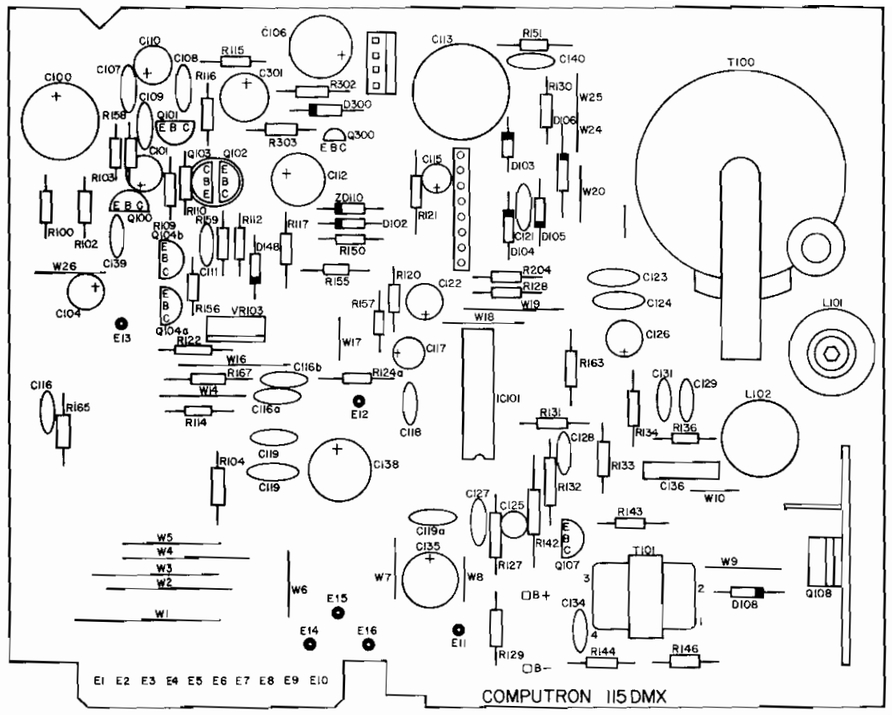
CRT FILTER PC BOARD (TOP)



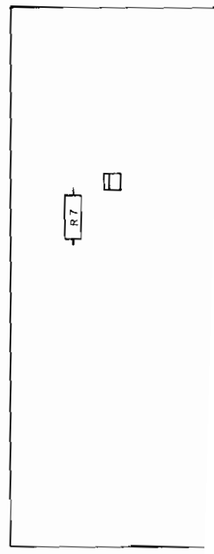
DETAIL **A**

Figure 5-6 Computron[T.M.] CRT Module (Sheet 1 of 2)
(D-0000-5314-900-D)

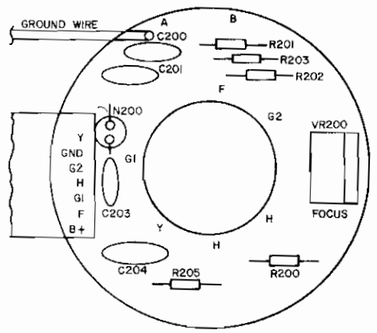




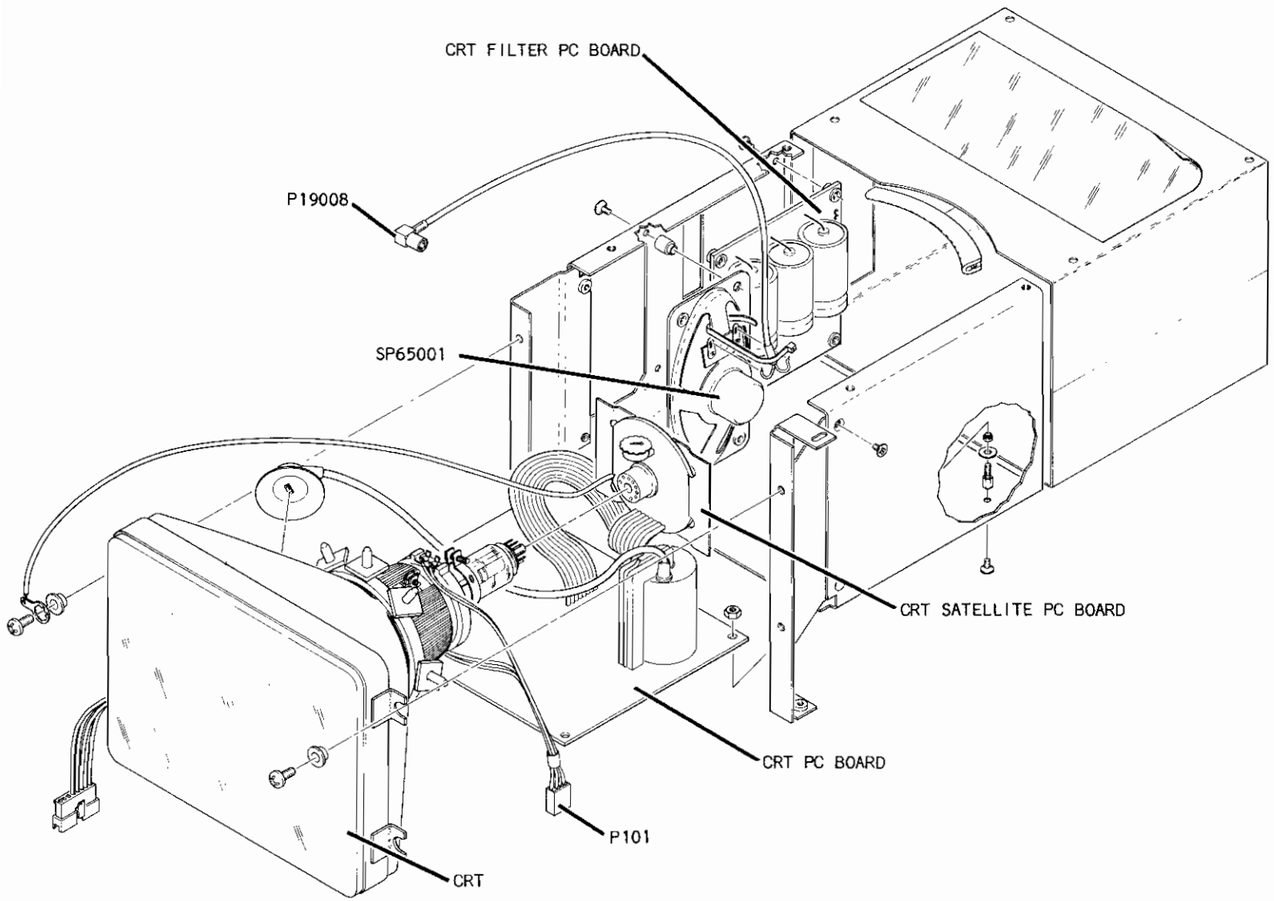
CRT PC BOARD



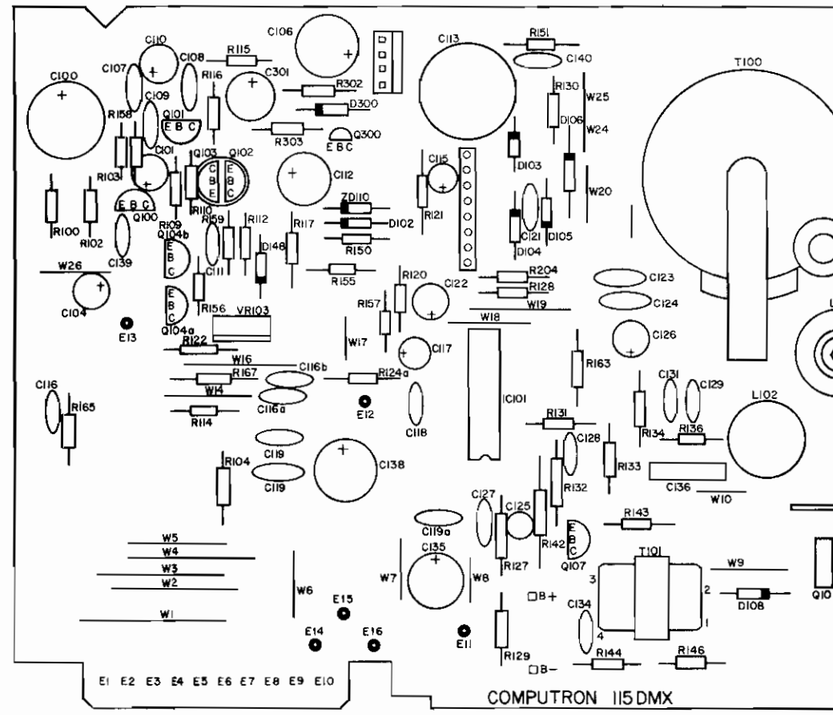
CRT FILTI



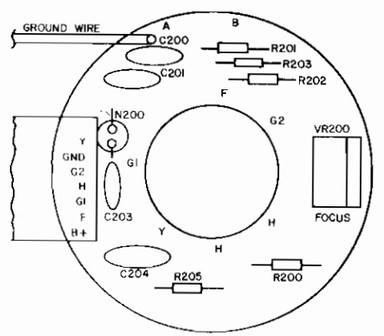
CRT SATELLITE PC BOARD



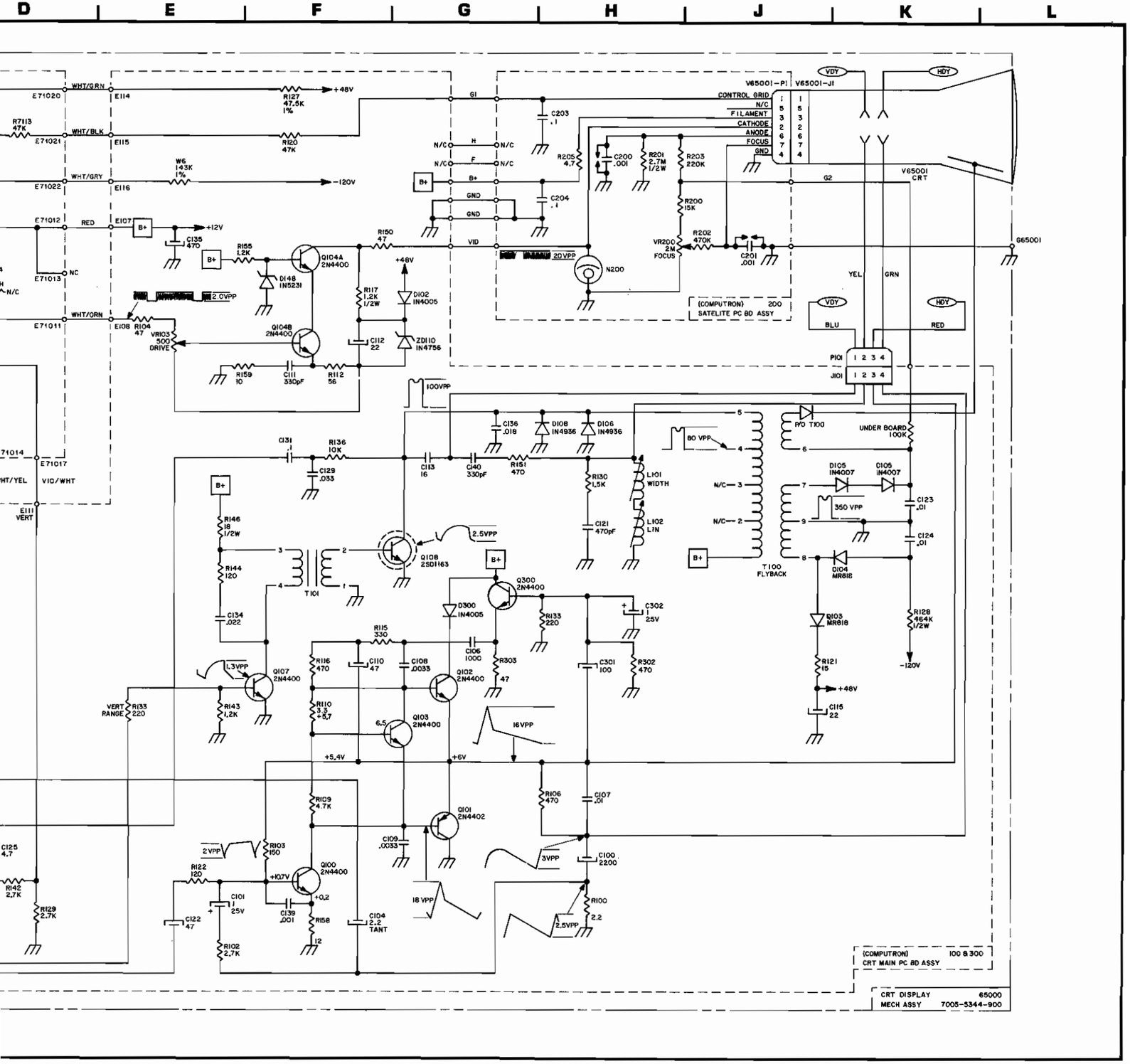
CRT DISPLAY ASSY



CRT PC BOARD



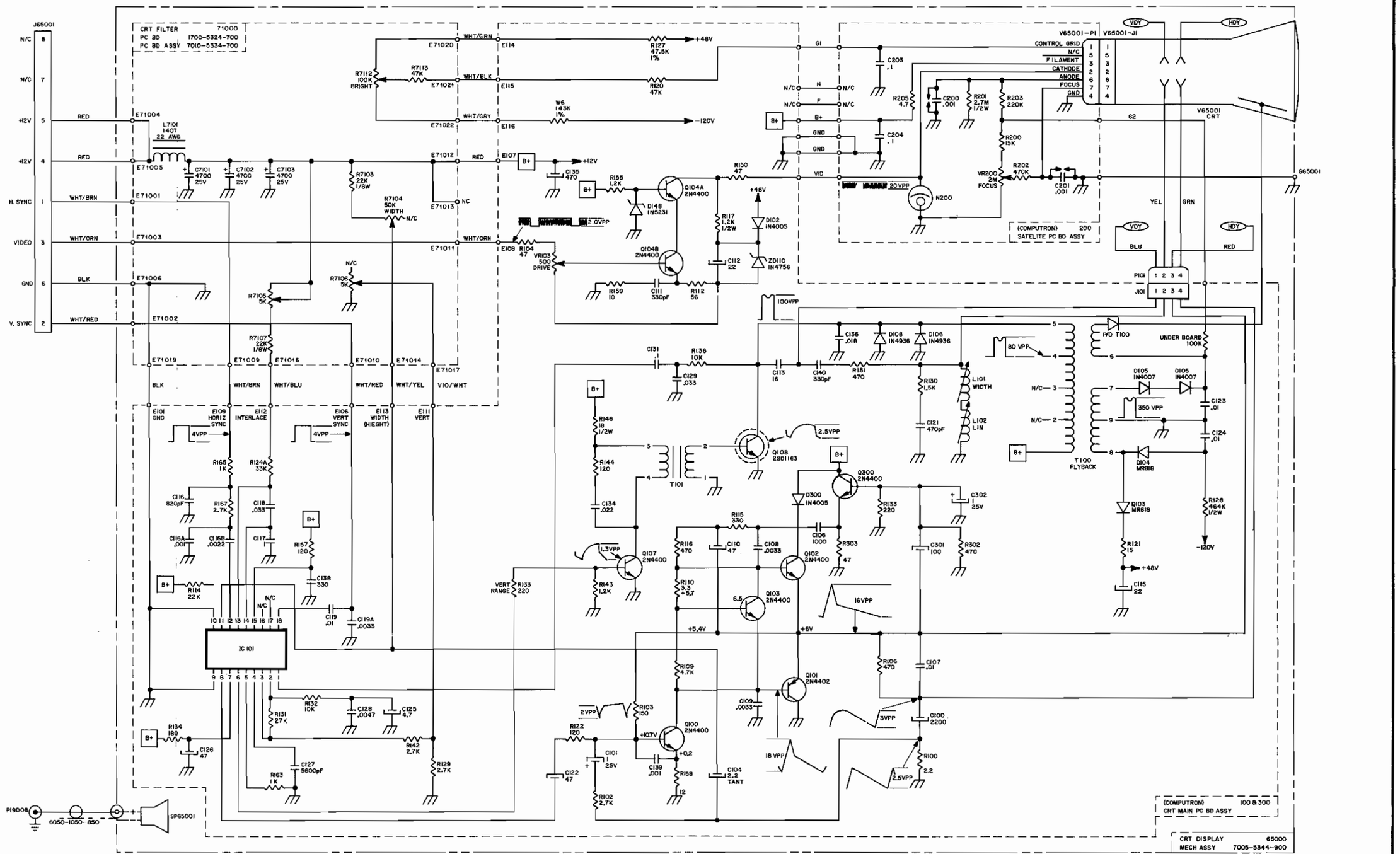
CRT SATELLITE PC BOARD

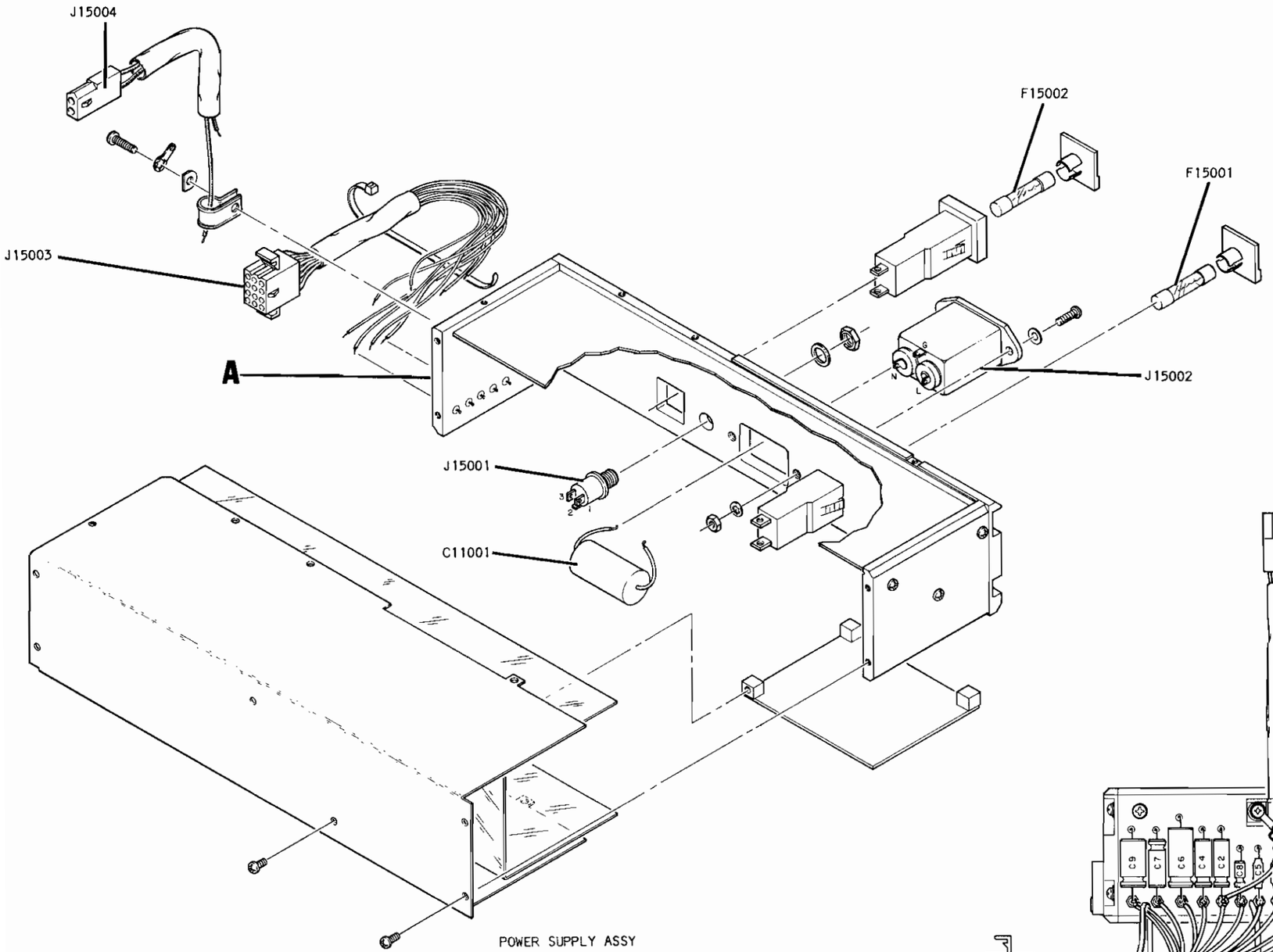


NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES:
   - A. MECHANICAL ASSY IS 65000 (R1 IS R65001).
   - B. COMPUTRON SATELLITE PC BD ASSY-200.
   - C. COMPUTRON CRT MAIN PC BD ASSY'S-100 AND 300.
   - D. CRT FILTER PC BD ASSY-71000.
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS (UNLESS SPECIFIED).
5. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRYS (UNLESS SPECIFIED).

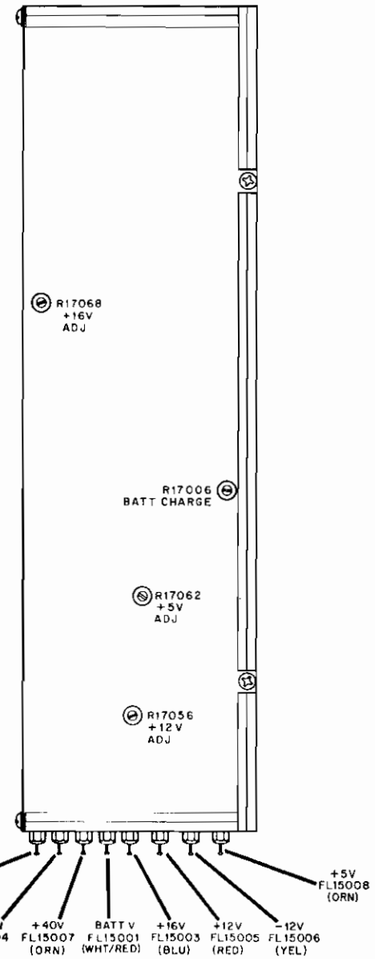
Figure 5-6 Computron[T.M.] CRT Module (Sheet 2 of 2) (D-0000-5314-900-D)


CRT FILTER 71000
PC BD 1700-5324-700
PC BD ASSY 7010-5334-700
J65001
N/C 8
N/C 7
+12V 5
+12V 4
H. SYNC 1
VIDEO 3
GND 6
V. SYNC 2
RED
RED
WHT/BRN
WHT/ORN
BLK
WHT/RED
E71004
E71005
E71001
E71003
E71006
E71002
L7101 140T 22 AWG
C7101 4700 25V
C7102 4700 25V
C7103 4700 25V
R7103 22K 1/8W
R7104 50K WIDTH
R7105 5K
R7106 5K
R7107 22K 1/8W
E71020
E71021
E71022
E71012
E71013
E71011
E71019
E71009
E71016
E71010
E71014
E71017
WHT/GRN
WHT/BLK
WHT/GRY
RED
NC
WHT/ORN
BLK
WHT/BRN
WHT/BLU
WHT/RED
WHT/YEL
VIO/WHT
R7112 100K BRIGHT
R7113 47K
E114
E115
E116
R127 47.5K 1%
R120 47K
W6 143K 1%
+48V
-120V
E107
+12V
C135 470
R155 1.2K
Q104A 2N4400
D148 IN5231
2.0VPP
R150 47
R117 1.2K 1/2W
D102 IN4005
ZD110 IN4756
C112 22
Q104B 2N4400
E108 R104 47
VR103 500 DRIVE
R159 10
C111 330pF
R112 56
E101 GND
E109 HORIZ SYNC
E112 INTERLACE
E106 VERT SYNC
E113 WIDTH (HIEGHT)
E111 VERT
4VPP
R165 1K
R124A 33K
C116 820pF
R167 2.7K
C116A .001
C116B .0022
C118 .033
C117
R157 120
C138 330
R114 22K
C119 .01
C119A .0033
N/C
IC 101
10 11 12 13 14 15 16 17 18
9 8 7 6 5 4 3 2 1
R131 27K
R132 10K
C128 .0047
C125 4.7
R134 180
C126 47
R142 2.7K
R129 2.7K
R163 1K
C127 5600pF
P19008
6050-1050-850
SP65001
GI
N/C
N/C
B+
GND
GND
VID
C203 .1
C204 .1
R205 4.7
C200 .001
R201 2.7M 1/2W
R203 220K
R200 15K
VR200 2M FOCUS
R202 470K
C201 .001
20VPP
N200
G65001
V65001-P1
V65001-J1
CONTROL GRID
N/C
FILAMENT
CATHODE
ANODE
FOCUS
GND
G2
V65001 CRT
VDY
HDY
YEL
GRN
BLU
RED
(COMPUTRON) 200
SATELITE PC BD ASSY
P101 1 2 3 4
J101 1 2 3 4
100VPP
C131
R136 10K
C129 .033
C113 16
C140 330pF
R181 470
C136 .018
D108 IN4936
D106 IN4936
80 VPP
R130 1.5K
L101 WIDTH
L102 LIN
C121 470pF
P/O T100
UNDER BOARD 100K
D105 IN4007
D105 IN4007
C123 .01
C124 .01
350 VPP
D104 MR816
D103 MR818
R121 15
C115 22
R128 464K 1/2W
-120V
+48V
T100 FLYBACK
N/C
R146 18 1/2W
R144 120
C134 .022
T101
Q108 2SD1163
2.5VPP
Q300 2N4400
D300 IN4005
R133 220
C302 25V
C301 100
R302 470
R115 330
R116 470
C110 47
C108 .0033
C105 1000
R303 47
Q107 2N4400
1.3VPP
R143 1.2K
Q102 2N4400
R110 3.3 +5%
Q103 2N4400
6.5
16VPP
VERT RANGE R133 220
+5.4V
+6V
R109 4.7K
Q101 2N4402
C109 .0033
R106 470
C107 .01
C100 2200
3VPP
2VPP
R103 150
Q100 2N4400
+10.7V
+0.2
R122 120
C101 25V
C139 .001
C104 2.2 TANT
18 VPP
2.5VPP
R100 2.2
R158 12
C122 47
R102 2.7K
(COMPUTRON) 100 & 300
CRT MAIN PC BD ASSY
CRT DISPLAY 65000
MECH ASSY 7005-5344-900

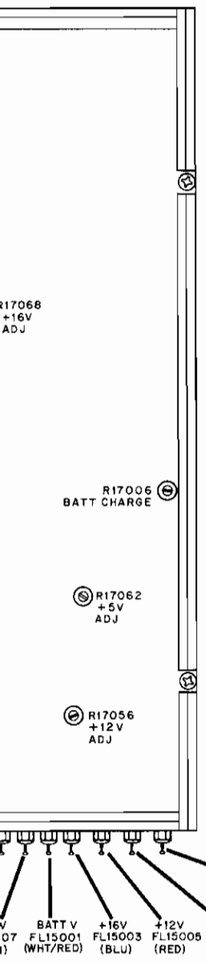


POWER SUPPLY ASSY

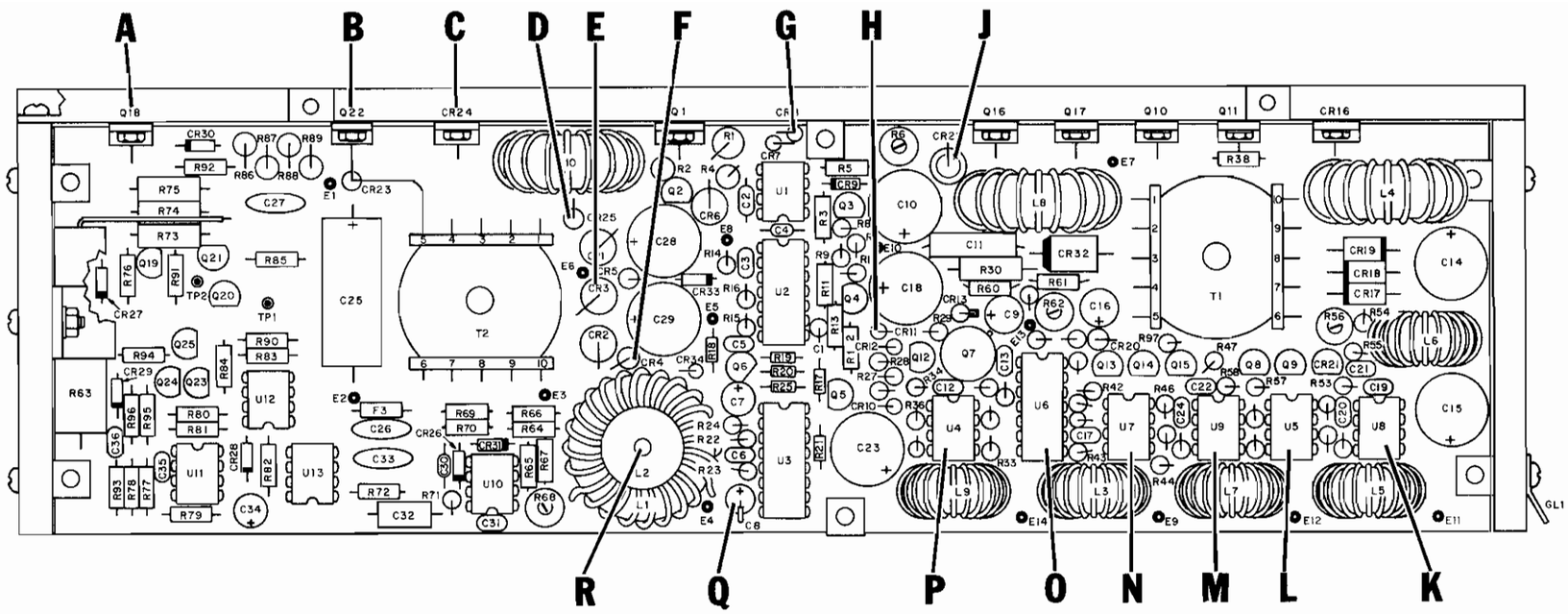
DETAIL **A**



POWER SUPPLY ASSY (BOTTOM)

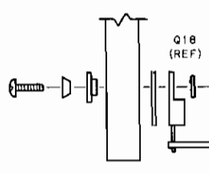


SUPPLY ASSY (BOTTOM)

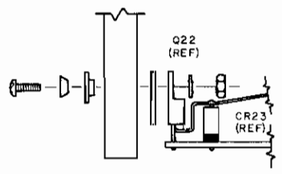


POWER SUPPLY PC BOARD

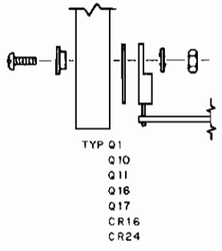
LINE RECTIFIER PC



DETAIL **A**



DETAIL **B**



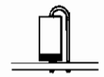
DETAIL **C**



DETAIL **D**



DETAIL **E**



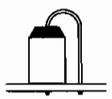
DETAIL **F**



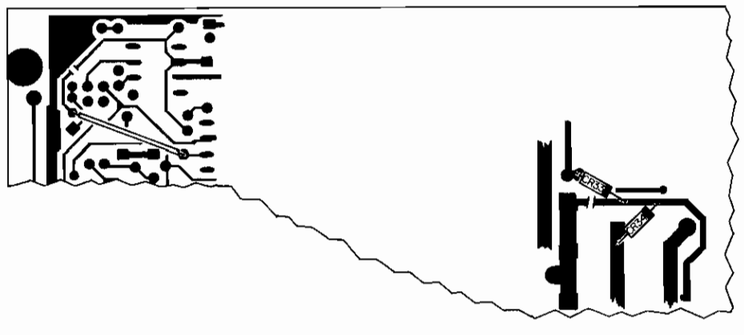
DETAIL **G**



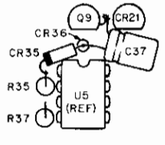
DETAIL **H**



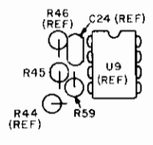
DETAIL **J**



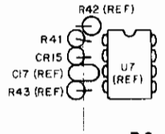
POWER SUPPLY PC BOARD (BOTTOM)



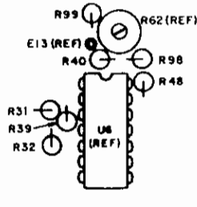
DETAIL **L**



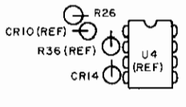
DETAIL **M**



DETAIL **N**

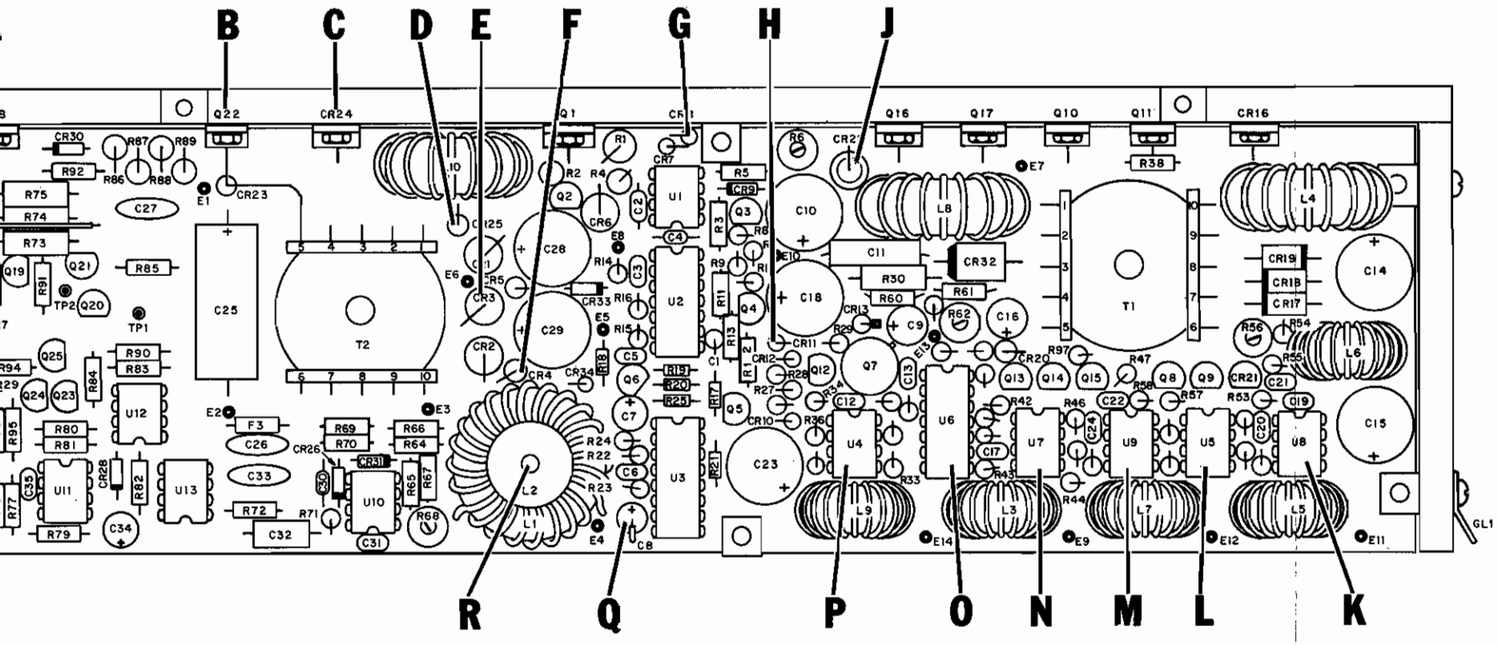


DETAIL **O**

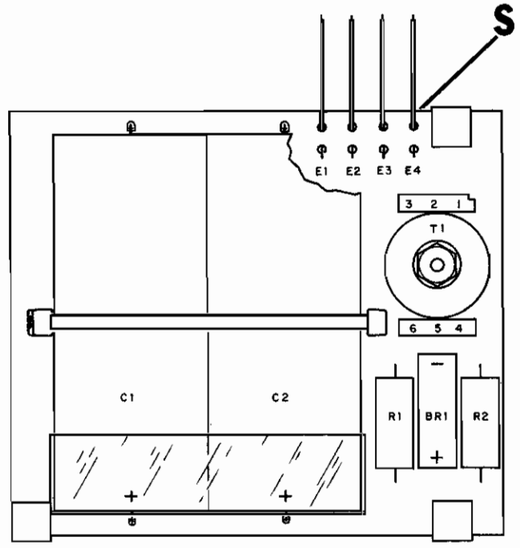


DETAIL **P**

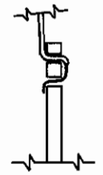
Figure 5-7 Power Supp
(D-0000-53



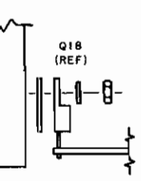
POWER SUPPLY PC BOARD



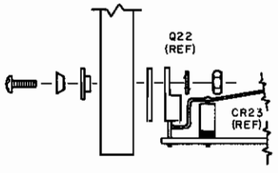
LINE RECTIFIER PC BOARD



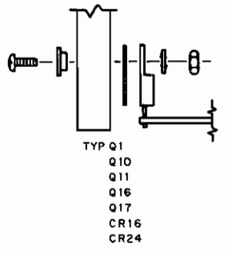
DETAIL **S**



IL **A**



DETAIL **B**



DETAIL **C**



DETAIL **D**



DETAIL **E**



DETAIL **F**



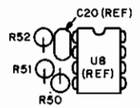
DETAIL **G**



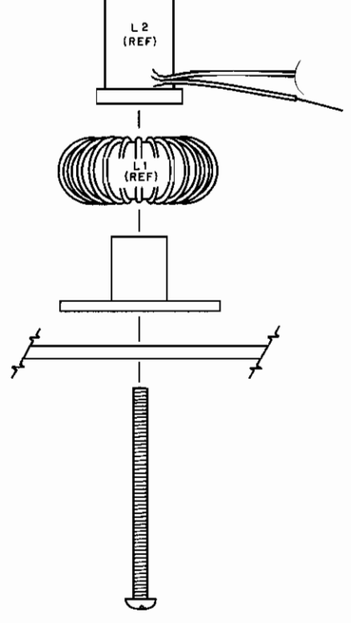
DETAIL **H**



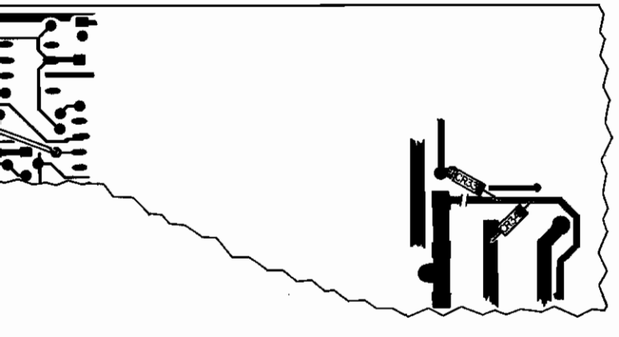
DETAIL **J**



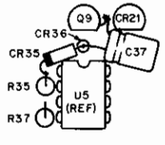
DETAIL **K**



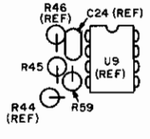
DETAIL **R**



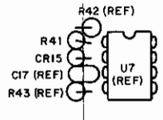
POWER SUPPLY PC BOARD (BOTTOM)



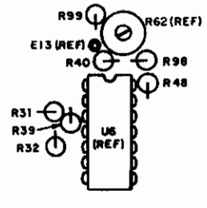
DETAIL **L**



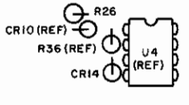
DETAIL **M**



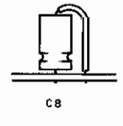
DETAIL **N**



DETAIL **O**

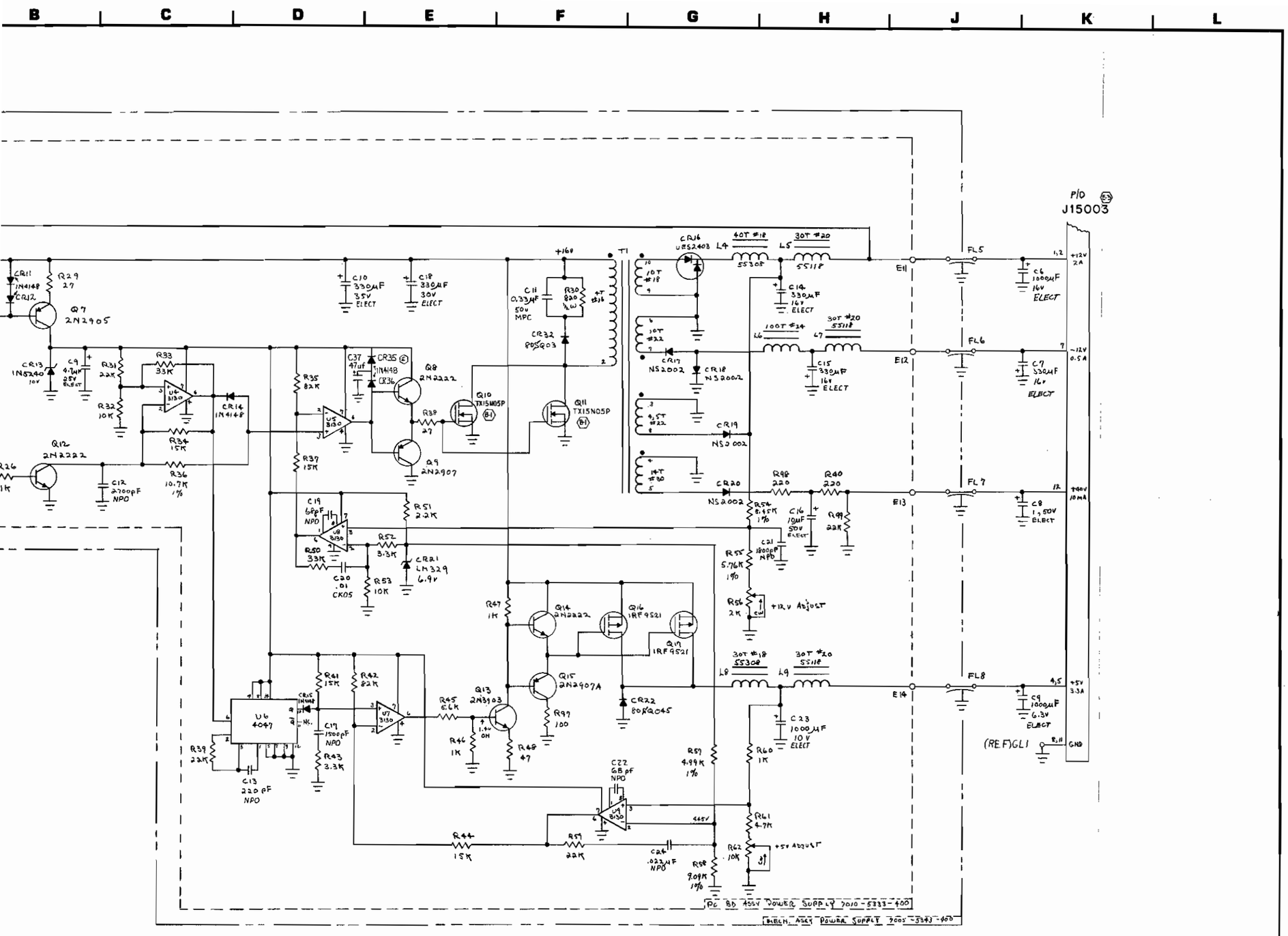


DETAIL **P**



DETAIL **Q**

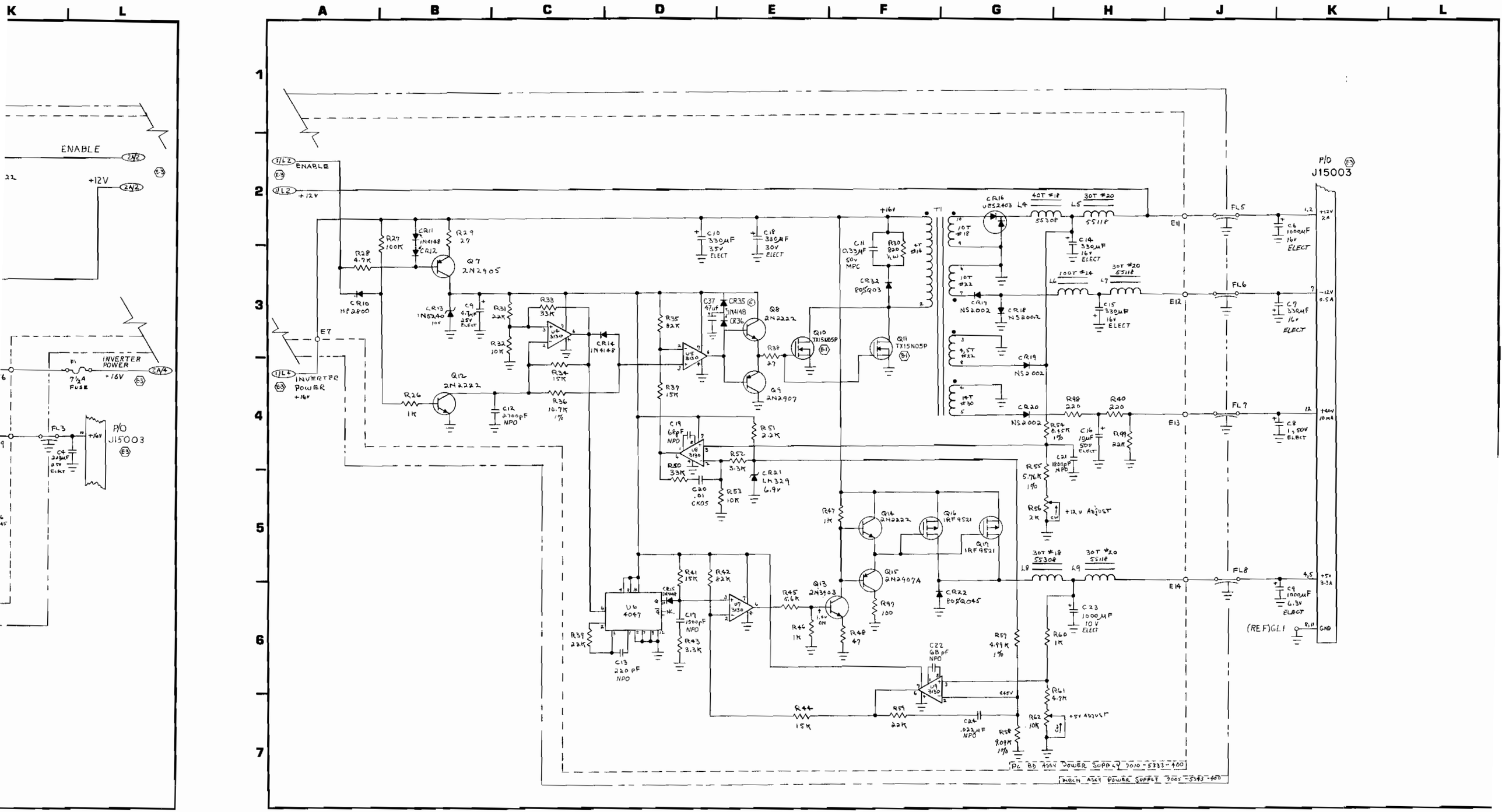
Figure 5-7 Power Supply Module (Sheet 1 of 2)
(D-0000-5313-400-E4)



NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. POWER SUPPLY PC BD - 17000 (E.G., R1 IS R17001).
   - B. LINE RECTIFIER PC BD -16000 (E.G., R1 IS R16001).
   - C. MECH ASSY - 15000.
2. ALL RESISTORS ARE 1/4 W, 5%, TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS (UNLESS SPECIFIED).

Figure 5-7 Power Supply Module (Sheet 2 of 2) (D-0000-5313-400-E4)


ENABLE
+12V
INVERTER POWER
7½A FUSE
+16V
P/O J15003
INVERTER POWER +16V
+12V 2A
+16V 10mA
+5V 3.3A
GND
(REF)GL1
PC BD ASSY POWER SUPPLY 7010-5333-400
MECH ASSY POWER SUPPLY 7005-5343-400

Figure

P/O J15003

BATT ON

BATT

J15004

EXT DC

N/C

J15001

J15002

AC POWER

SERIES 16000 PC BD ASSY LINE RECTIFIER 7010-4831-700

FLOATING GROUND

BIFILER WOUND INDUCTOR

BR1 PH60

L1 30T #18 TOROID

L2 160T #22 BWN TOROID

CR1 80SQ045

CR2 80SQ045

CR3 80SQ045

CR4 80SQ045

CR5 NS2002

CR6 80SQ045

CR6 NS2002

CR7 CR8 1N4148

CR23 1N4997

CR24 1N4148

CR25 NS2002

CR26 UES2403

CR27 1N5245

CR28 1N4148

CR29 1N4148

CR30 1N4148

CR31 1N5231

CR33 1N4004

CR34 1N4004

Q1 2N6109

Q2 2N2907

Q4 2N2907

Q5 2N2222

Q6 2N2907

Q18 MJE13005

Q19 2N2222

Q20 2N3227

Q21 2N2907

Q22 MTP3N40

Q23 2N3905

Q24 2N3905

Q25 2N2222

U2B 4013

U3 4536

U10 3130

U11 3130

U12 3130

U13 6N135

U14 741

ENABLE

+12V

INVERTER POWER +16V

+16V ADJUST

+5.1V CR9 LM329

+15V

TP1

TP2

T2 35.5T #22

L3 30T #20 5511B

L10 30T #18 5511B 4μH

T3 #22

F3 3A PICO

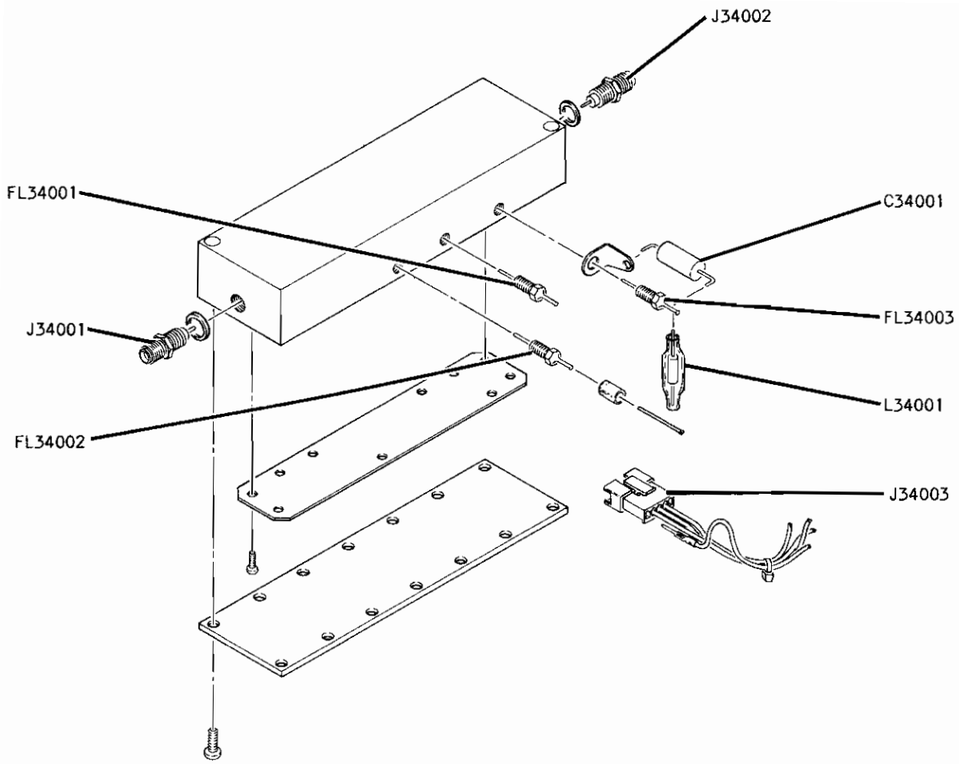
FL1 FL2 FL3 FL4

GL1

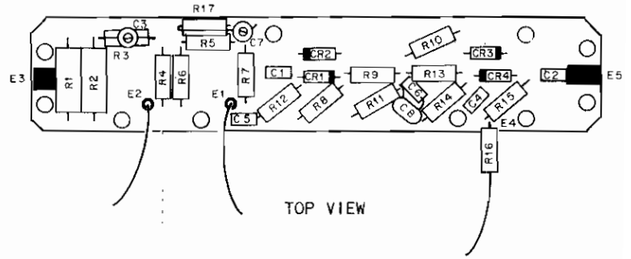
R101 33Ω ½W

PC BD ASSY POWER SUPPLY 7010-5338-400

MECH ASSY POWER SUPPLY 7005-5349-400



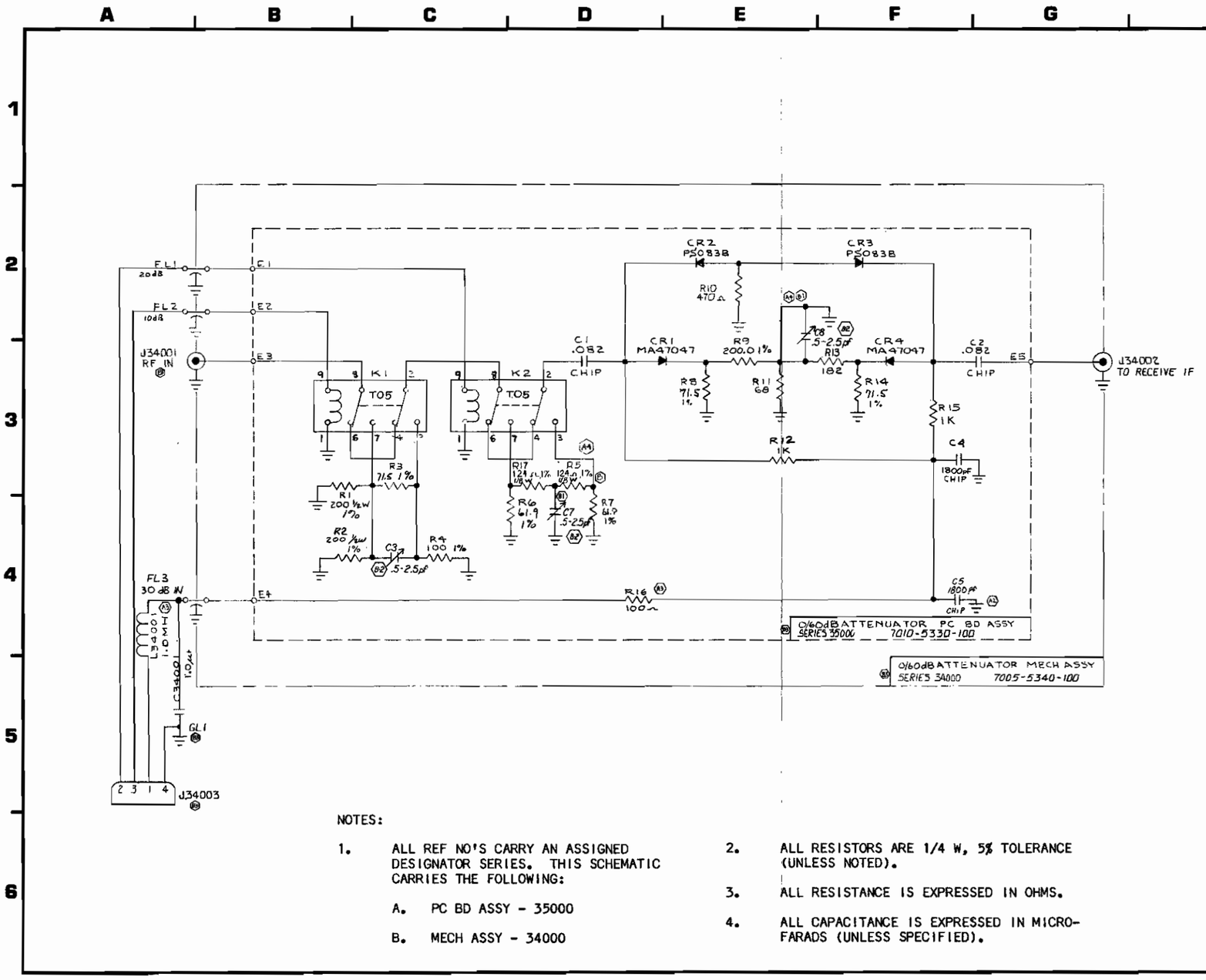
0-60 dB INPUT ATTENUATOR ASSY





BOTTOM VIEW

0-60 dB PC BOARD



NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. PC BD ASSY - 35000
   - B. MECH ASSY - 34000
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS SPECIFIED).

Figure 5-8 Attenuator Input Module, 0-60 dB (D-0000-5310-100-B4)

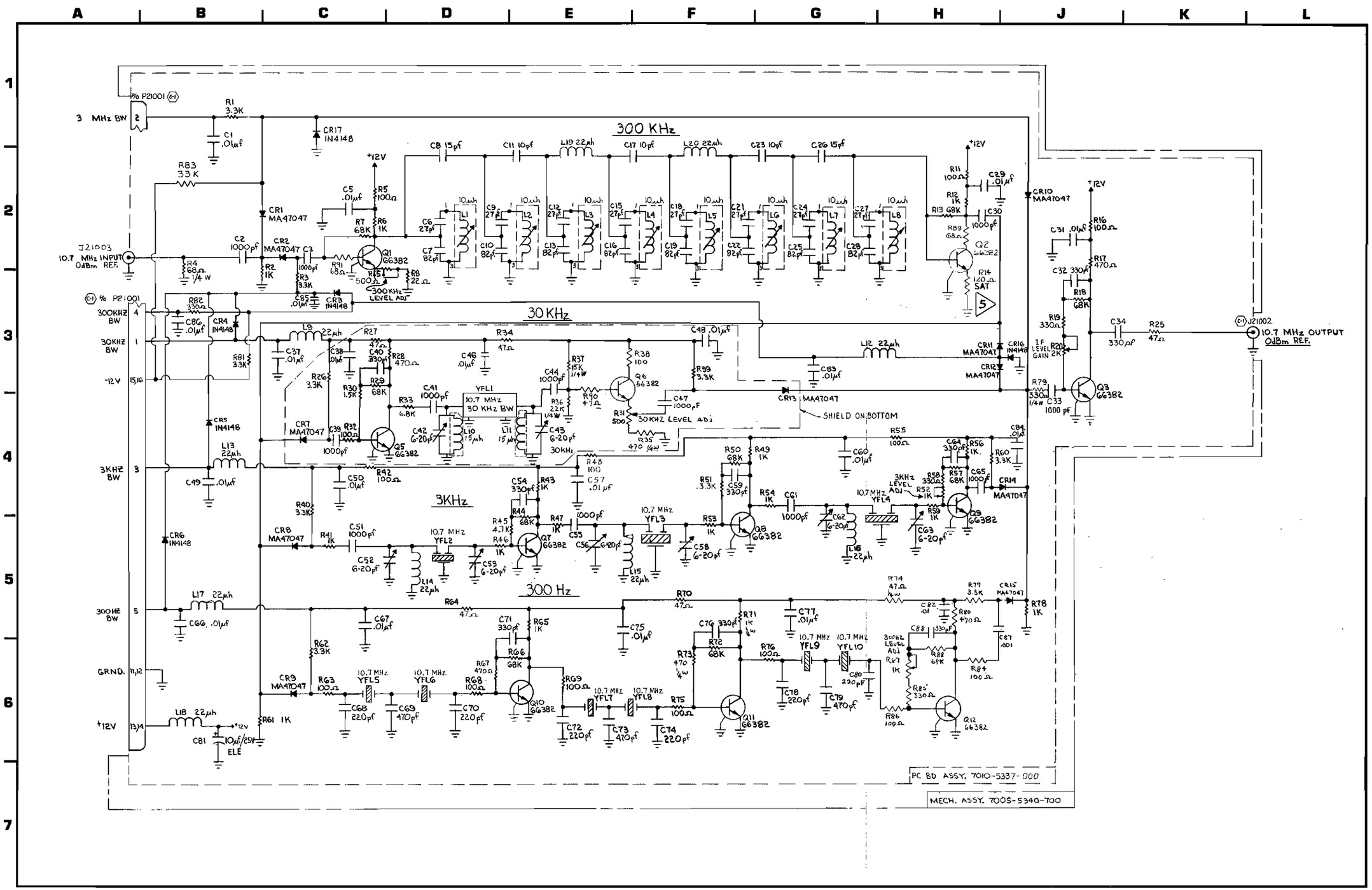
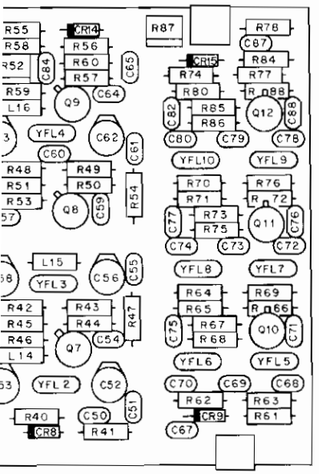
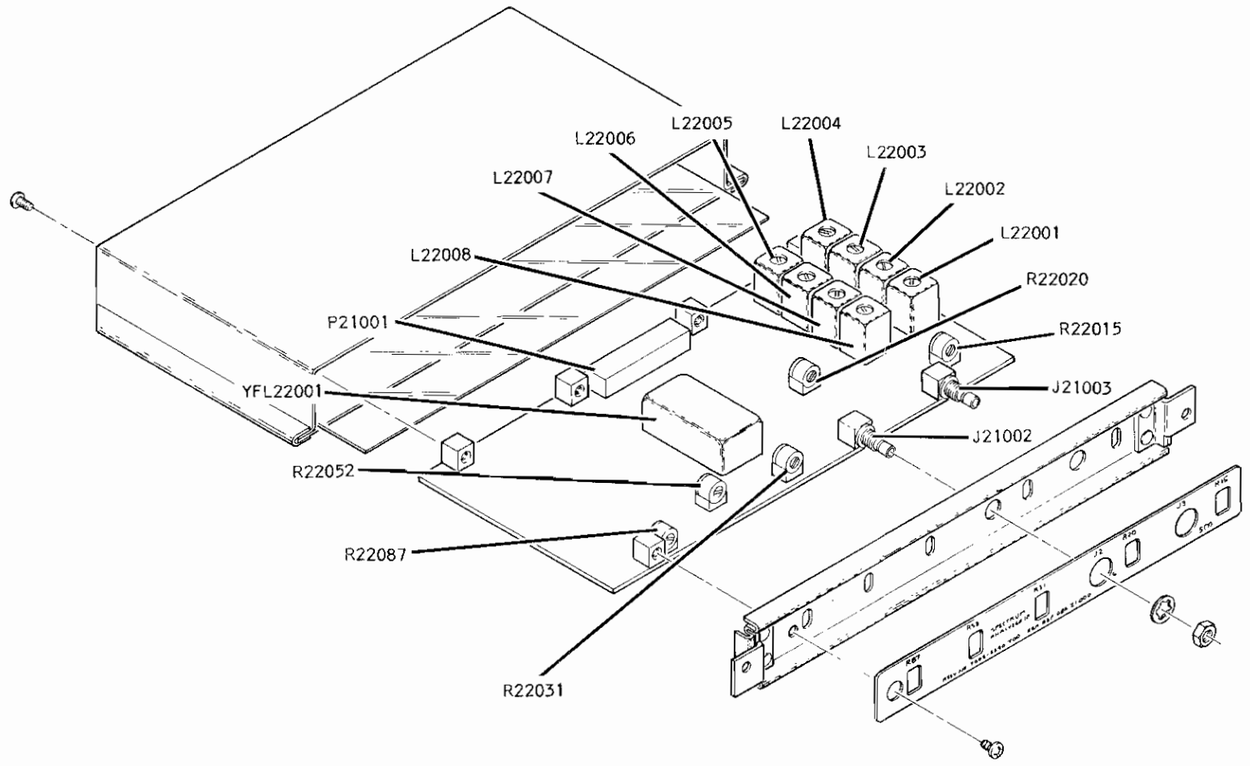


Figure 5-9 Analyzer IF Module
(D-0000-5317-000-C1)





ANALYZER IF ASSY

NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. PC BD ASSY - 22000 (R1 IS R22001).

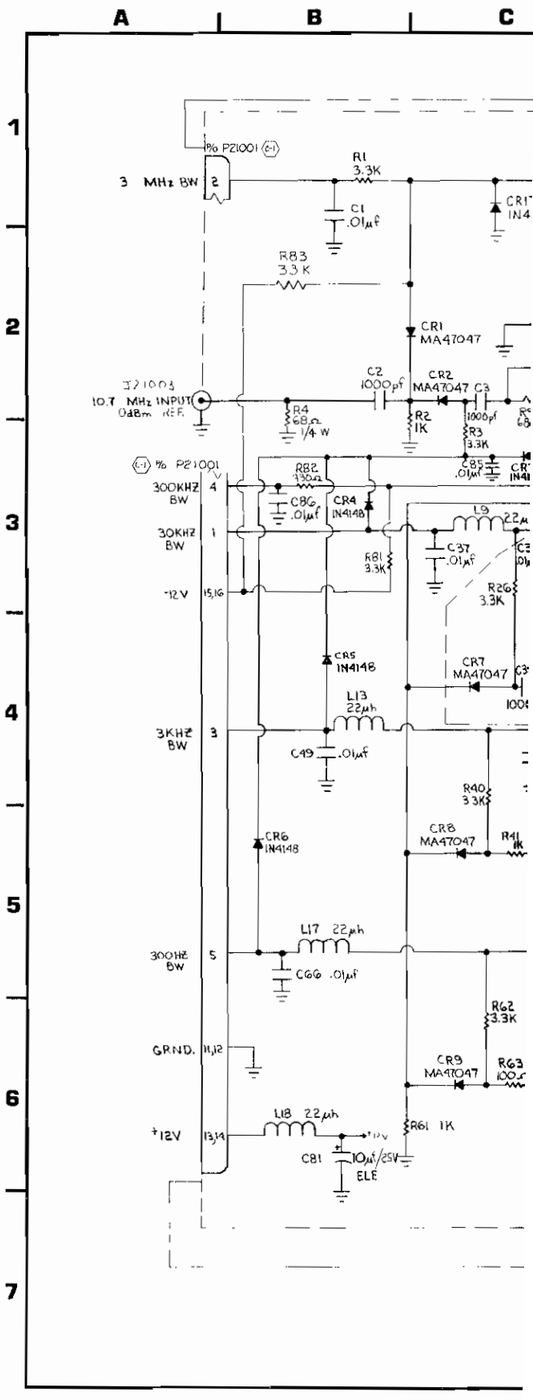
   B. MECH ASSY - 21000 (J1 IS J21001).

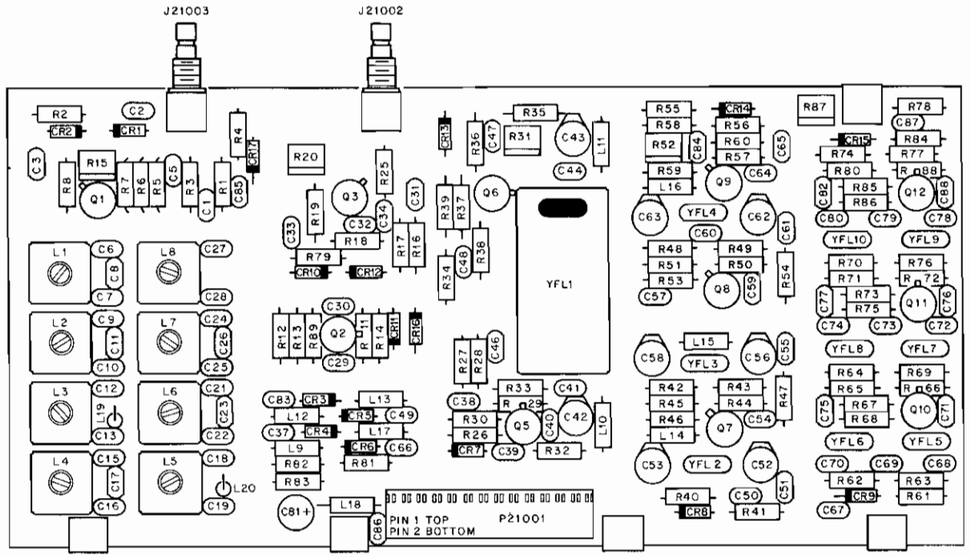
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

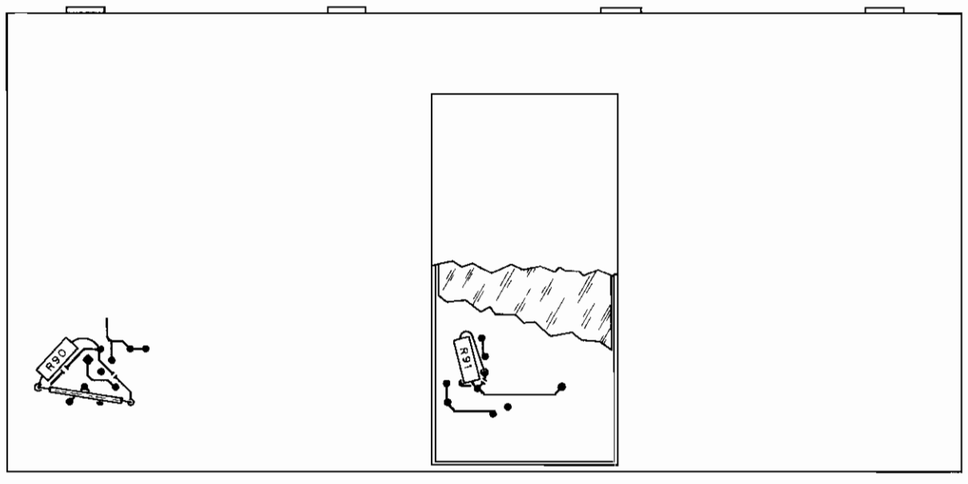
4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS SPECIFIED).

5. R22014 IS SELECTED AT TEST (S.A.T.) NOMINAL VALUE IS 120 OHMS. RANGE IS 68 TO 120 OHMS.



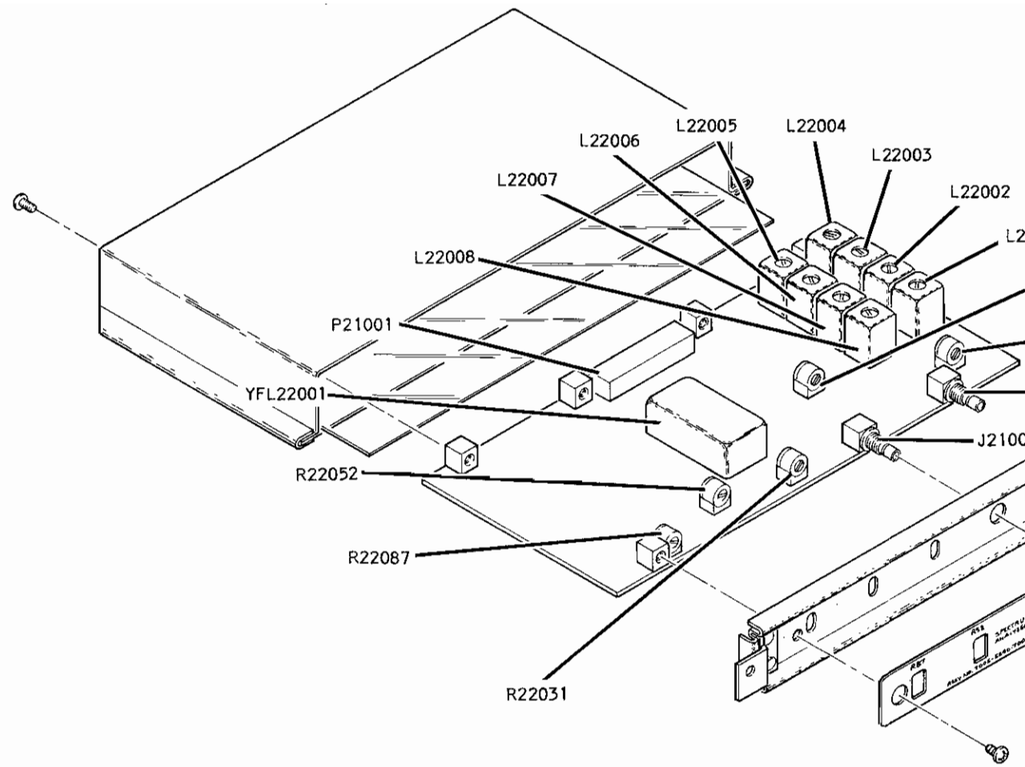


TOP VIEW



BOTTOM VIEW

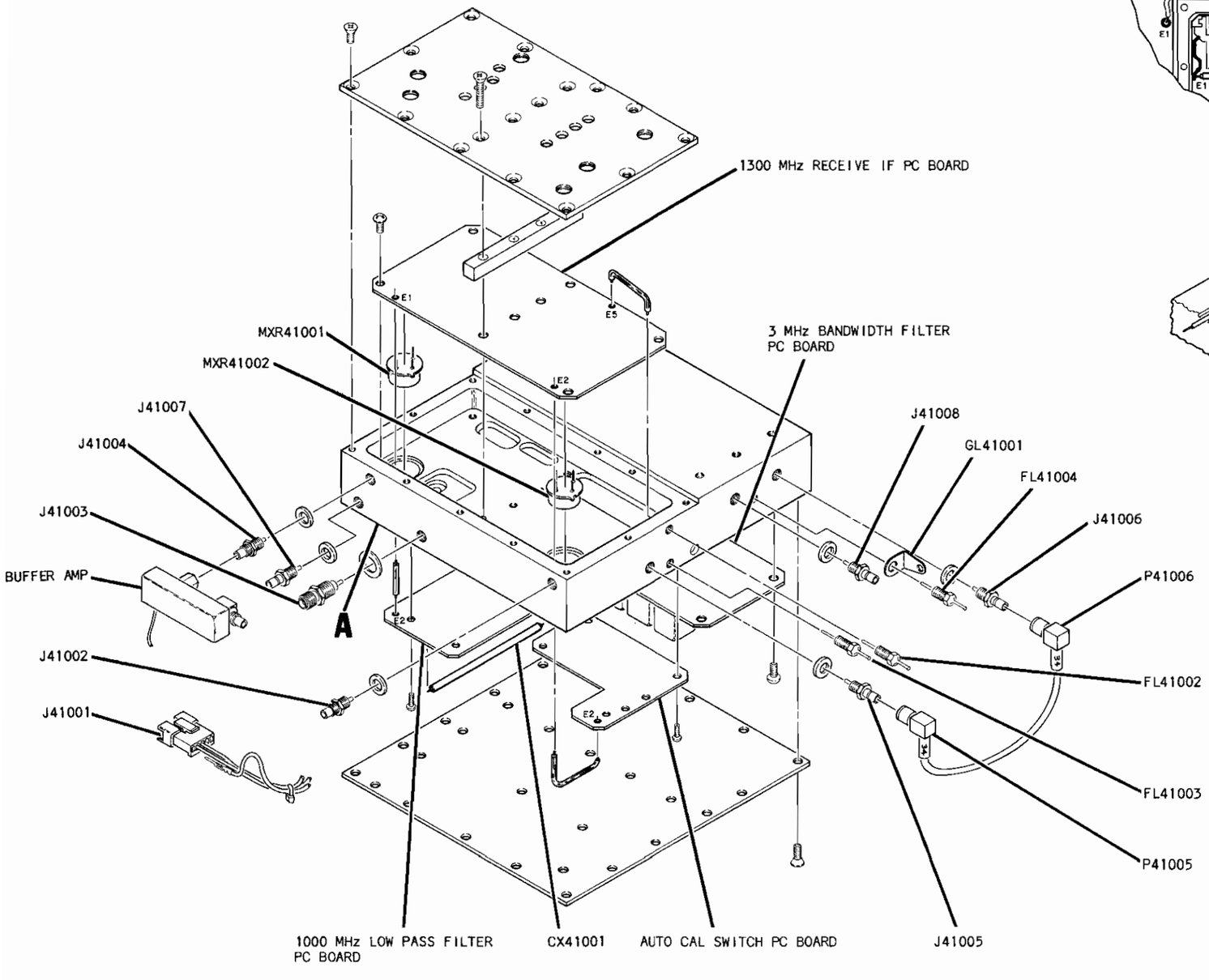
ANALYZER IF PC BOARD



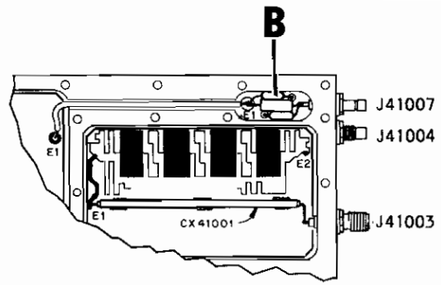
ANALYZER IF ASSY

NOTES:

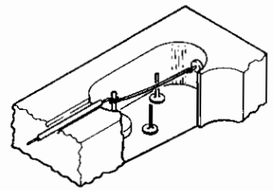
1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. PC BD ASSY - 22000 (R1 IS R22001).
   - B. MECH ASSY - 21000 (J1 IS J21001).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS (UNLESS SPECIFIED).
5. R22014 IS SELECTED AT TEST (S.A.T.) NOMINAL VALUE IS 120 OHMS. RANGE IS 68 TO 120 OHMS.



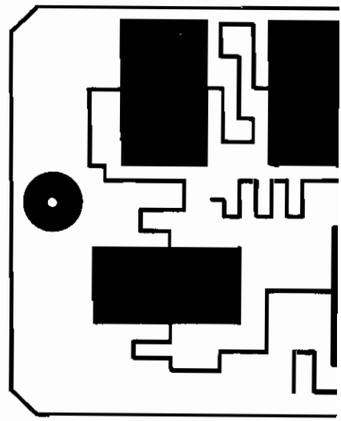
RECEIVE IF ASSY



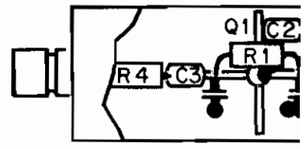
DETAIL **A**



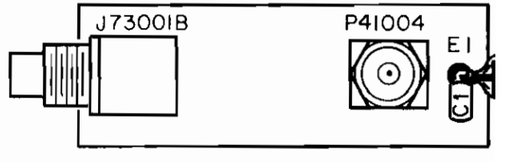
DETAIL **B**



1000 MHz LOW PASS FILT

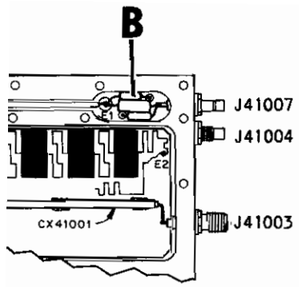


TOP VIEW

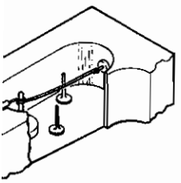


BOTTOM VIE

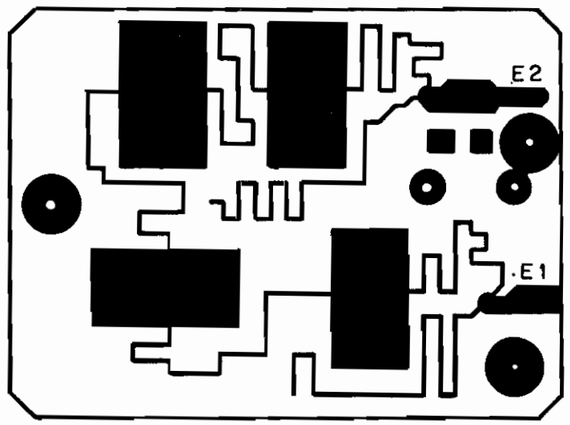
BUFFER AMP A



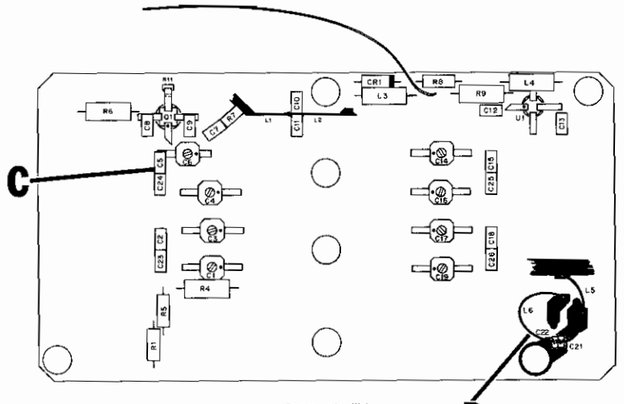
TAIL **A**



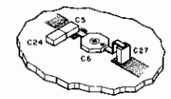
ETAIL **B**



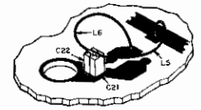
1000 MHz LOW PASS FILTER PC BOARD



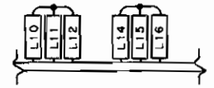
TOP VIEW



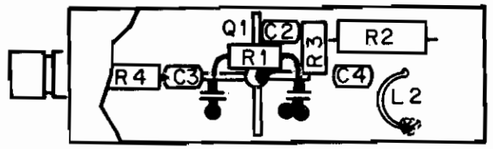
DETAIL **C**



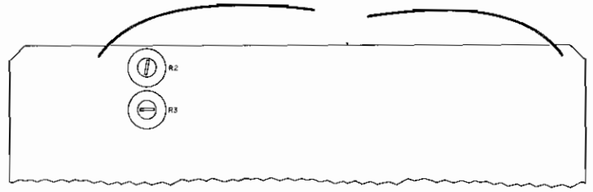
DETAIL **D**



DETAIL **E**

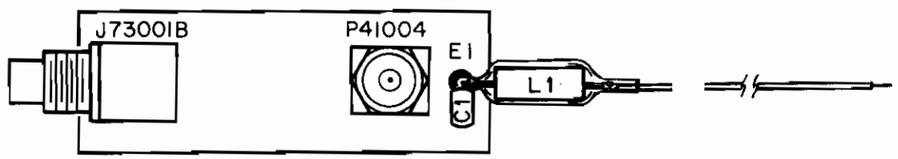


TOP VIEW



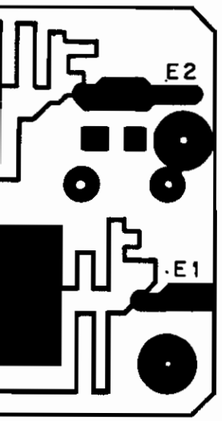
BOTTOM VIEW

1300 MHz RECEIVE IF PC BOARD

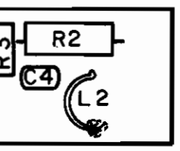


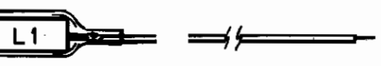
BOTTOM VIEW

BUFFER AMP ASSY

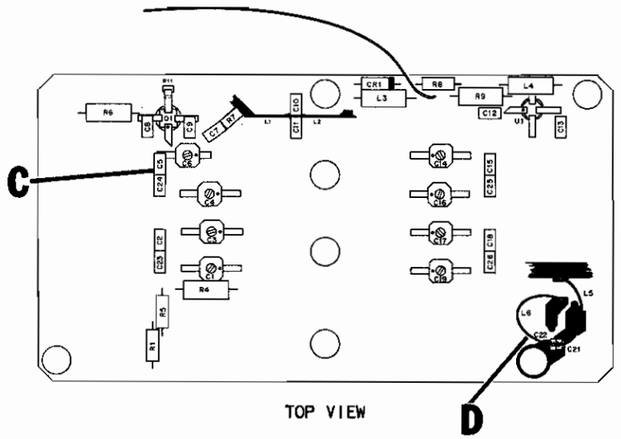


ER PC BOARD

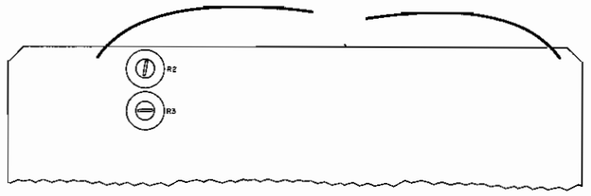




SY

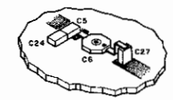


TOP VIEW

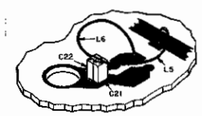


BOTTOM VIEW

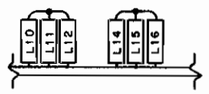
1300 MHz RECEIVE IF PC BOARD



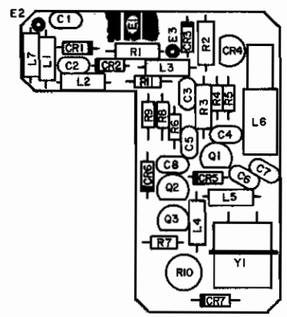
DETAIL **C**



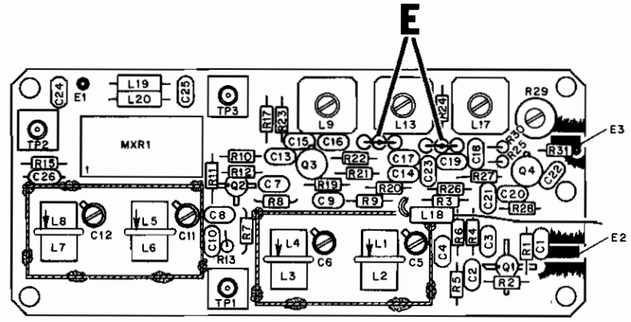
DETAIL **D**



DETAIL **E**



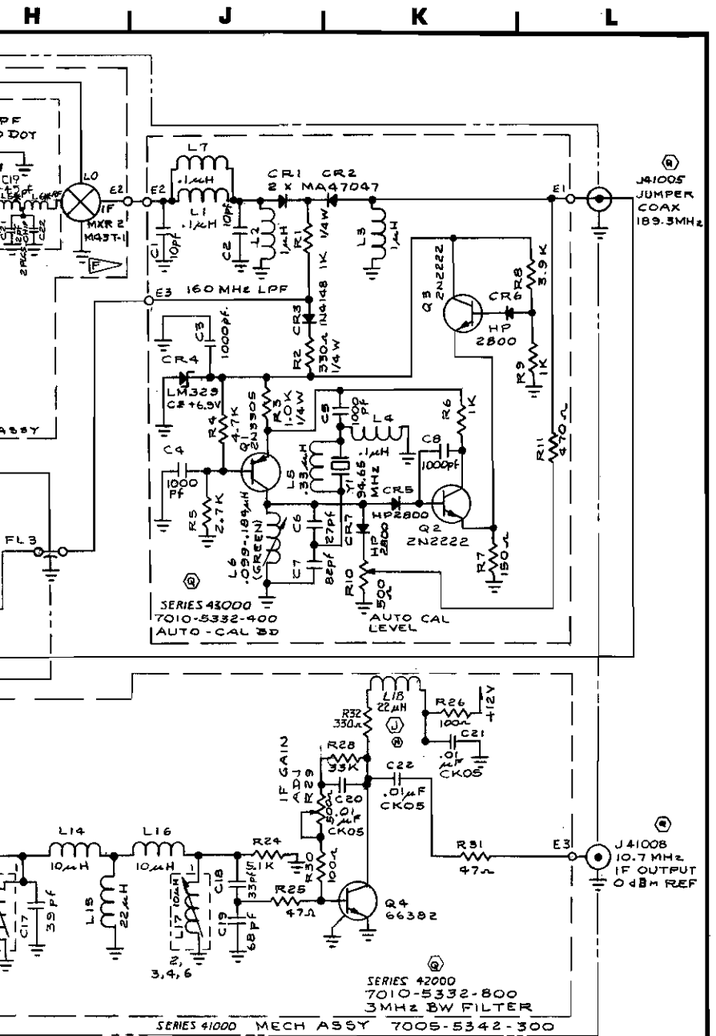
AUTO CAL SWITCH PC BOARD



S/N 1051 & ON

3 MHz BANDWIDTH FILTER PC BOARD

Figure 5-10 Receive IF Module (Sheet 1 of 2)
(D-0000-5312-300-R)



NOTES:

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. BUFFER AMP - 73000 (E.G., R1 IS R73001).

   B. RECV IF BD - 45000 (E.G., R1 IS R45001).

   C. AUTO CAL BD - 43000 (E.G., R1 IS R43001).

   D. 3 MHz FILTER BD - 42000 (E.G., R1 IS R42001).

   E. MECH ASSY - 41000 (E.G., J1 IS J41001).

2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).

3. ALL RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).

4. ALL CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS NOTED).

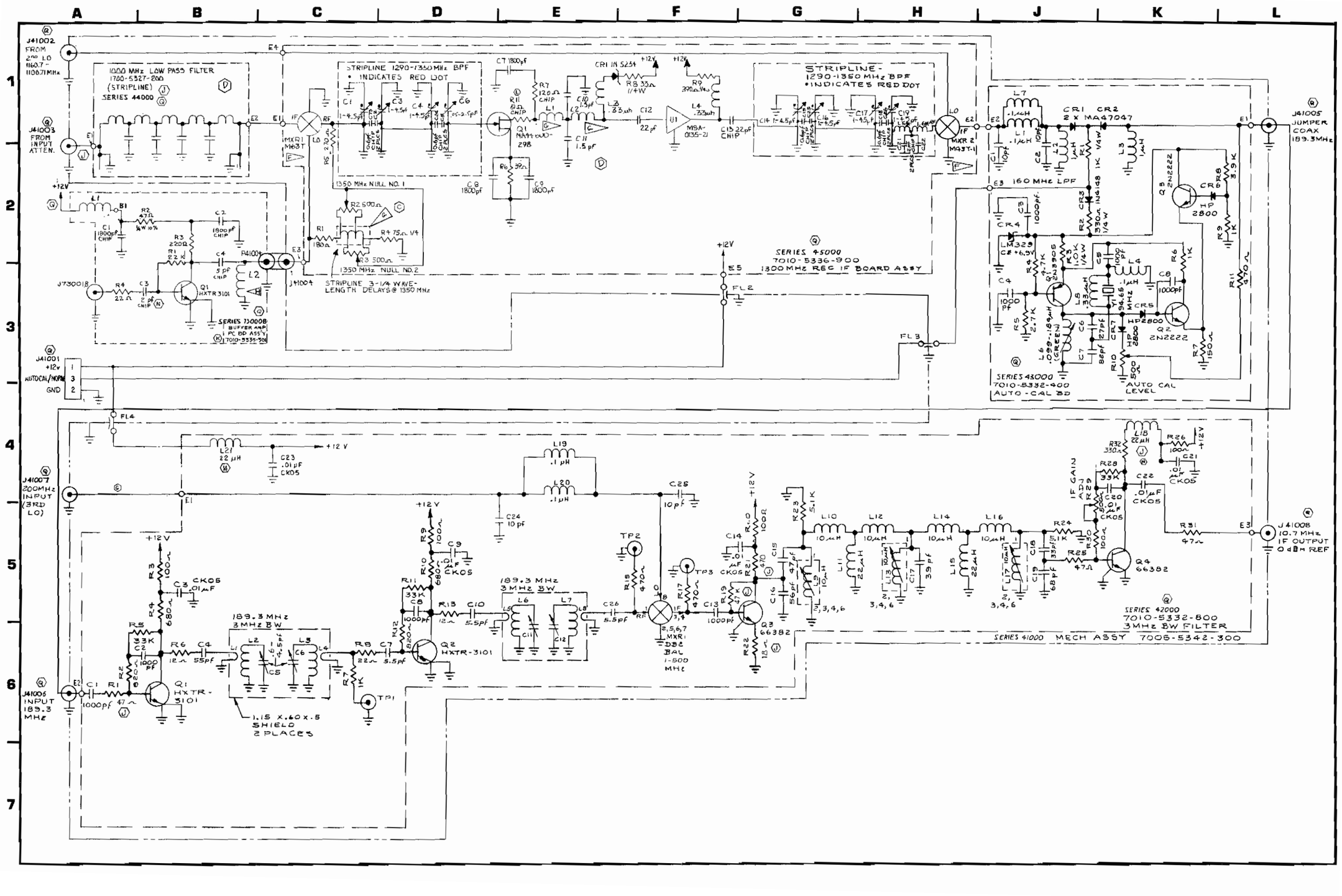
5. A THRU E NOT USED.

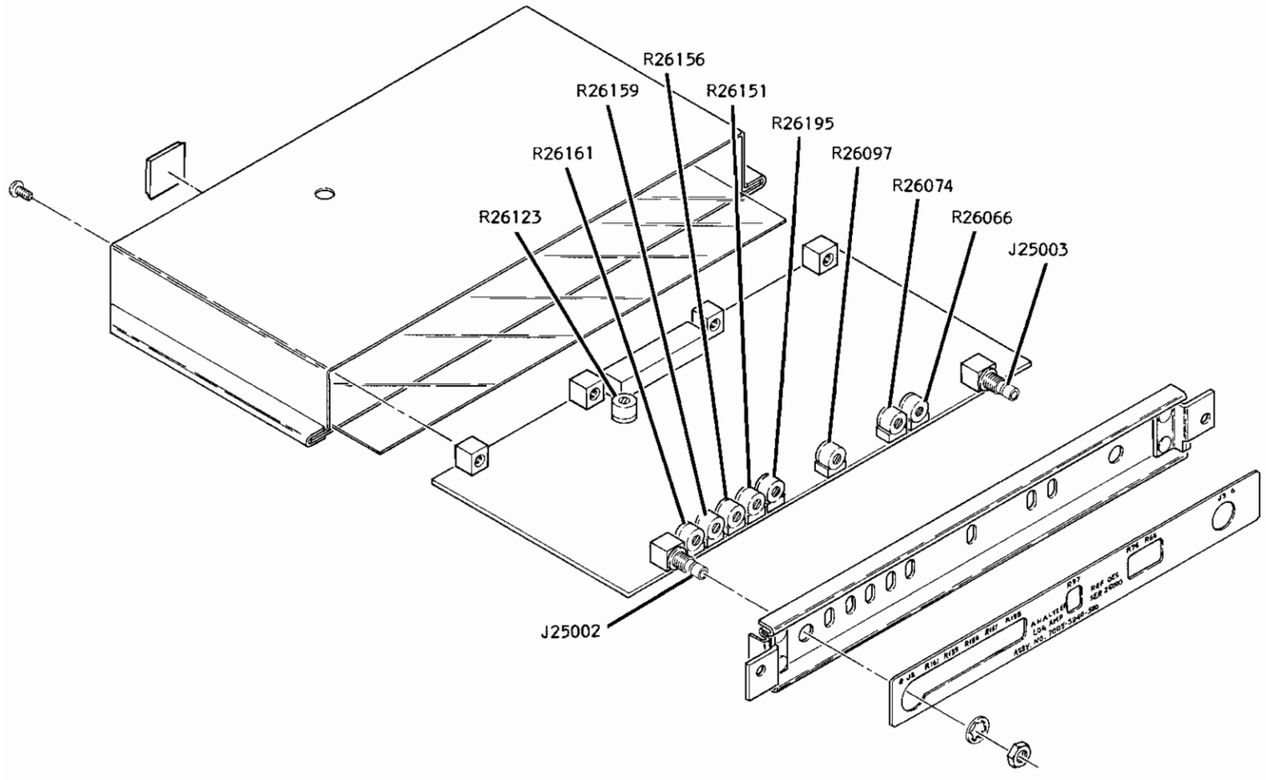
F. MXR41001 & MXR41002 INSTALLED AT MECH ASSY LEVEL.

G. INDUCTORS ARE PRINTED ON CIRCUIT BOARD.

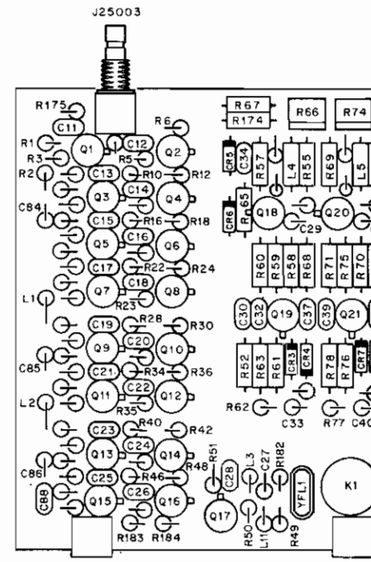
H. L73002 IS A .5" LOOP OF 22 AWG BUS WIRE.

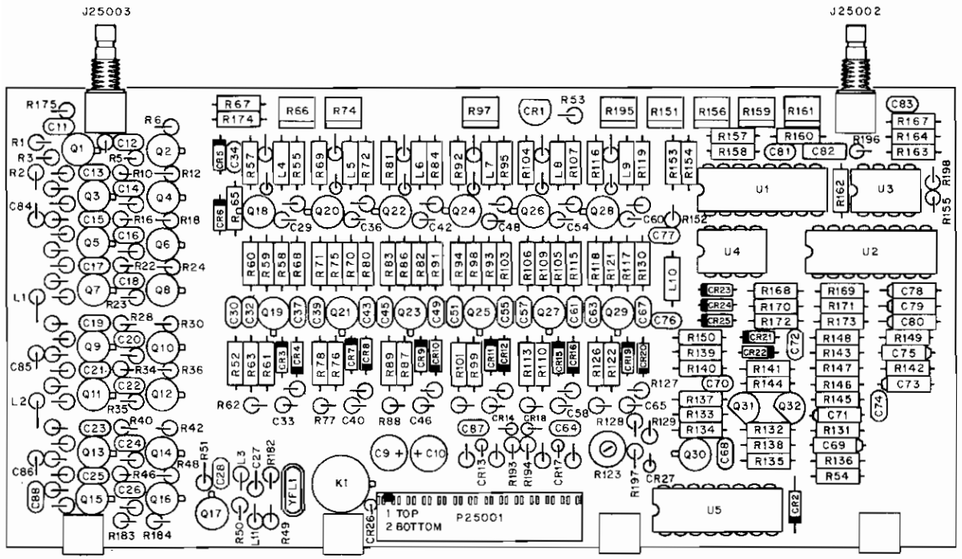
Figure 5-10 Receive IF Module (Sheet 2 of 2) (D-0000-5312-300-R)


A
B
C
D
E
F
G
H
J
K
L
1
2
3
4
5
6
7
J41002 FROM 2ND LO 1160.7 - 1106.71MHz
J41003 FROM INPUT ATTEN.
1000 MHz LOW PASS FILTER 1700-5327-200 (STRIPLINE) SERIES 44000
STRIPLINE 1290-1350MHz BPF • INDICATES RED DOT
1350 MHz NULL NO. 1
1350 MHz NULL NO. 2
STRIPLINE 3-1/4 WAVE-LENGTH DELAYS @ 1350 MHz
MXR1 M63T
MXR 2 MA5T-1
Q1 NMT1000-298
U1 MSA-0335-2J
CR1 1N 5234
+12V
SERIES 45000 7010-5336-900 1300MHz REC IF BOARD ASSY
J41004
J730018
P41004
Q1 HXTR 3101
SERIES 73000B BUFFER AMP PC BD ASSY 7010-5336-501
J41001 +12v AUTOCAL/NORM GND
FL2
FL3
FL4
J41005 JUMPER COAX 189.3MHz
E3 160 MHz LPF
CR1 CR2 2 x MA47047
LM329
Q1 2N3905
Q2 2N2222
Q5 2N2222
HP 2800
SERIES 43000 7010-5332-400 AUTO-CAL BD
AUTO CAL LEVEL
J41007 200MHz INPUT (3RD LO)
L21 22 µH
C23 .01µF CK05
L19 .1 µH
L20 .1 µH
C24 10 pf
C25 10pf
J41006 INPUT 189.3 MHz
Q1 HXTR-3101
Q2 HXTR-3101
189.3 MHz 3MHz BW
1.15 X.60 X.5 SHIELD 2 PLACES
TP1
TP2
TP3
2,5,6,7 MXR1 DBL BAL 1-500 MHz
Q3 66382
Q4 66382
SERIES 42000 7010-5332-800 3MHz BW FILTER
SERIES 41000 MECH ASSY 7005-5342-300
J41008 10.7 MHz IF OUTPUT 0 dBm REF

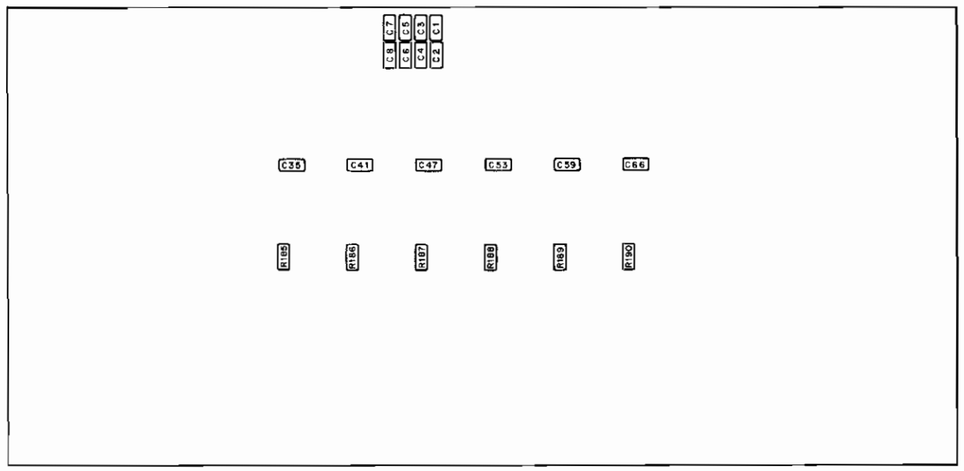

R26156
R26159
R26151
R26195
R26161
R26097
R26074
R26123
R26066
J25003
J25002

LOG AMP ASSY


J25003
R175
C11
R1
R3
R2
Q1
C12
R5
R6
Q2
C13
R10
R12
Q3
C14
Q4
C84
C15
R16
R18
C16
Q5
Q6
C17
R22
R24
C18
Q7
Q8
L1
R23
C19
R28
R30
Q9
C20
Q10
C85
C21
R34
R36
L2
Q11
C22
Q12
R35
R40
R42
C23
Q13
C24
Q14
C86
C25
R46
R48
C88
Q15
C26
Q16
R183
R184
Q17
R50
L11
R49
C28
L3
C27
R182
YFL1
K1
R67
R174
R66
R74
C83
C34
R57
L4
R55
R69
L5
C85
R65
Q18
Q20
C29
R60
R59
R58
R71
R75
R70
C30
C32
Q19
C37
C39
Q21
R52
R63
R61
C43
C44
R78
R76
C47
R62
C33
R77
C40

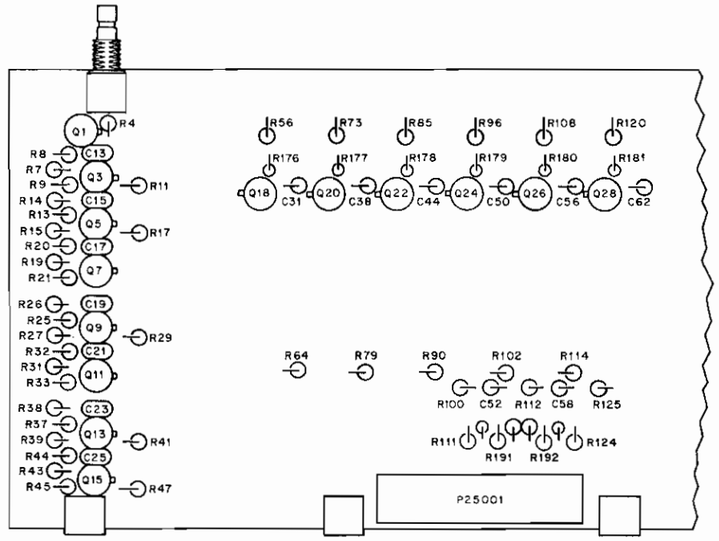


(TOP VIEW)



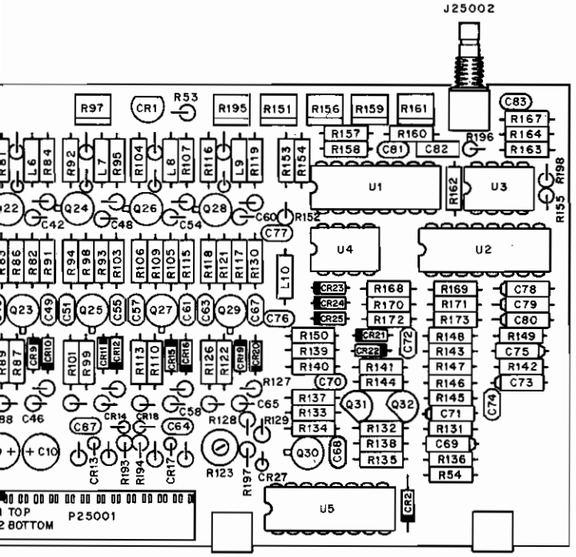
(BOTTOM VIEW)

LOG AMP PC BOARD

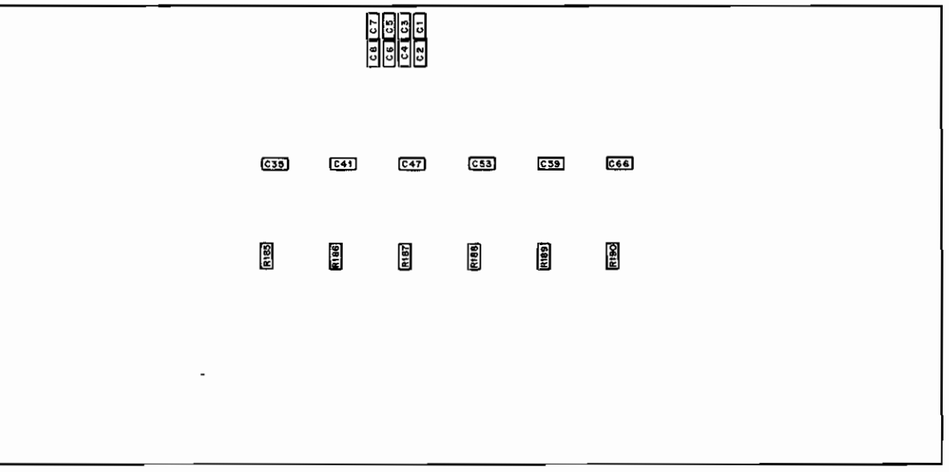


LOG AMP PC BOARD DETAILS (TOP)

Figure 5-11 Lo
(D

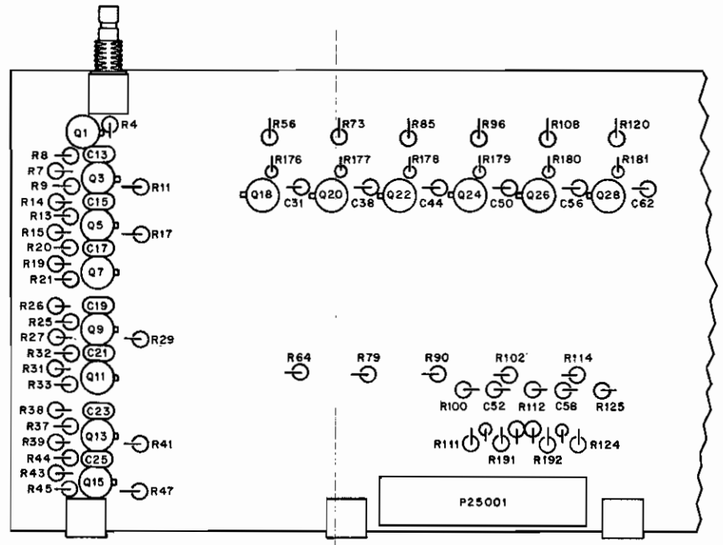


(TOP VIEW)



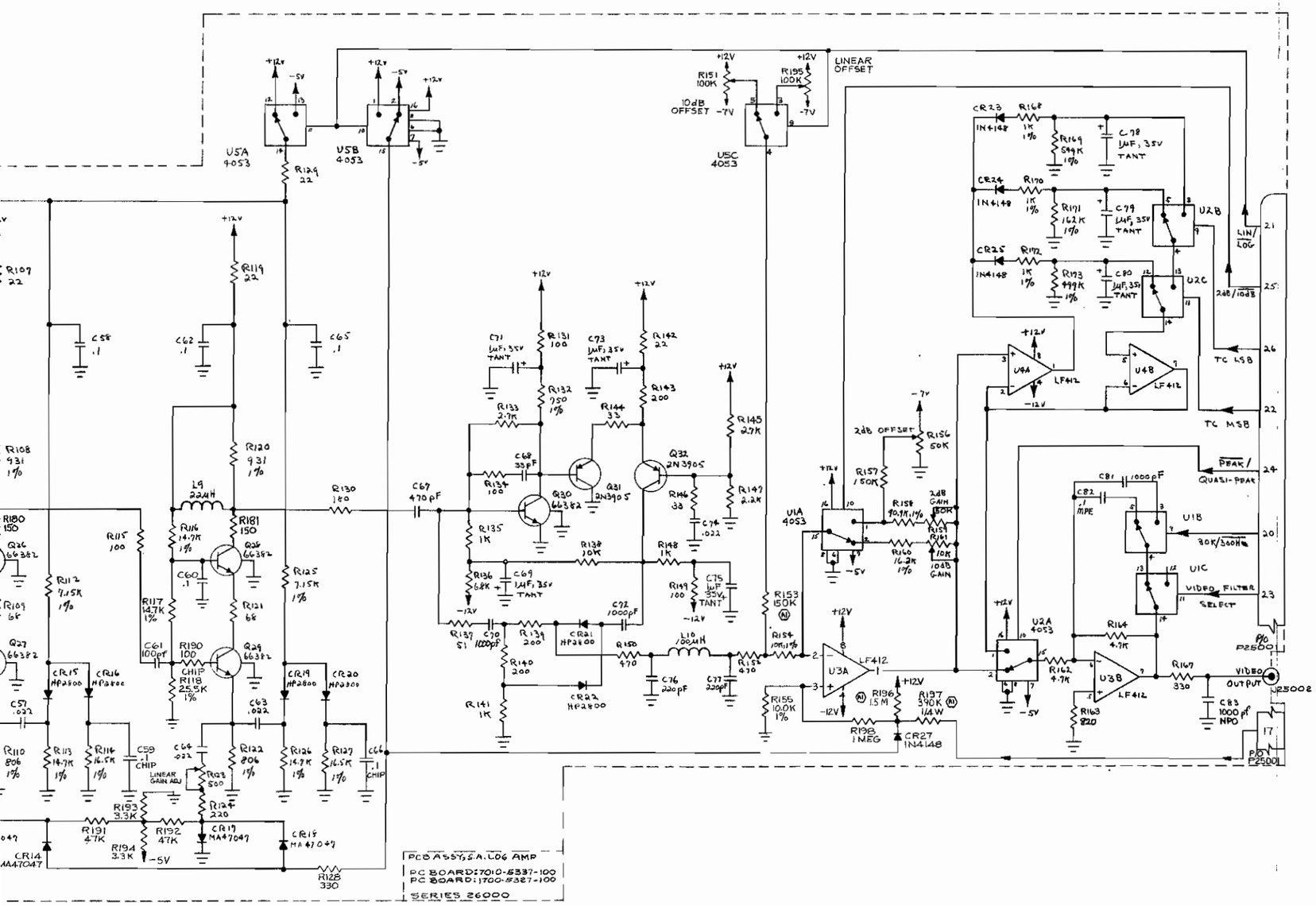
(BOTTOM VIEW)

LOG AMP PC BOARD



LOG AMP PC BOARD DETAILS (TOP)

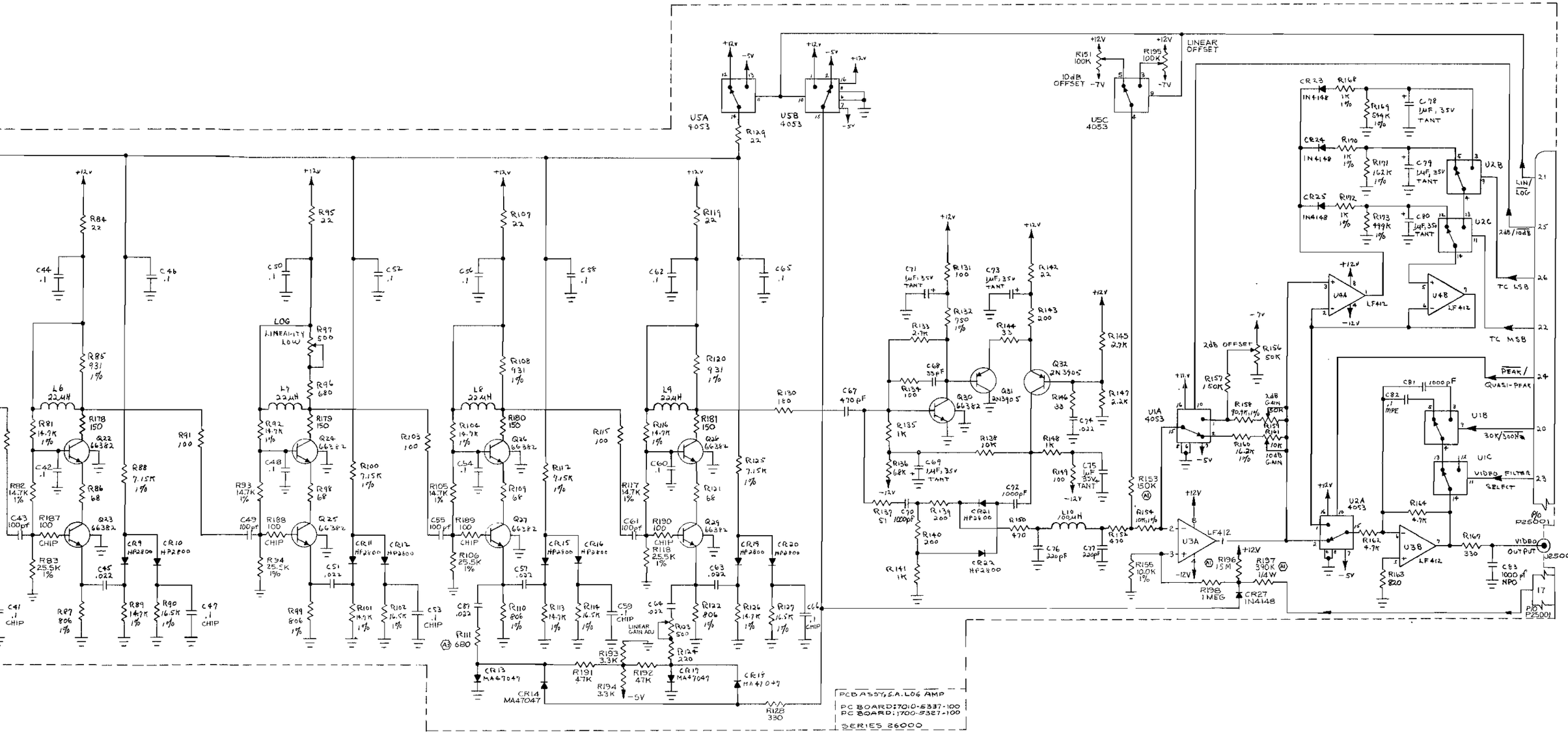
Figure 5-11 Log Amp Module (Sheet 1 of 2)
(D-0000-5317-100-A4)

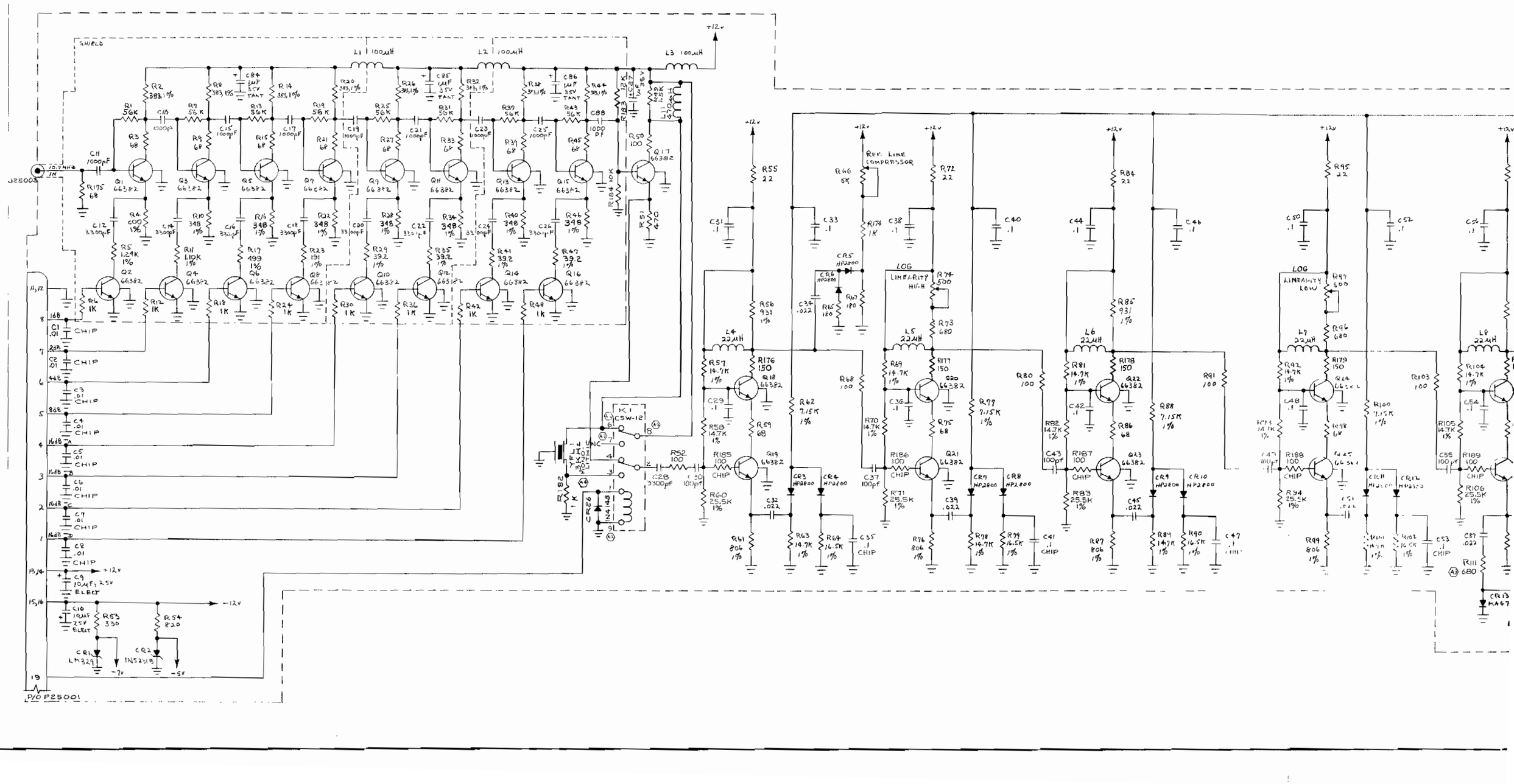


NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. LOG AMP PC BD - 26000 (E.G., R1 IS R26001).
   - B. MECH ASSY - 25000 (E.G., J1 IS J25001).
2. ALL RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS SPECIFIED).
3. RESISTANCE IS EXPRESSED IN OHMS.
4. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS SPECIFIED).

Figure 5-11 Log Amp Module (Sheet 2 of 2) (D-0000-5317-100-A4)


+12V
-5V
-7V
-12V
U5A 4053
U5B 4053
U5C 4053
R129 22
R84 22
R95 22
R107 22
R119 22
R130 180
C67 470pF
C44 .1
C46 .1
C50 .1
C52 .1
C56 .1
C58 .1
C62 .1
C65 .1
R85 931 1%
R96 680
R108 931 1%
R120 931 1%
LOG LINEARITY ADJ
R97 500
L6 22μH
L7 22μH
L8 22μH
L9 22μH
R81 14.7K 1%
R178 150
Q22 66382
R92 14.7K 1%
R179 150
Q24 66382
R104 14.7K 1%
R180 150
Q26 66382
R116 14.7K 1%
R181 150
Q28 66382
C42 .1
C48 .1
C54 .1
C60 .1
R88 7.15K 1%
R91 100
R100 7.15K 1%
R103 100
R112 7.15K 1%
R115 100
R125 7.15K 1%
R86 68
R98 68
R109 68
R121 68
R82 14.7K 1%
R93 14.7K 1%
R105 14.7K 1%
R117 14.7K 1%
C43 100pF
R187 100 CHIP
Q23 66382
C49 100pF
R188 100 CHIP
Q25 66382
C55 100pF
R189 100 CHIP
Q27 66382
C61 100pF
R190 100 CHIP
Q29 66382
R83 25.5K 1%
R94 25.5K 1%
R106 25.5K 1%
R118 25.5K 1%
C45 .022
C51 .022
C57 .022
C63 .022
CR9 HP2800
CR10 HP2800
CR11 HP2800
CR12 HP2800
CR15 HP2800
CR16 HP2800
CR19 HP2800
CR20 HP2800
R89 14.7K 1%
R90 16.5K 1%
R99 806 1%
R101 14.7K 1%
R102 16.5K 1%
R110 806 1%
R113 14.7K 1%
R114 16.5K 1%
R122 806 1%
R126 14.7K 1%
R127 16.5K 1%
C47 .1 CHIP
C53 .1 CHIP
C59 .1 CHIP
C64 .022
C66 .1 CHIP
C87 .022
R111 680
R103 500
LINEAR GAIN ADJ
R124 220
R193 3.3K
R191 4.7K
R192 47K
R194 3.3K
CR13 MA47047
CR14 MA47047
CR17 MA47047
CR18 MA47047
R123 330
C41 .1 CHIP
R87 806 1%
C67 470pF
C71 1μF, 35V TANT
R131 100
R132 750 1%
R133 2.7K
C68 33pF
R134 100
R135 1K
R136 68K
C69 1μF, 35V TANT
C70 1000pF
R137 51
R139 200
R140 200
R141 1K
C73 1μF, 35V TANT
R142 22
R143 200
R144 33
Q32 2N3905
Q31 2N3905
Q30 66382
R145 2.7K
R146 33
R147 2.2K
C74 .022
R138 10K
R148 1K
R149 100
C75 1μF 35V TANT
C92 1000pF
CR21 HP2800
CR22 HP2800
L10 100μH
R150 470
R152 470
C76 220pF
C77 220pF
R151 100K
10dB OFFSET -7V
R195 100K
LINEAR OFFSET
R153 150K
R154 10M 1%
R155 10.0K 1%
U3A LF412
R196 15M
R197 390K 1/4W
R198 1MEG
CR27 IN4148
U1A 4053
R156 50K
2dB OFFSET
R157 150K
R158 90.9K 1%
2dB GAIN
R159 50K
R160 16.2K 1%
R161 10K
10dB GAIN
CR23 IN4148
R168 1K 1%
R169 549K 1%
C78 1μF, 35V TANT
CR24 IN4148
R170 1K 1%
R171 162K 1%
C79 1μF, 35V TANT
CR25 IN4148
R172 1K 1%
R173 499K 1%
C80 1μF, 35V TANT
U2B
U2C
LIN/LOG
2dB/10dB
TC LSB
TC MSB
U4A LF412
U4B LF412
C81 1000pF
C82 .1 MPE
U1B
30K/300K
U1C
VIDEO FILTER SELECT
PEAK/QUASI-PEAK
U2A 4053
R162 4.7K
R163 820
R164 4.7K
R167 330
VIDEO OUTPUT
C83 1000pF NPO
P/O P25001
J25002
PCB A557, S.A. LOG AMP
PC BOARD: 7010-5337-100
PC BOARD: 1700-5327-100
SERIES 26000


SHIELD
L1 100uH
L2 100uH
L3 100uH
+12v
J25003
10.7MHz IN
C11 1000pF
R1 56K
R2 383 1%
R3 68
R4 600 1%
R5 1.24K 1%
R7 56K
R8 383 1%
R9 68
R10 348 1%
R11 1.10K 1%
R13 56K
R14 383 1%
R15 68
R16 348 1%
R17 499 1%
R19 56K
R20 383 1%
R21 68
R22 348 1%
R23 191 1%
R25 56K
R26 383 1%
R27 68
R28 348 1%
R29 39.2 1%
R31 56K
R32 383 1%
R33 68
R34 348 1%
R35 39.2 1%
R37 56K
R38 383 1%
R39 68
R40 348 1%
R41 39.2 1%
R43 56K
R44 383 1%
R45 68
R46 348 1%
R47 39.2 1%
C84 1uF 35V TANT
C85 1uF 35V TANT
C86 1uF 35V TANT
C88 1000 PF
R183 12K
R184 10K
L11 470uH
R50 100
Q17 66382
R51 470
Q1 66382
Q2 66382
Q3 66382
Q4 66382
Q5 66382
Q6 66382
Q7 66382
Q8 66382
Q9 66382
Q10 66382
Q11 66382
Q12 66382
Q13 66382
Q14 66382
Q15 66382
Q16 66382
R175 68
C12 33.0pF
C14 33.0pF
C16 330pF
C18 330pF
C20 330pF
C22 330pF
C24 330pF
C26 330pF
R12 1K
R18 1K
R24 1K
R30 1K
R36 1K
R42 1K
R48 1K
C15 1000pF
C17 1000pF
C19 1000pF
C21 1000pF
C23 1000pF
C25 1000pF
C13 1000pF
11,12
8 16B C1 .01 CHIP
7 28B C2 .01 CHIP
6 44B C3 .01 CHIP
5 86B C4 .01 CHIP
4 16B A C5 .01 CHIP
3 16B B C6 .01 CHIP
2 16B C C7 .01 CHIP
1 16B D C8 .01 CHIP
13,14 +12v
C9 10uF, 25V ELECT
15,16 -12v
C10 10uF 25V ELECT
R53 330
R54 820
CR1 LM329 -7v
CR2 IN5231B -5v
19
P/O P25001
K1 CSW-12
R182 1K
CR26 IN4148
C28 3300pF
R52 100
± 30 100pF
R55 22
C31 .1
R56 931 1%
L4 22uH
R57 14.7K 1%
R176 150
Q18 66382
C29 .1
R58 14.7K 1%
R59 68
R185 100 CHIP
Q19 66382
R60 25.5K 1%
R61 806 1%
C32 .022
R62 7.15K 1%
R63 14.7K 1%
R64 16.5K 1%
CR3 HP2800
CR4 HP2800
C35 .1 CHIP
R68 100
REF. LINE COMPRESSOR
R66 5K
R174 1K
C33 .1
CR5 HP2800
CR6 HP2800
C34 .022
R65 180
R67 180
R72 22
C38 .1
LOG LINEARITY HIGH
R74 500
R73 680
L5 22uH
R69 14.7K 1%
R177 150
Q20 66382
C36 .1
R75 68
R186 100 CHIP
Q21 66382
R70 14.7K 1%
C37 100pf
R71 25.5K 1%
R76 806 1%
C39 .022
R77 7.15K 1%
R78 14.7K 1%
R79 16.5K 1%
CR7 HP2800
CR8 HP2800
C41 .1 CHIP
R80 100
C40 .1
R84 22
L6 22uH
R81 14.7K 1%
R178 150
Q22 66382
C42 .1
R86 68
R187 100 CHIP
Q23 66382
R82 14.7K 1%
C43 100pf
R83 25.5K 1%
R87 806 1%
C45 .022
R85 931 1%
R88 7.15K 1%
R89 14.7K 1%
R90 16.5K 1%
CR9 HP2800
CR10 HP2800
C47 .1 CHIP
R91 100
C44 .1
C46 .1
R95 22
C50 .1
LOG LINEARITY LOW
R97 500
R96 680
L7 22uH
R92 14.7K 1%
R179 150
Q24 66382
C48 .1
R98 68
R188 100 CHIP
Q25 66382
R94 25.5K 1%
R99 806 1%
C51 .022
R93 7.15K 1%
R100 7.15K 1%
R101 14.7K 1%
R102 16.5K 1%
CR11 HP2800
CR12 HP2800
C53 .1 CHIP
R103 100
C52 .1
C56 .1
L8 22uH
R104 14.7K 1%
R180 150
Q26 66382
C54 .1
R105 14.7K 1%
C55 100pf
R189 100 CHIP
Q27 66382
R106 25.5K 1%
C57 .022
R111 680
A3
CR13 MA47

B 12.5 M

BDE

U13 COUNT

U27 PIN 15

U27 PIN 10

U27 PIN 14

U27 PIN 12

U8 PIN 15

B 12.5 M

U20 PIN 14

U22 PIN 15

U21 PIN 3

U20/U21 OPERATION

B 12.5 M

U14 PIN 14

U22 PIN 2

U15 PIN 3

U14/U15 OPERATION

B 12.5

BDE

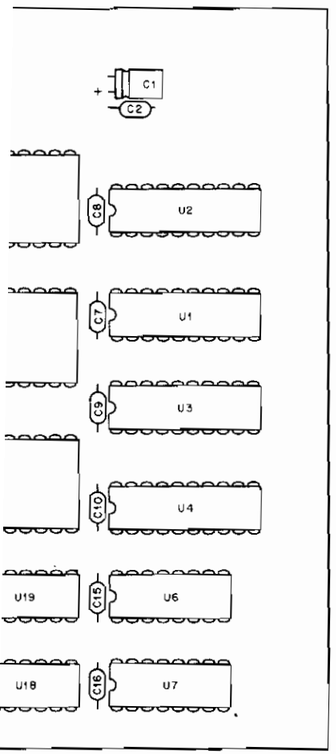
U21 PIN 3 & U15 PIN 3

U20/U21 & U14/U15 OPERATION

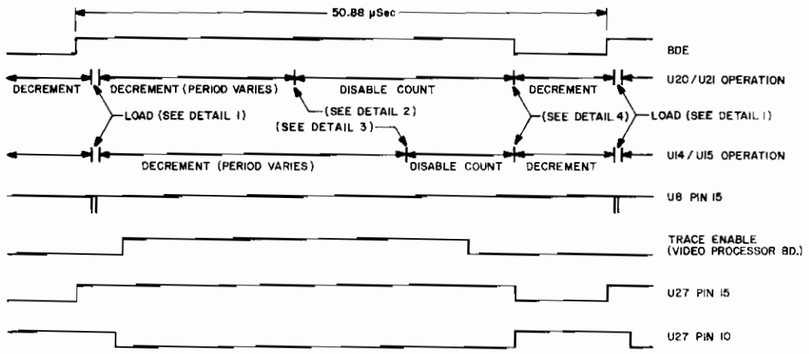
NOTES:

1. TEST POINT WAVEFORMS WITH 5 mSEC/DIV SWEEP RATE.
2. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR 32000 (E.G., R1 IS R32001).
3. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS SPECIFIED).
4. RESISTANCE IS EXPRESSED IN OHMS (UNLESS SPECIFIED).
5. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS SPECIFIED).

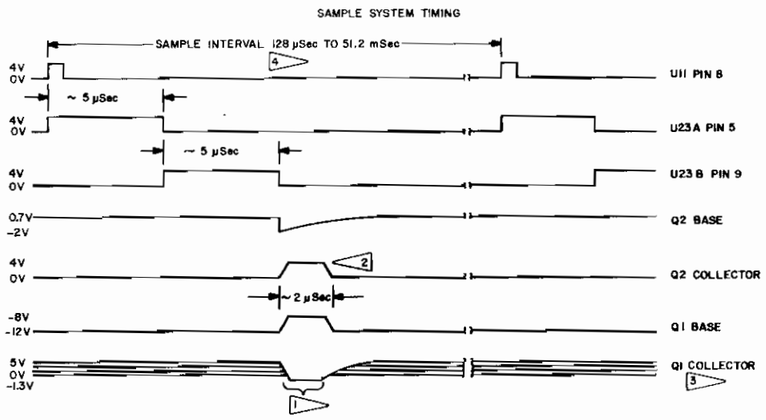
Figure 5-12 Sweep Digitizer Module (D-0000-5314-300-C5)



TRACE GENERATOR OPERATION



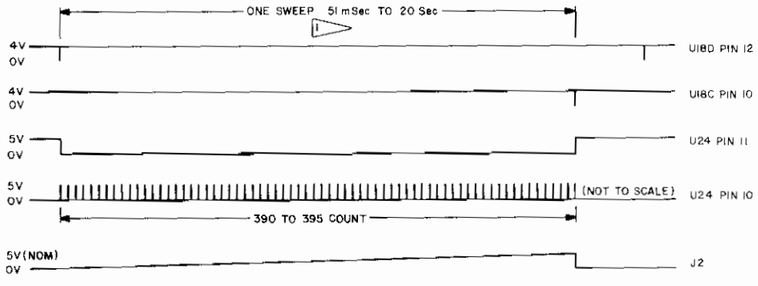
SAMPLE SYSTEM TIMING



NOTES:

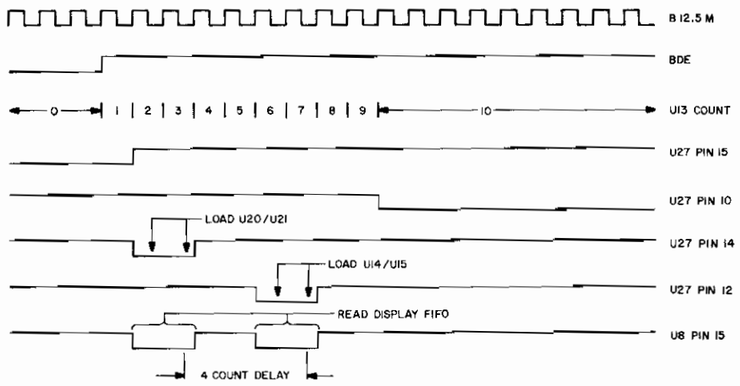
1. PEAK CAPACITOR DISCHARGE
2. TP 2 WAVEFORM
3. TP 1 WAVEFORM
4. DEPENDS ON SWEEP RATE

SWEEP WAVEFORMS

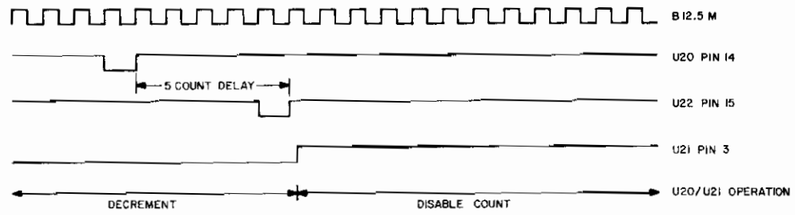


NOTES:

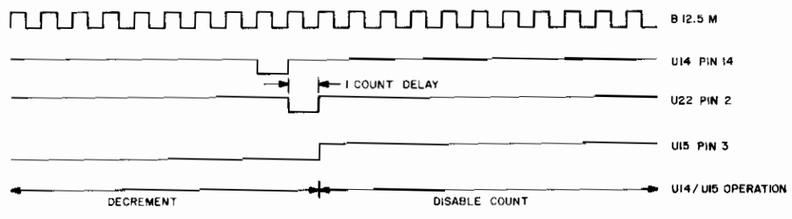
1. DEPENDS ON SWEEP RATE



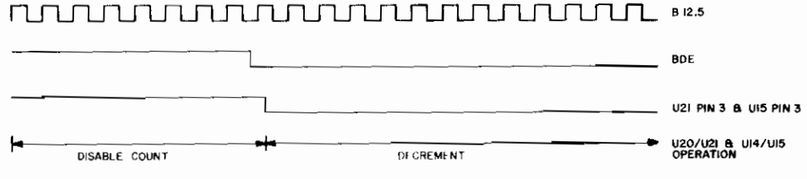
DETAIL 1



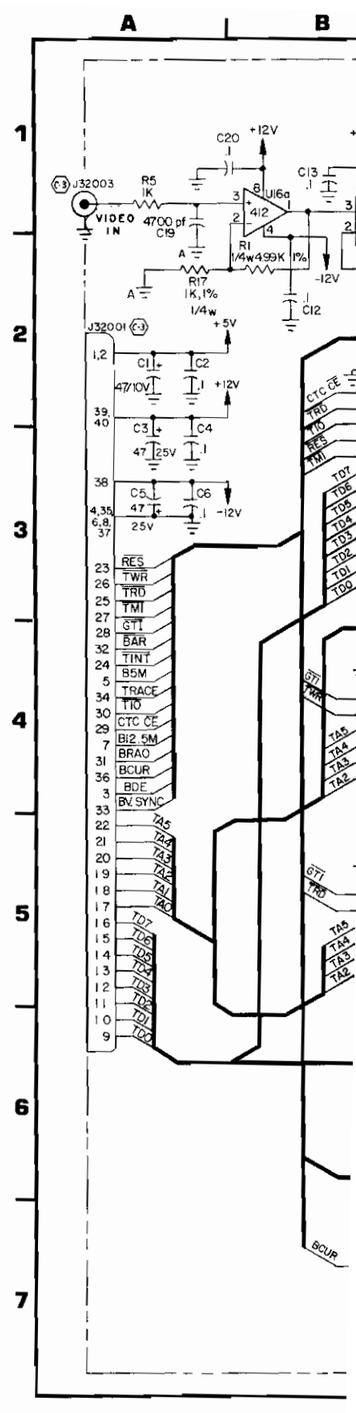
DETAIL 2



DETAIL 3

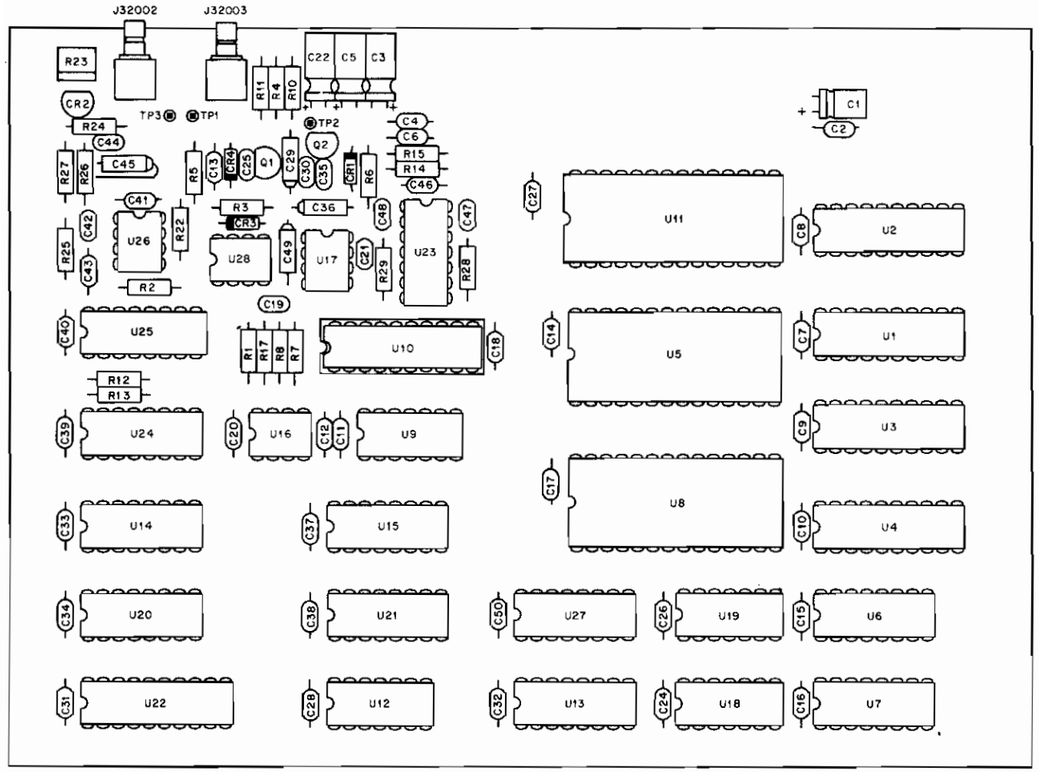


DETAIL 4

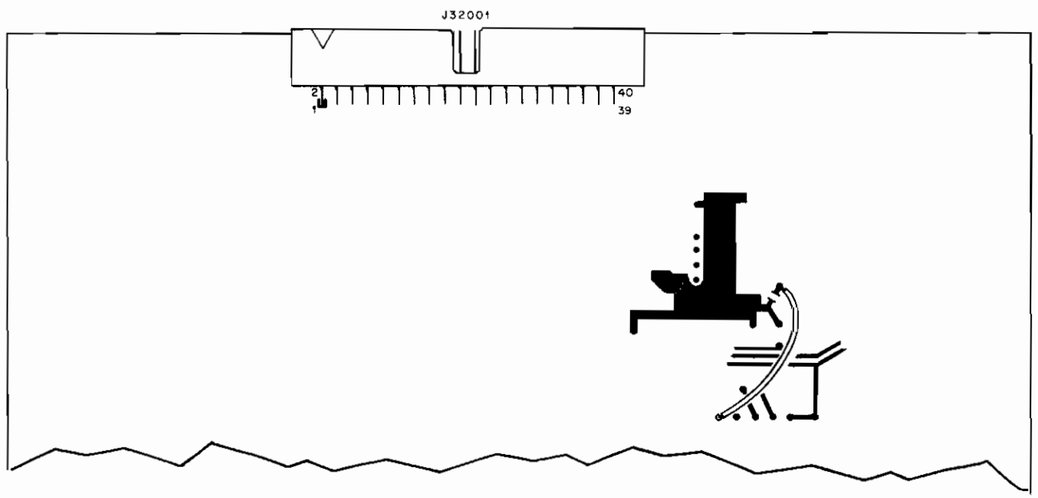


NOTES:

1. TEST POINT WAVEFORMS WI SWEEP RATE.
2. ALL REF NOS ARE ASSIGNE DESIGNATOR SERIES. THI CARRIES DESIGNATOR 3200 R32001).

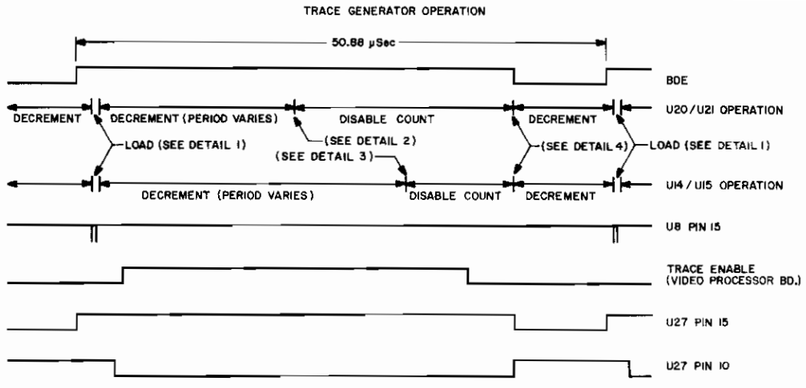


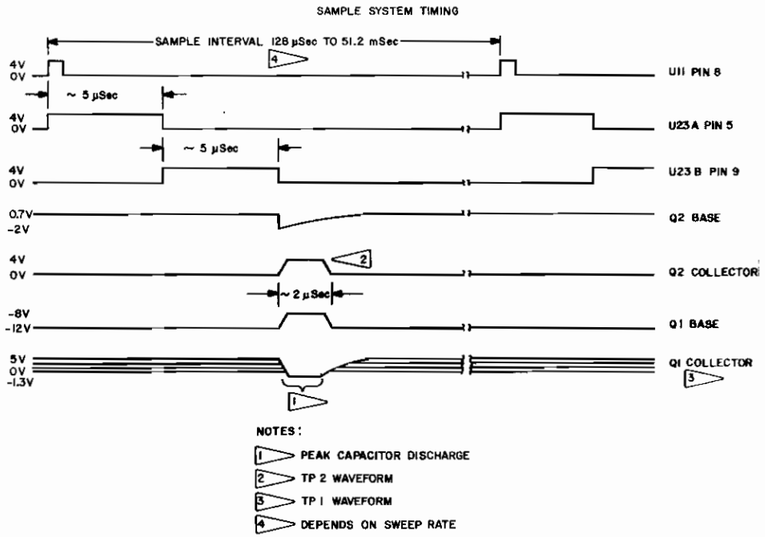
TOP VIEW

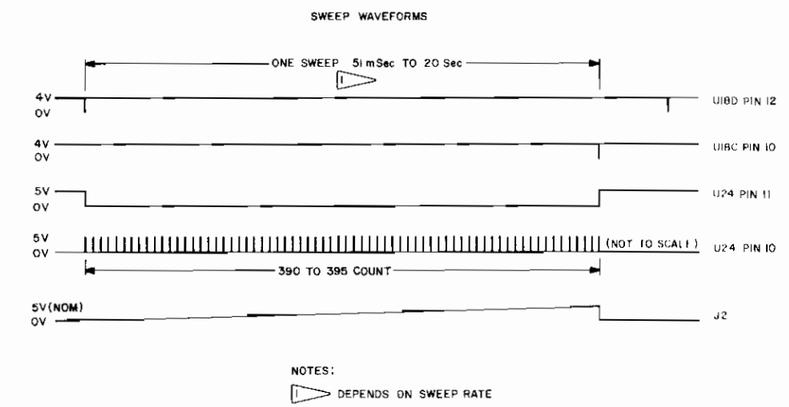


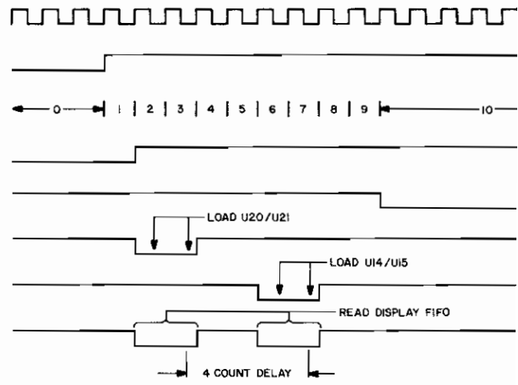
BOTTOM VIEW

SWEEP DIGITIZER PC BOARD

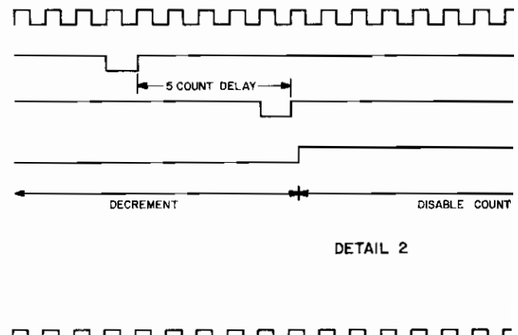




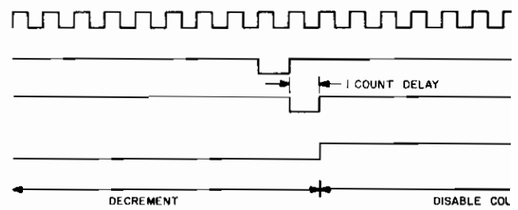




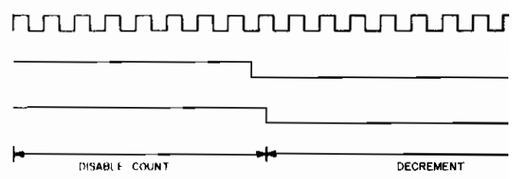
DETAIL 1



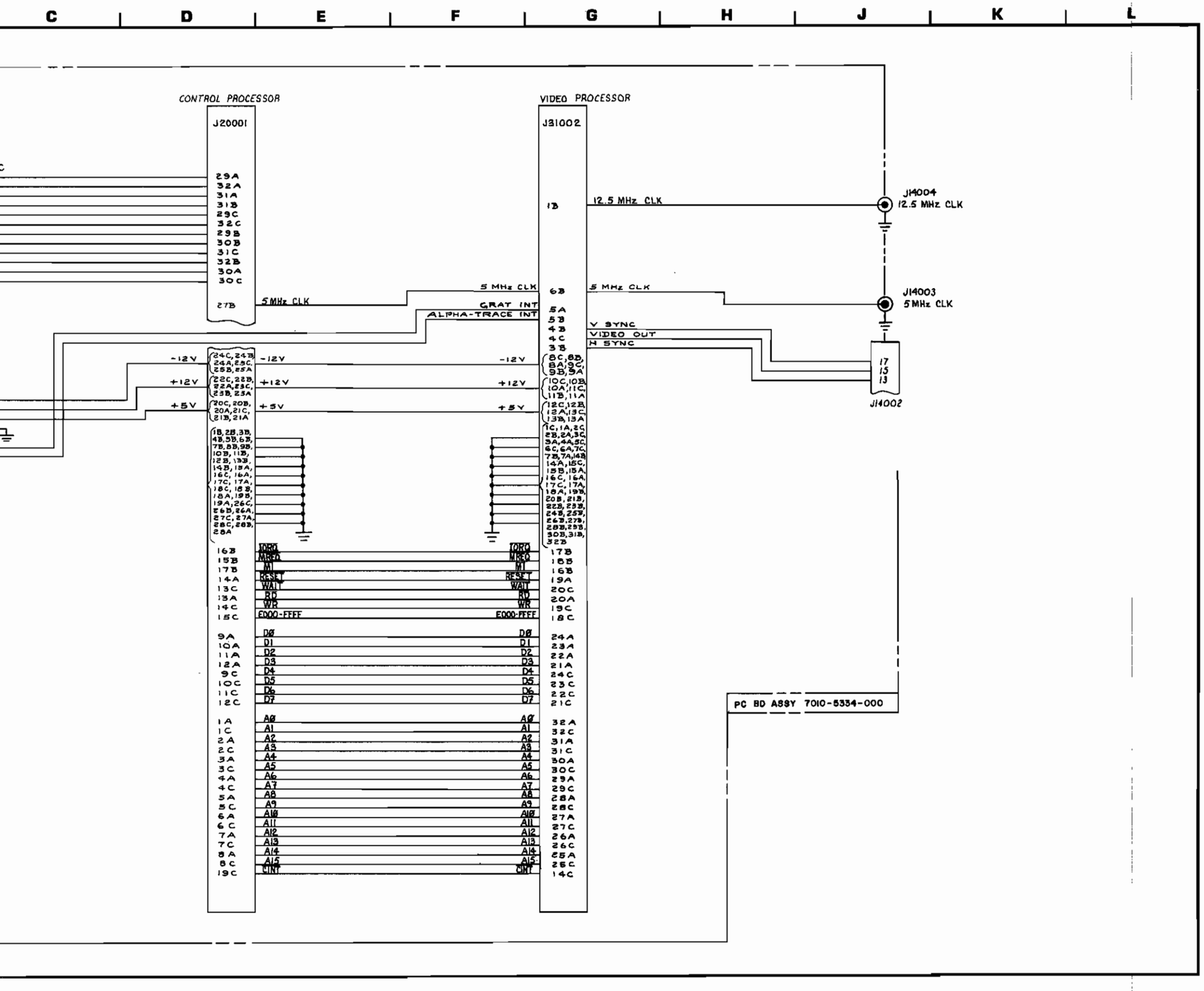
DETAIL 2



DETAIL 3



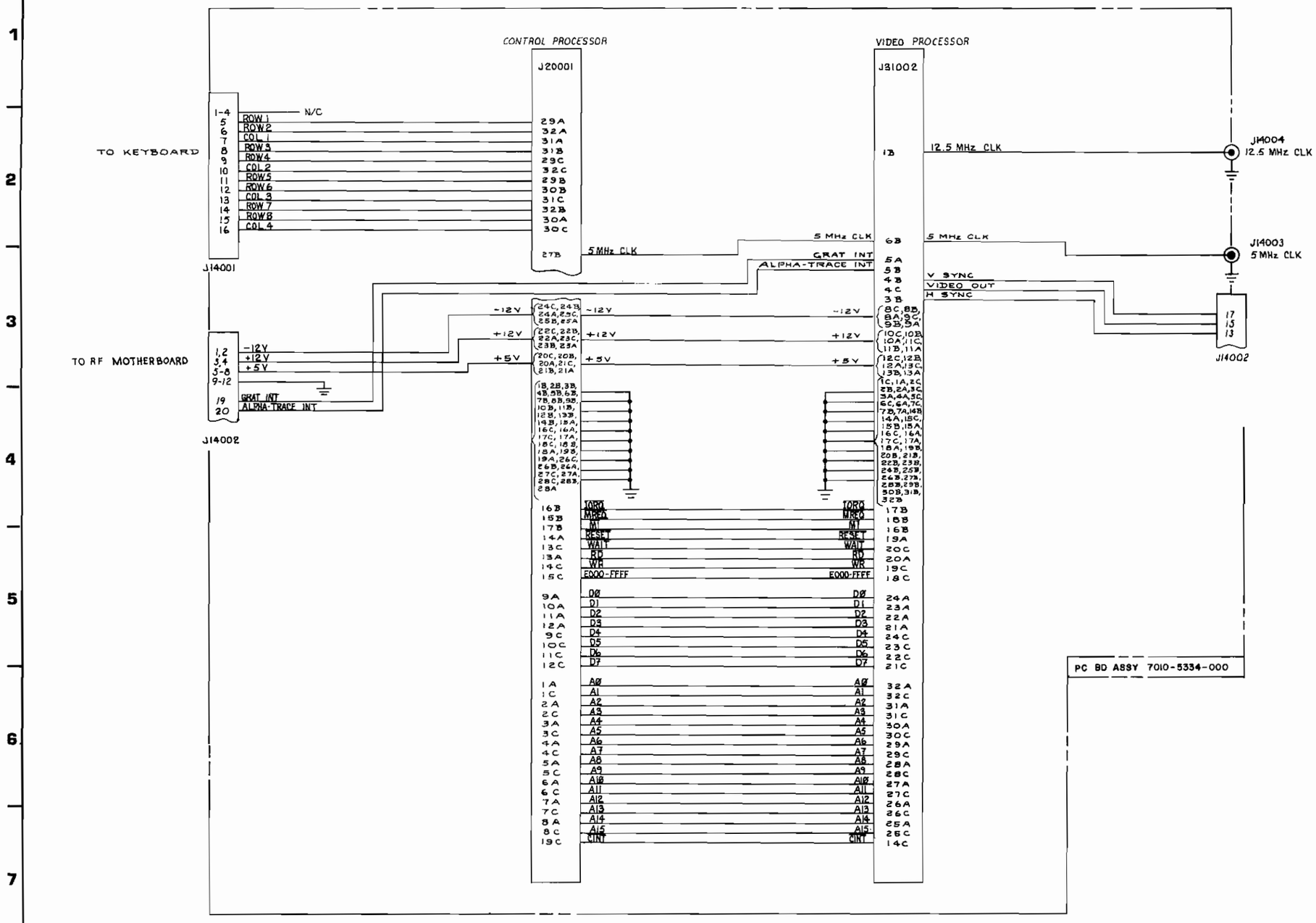
DETAIL 4

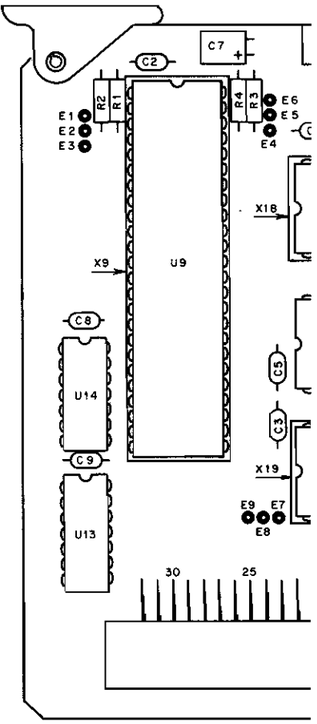


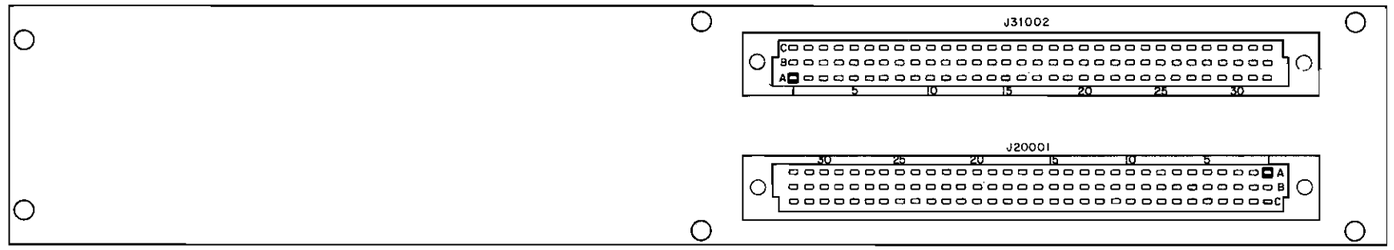
NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR SERIES 14000 (E.G., J1 IS J14001).

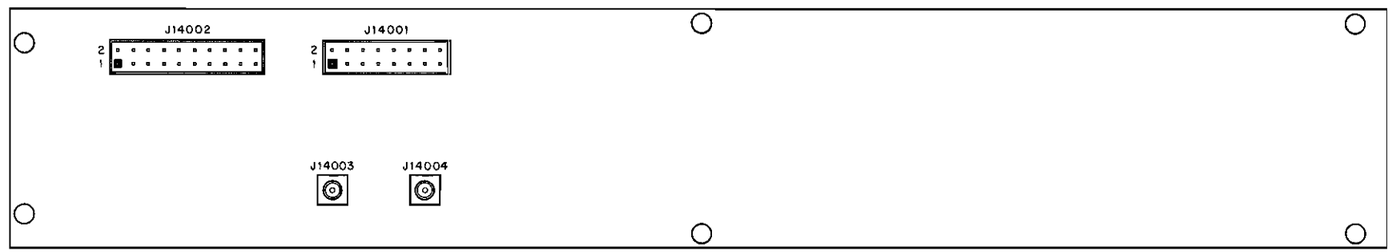
Figure 5-13 Digital Motherboard (D-0000-5314-000-C2)


CONTROL PROCESSOR
J20001
VIDEO PROCESSOR
J31002
TO KEYBOARD
J14001
1-4 N/C
5 ROW 1
6 ROW 2
7 COL 1
8 ROW 3
9 ROW 4
10 COL 2
11 ROW 5
12 ROW 6
13 COL 3
14 ROW 7
15 ROW 8
16 COL 4
29A
32A
31A
31B
29C
32C
29B
30B
31C
32B
30A
30C
27B 5MHz CLK
6B 5 MHz CLK
5A GRAT INT
5B ALPHA-TRACE INT
TO RF MOTHERBOARD
J14002
1,2 -12V
3,4 +12V
5-8 +5V
9-12
19 GRAT INT
20 ALPHA-TRACE INT
-12V
+12V
+5V
1B 12.5 MHz CLK
4B V SYNC
4C VIDEO OUT
3B H SYNC
J14004
12.5 MHz CLK
J14003
5 MHz CLK
J14002
17
15
13
IORQ
MREQ
M1
RESET
WAIT
RD
WR
E000-FFFF
D0
D1
D2
D3
D4
D5
D6
D7
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
CINT
PC BD ASSY 7010-5334-000



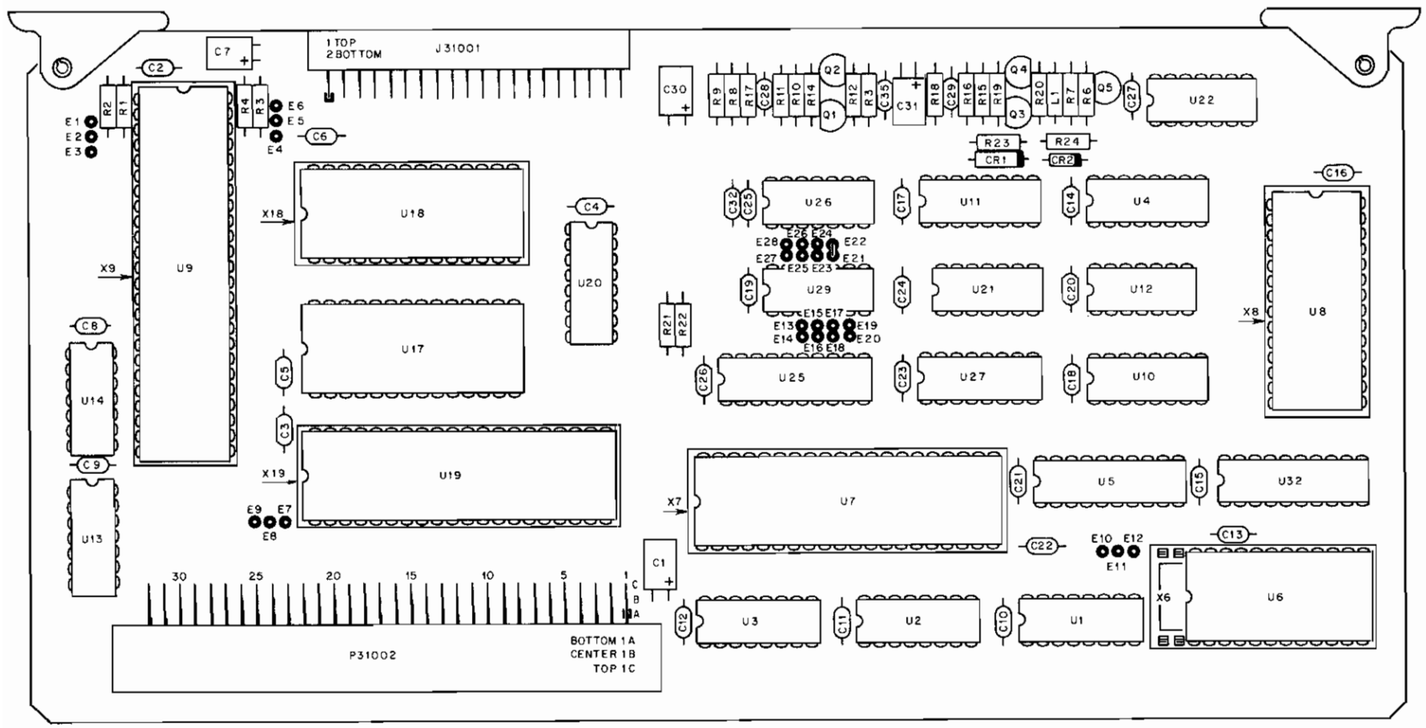


TOP VIEW

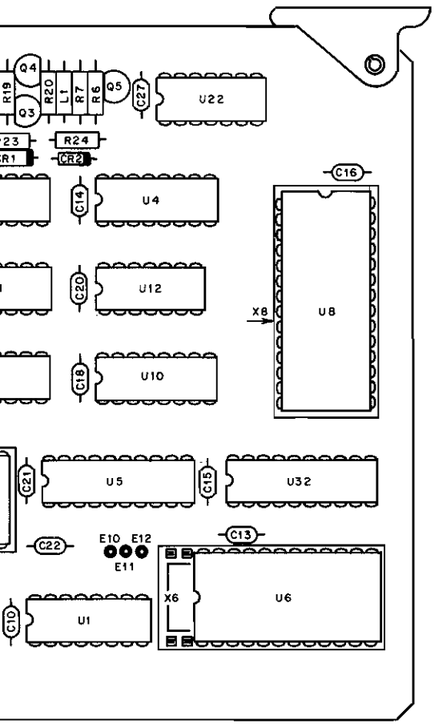


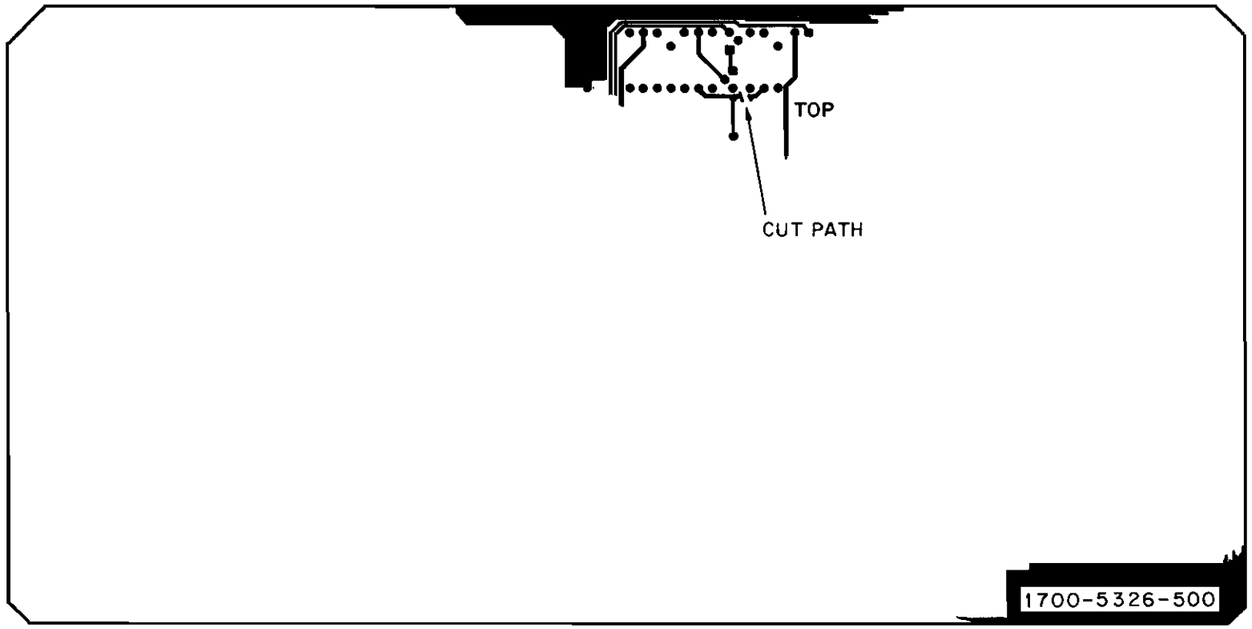
BOTTOM VIEW

DIGITAL MOTHERBOARD PC ASSY

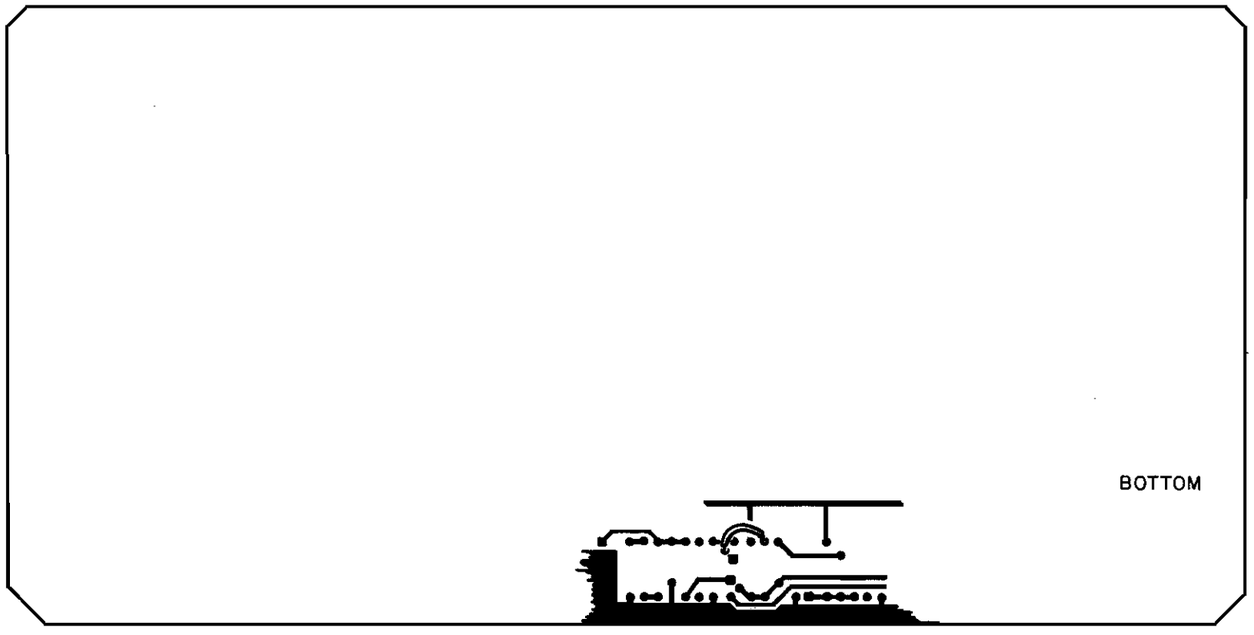


VIDEO PROCESSOR PC BOARD

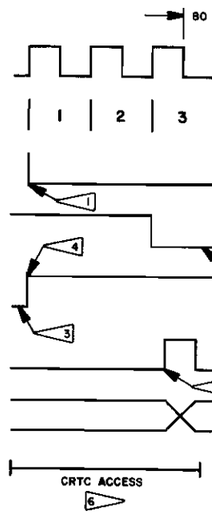


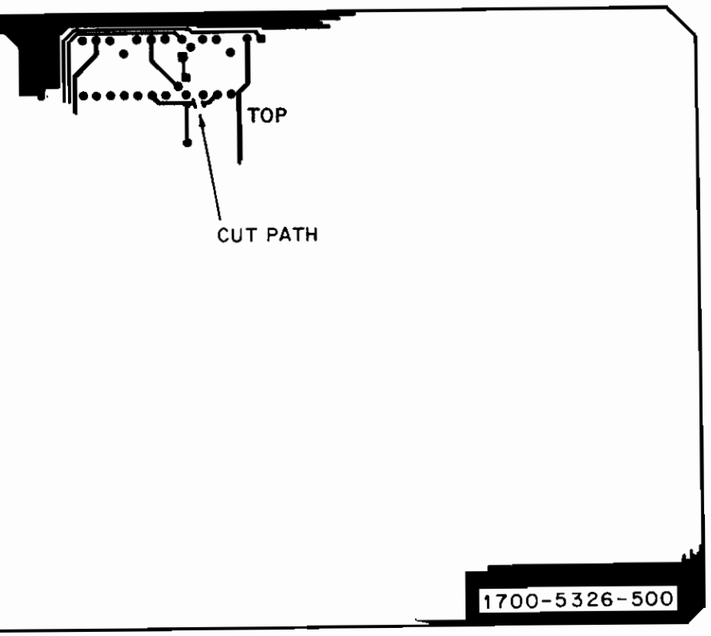


TOP SIDE REV A

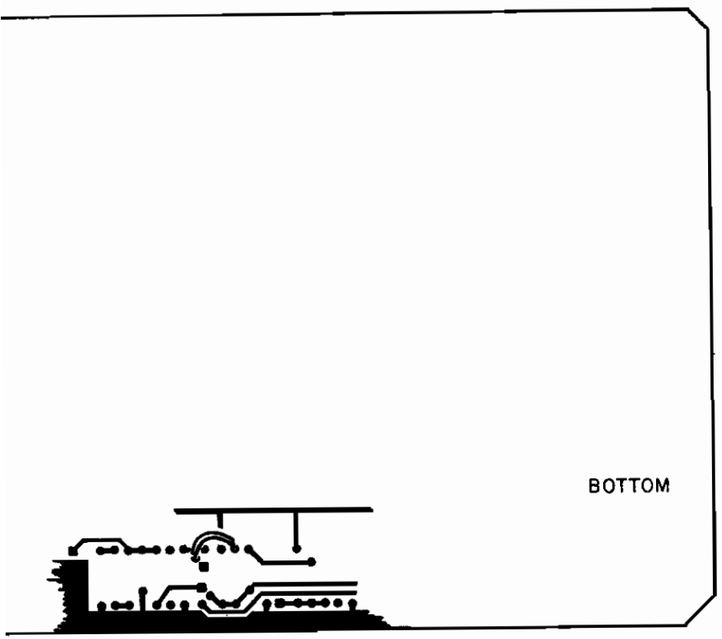


BOTTOM SIDE REV A



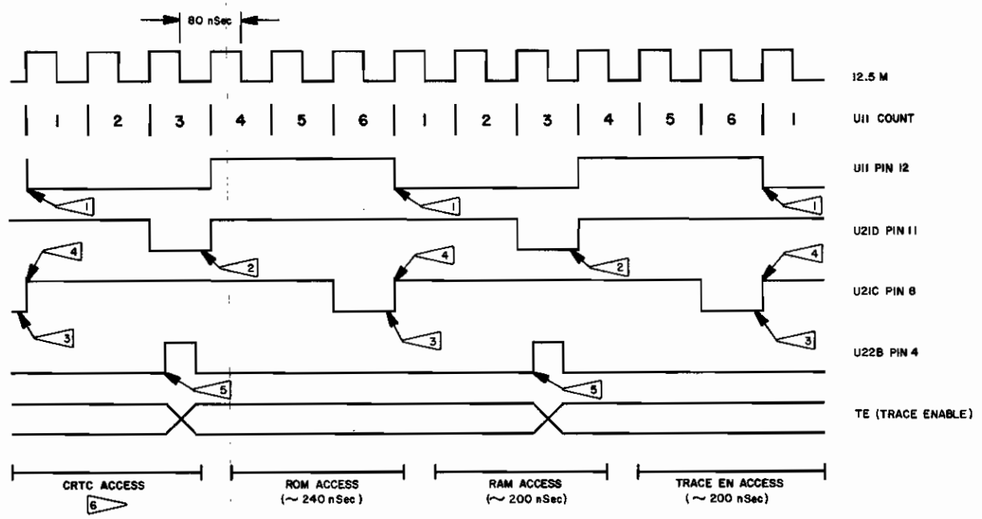


OP SIDE REV A



TOM SIDE REV A

ALPHANUMERIC AND TE TIMING



NOTES:

1. CLOCK CRTC (U7)
2. LOAD VIDEO SHIFT REGISTER (U10)
3. PRESET DOT DIVIDER (U11)
4. LATCH RAM DATA
5. LATCH TRACE ENABLE (U8 PIN 19)
6. MAXIMUM SPECIFIED VALUE

Figure 5-14 Video Processor Module (Sheet 1 of 2)
(D-0000-5314-500-D2)

NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR SERIES 32000 (E.G., R1 IS R32001).

2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).

3. RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).

4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

5. U32006 IS A 24-PIN IC INSTALLED IN A 28-PIN SOCKET. THE PIN NUMBERS INDICATED ARE RELATIVE TO THE SOCKET AND NOT A 24-PIN IC. THEREFORE, PIN 3 OF THE SOCKET IS PIN 1 OF A 24-PIN IC.

6. P31002 PIN NUMBERS - 12a, 12b, 12c, 13a, 13b, 13c ARE +5V.

7. P31002 PIN NUMBERS - 10a, 10b, 10c, 11a, 11b, 11c ARE +12V.

8. P31002 PIN NUMBERS - 8a, 8b, 8c, 9a, 9b 9c, ARE -12V.

9. P31002 PIN NUMBERS - 1a, 1c, 2a, 2b, 2c, 3a, 3c, 4a, 5c, 6a, 6c, 7a, 7b, 7c, 14a, 14b, 15a, 15b, 15c, 16a, 16c, 17a, 17c, 18a, 19b, 20b, 21b, 22b, 23b, 24b, 25b, 26b, 27b, 28b, 29b, 30b, 31b, 32b ARE GROUNDS.

Figure 5-14 Video Processor Module (Sheet 2 of 2) (D-0000-5314-500-D2)

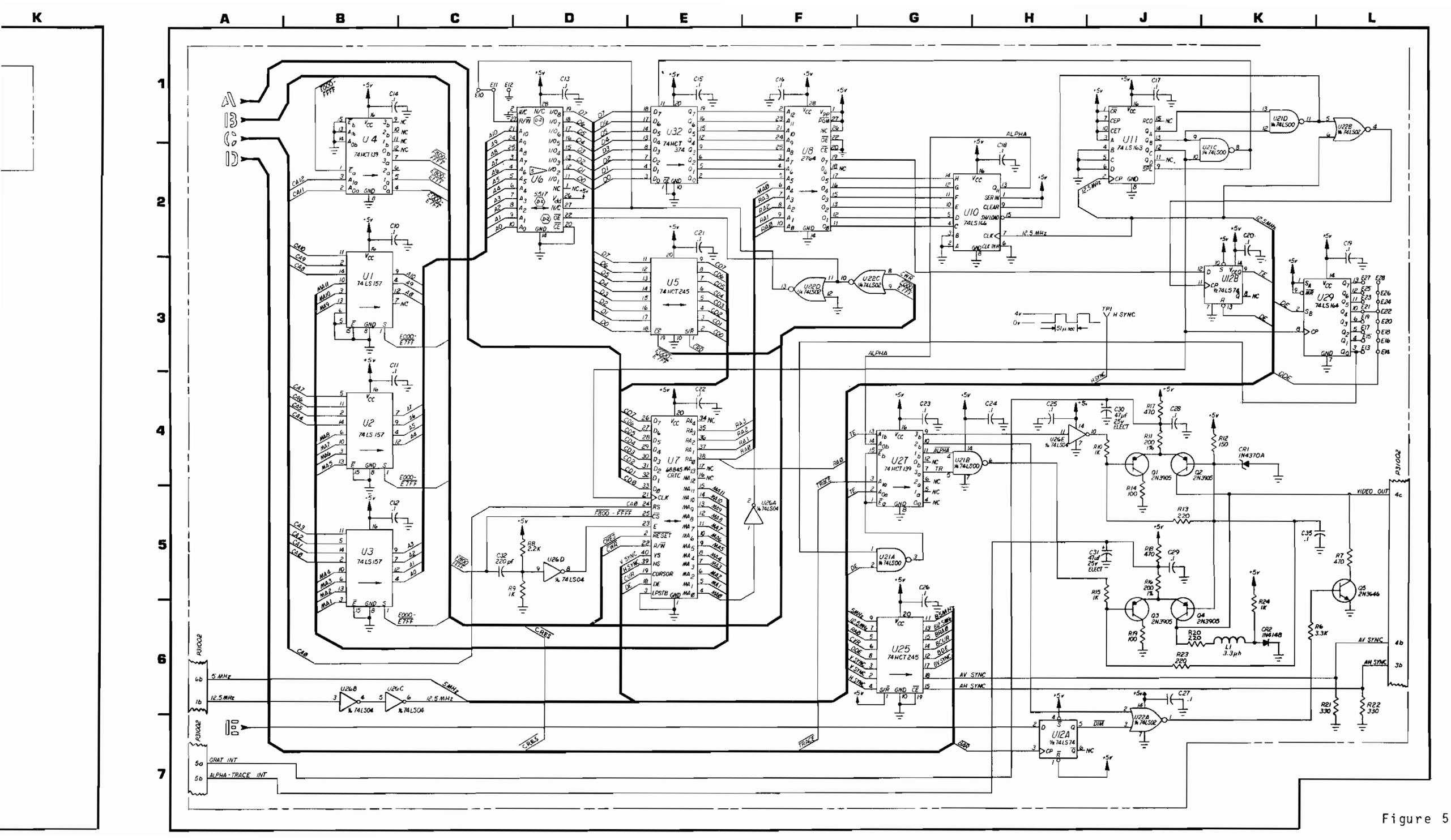
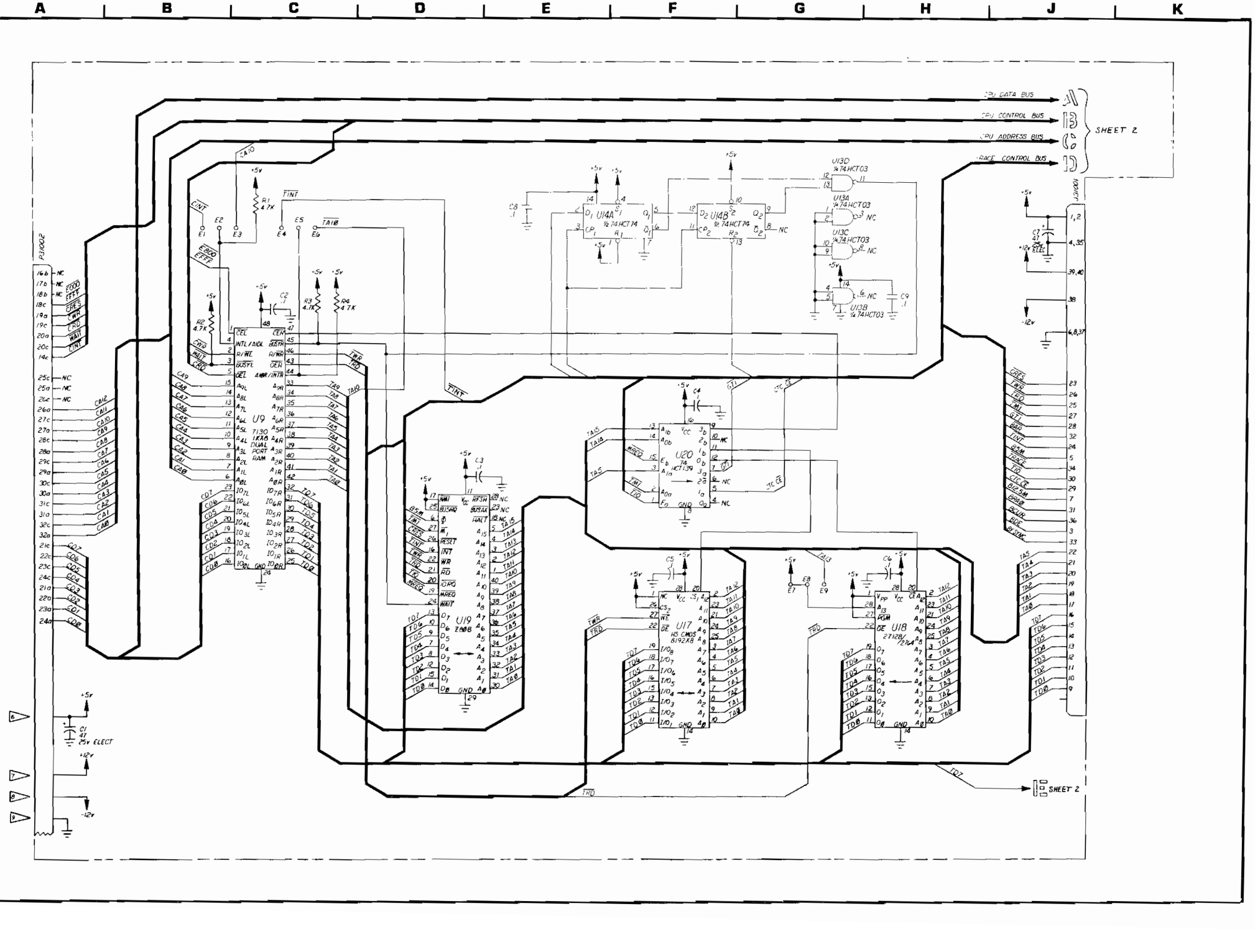
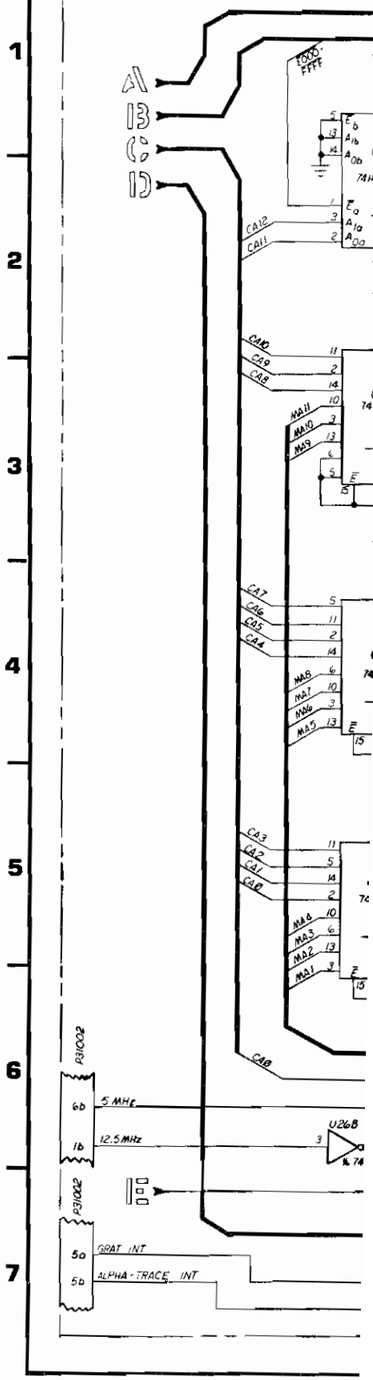
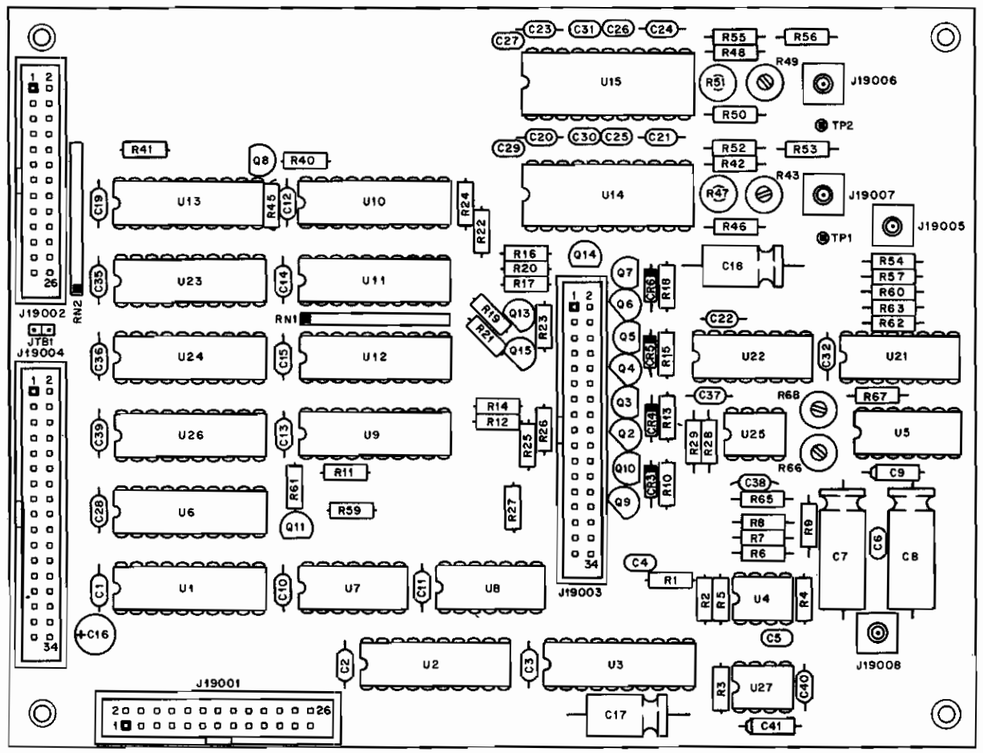

A
B
C
D
1
2
3
4
5
6
7
U1 74LS157
U2 74LS157
U3 74LS157
U4 74HCT139
U5 74HCT245
U6 5517
U7 6845 CRTC
U8 2764
U32 74HCT374
U10 74LS164
U11 74LS163
U12 74LS74
U29 74LS164
U25 74HCT245
U27 74HCT139
U21 74LS00
U22 74LS02
U26 74LS04
U12A 74LS74
P31002
ALPHA
12.5 MHz
H SYNC
V SYNC
AV SYNC
AH SYNC
VIDEO OUT
CRES
TRACE
GRAT INT
ALPHA-TRACE INT

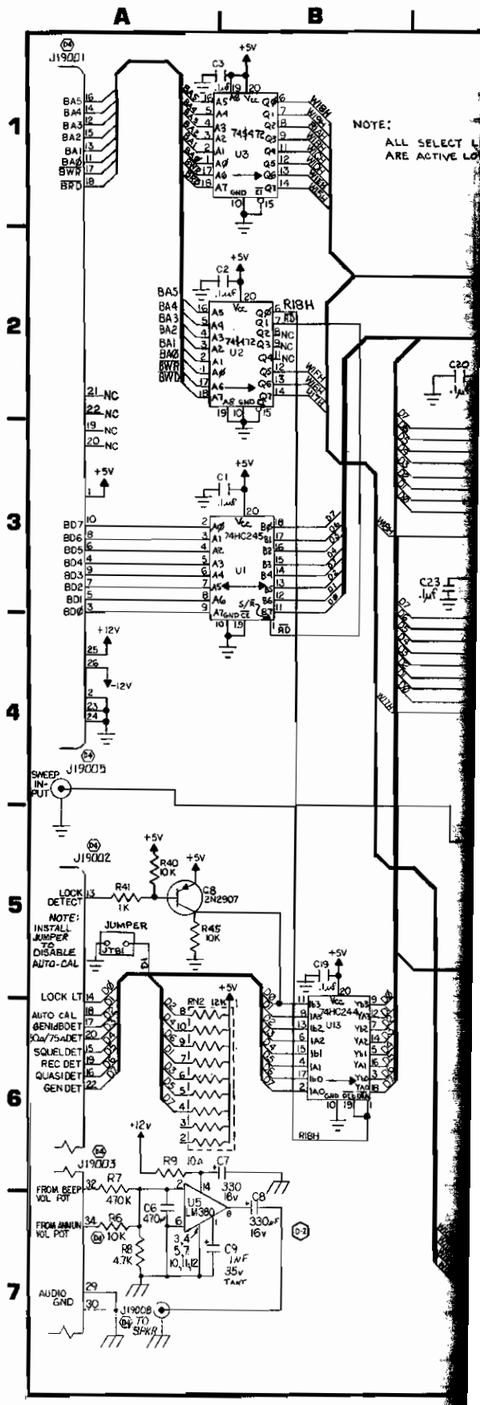
Figure 5-

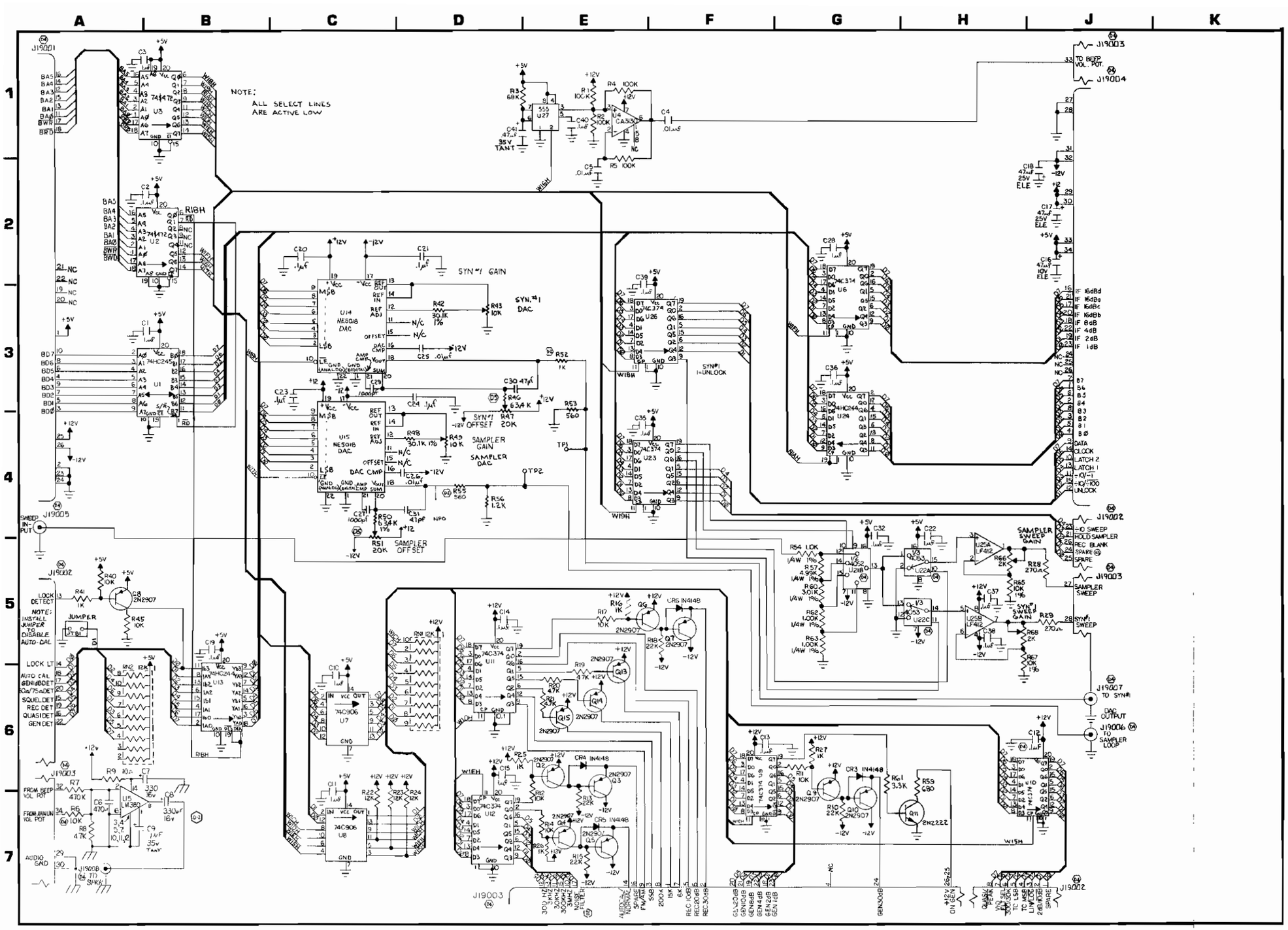

CPU DATA BUS
CPU CONTROL BUS
CPU ADDRESS BUS
GRACE CONTROL BUS
SHEET 2
P31002
U9 7130 1KX8 DUAL PORT RAM
U19 2808
U17 HS CMOS 8192X8
U18 27128/27C64
U20 74HCT139
U14A 1/2 74HCT74
U14B 1/2 74HCT74
U13A 1/4 74HCT03
U13B 1/4 74HCT03
U13C 1/4 74HCT03
U13D 1/4 74HCT03
U30001
+5v
-12v
SHEET 2


P31002
5 MHz
12.5 MHz
GRAT INT
ALPHA-TRACE INT



INTERFACE PC BOARD

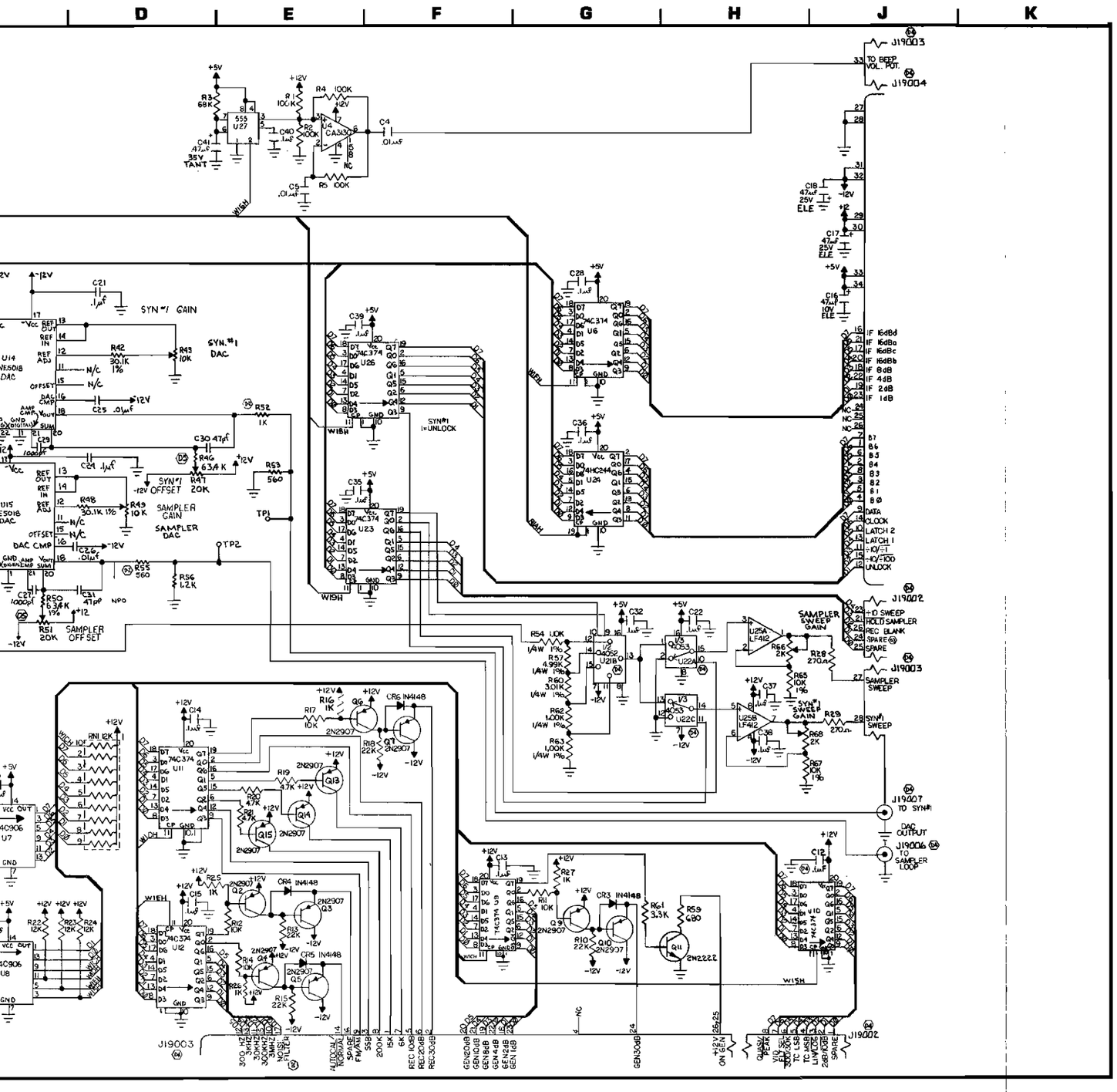




NOTES:

1. ALL REF DESIGNA CARRIES (E.G., I
2. RESISTO (UNLESS
3. RESISTA (UNLESS
4. CAPACIT NOTED).

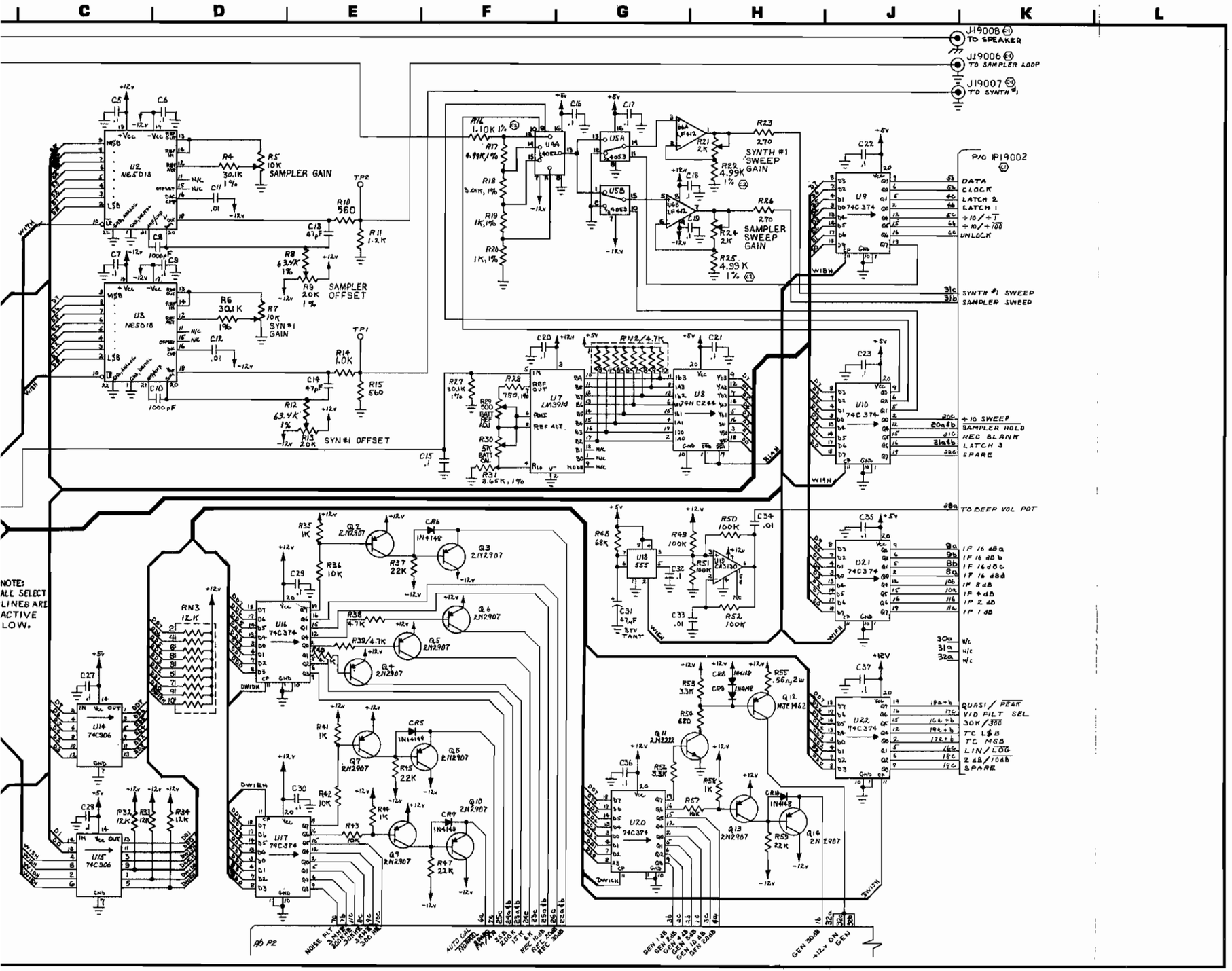
Figure 5-15 Interface (S/N 1001



NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR SERIES 19000 (E.G., R1 IS R19001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

Figure 5-15 Interface PC Board (Sheet 1 of 2) (S/N 1001 Thru S/N 1476) (D-0000-5311-500-D6)



NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR SERIES 19000 (E.G., R1 IS R19001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

Figure 5-15 Interface PC Board (Sheet 2 of 2) (S/N 1476 & On) (D-0000-5315-200-C2)

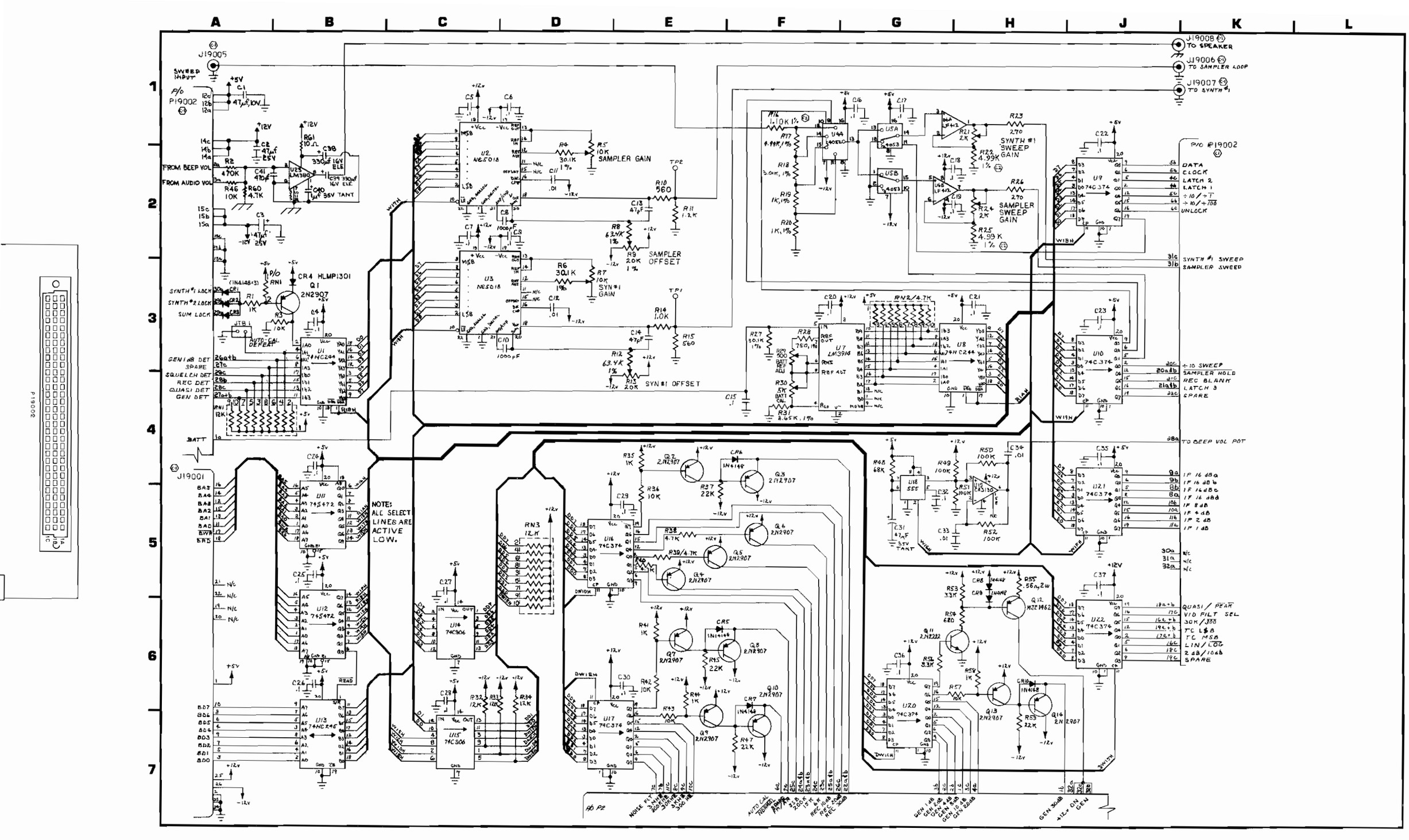
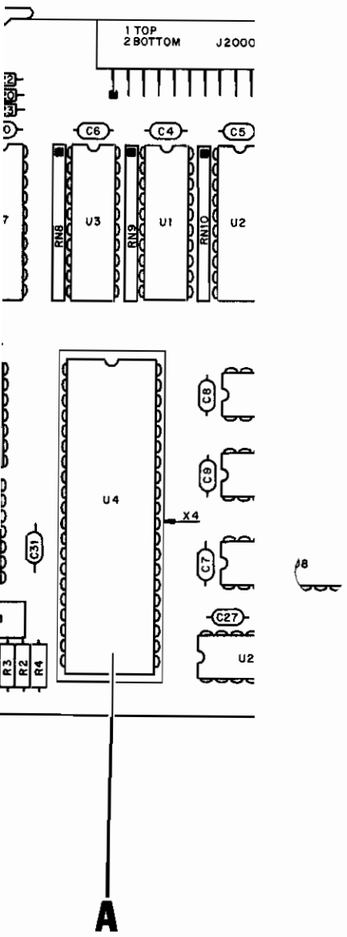
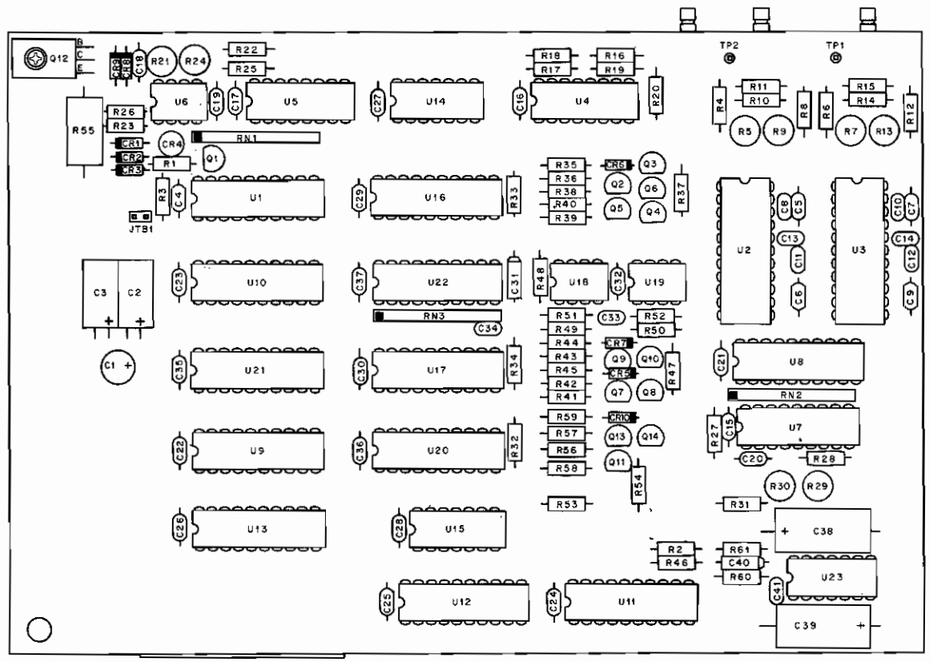
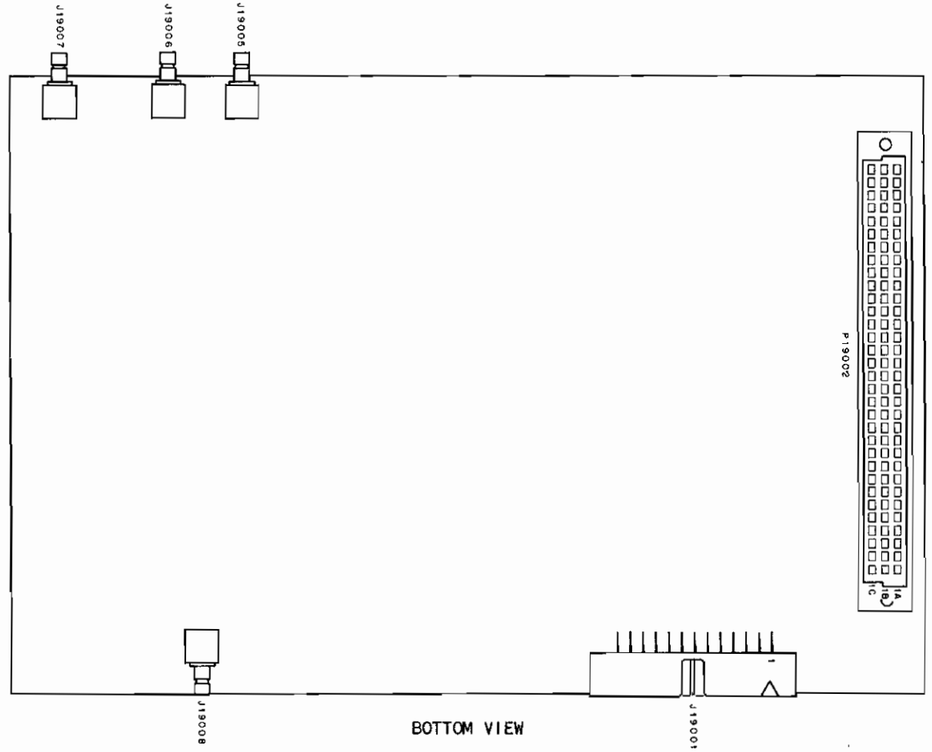

J19005
SWEEP INPUT
P/O P19002
FROM BEEP VOL
FROM AUDIO VOL
SYNTH #1 LOCK
SYNTH #2 LOCK
SUM LOCK
GEN 1dB DET
SPARE
SQUELCH DET
REC DET
QUASI DET
GEN DET
AUTO CAL DEFEAT
BATT
J19001
NOTE: ALL SELECT LINES ARE ACTIVE LOW.
J19008 TO SPEAKER
J19006 TO SAMPLER LOOP
J19007 TO SYNTH #1
SYNTH #1 SWEEP
SAMPLER SWEEP
DATA
CLOCK
LATCH 2
LATCH 1
÷10/÷7
÷10/÷100
UNLOCK
÷10 SWEEP
SAMPLER HOLD
REC BLANK
LATCH 3
SPARE
TO BEEP VOL POT
IF 16 dB a
IF 16 dB b
IF 16dB c
IF 16 dBd
IF 8dB
IF 4dB
IP 2 dB
IP 1 dB
QUASI / PEAR
VID FILT SEL
30K/300
TC LSB
TC MSB
LIN/LOG
2 dB/10dB
SPARE
SAMPLER GAIN
SAMPLER OFFSET
SYN#1 GAIN
SYN#1 OFFSET
SYNTH #1 SWEEP GAIN
SAMPLER SWEEP GAIN
SYNTH #1 SWEEP OFFSET
SAMPLER SWEEP OFFSET
+12V ON GEN

Figure 5-1



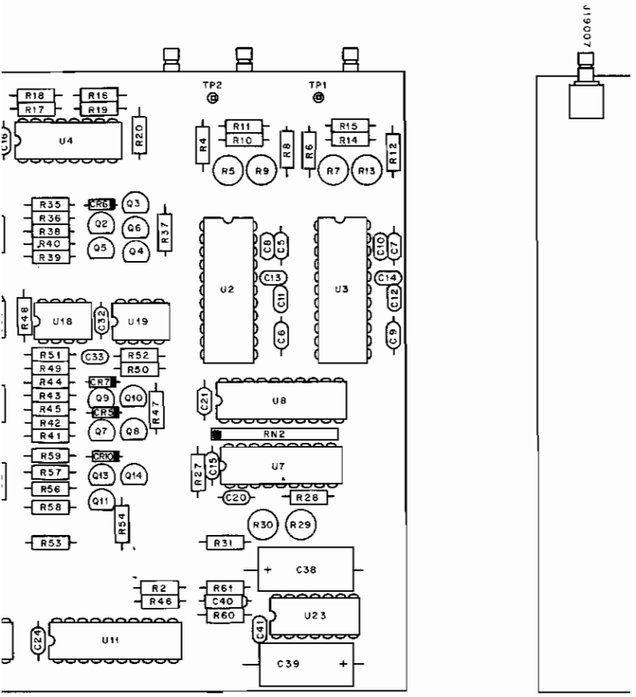


TOP VIEW

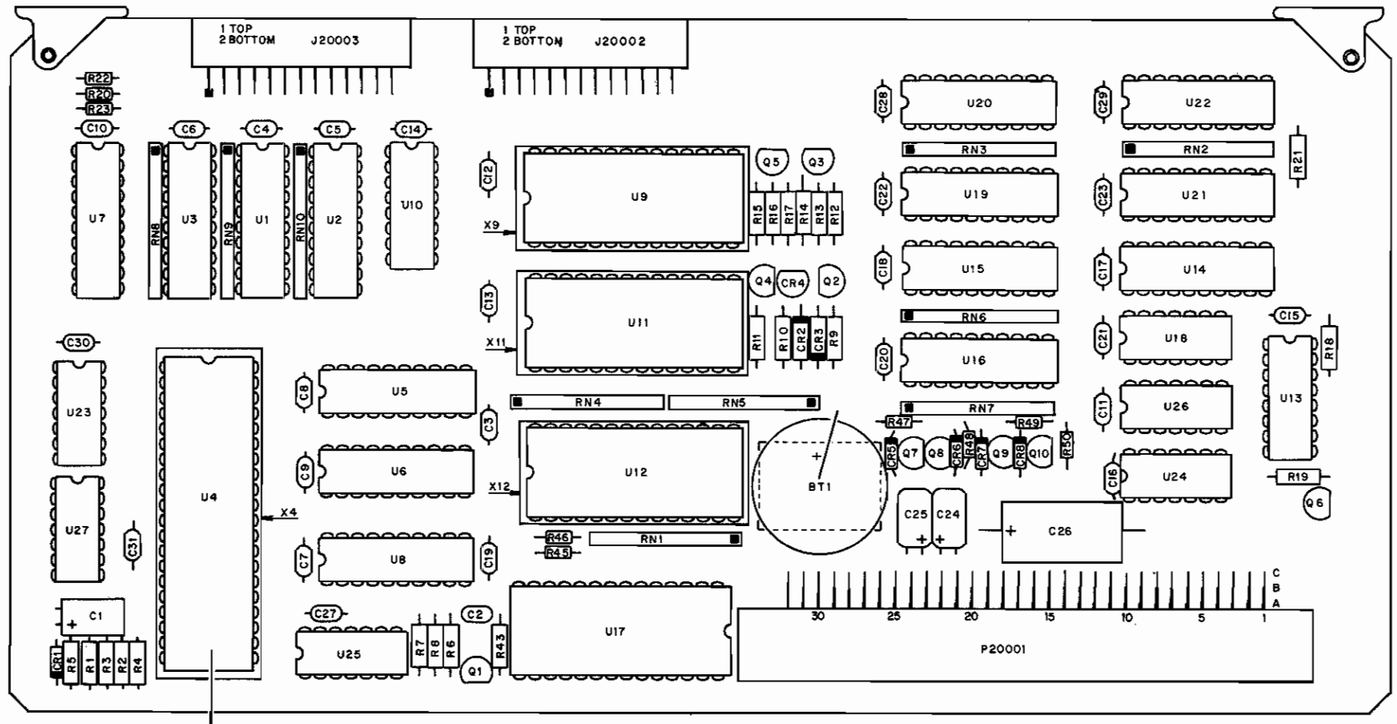


BOTTOM VIEW

INTERFACE PC BOARD

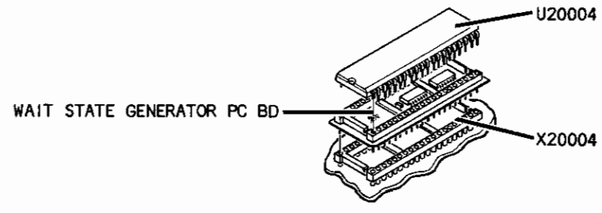


INTERFACE PC BOARD

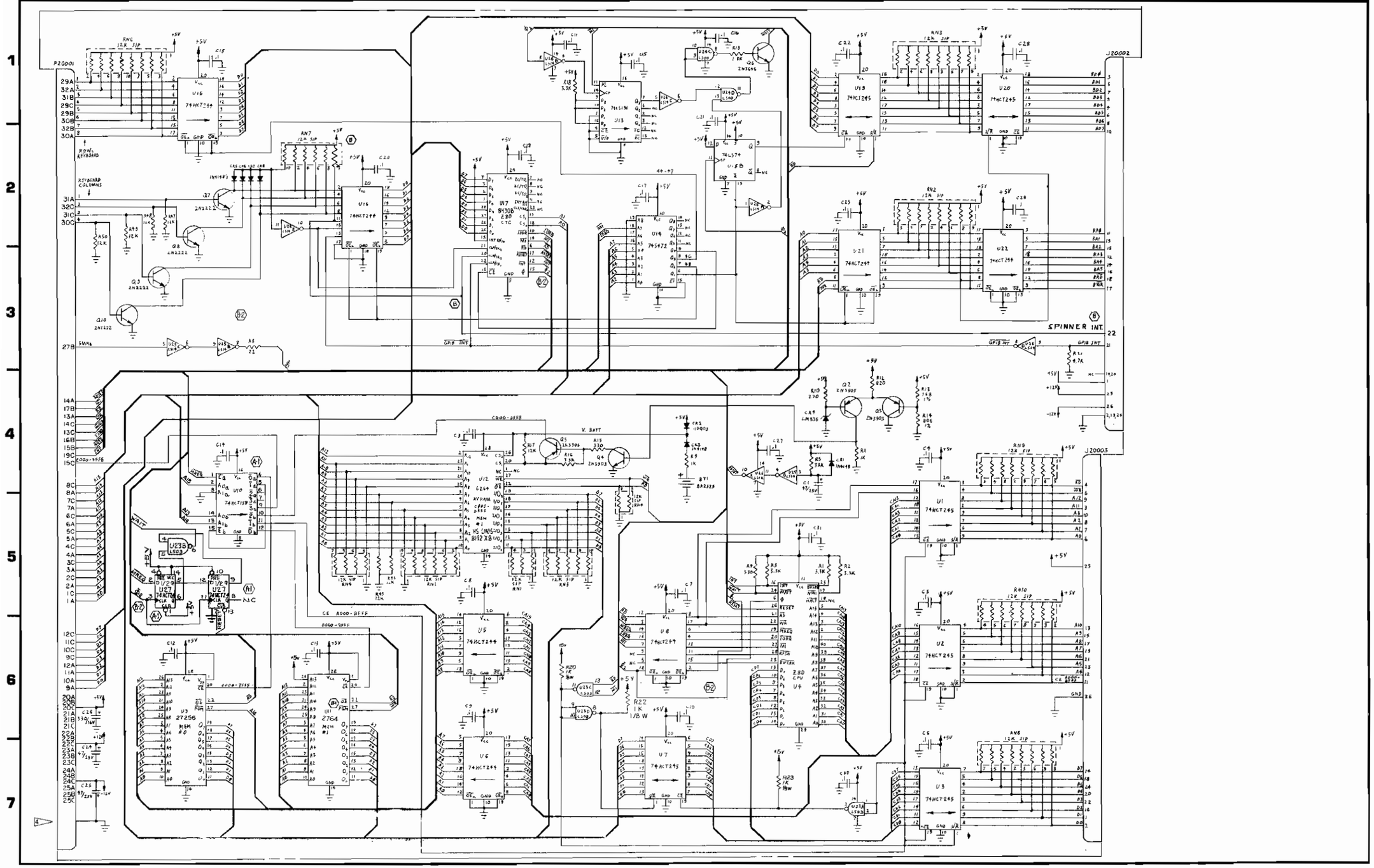


CONTROL PROCESSOR PC BOARD

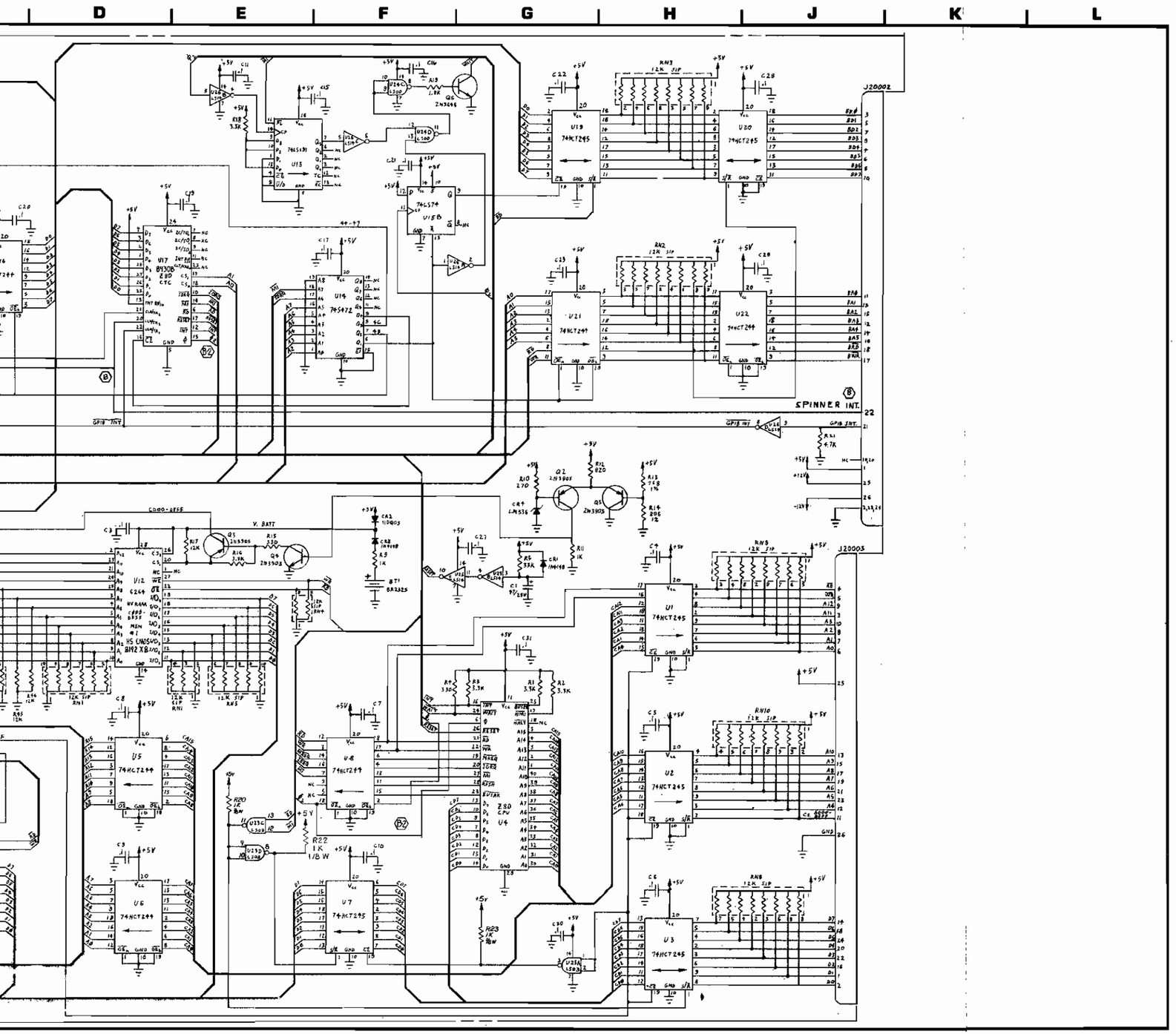
A



DETAIL A


A
B
C
D
E
F
G
H
J
K
L
1
2
3
4
5
6
7
P20001
J20002
J20003
ROW/KEYBOARD
KEYBOARD COLUMNS
SPINNER INT
GPIB INT
V. BATT
U16 74HCT244
U15 74HCT244
U17 8430B Z80 CTC
U18 74S472
U13 74LS138
U14 74LS37
U19 74HCT245
U20 74HCT245
U21 74HCT299
U22 74HCT244
U1 74HCT245
U2 74HCT245
U3 74HCT245
U4 Z80 CPU
U5 74HCT244
U6 74HCT244
U7 74HCT245
U8 74HCT244
U9 74HCT139
U10 74HCT139
U11 2764
U12 6264
U23 LS03
U24 LS04
U25 LS08
U26 LS14
U27 74HCT86
U28 LS03
U29 74HCT86
Q1 2N3906
Q2 2N3906
Q3 2N3904
Q4 2N3906
Q5 2N3906
Q6 2N3906
Q7 2N2222
Q8 2N2222
Q9 2N2222
Q10 2N2222
CR1 1N4148
CR2 1N4003
CR3 1N4148
CR4 1N4148
CR5 LM336
CR6 LM336
BT1 BR2325
RN1 12K SIP
RN2 12K SIP
RN3 12K SIP
RN4 12K SIP
RN5 12K SIP
RN6 12K SIP
RN7 12K SIP
RN8 12K SIP
RN9 12K SIP
RN10 12K SIP
R1 5.1K
R2 5.1K
R3 5.1K
R4 5.1K
R5 5.1K
R9 1K
R10 270
R11 820
R12 3.3K
R13 7.68 1%
R14 806 1%
R15 330
R16 3.3K
R17 12K
R18 12K
R19 12K
R20 1K 1/8W
R21 1K 1/8W
R22 1K 1/8W
R23 1K 1/8W
R45 12K
R46 12K
R47 12K
R48 12K
R49 12K
R50 12K
C1 10/16V
C2 .1
C3 .1
C4 .1
C5 .1
C6 .1
C7 .1
C8 .1
C9 .1
C10 .1
C11 .1
C12 .1
C13 .1
C14 .1
C15 .1
C16 .1
C17 .1
C18 .1
C19 .1
C20 .1
C21 .1
C22 .1
C23 .1
C24 330/16V
C25 330/16V
C26 .1
C27 .1
C28 .1
C29 .1
C30 .1
C31 .1
U10 74HCT139
U11 2764 MEM #1
U12 6264 NV RAM #1 BB2X8 HS CMOS SRAM
U3 27256 MEM #0
U23A LS03
U23B LS03
U23C LS03
U23D LS03
U24A LS04
U24B LS04
U24C LS04
U24D LS04
U25A LS08
U25B LS08
U25C LS08
U25D LS08
U26A LS14
U26B LS14
U26C LS14
U26D LS14
U27A 74HCT86
U27B 74HCT86
U27C 74HCT86
U27D 74HCT86
U28A LS03
U28B LS03
U28C LS03
U28D LS03
U29A 74HCT86
U29B 74HCT86
U29C 74HCT86
U29D 74HCT86
+5V
+12V
-12V
GND
WAIT
GPIB INT
SPINNER INT
8000-9FFF
A000-BFFF
C000-DFFF
E000-FFFF
NC

Figure



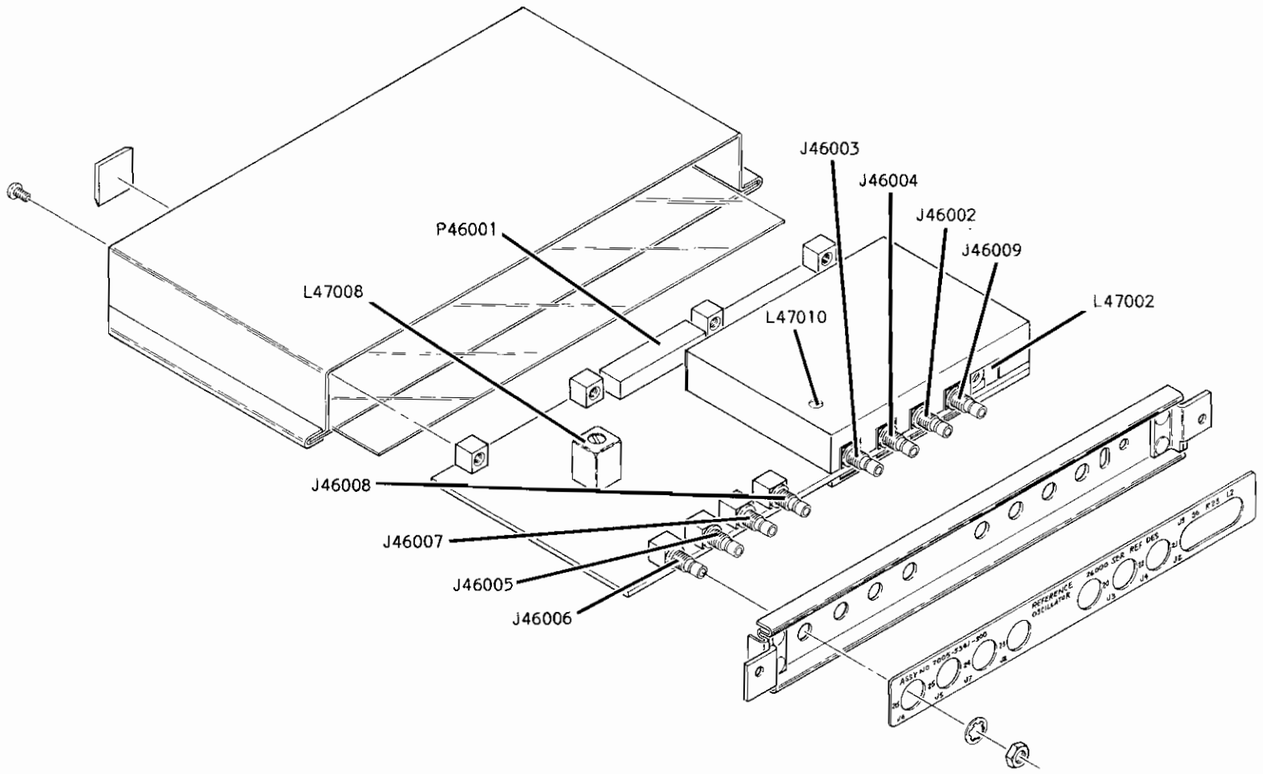
NOTES:

1. NOT USED.
2. NOT USED.
3. NOT USED.
4. J20001 PIN NUMBERS TO GROUND:

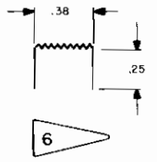
   ROW A - PINS 15 THRU 19, 26 THRU 28
   ROW B - PINS 1 THRU 14, 18, 19 & 28
   ROW C - PINS 16 THRU 18, 26 THRU 28

5. NOT USED.
6. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES DESIGNATOR SERIS 20000 (E.G., R1 IS R20001).
7. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
8. RESISTANCE IS IN OHMS.
9. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

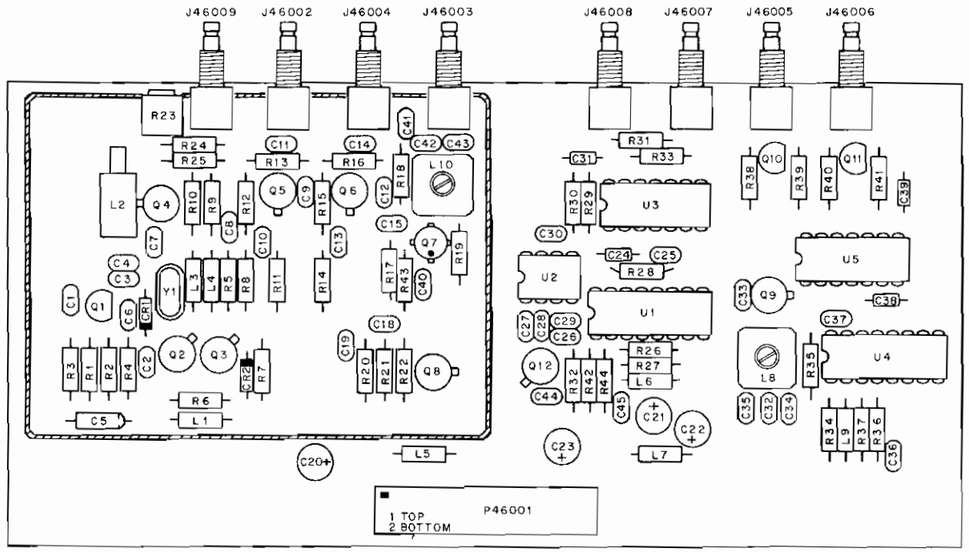
Figure 5-16 Control Processor (D-0000-5316-600-B2)



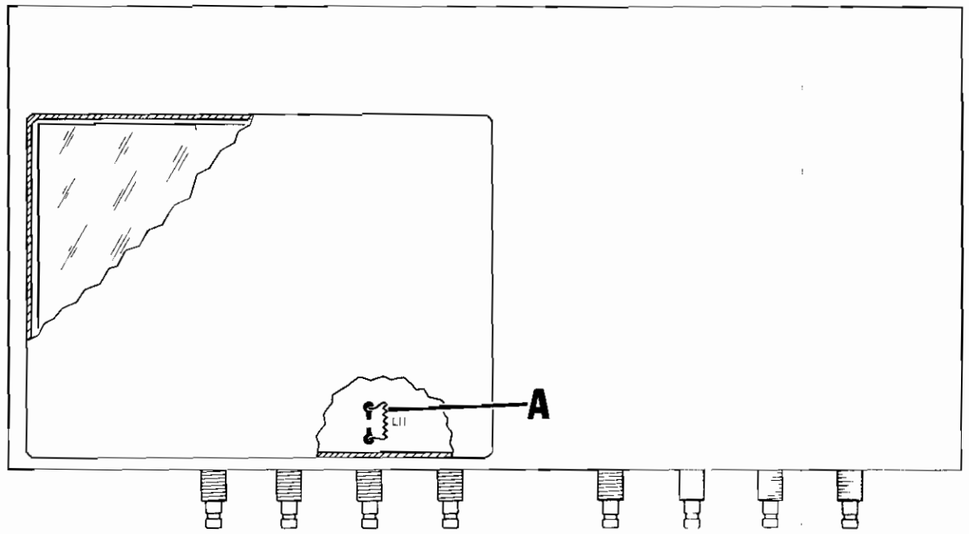
REFERENCE OSCILLATOR ASSY



DETAIL **A**

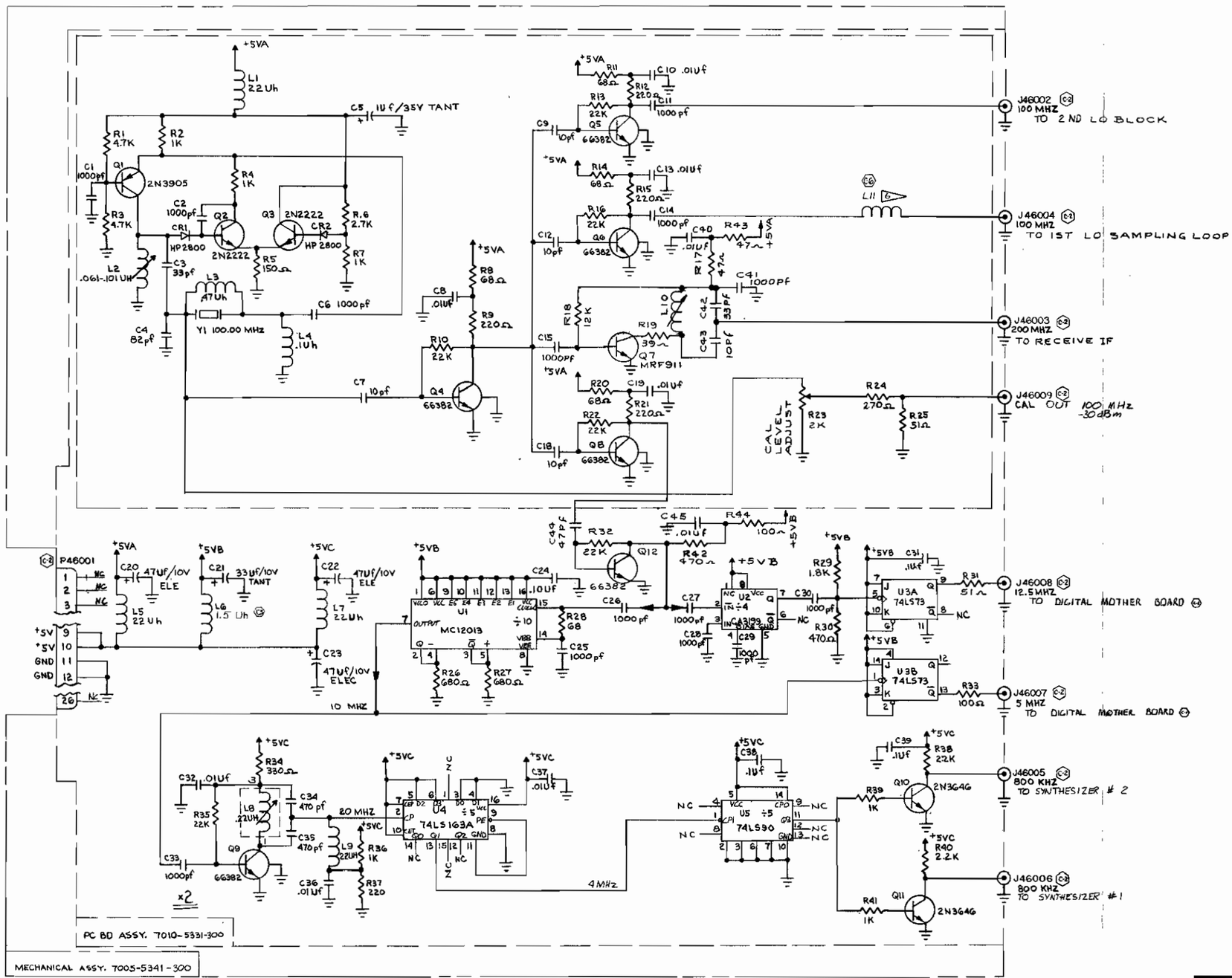


TOP VIEW



BOTTOM VIEW

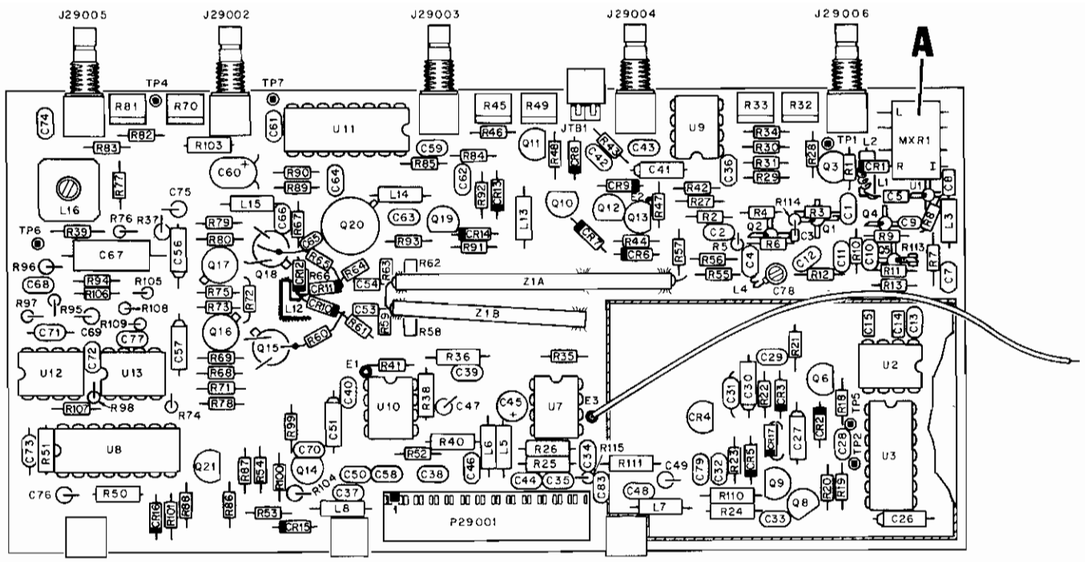
REFERENCE OSCILLATOR PC BOARD



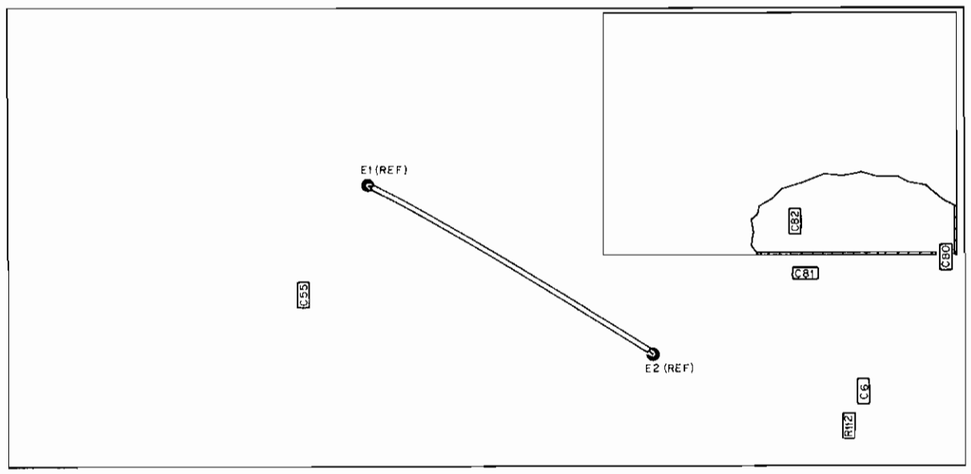
NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. MECH ASSY - 46000 (E.G, J1 IS 46001).
   - B. PC BD ASSY - 47000 (E.G., R1 IS 47001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS AS NOTED.
5. NOT USED.
6. L47011 IS TEN TURNS OF 38 AWG ENAMELED WIRE AROUND A .038 DIA CORE.

Figure 5-17 Reference Oscillator Module (D-0000-5311-300-C6)

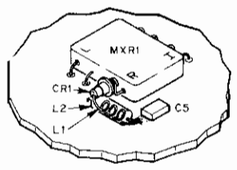


TOP VIEW



BOTTOM VIEW

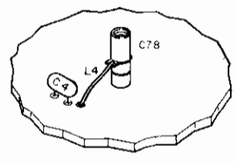
1ST LO SAMPLER LOOP PC BOARD



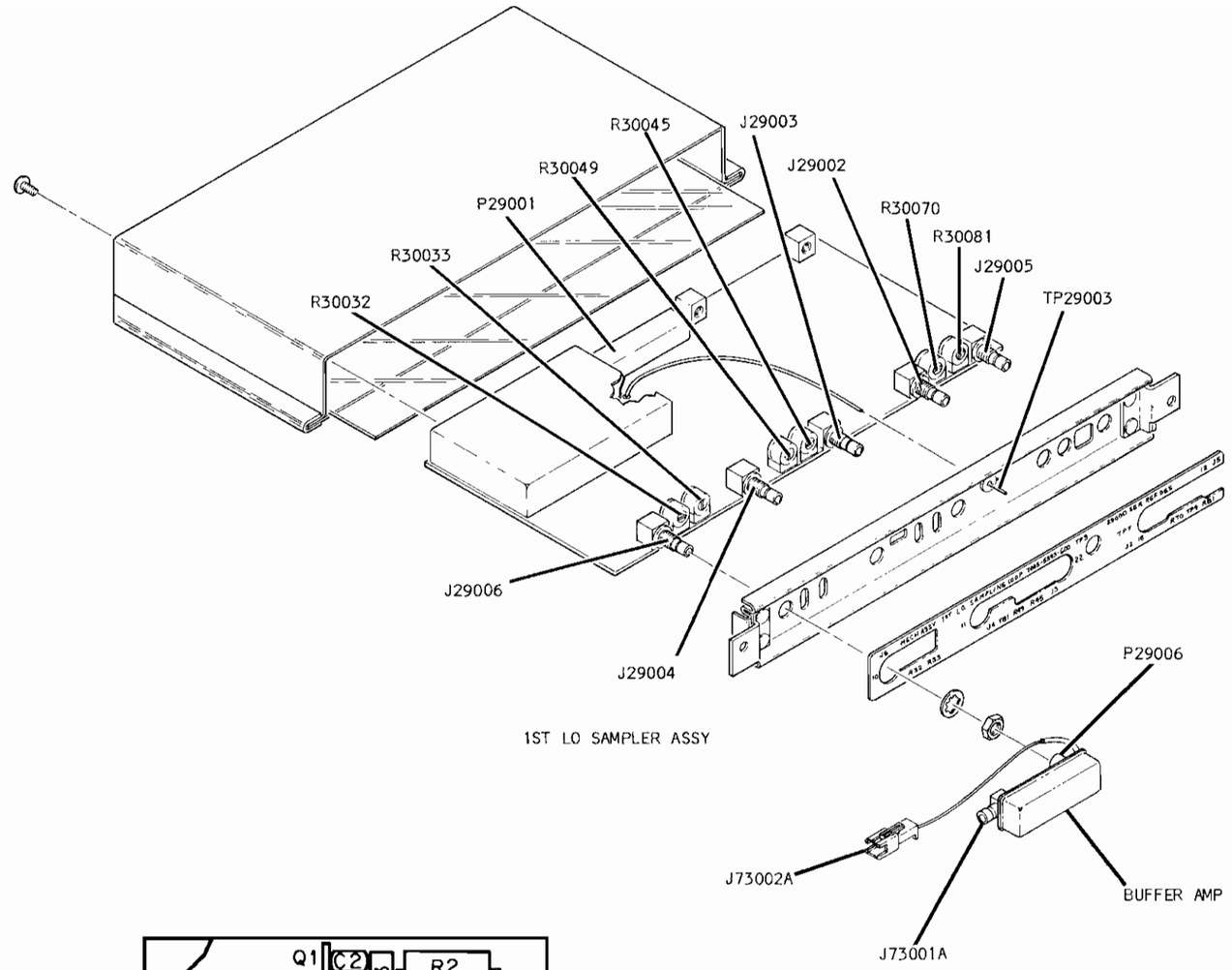
DETAIL **A**



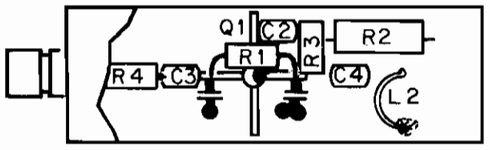
DETAIL **B**



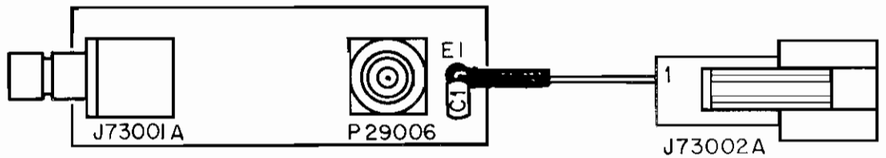
DETAIL **C**



1ST LO SAMPLER ASSY

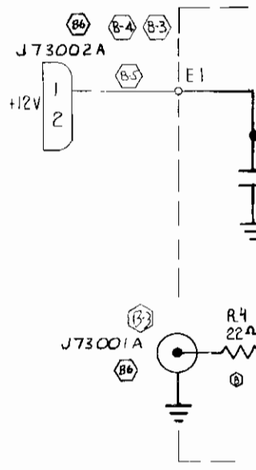


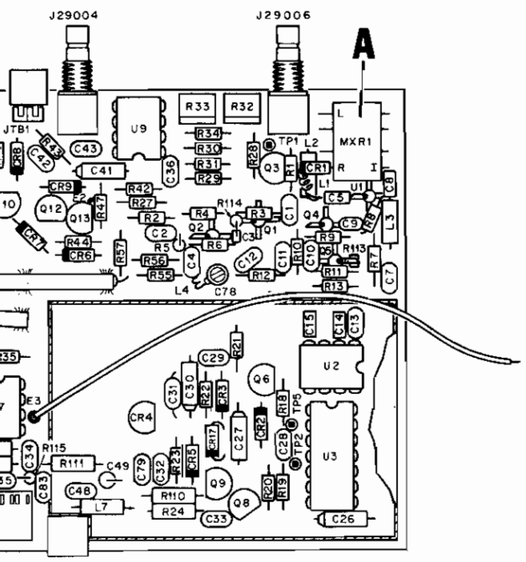
TOP VIEW

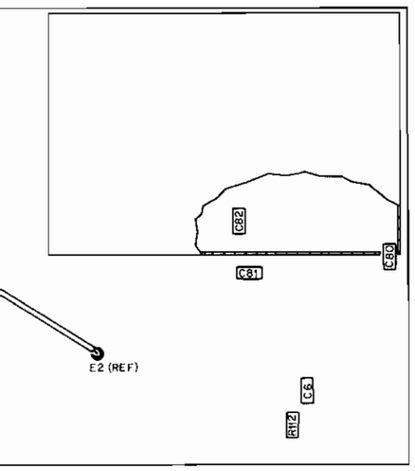


BOTTOM VIEW

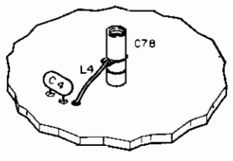
BUFFER AMP ASSY



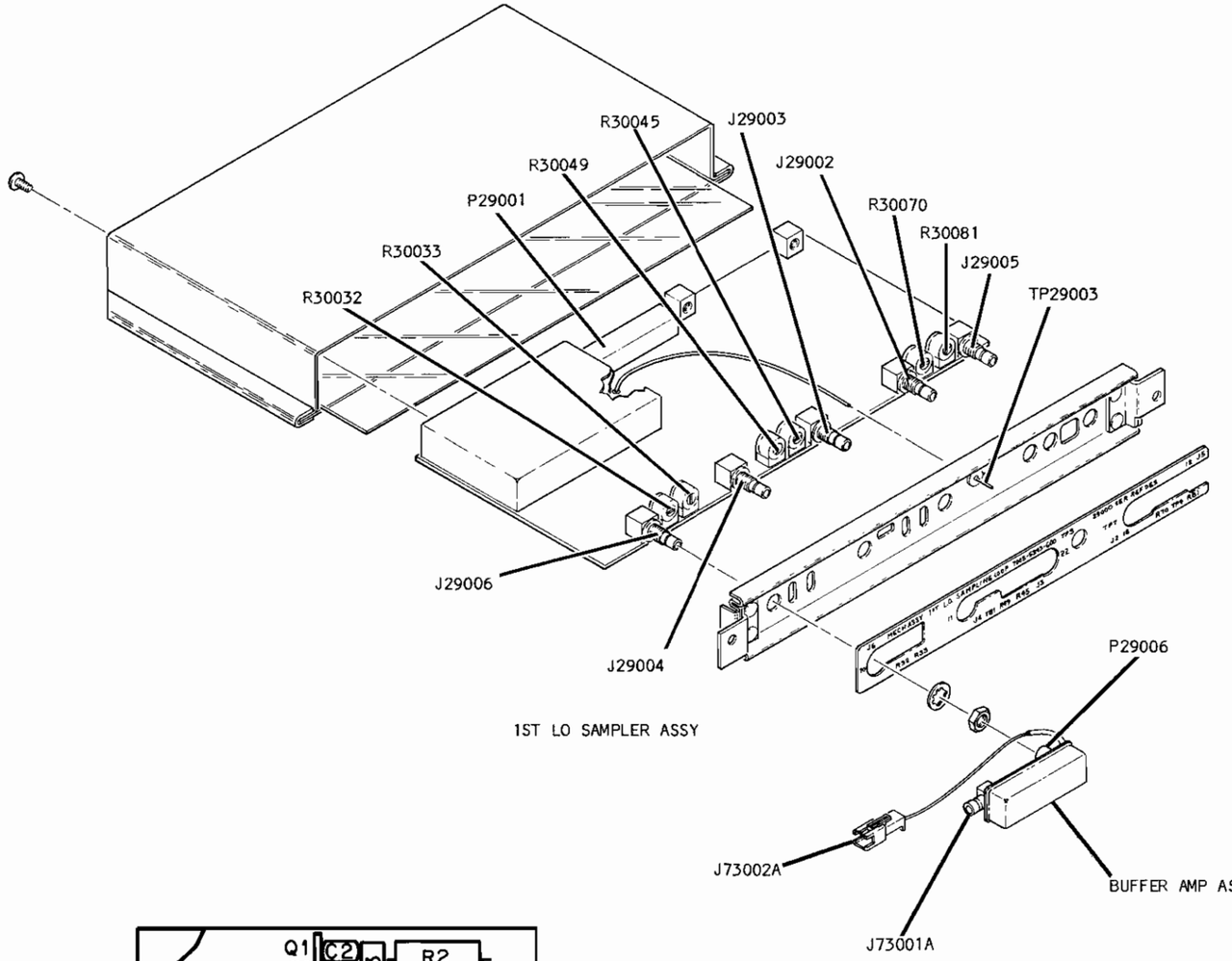




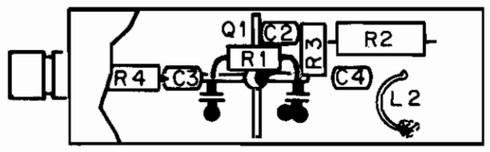
C BOARD



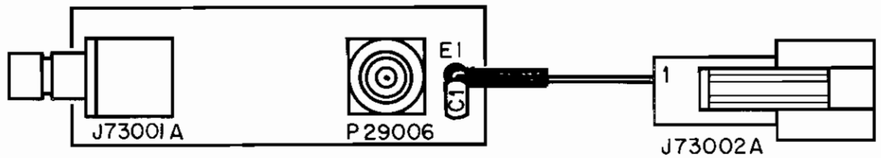
DETAIL C



1ST LO SAMPLER ASSY



TOP VIEW



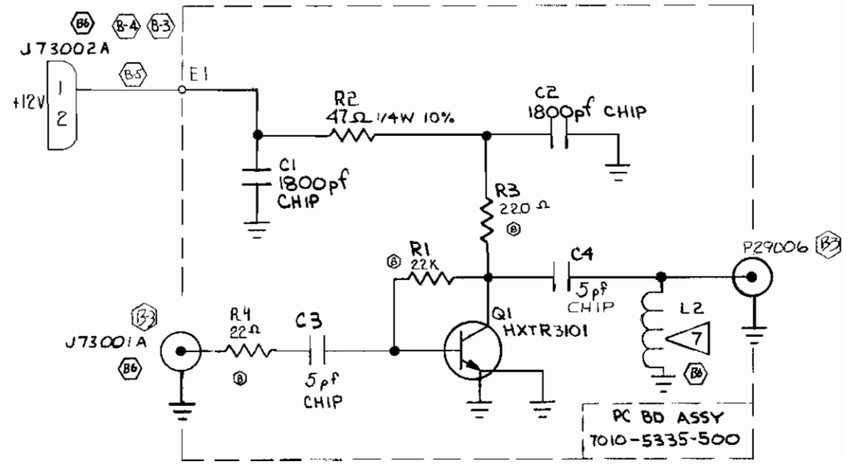
BOTTOM VIEW
BUFFER AMP ASSY

NOTES (1ST LO SAMPLING MODULE SCHEM):

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. MECH ASSY - 29000 (E.G., J1 IS J29001).
   - B. PC BD ASSY - 30000 (E.G., R1 IS R30001).
2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).
4. CAPACITANCE IS AS DESIGNATED.
5. L29012 IS A .020" X 0.2" PATH ON PC BD.

NOTES (BUFFER AMP SCHEM):

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 73000 (E.G., R1 IS R73001).
2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).
3. ALL RESISTANCE IS EXPRESSED IN OHMS.
4. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS (UNLESS SPECIFIED).
5. NOT USED.
6. NOT USED.
7. L73002 IS A .5" LOOP OF .26 GA BUS WIRE.



NOTES (1ST LO SAMPLING MODULE SCHEM):

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. MECH ASSY - 29000 (E.G., J1 IS J29001).

   B. PC BD ASSY - 30000 (E.G., R1 IS R30001).

2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).

3. RESISTANCE IS EXPRESSED IN OHMS (UNLESS NOTED).

4. CAPACITANCE IS AS DESIGNATED.

5. L29012 IS A .020" X 0.2" PATH ON PC BD.

NOTES (BUFFER AMP SCHEM):

1. ALL REF NO'S CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 73000 (E.G., R1 IS R73001).

2. ALL RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. ALL CAPACITANCE IS EXPRESSED IN PICO-FARADS (UNLESS SPECIFIED).

5. NOT USED.

6. NOT USED.

7. L73002 IS A .5" LOOP OF .26 GA BUS WIRE.

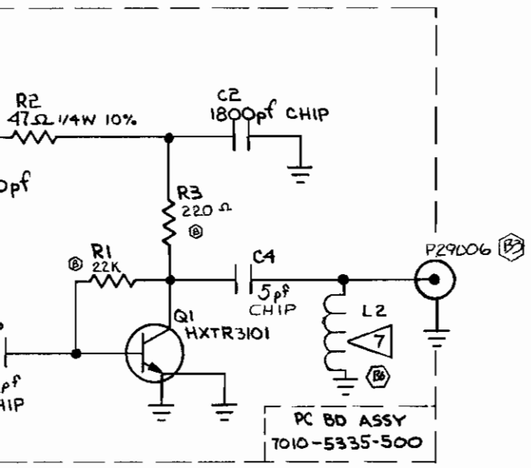
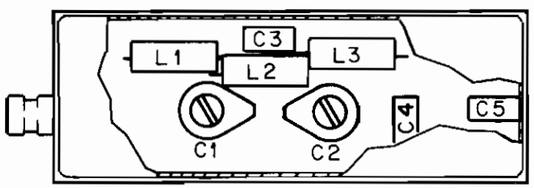
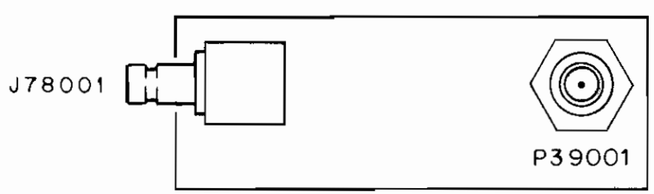


Figure 5-18 1st L.O. Sampling Loop Module (B-0000-5315-500-B5) (D-0000-5314-600-F7)

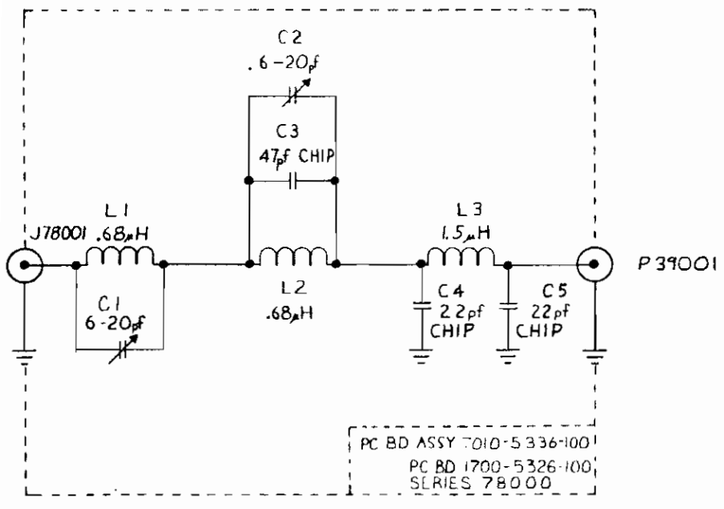


BOTTOM



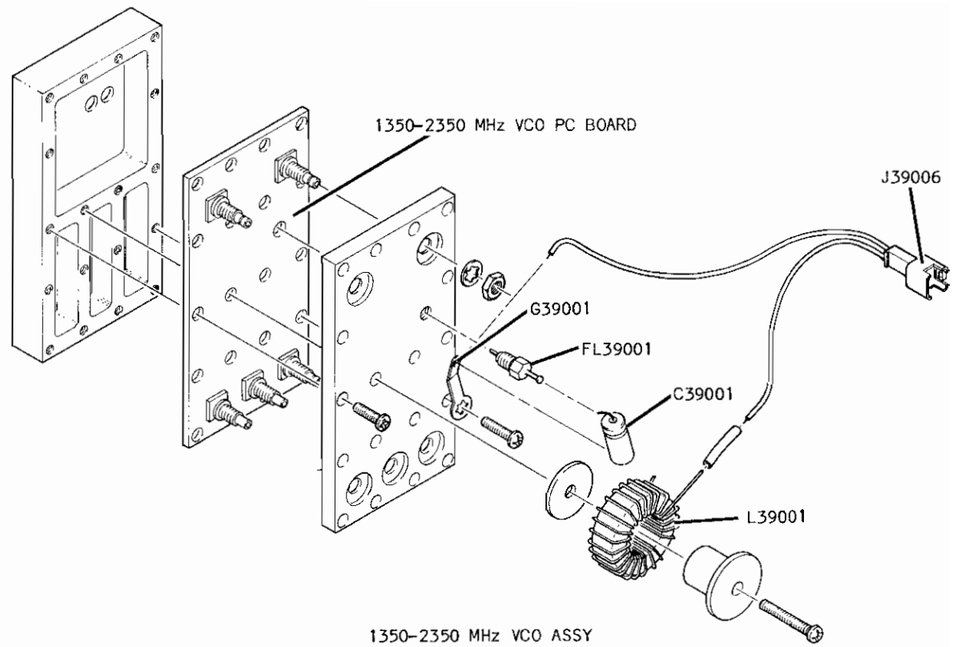
TOP

VCO FILTER

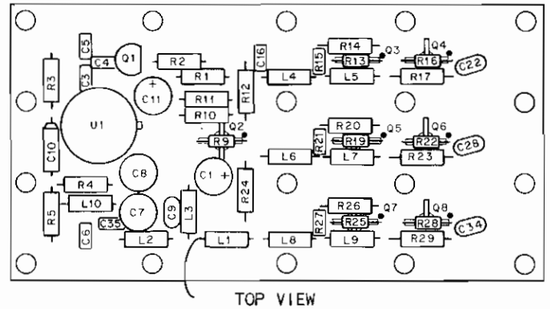


NOTES:

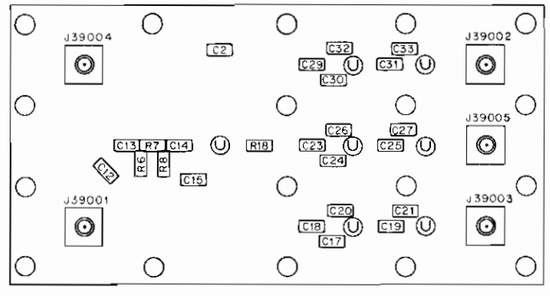
1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES 78000 (E.G., L1 IS L78001).



1350-2350 MHz VCO ASSY

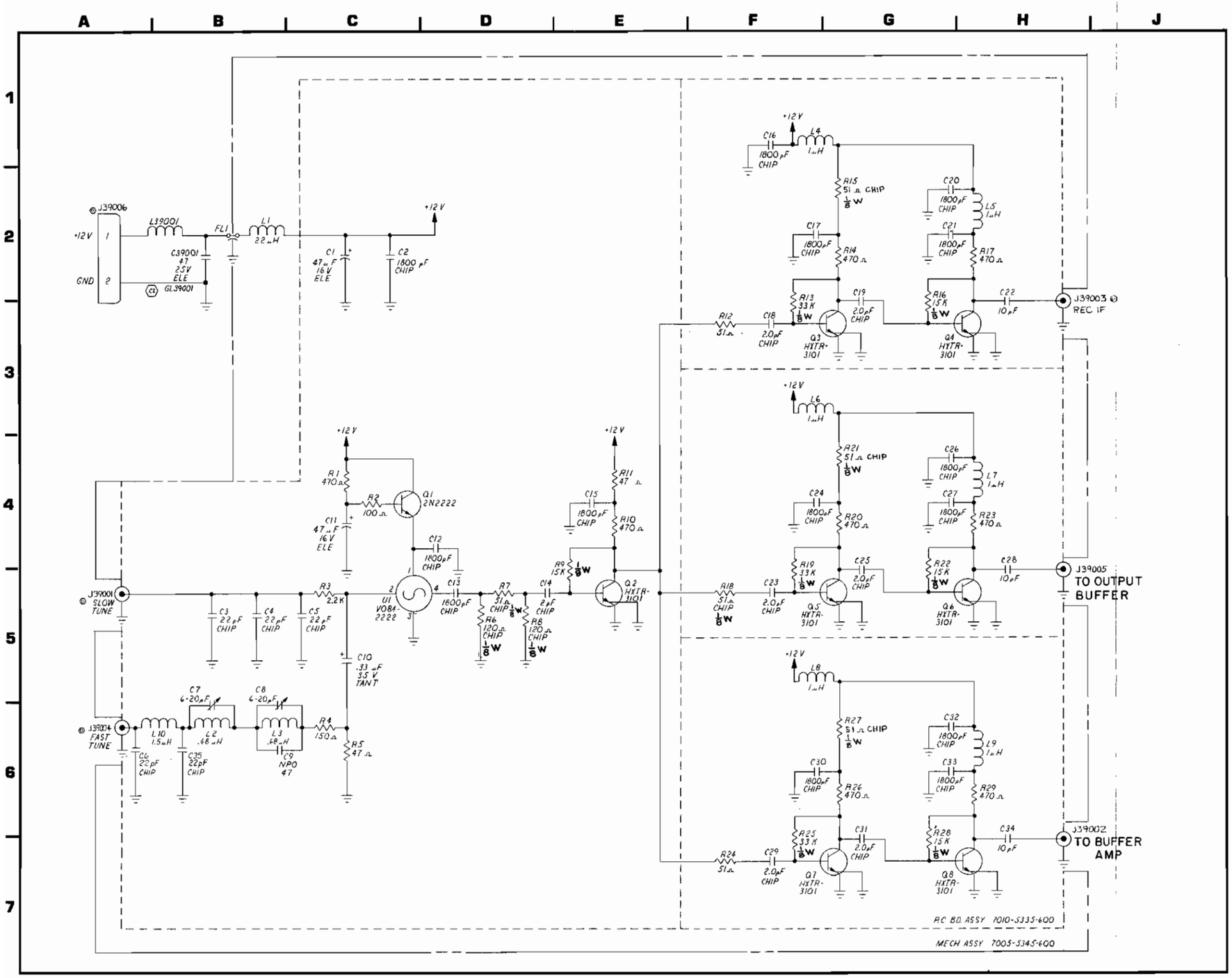


TOP VIEW



BOTTOM VIEW

1350-2350 MHz VCO PC BOARD



NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. MECH ASSY - 39000 (E.G., L1 IS L39001).

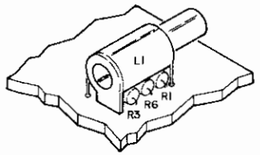
   B. PC BD ASSY - 40000 (E.G., R1 IS R40001).

2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).

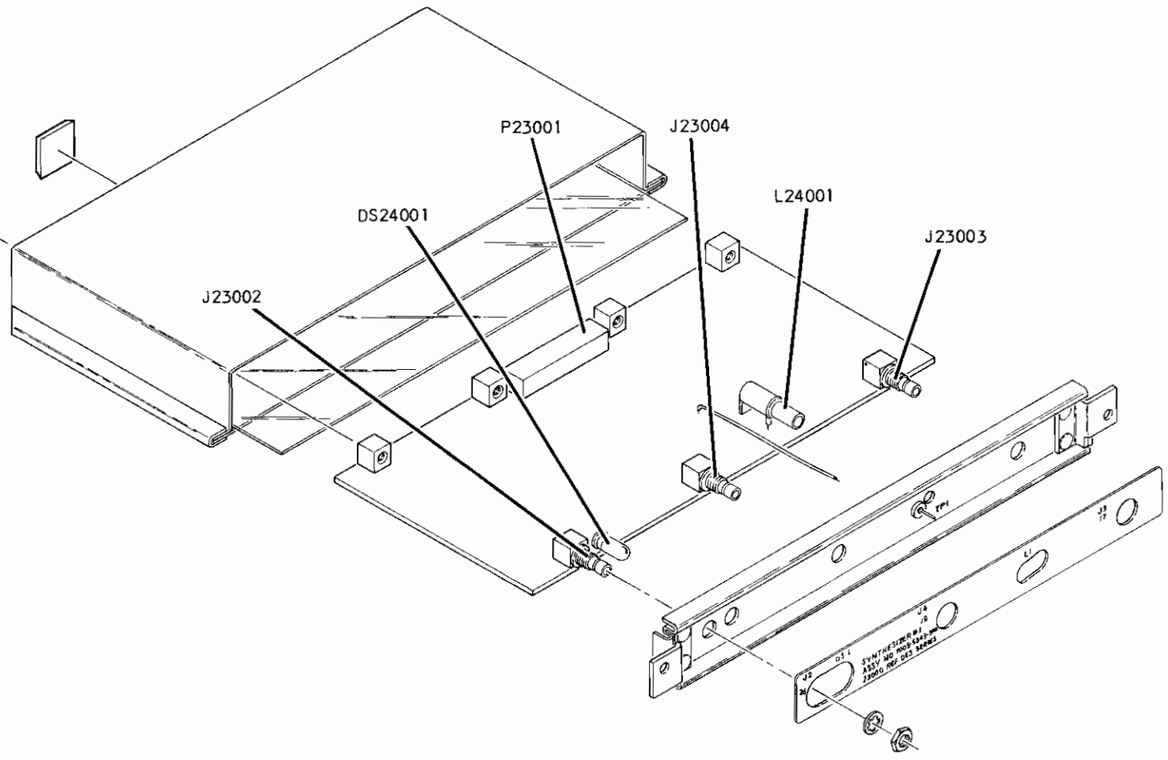
3. RESISTANCE IS IN OHMS.

4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

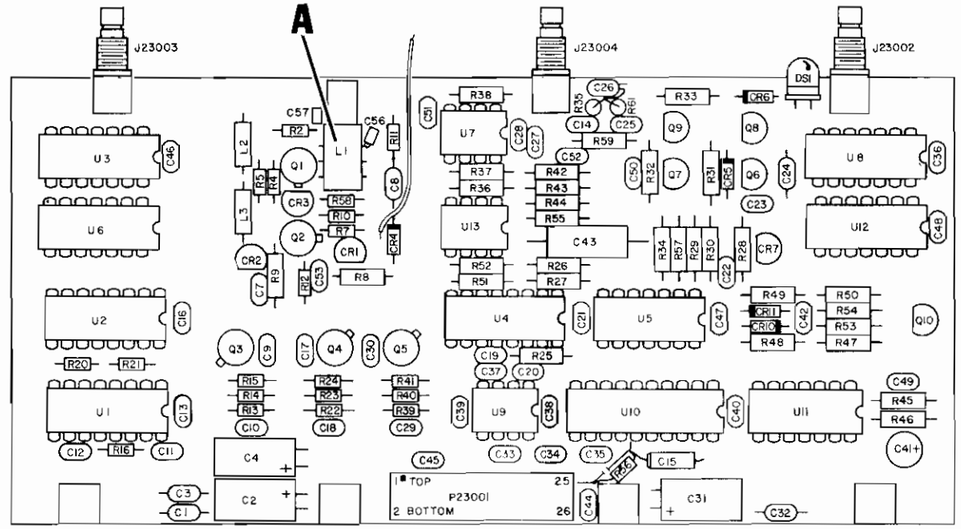
Figure 5-19 1350-2350 MHz VCO Module (D-0000-5315-600-C2)



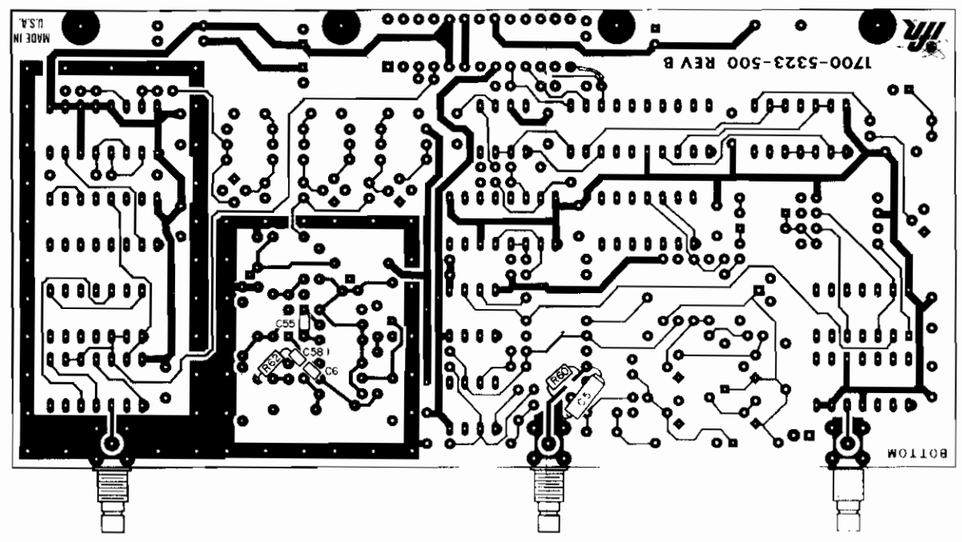
DETAIL **A**



SYNTHESIZER #1 ASSY

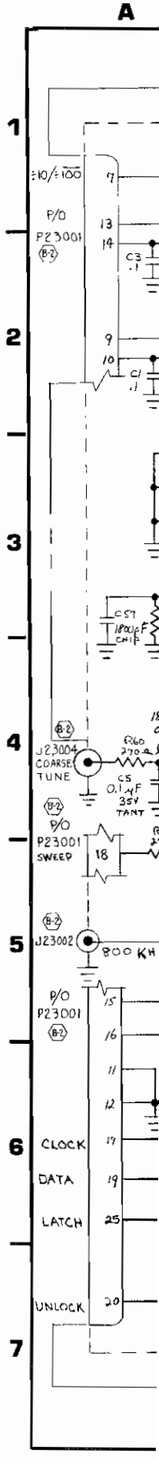


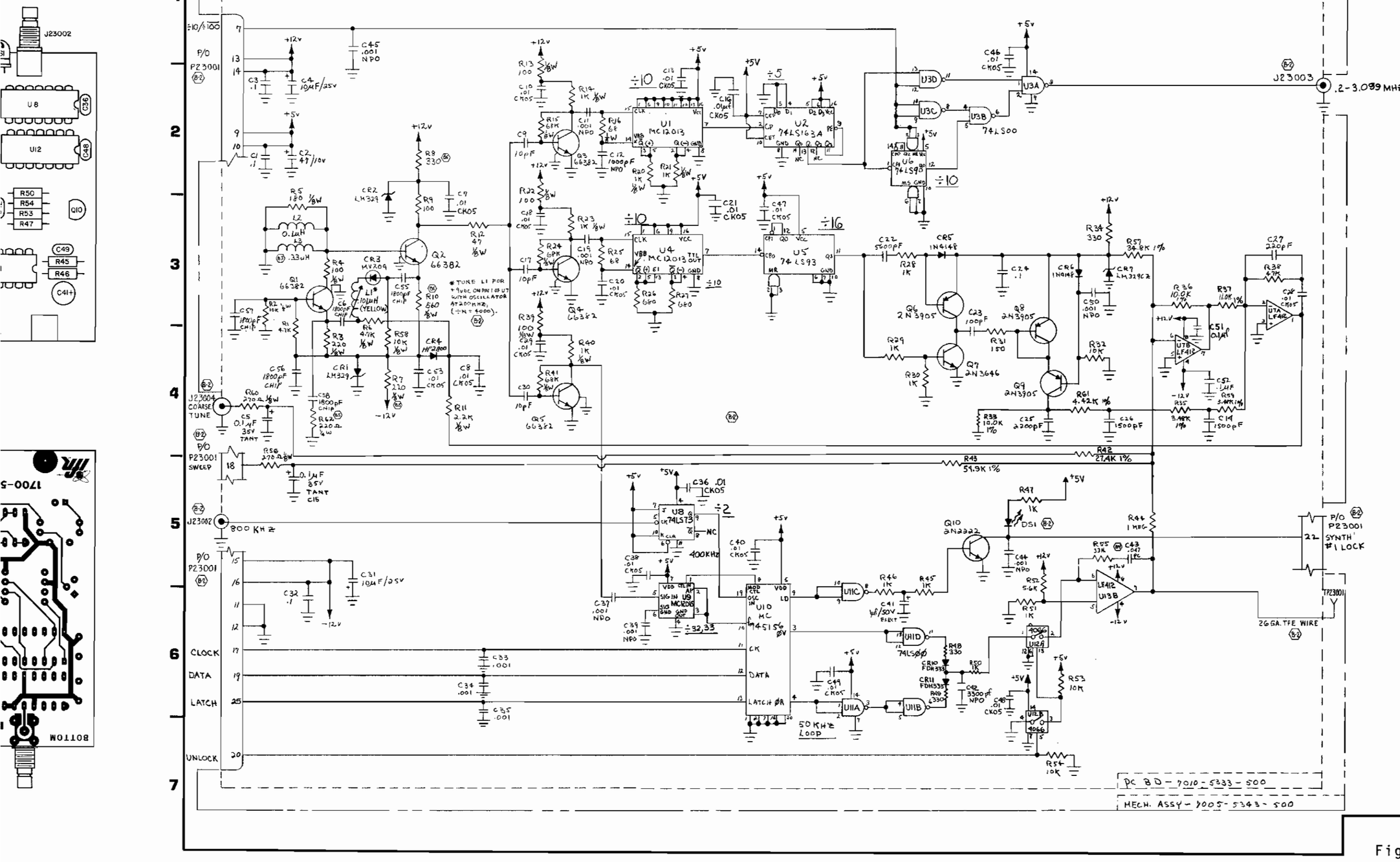
TOP VIEW



BOTTOM VIEW

SYNTHESIZER #1 PC BOARD

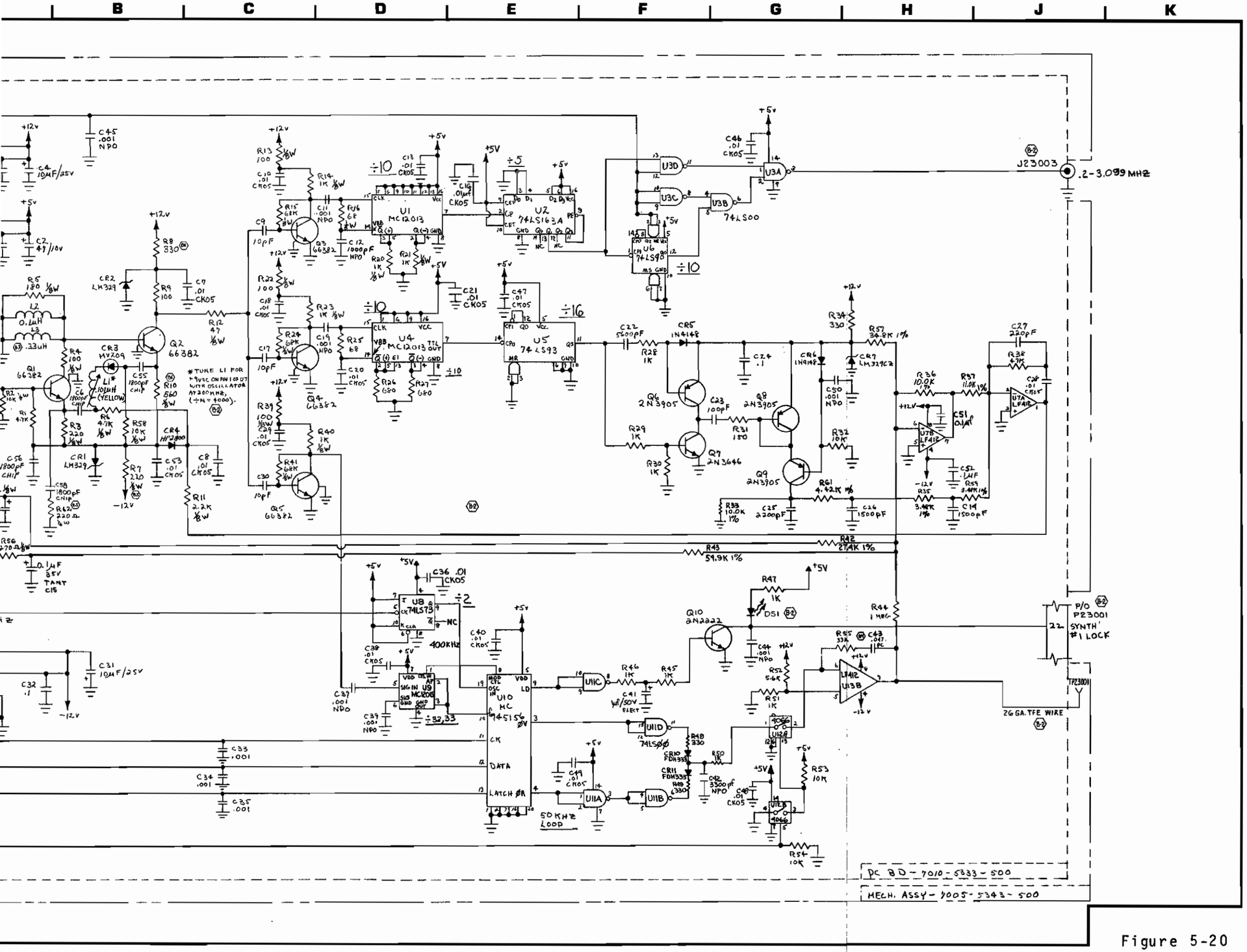




NOTES:

1. ALL RE DESIGNA CARRIES
   - A. PC R24
   - B. MEC P23
2. RESISTO (UNLESS
3. RESISTA
4. CAPACIT NOTED).

Figure 5-20 Synthesizer #1 M (D-0000-5313-500



NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. PC BD ASSY - 24000 (E.G, R1 IS R24001).
   - B. MECH ASSY - 23000 (E.G., P1 IS P23001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

Figure 5-20 Synthesizer #1 Module (D-0000-5313-500-B6)

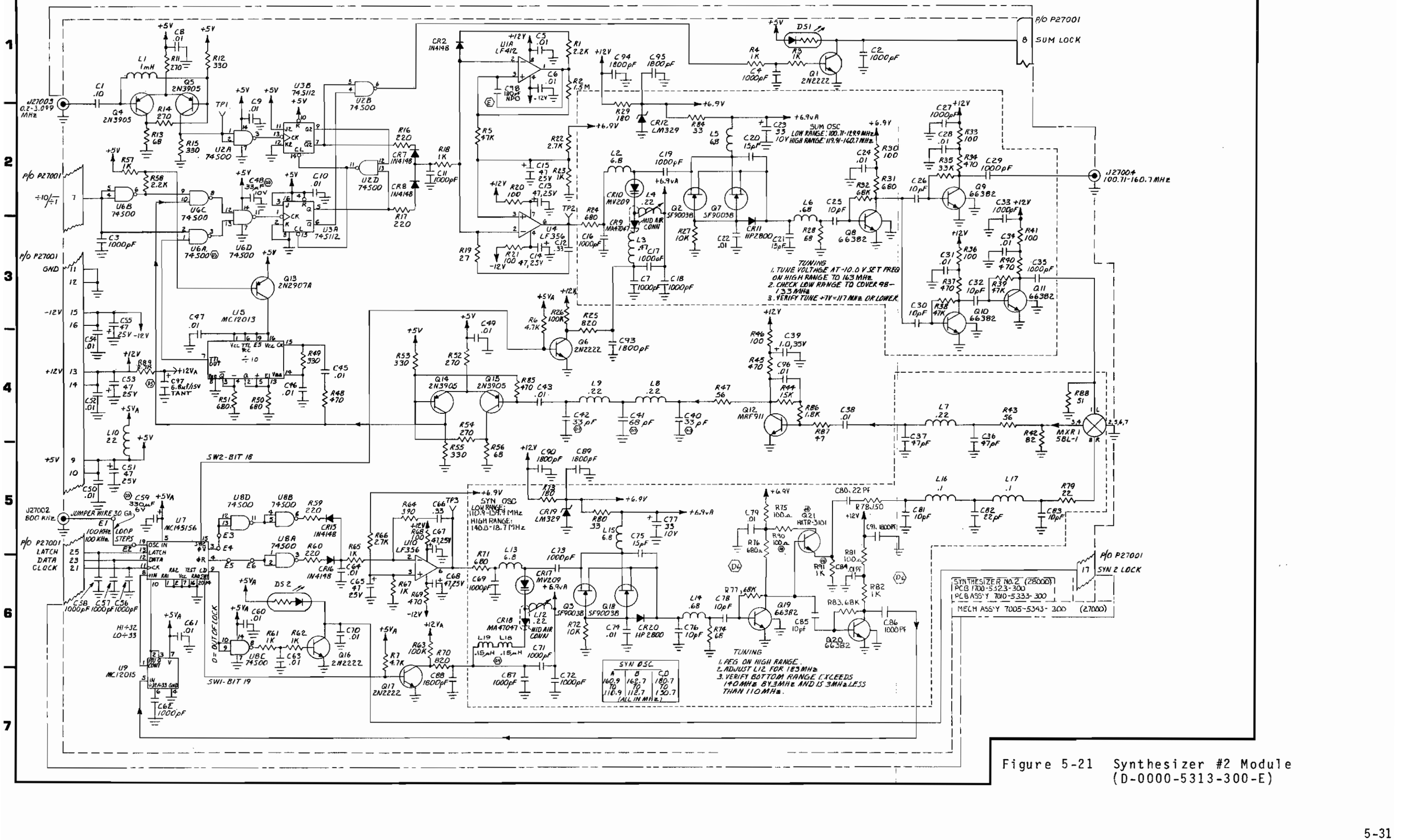
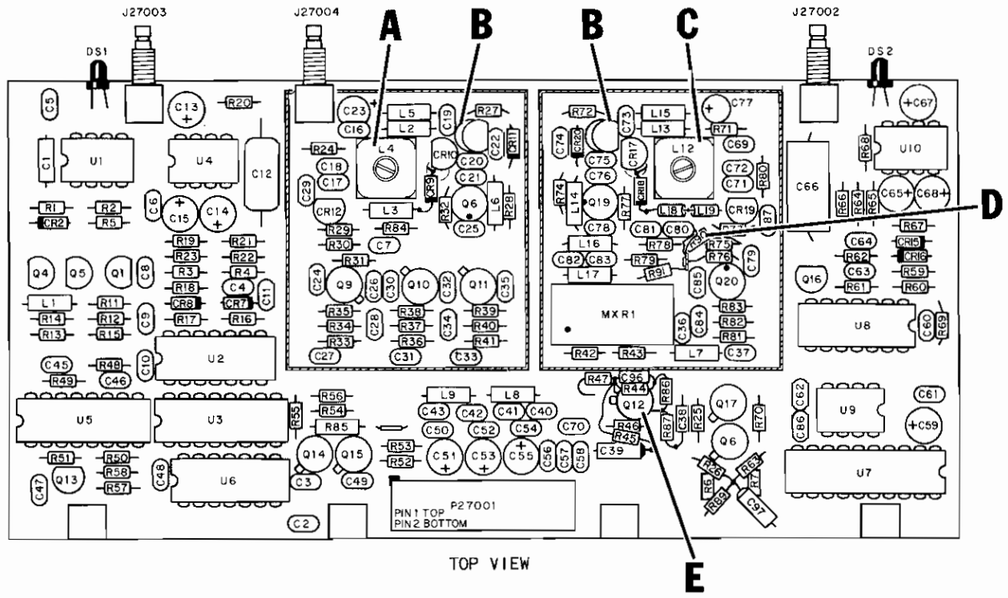
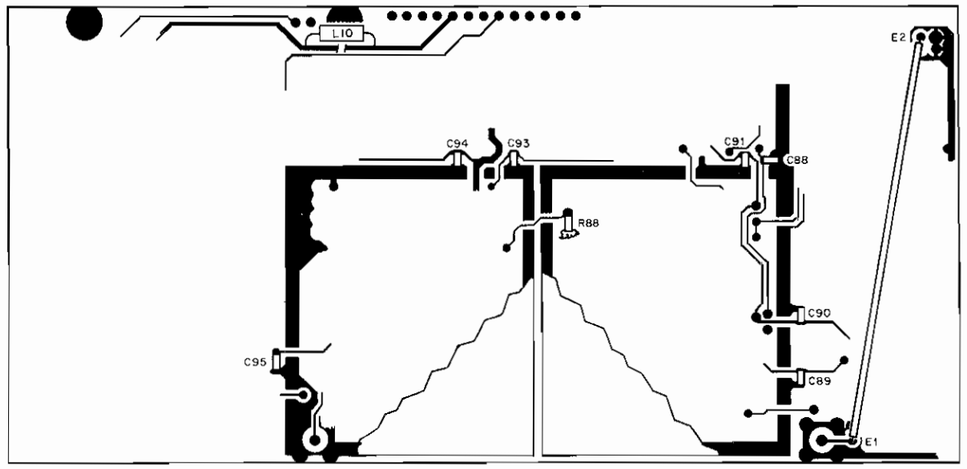


Figure 5-21 Synthesizer #2 Module (D-0000-5313-300-E)

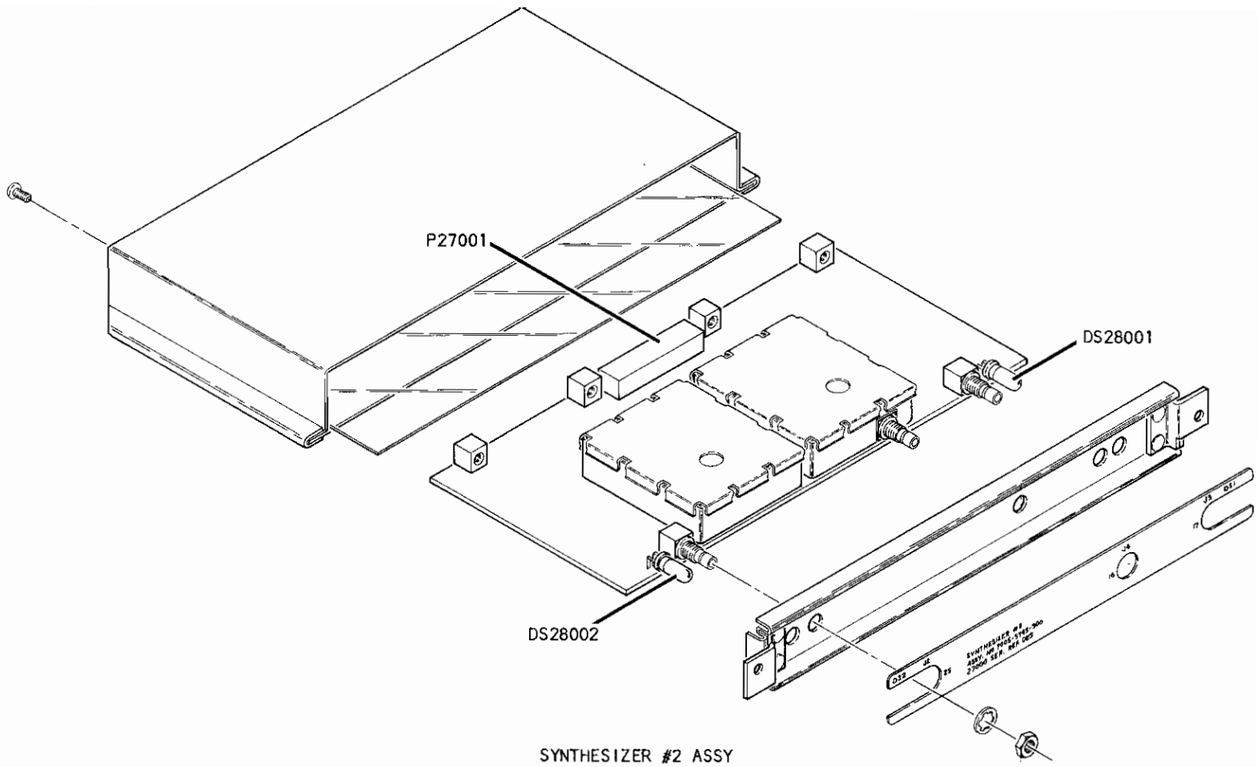


TOP VIEW

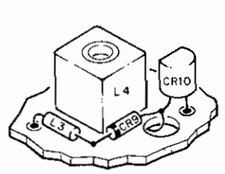


BOTTOM VIEW

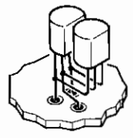
SYNTHESIZER #2 PC BOARD



SYNTHESIZER #2 ASSY

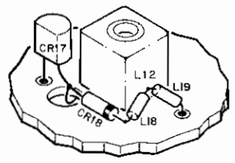


DETAIL **A**

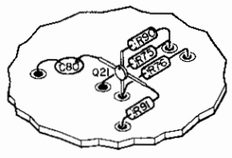


Q18 & Q3, Q2 & Q7

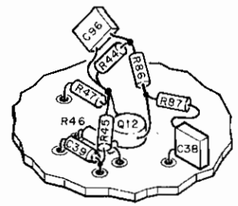
DETAIL **B**



DETAIL **C**



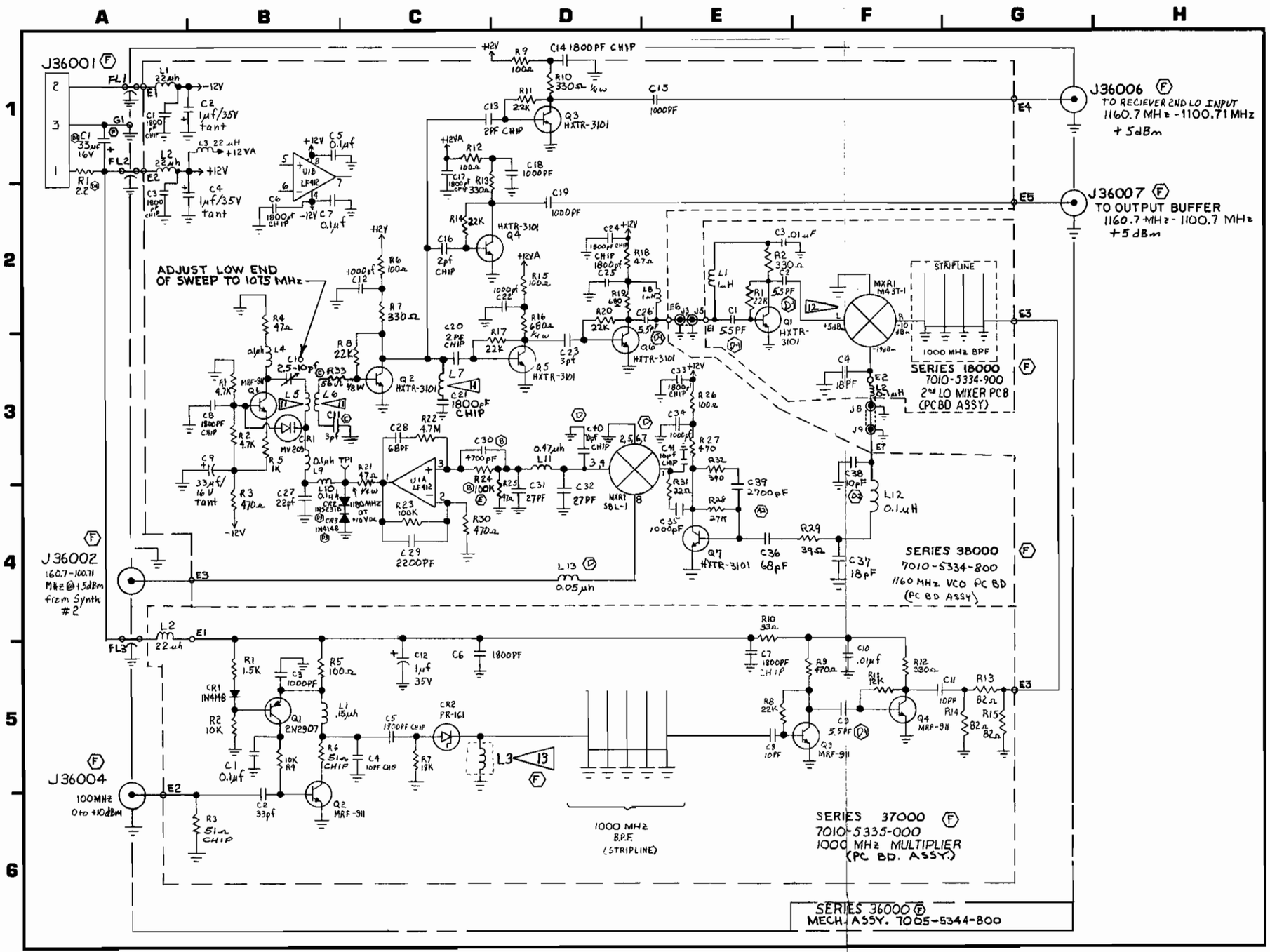
DETAIL **D**



DETAIL **E**

NOTES:

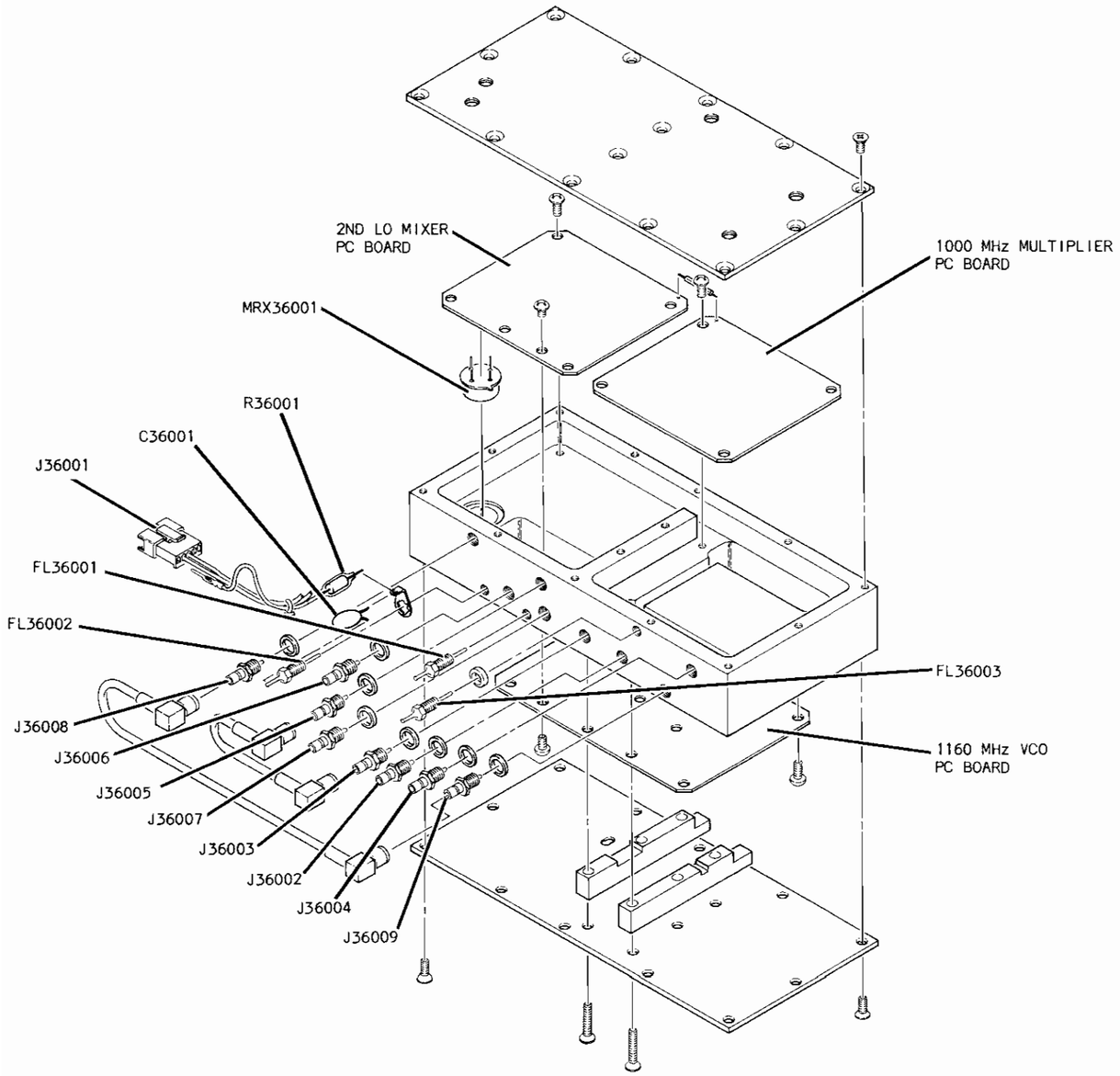
1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   A. PC BD ASSY IS 28000 (E.G., R1 IS R28001).
   B. MECH ASSY IS 27000 (E.G., J1 IS J27001).
2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS.
4. WHEN ÷10/÷1 IS LOW, THE SUMMING OSCILLATOR IS SWITCHED TO HIGH RANGE WHEN THE SYNTHESIZED OSCILLATOR IS 125.0 MHz AND ABOVE.
5. WHEN ÷10/÷1 IS HIGH THE SUMMING OSCILLATOR IS SWITCHED TO HIGH RANGE WHEN THE SYNTHESIZED OSCILLATOR IS 150.0 MHz AND ABOVE.
6. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS NOTED).
7. INDUCTANCE IS EXPRESSED IN MICROHENRYS (UNLESS NOTED).



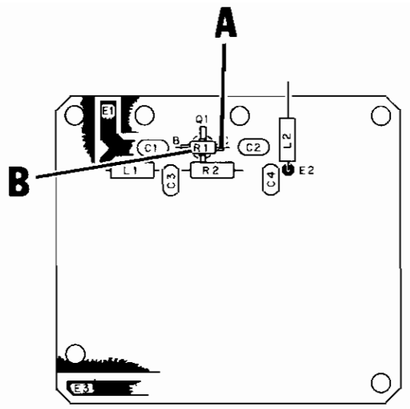
NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. 2ND LO PC BD IS 18000 (E.G., R1 IS R18001).
   - B. 1000 MHz MULTIPLIER PC BD IS 37000 (E.G., R1 IS R37001).
   - C. 1160 MHz VCO PC BD IS 38000 (E.G., R1 IS R38001).
   - D. MECH ASSY IS 36000 (E.G., J1 IS J36001).
2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS IN OHMS.
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).
5. NOT USED.
6. NOT USED.
7. NOT USED.
8. NOT USED.
9. NOT USED.
10. NOT USED.
11. INDUCTORS CREATED BY 0.2" OF .22 GA WIRE.
12. MXR36001 IS INSTALLED AT MECHANICAL
13. L37003 IS STRIPLINE TECHNOLOGY.

Figure 5-22 2nd L.O. Sampling Loop Module (D-0000-5314-800-F)

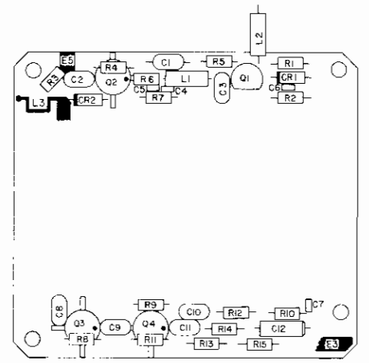


2ND L.O. BLOCK ASSY



TOP VIEW

2ND LO MIXER PC BOARD

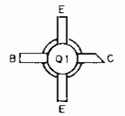


TOP VIEW



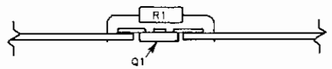
BOTTOM VIEW

1000 MHz MULTIPLIER PC BOARD

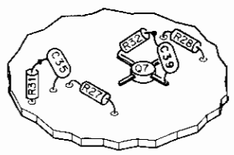


CLIP COLLECTOR
LEAD AT 45°
PRIOR TO INSTALLATION

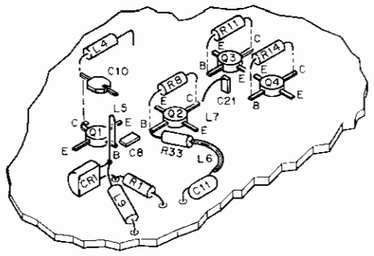
DETAIL **A**



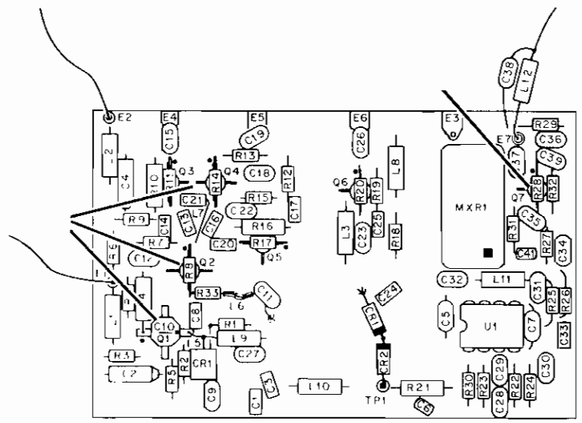
DETAIL **B**

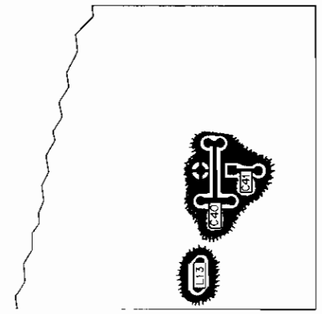


DETAIL **C**



DETAIL **D**





BOTTOM VIEW

1160 MHz VCO PC BOARD

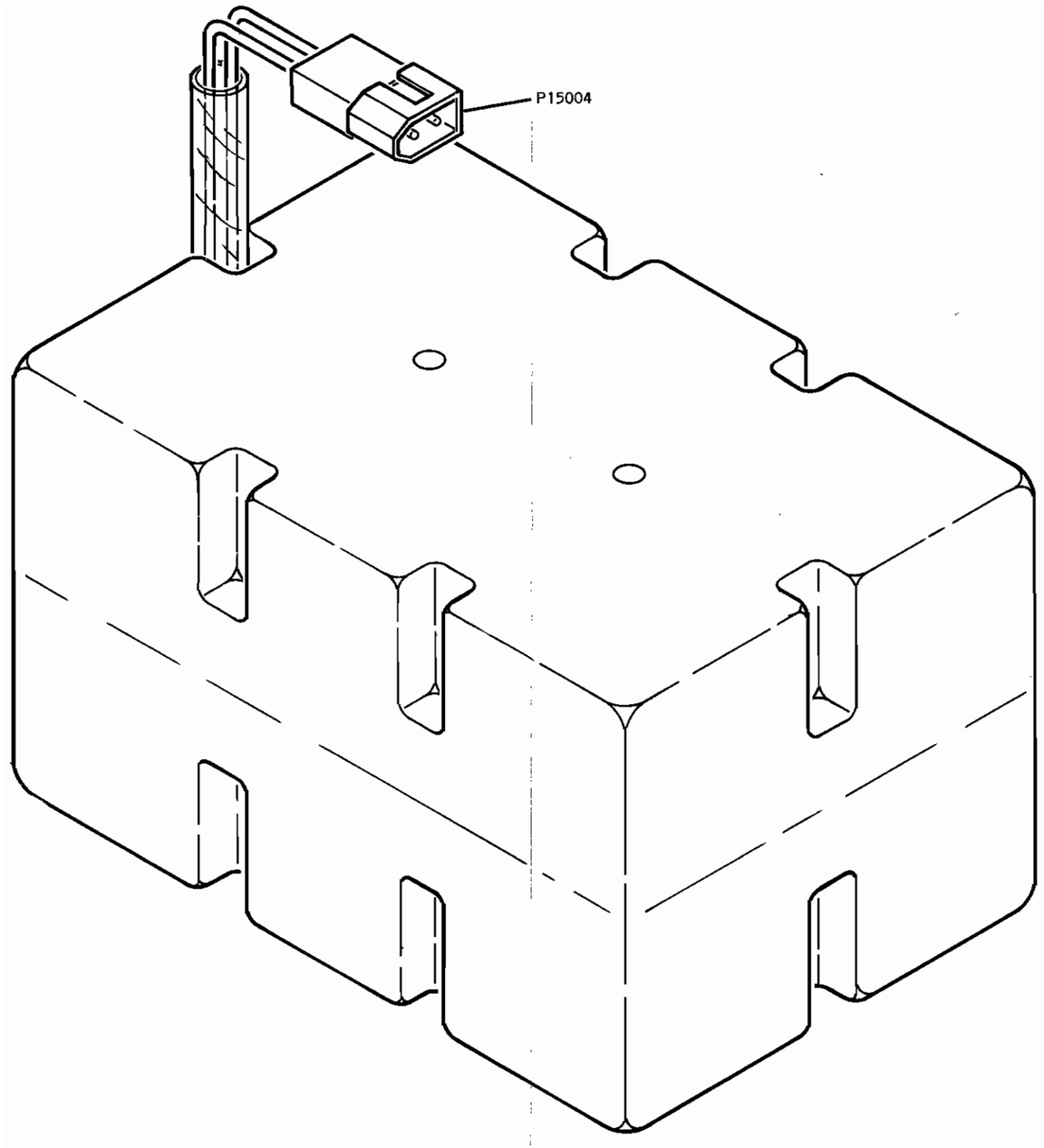
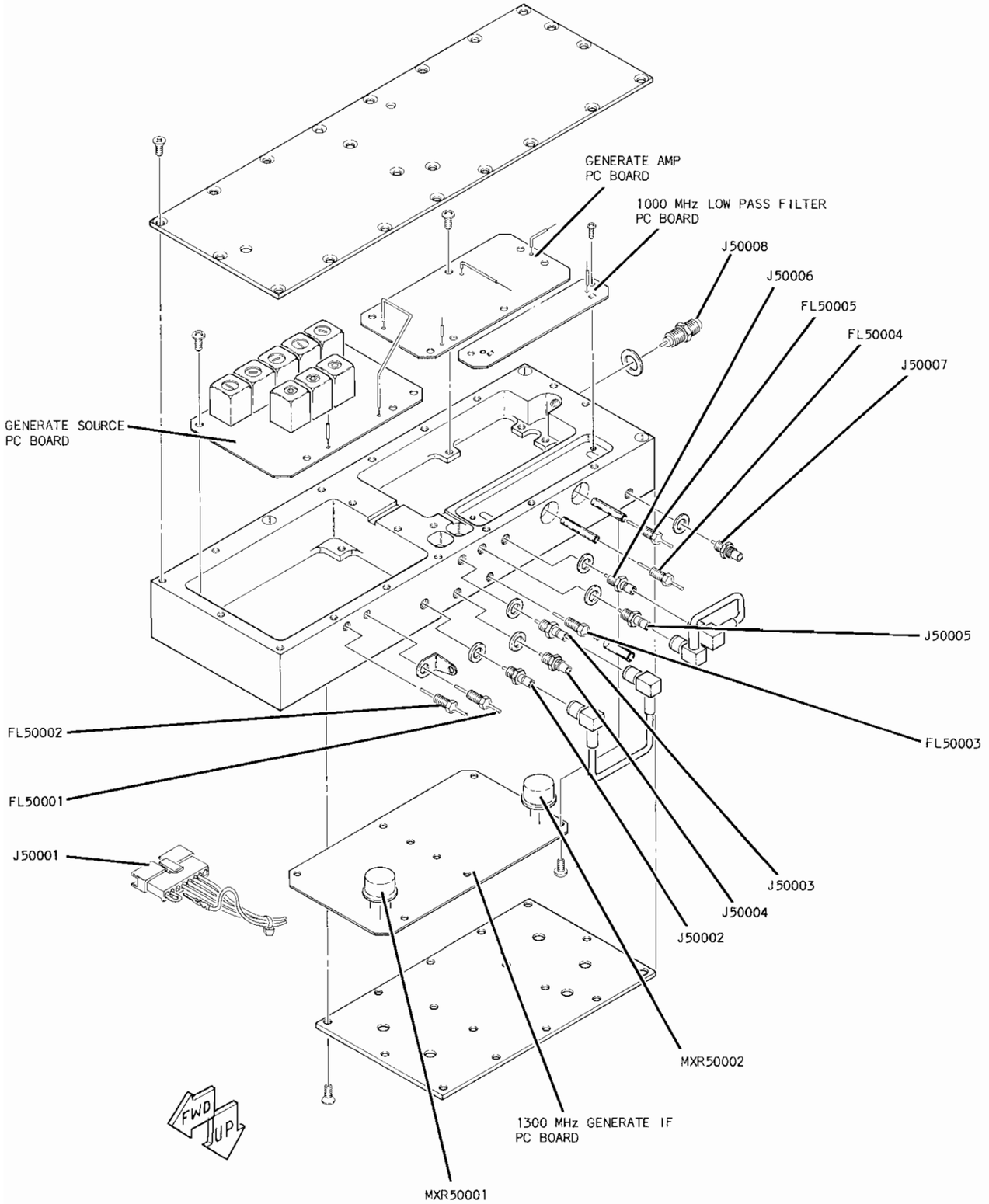
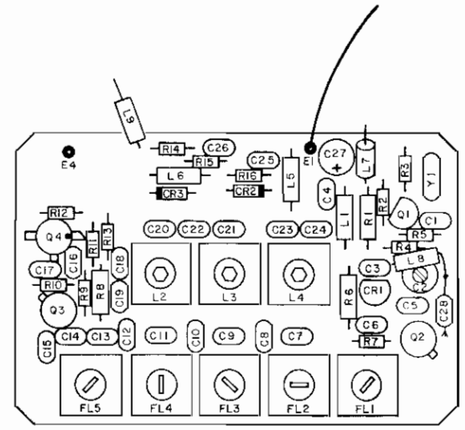
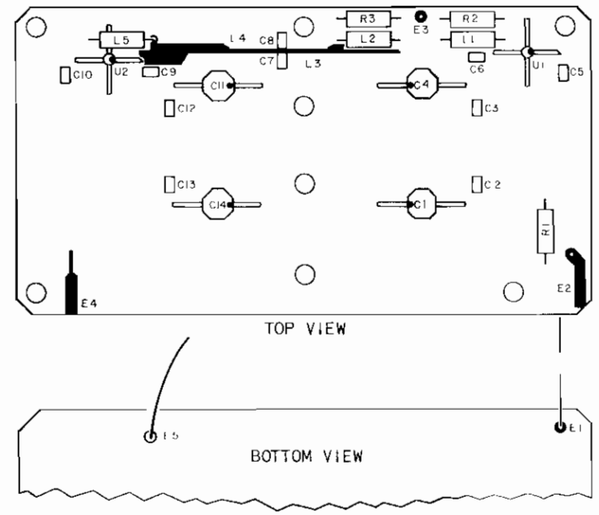
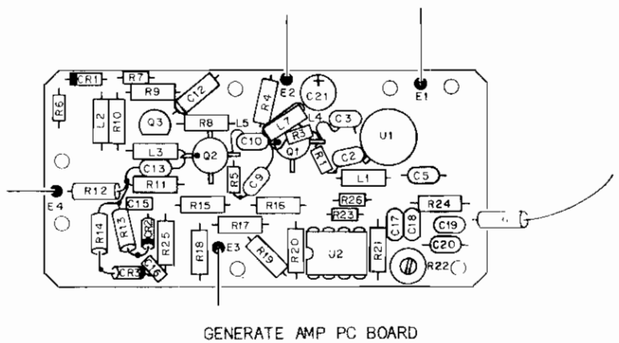


Figure 5-23 Option 1: Battery
(C-7005-7624-500-L)


GENERATE AMP
PC BOARD
1000 MHz LOW PASS FILTER
PC BOARD
J50008
J50006
FL50005
FL50004
J50007
GENERATE SOURCE
PC BOARD
J50005
FL50003
FL50002
FL50001
J50001
J50003
J50004
J50002
MXR50002
1300 MHz GENERATE IF
PC BOARD
MXR50001
FWD
UP


GENERATE SOURCE PC BOARD


TOP VIEW
BOTTOM VIEW
1300 MHz GENERATE IF PC BOARD


GENERATE AMP PC BOARD

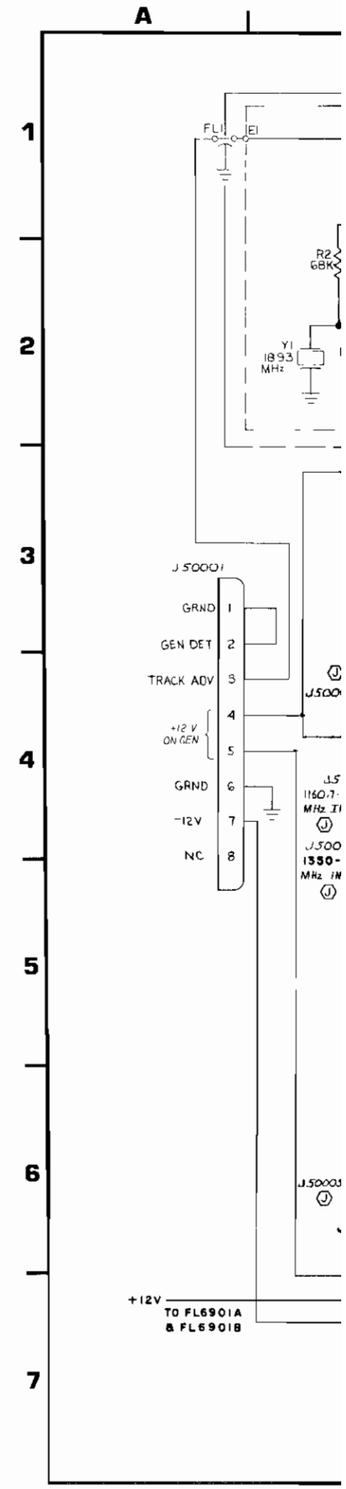
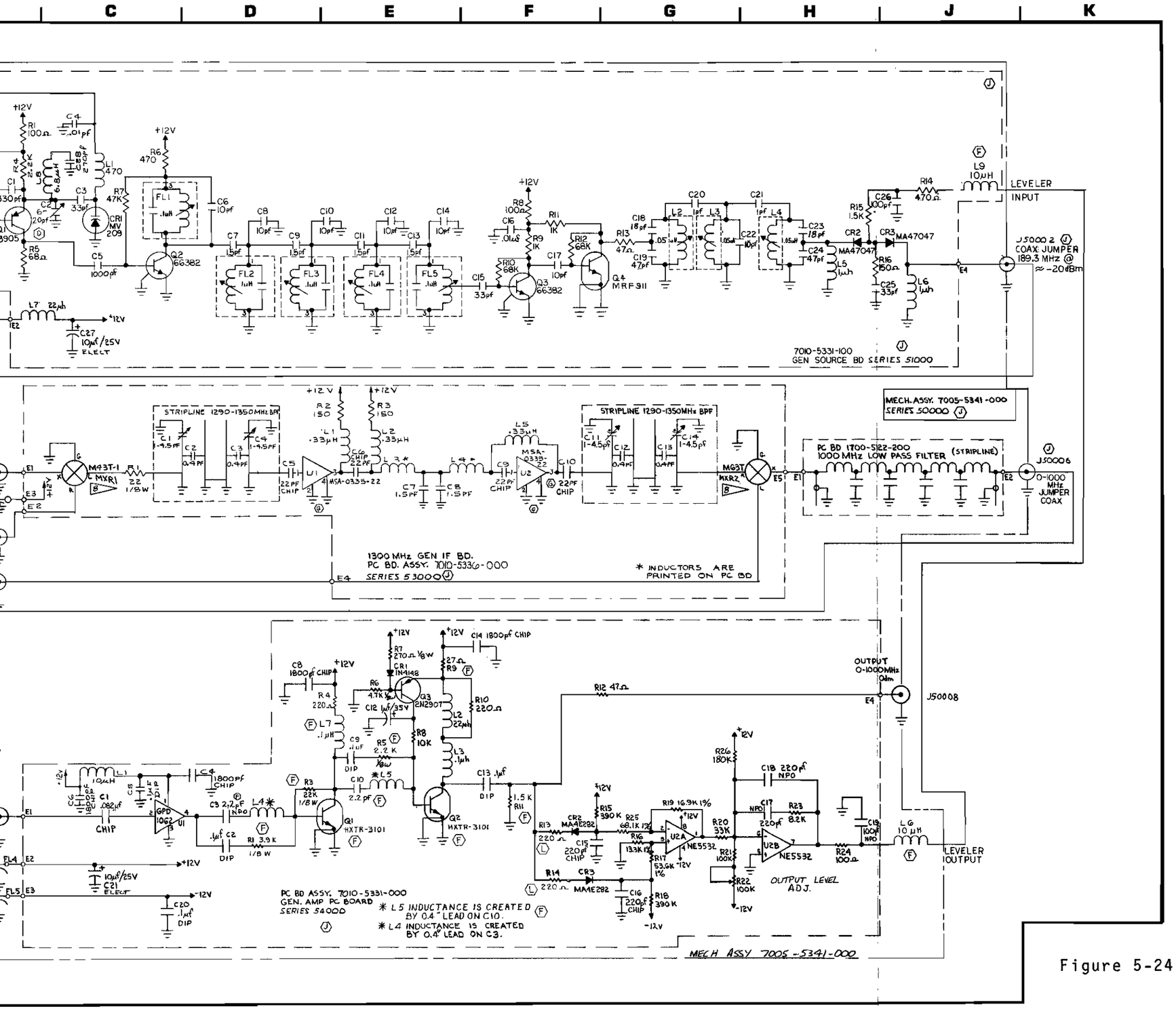

A
1
2
3
4
5
6
7
J50001
GRND
GEN DET
TRACK ADV
+12 V ON GEN
GRND
-12V
NC
+12V
TO FL6901A & FL69018

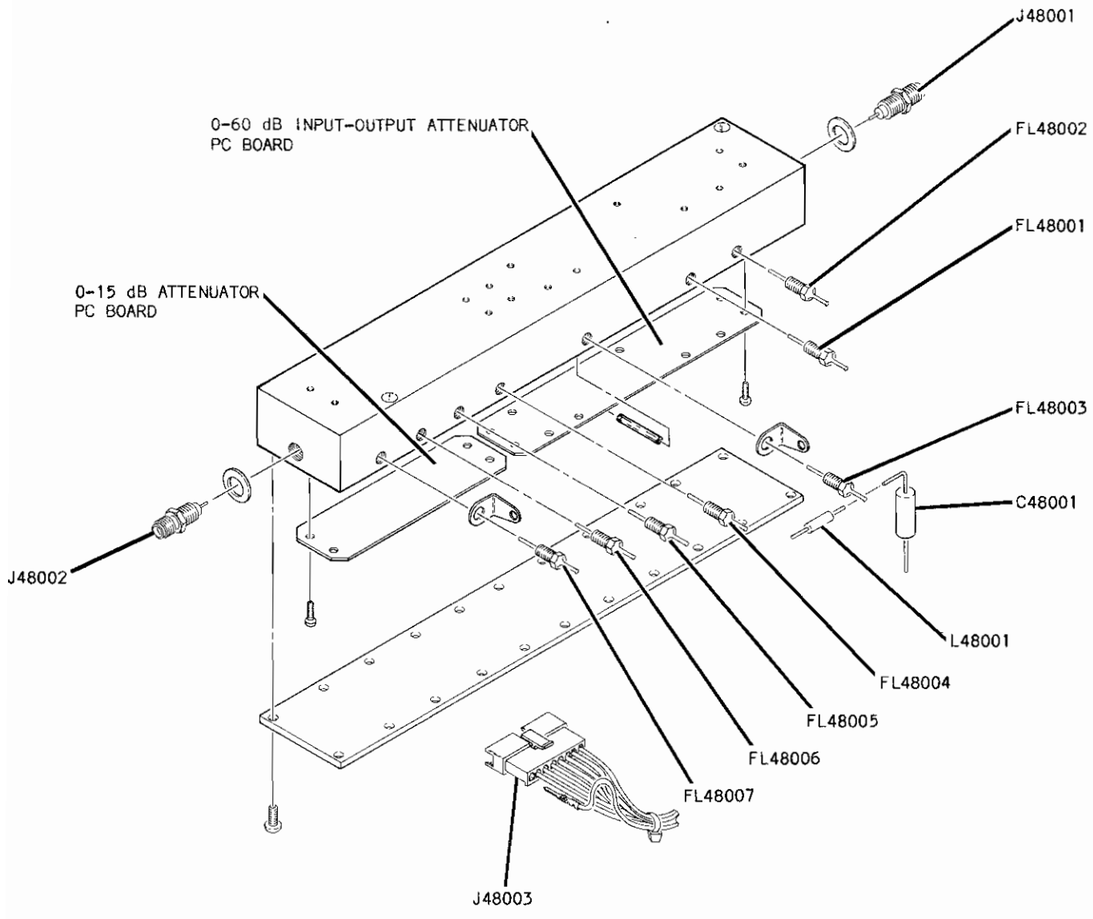
Figure 5-24 Option 2:
Attenuato
(D-0000-5



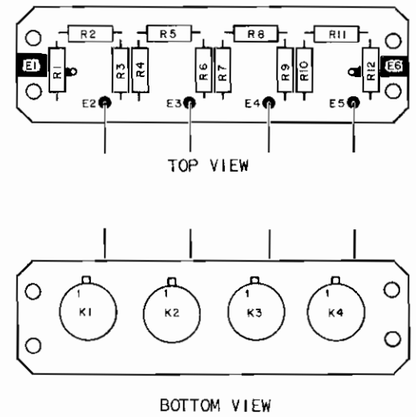
NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. GEN AMP PC BD IS 54000 (E.G., R1 IS R54001).
   - B. GEN SOURCE PC BD IS 51000 (E.G., R1 IS R51001).
   - C. 1300 MHz GEN IF PC BD IS 53000 (E.G., R1 IS R53001).
   - D. MECH ASSY IS 50000 (E.G., J1 IS J50001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS.
4. CAPACITANCE IS EXPRESSED AS NOTED.
5. L54004 INDUCTANCE IS CREATED BY 0.4" LEAD ON C50003.
6. L54005 INDUCTANCE IS CREATED BY 0.4" LEAD ON C54010.
7. NOT USED.
8. MIXERS ARE INSTALLED AT MECH ASSY LEVEL.

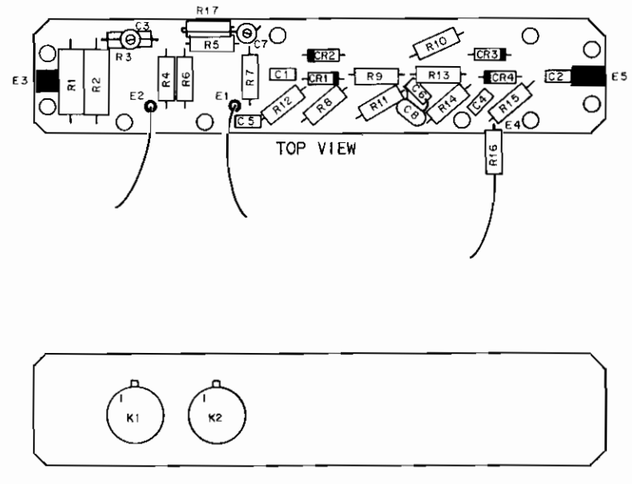
Figure 5-24 Option 2: Tracking Generator with 0/75 dB Attenuator (Sheet 1 of 3) (D-0000-5311-000-L)



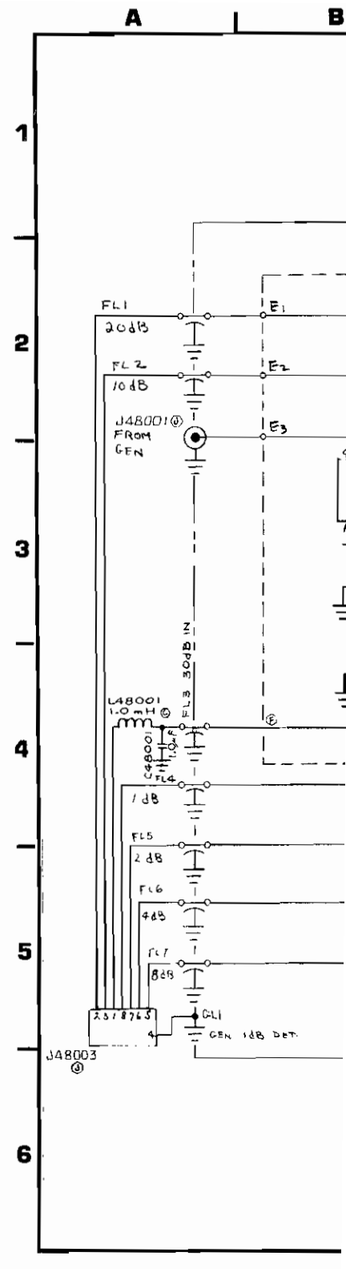
0-75 dB ATTENUATOR ASSY

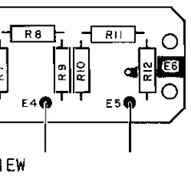


0-15 dB ATTENUATOR PC BOARD

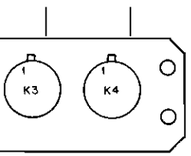


0-60 dB ATTENUATOR PC BOARD



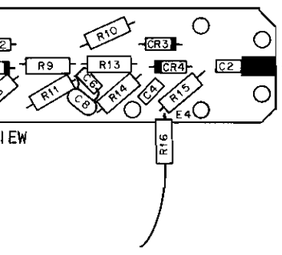


IEW



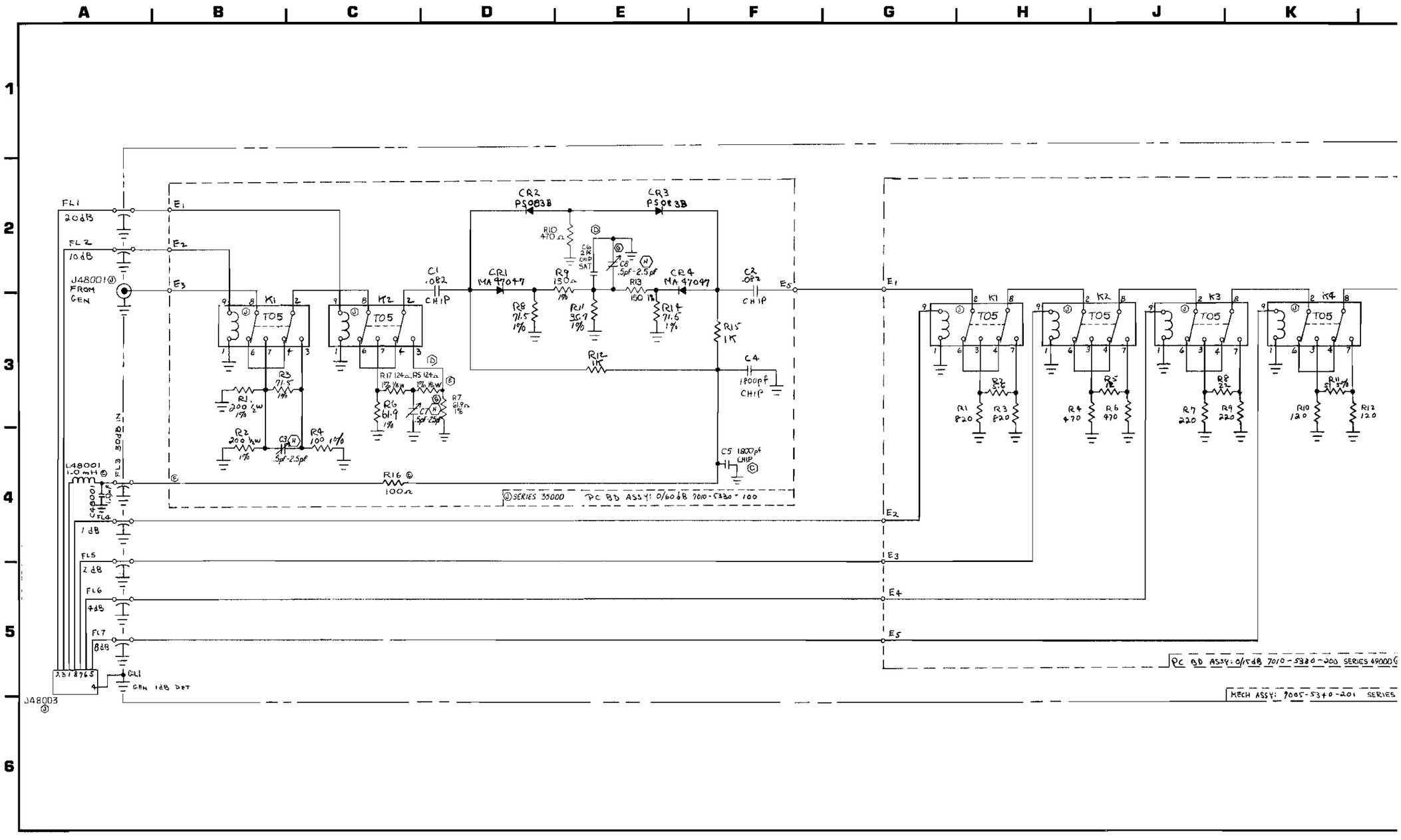
VIEW

ATOR PC BOARD

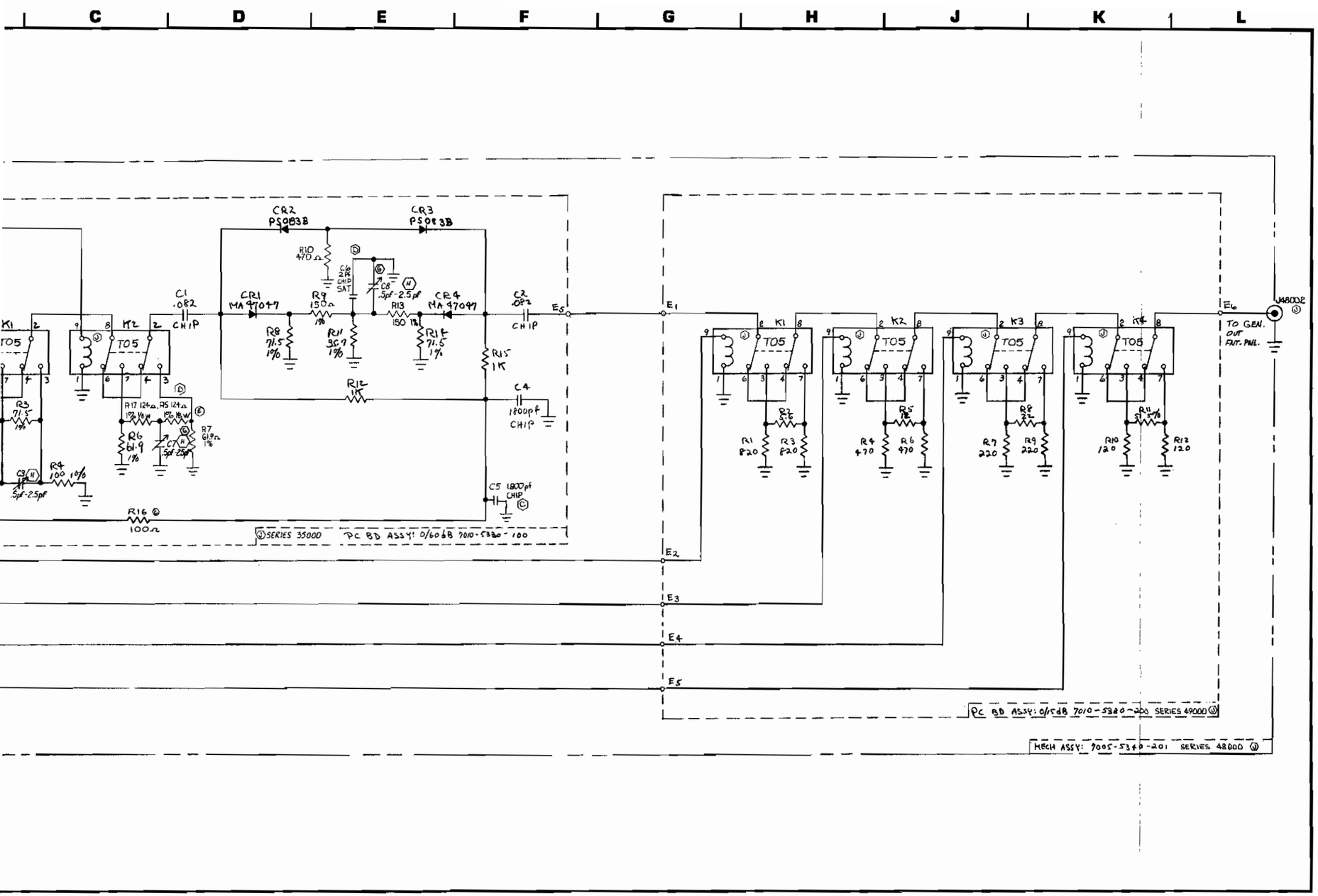


VIEW

ATOR PC BOARD



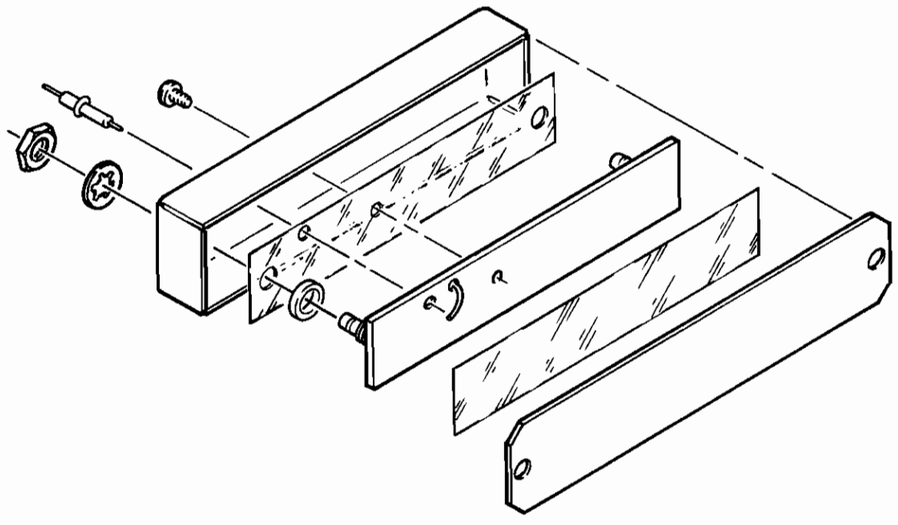
Figur



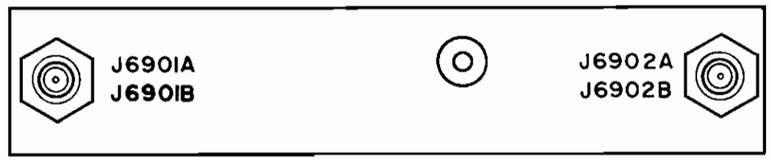
NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:
   - A. 0/60 dB PC BD IS 35000 (E.G., R1 IS R35001).
   - B. 0/15 dB PC BD IS 49000 (E.G., R1 IS R49001).
   - C. MECH ASSY IS 48000 (E.G., L1 IS L48001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS.
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).

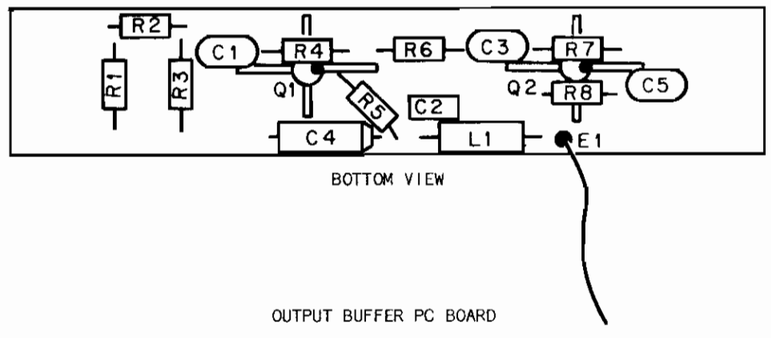
Figure 5-24 Option 2: Tracking Generator with 0/75 dB Attenuator (Sheet 2 of 3) (D-0000-5310-201-J)



OUTPUT BUFFER ASSY

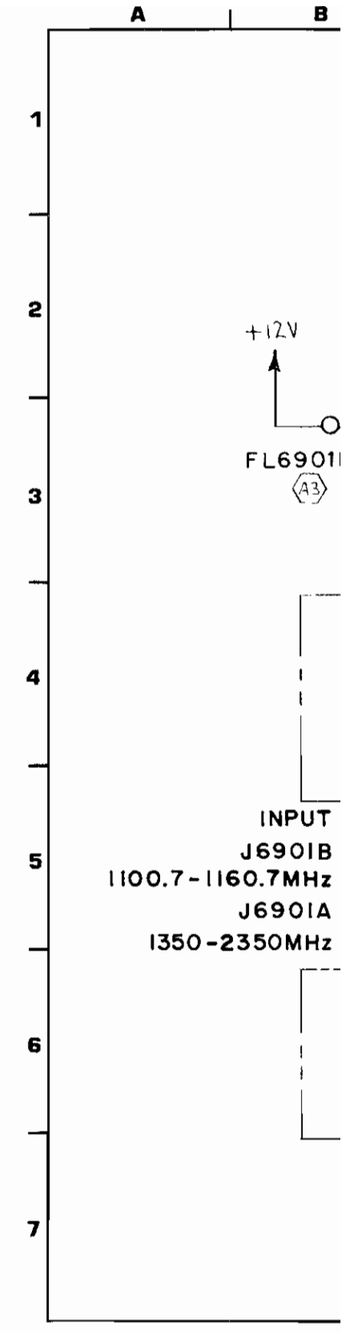


TOP VIEW

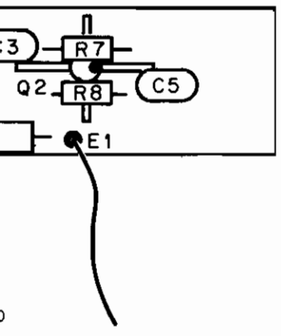


BOTTOM VIEW

OUTPUT BUFFER PC BOARD



J6902A
J6902B



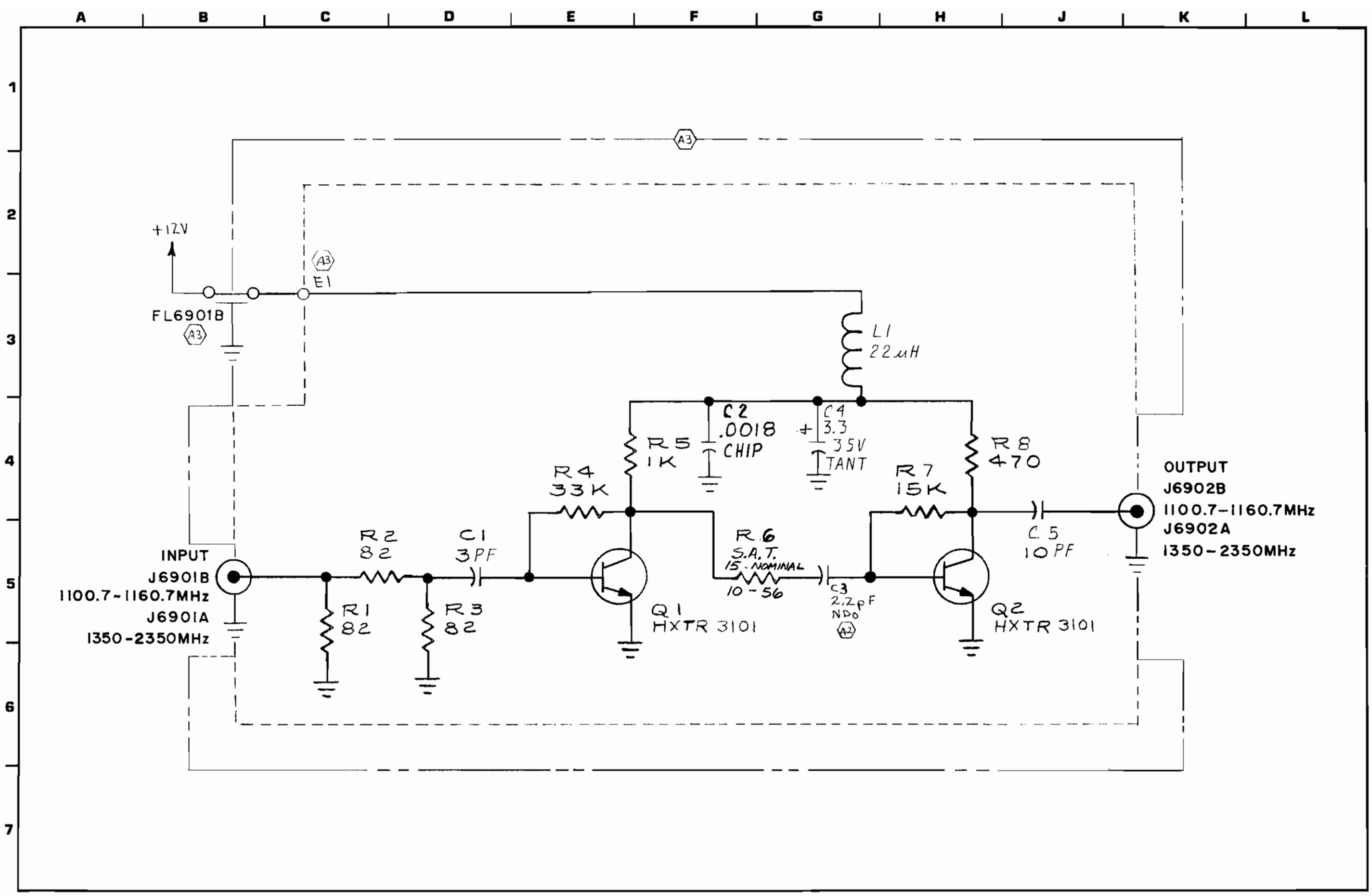
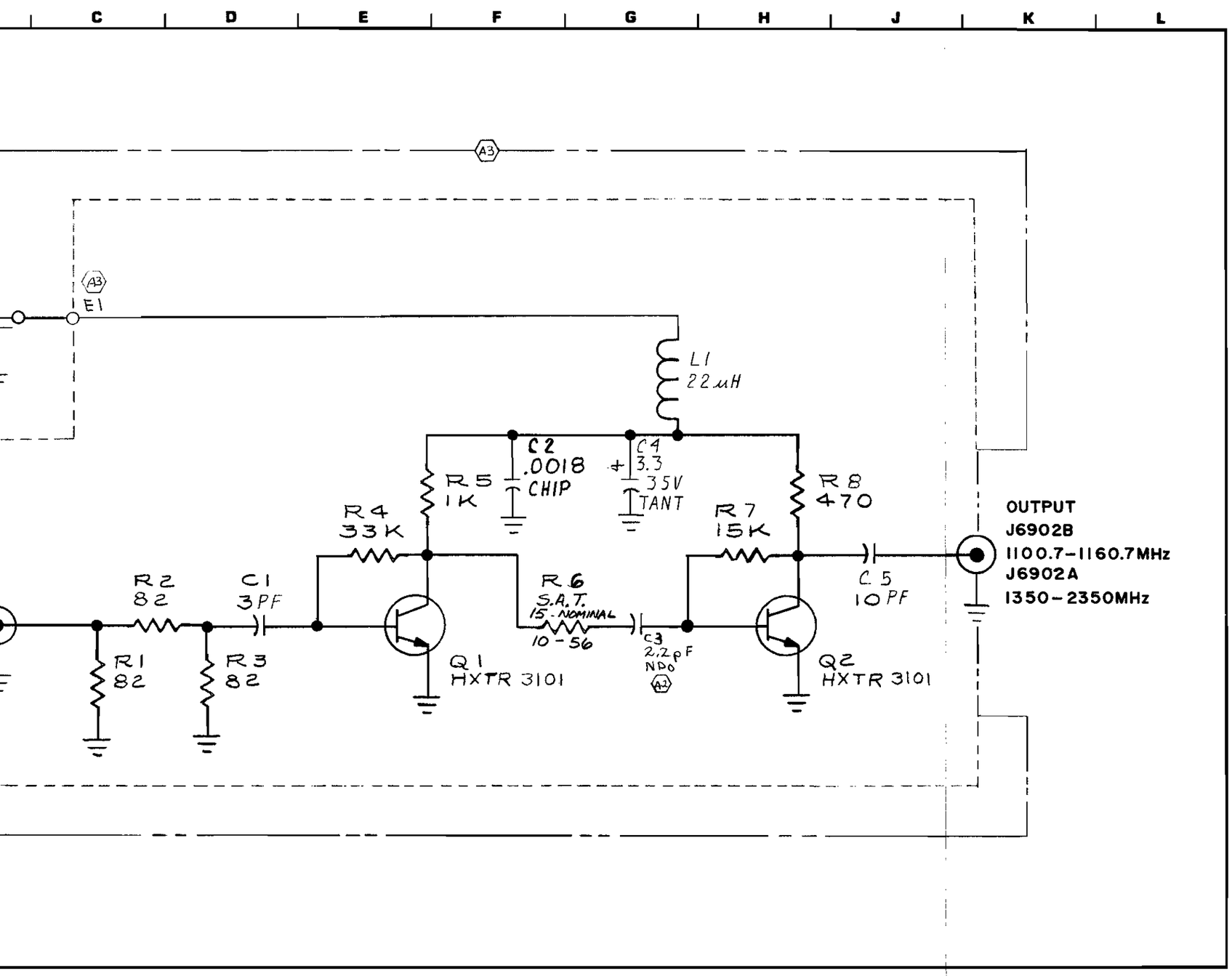


Figure 5-2



NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. OSC PC BD IS 6800 (E.G., R1 IS R6801).

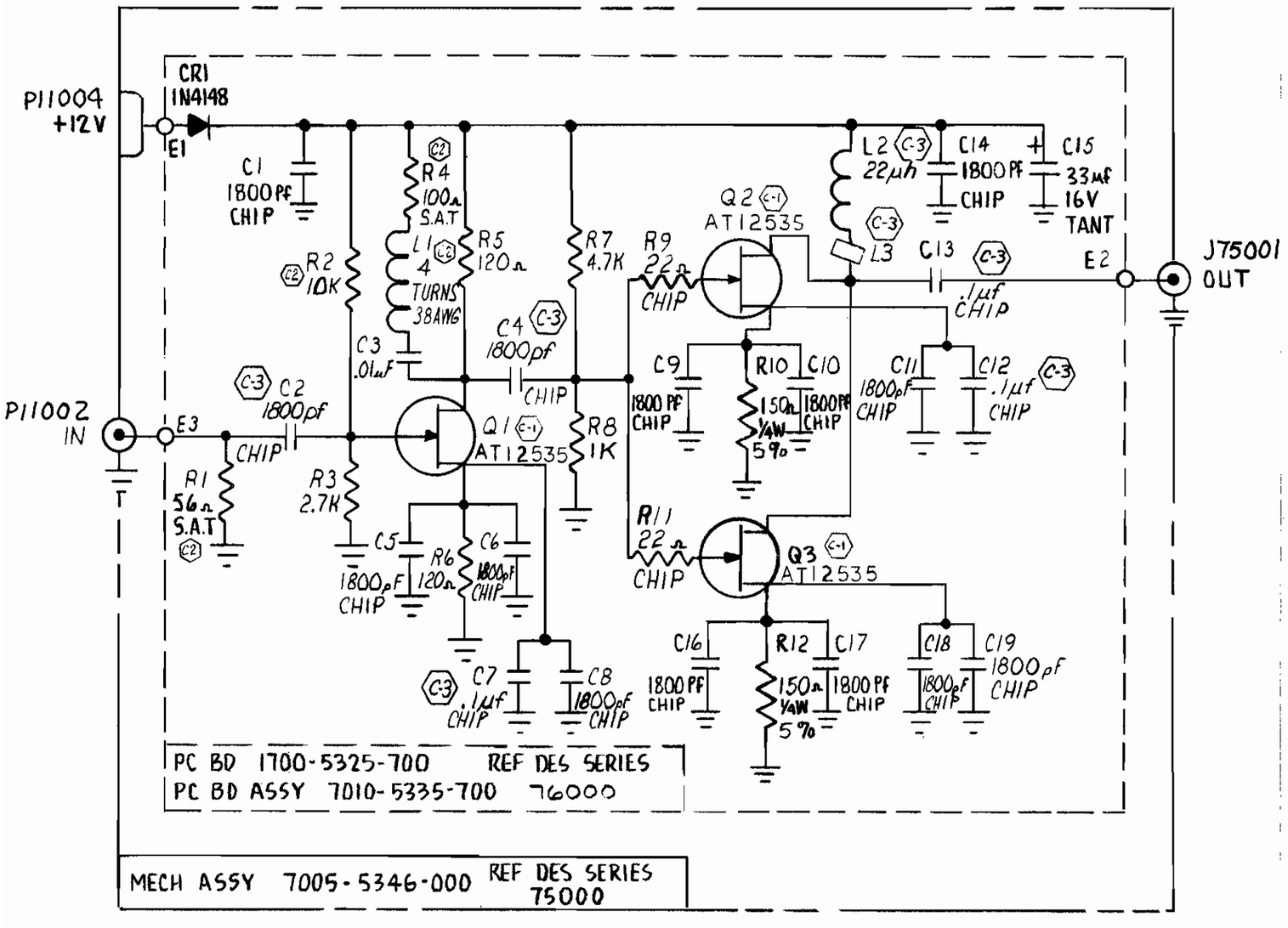
   B. MECH ASSY IS 6900B (E.G., FL1 IS FL6901B).

2. RESISTORS ARE 1/8 W, 10% TOLERANCE (UNLESS NOTED).

3. RESISTANCE IS EXPRESSED IN OHMS.

4. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS NOTED).

Figure 5-24 Option 2: Tracking Generator with 0/75 dB Attenuator (Sheet 3 of 3) (D-0000-5016-800-A3)



NOTES:

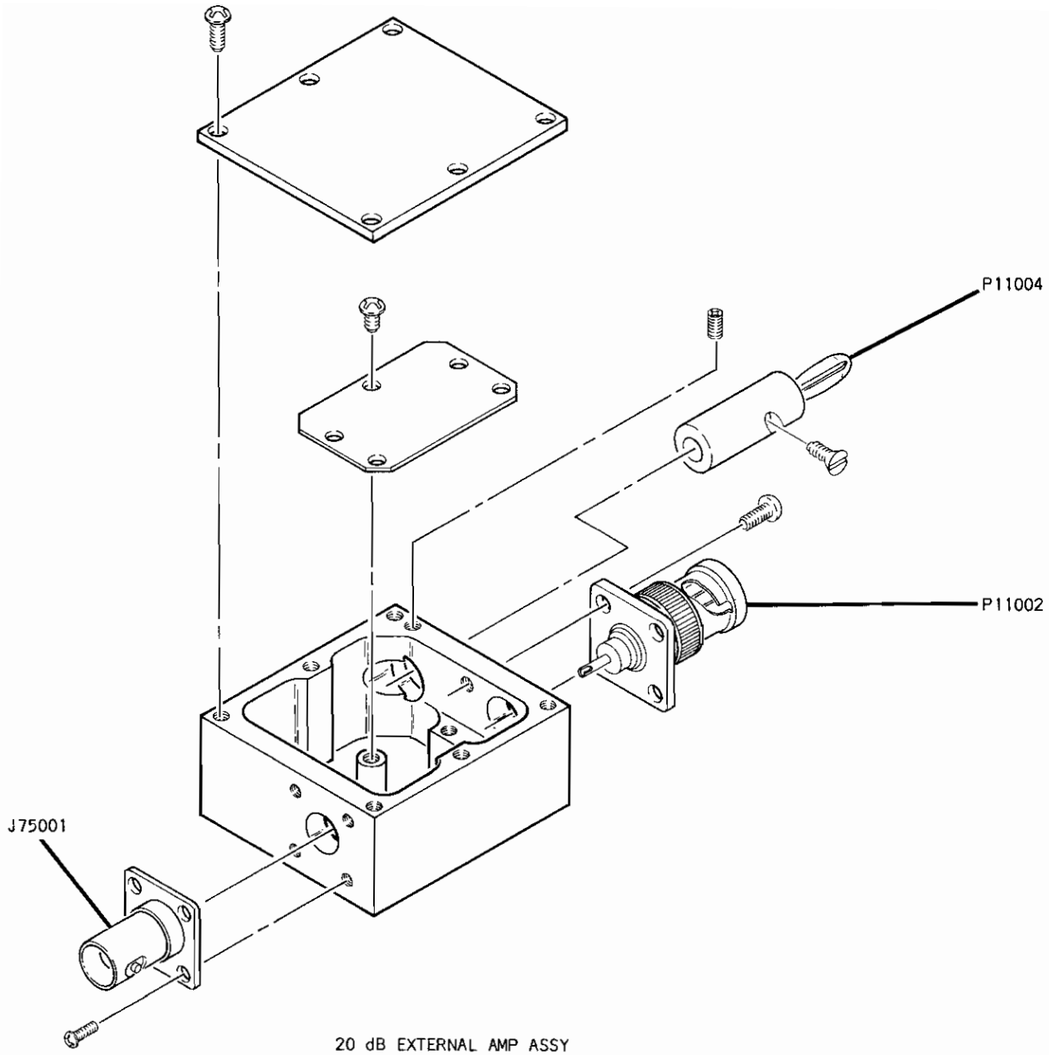
1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. 20 dB PC BD IS 76000 (E.G., R1 IS R76001).

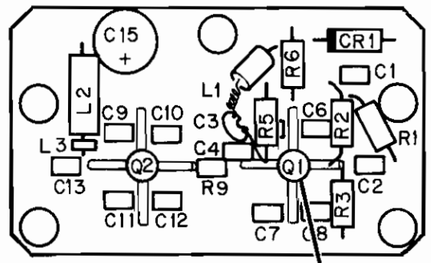
   B. MECH ASSY IS 75000 (E.G., J1 IS J75001).

2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).

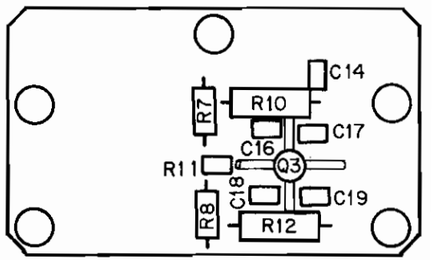
Figure 5-25 Option 3: 20 dB External Amplifier (B-0000-5315-700-C4)



20 dB EXTERNAL AMP ASSY



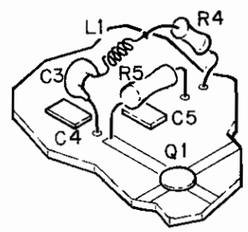
TOP VIEW



BOTTOM VIEW

A

20 dB PC BOARD



DETAIL **A**

NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

   A. PC BD IS REF DES SERIES 58000 (E.G, R1 IS R58001).

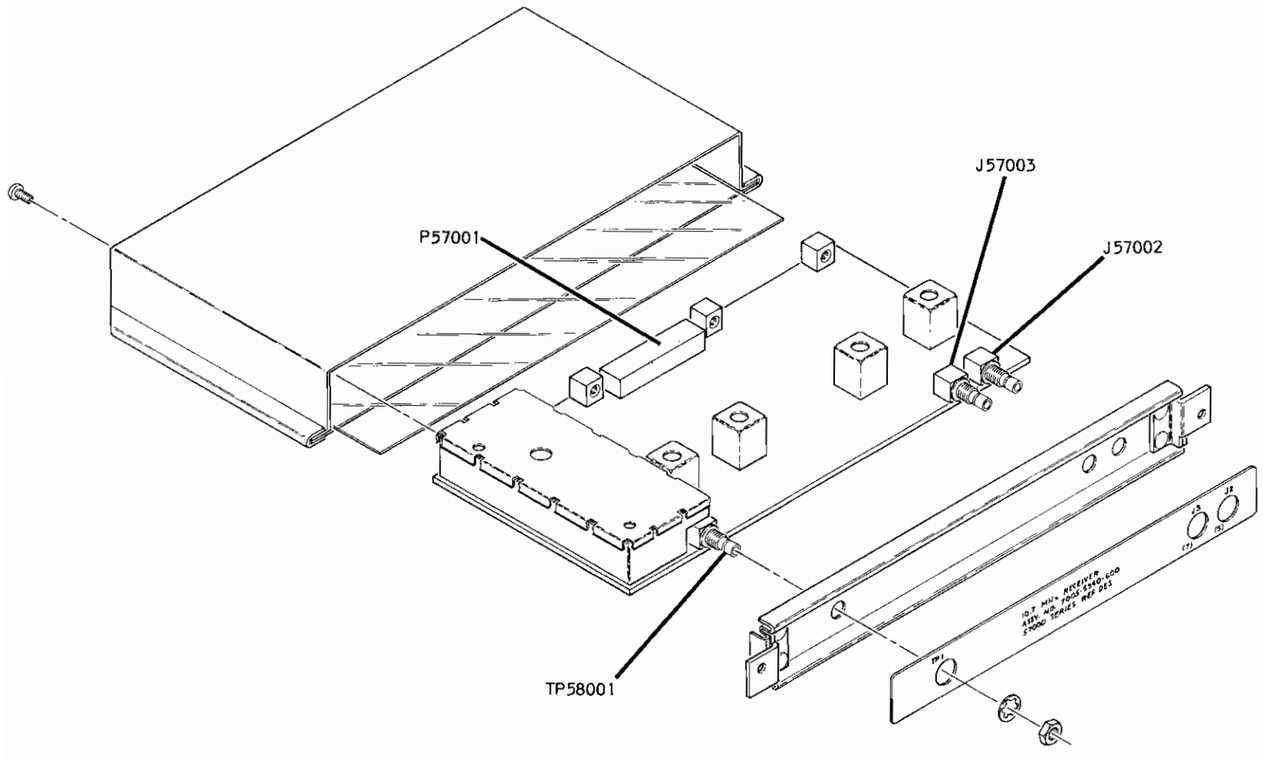
   B. MECH ASSY IS SERIES 57000 (E.G., J1 IS J57001).

2. RESISTORS ARE 1/8 W, 5% TOLERANCE (UNLESS NOTED).

3. RESISTANCE IS EXPRESSED IN OHMS.

4. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS NOTED).

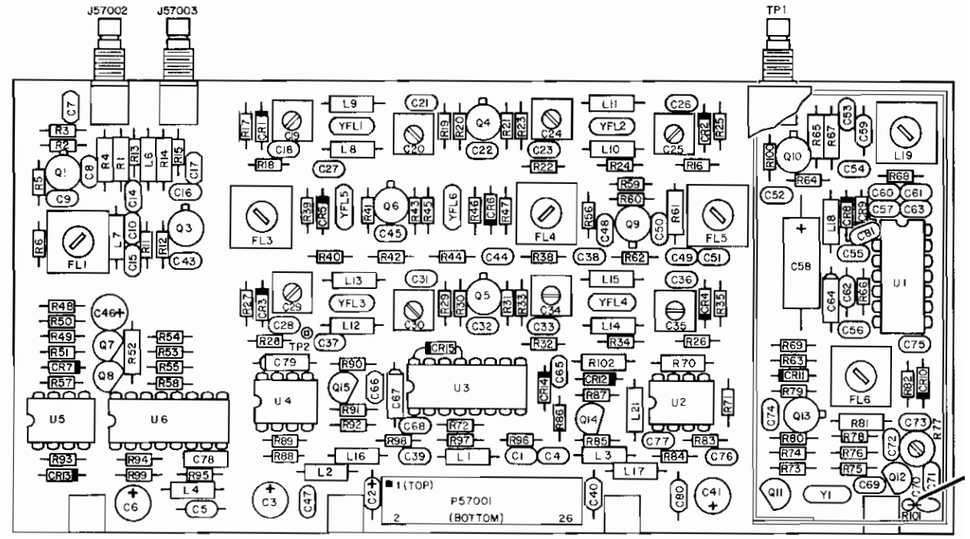
Figure 5-26 Option 4: 10.7 MHz Receiver (D-0000-5310-600-E)



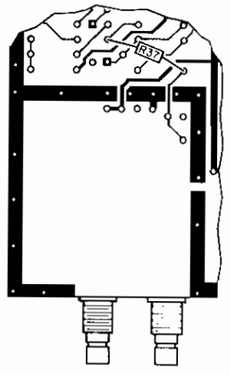
10.7 MHz RECEIVER ASSY



DETAIL **A**

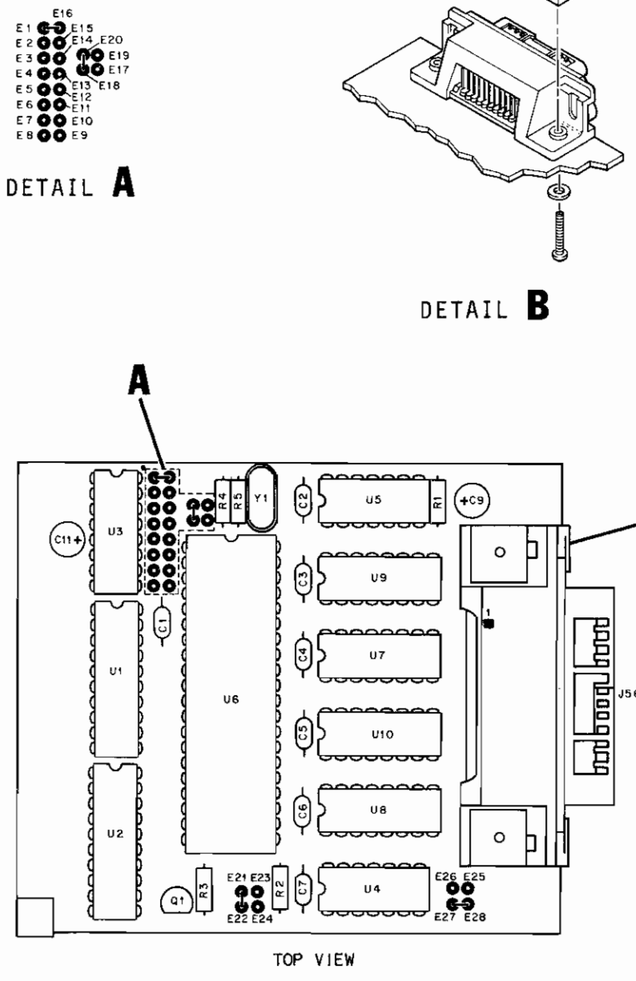


TOP VIEW



BOTTOM VIEW

10.7 MHz RECEIVER PC BOARD



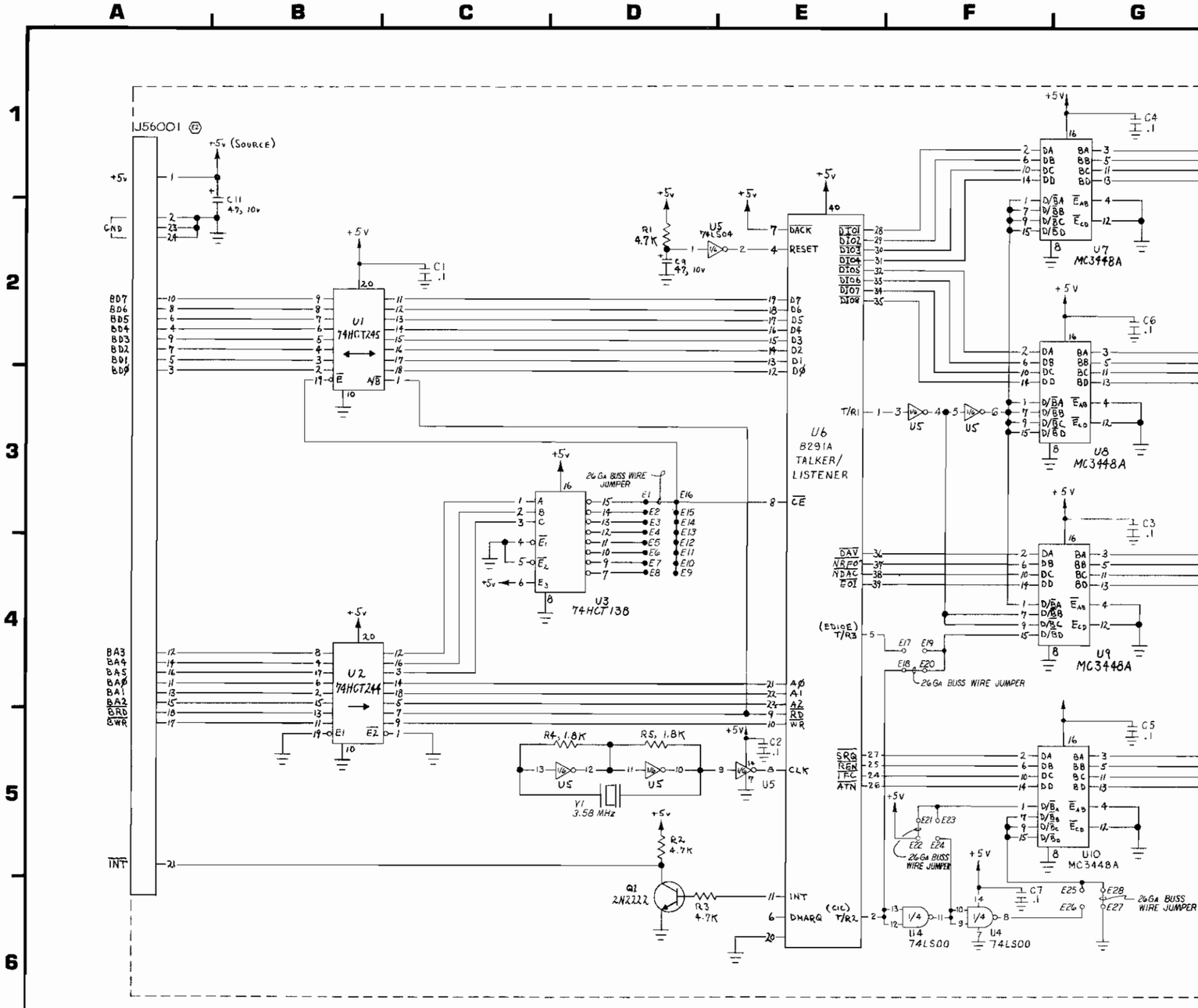
DETAIL **A**

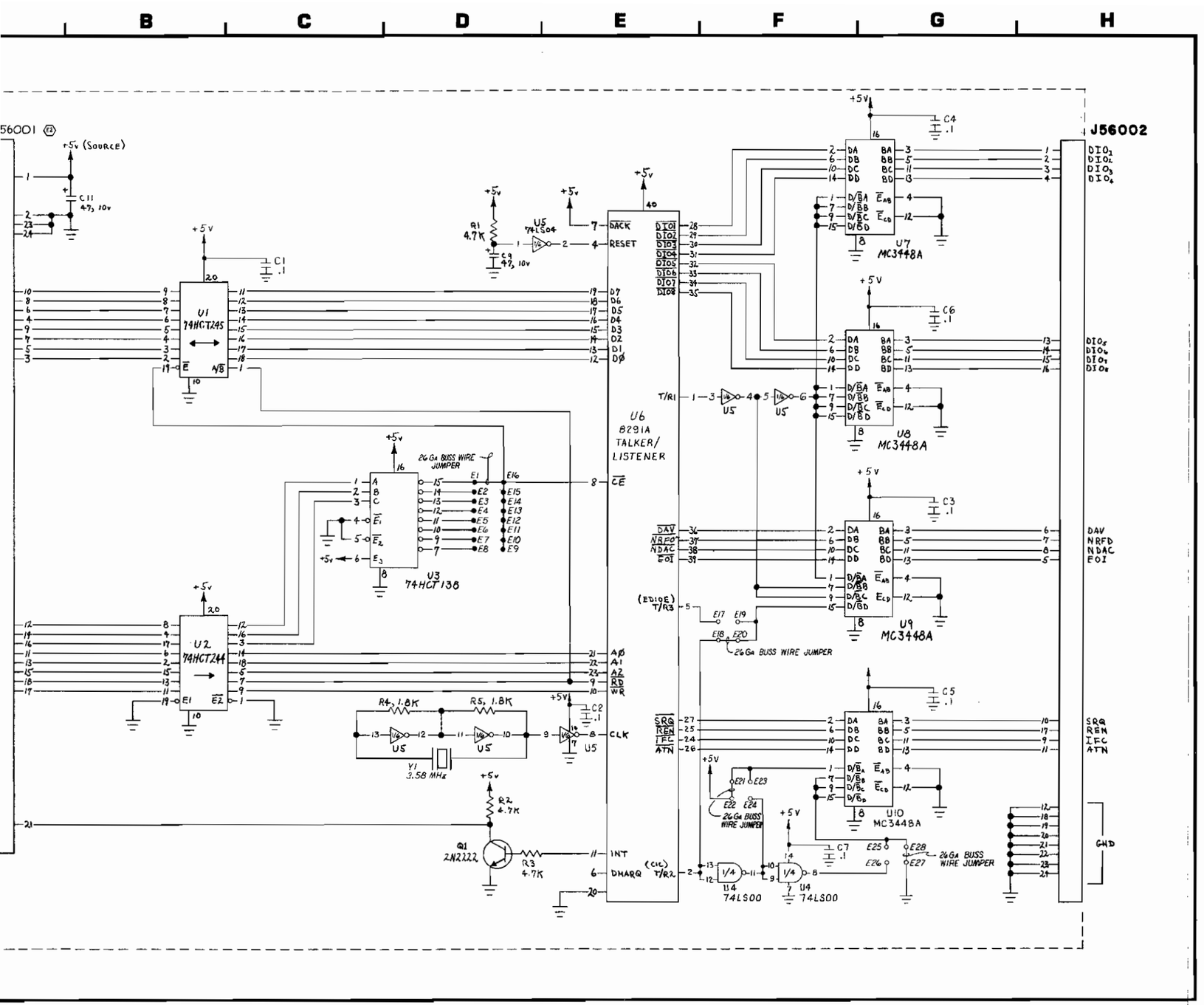
DETAIL **B**

M VIEW

TOP VIEW

GPIB INTERFACE PC BOARD





NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES THE FOLLOWING:

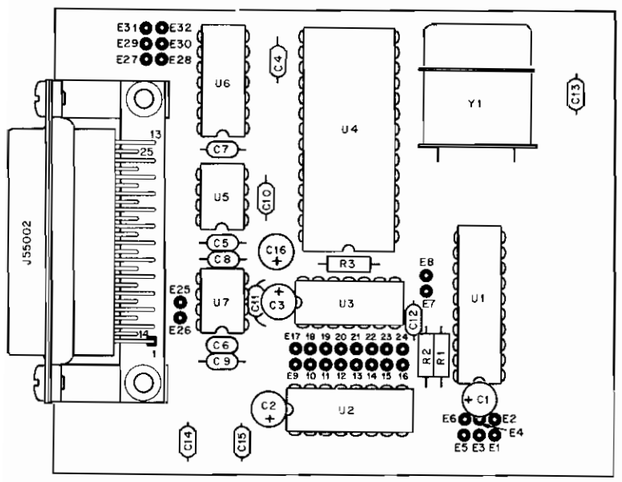
   A. PC BD SERIES IS 56000 (E.G., R1 IS R56001).

2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).

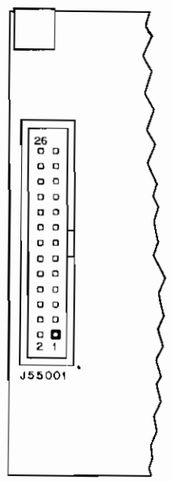
3. RESISTANCE IS EXPRESSED IN OHMS.

4. CAPACITANCE IS EXPRESSED IN MICROFARADS (UNLESS NOTED).

Figure 5-27 Option 5: GPIB PC Board (D-0000-5312-700-E2)

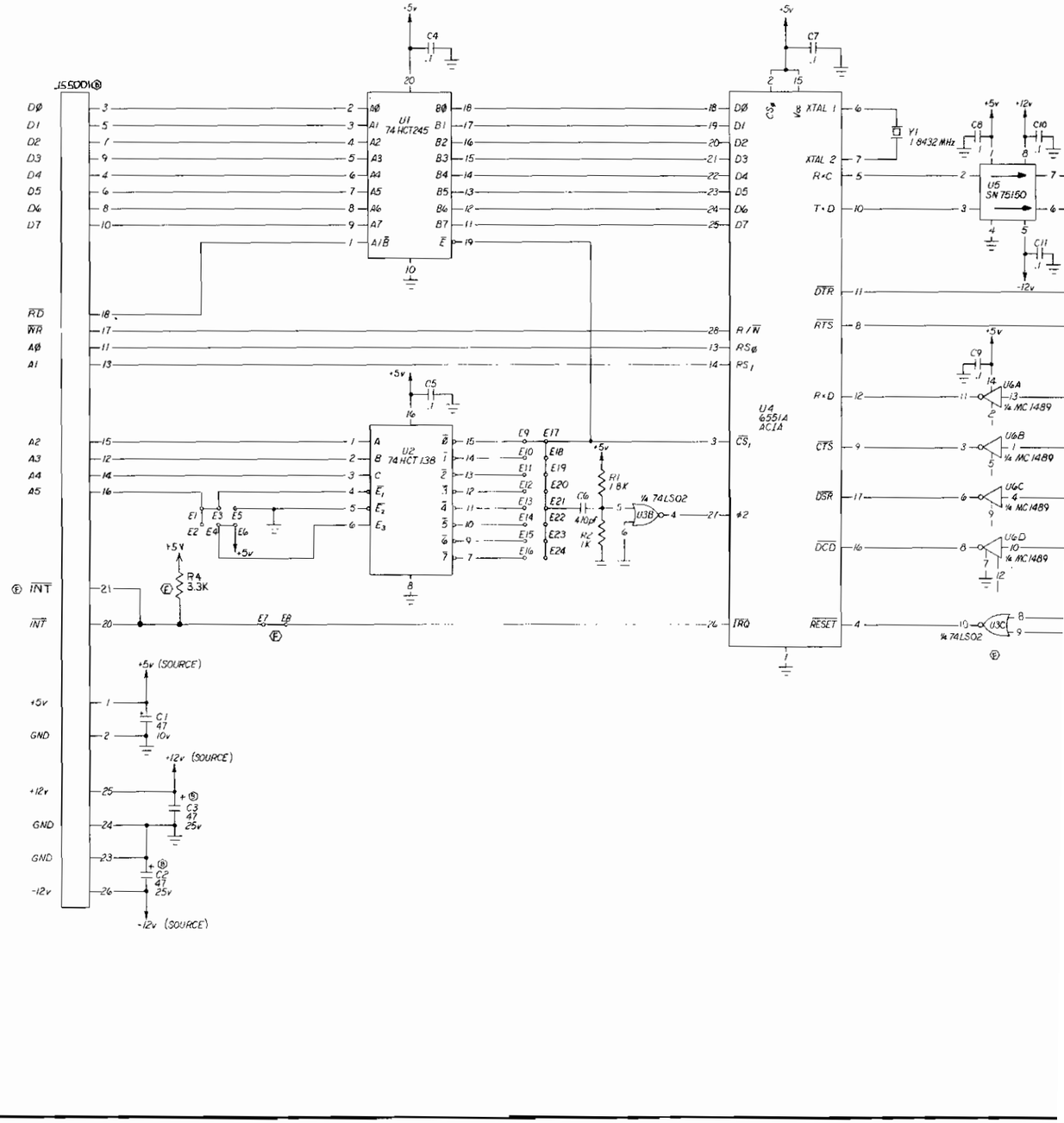


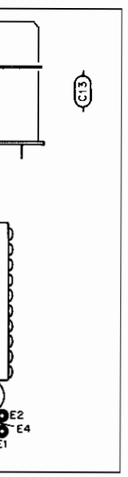
TOP VIEW



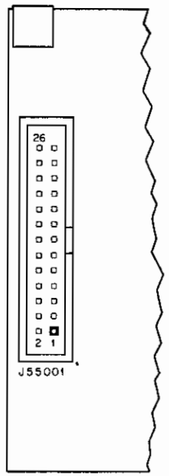
BOTTOM VIEW

RS232 INTERFACE PC BOARD

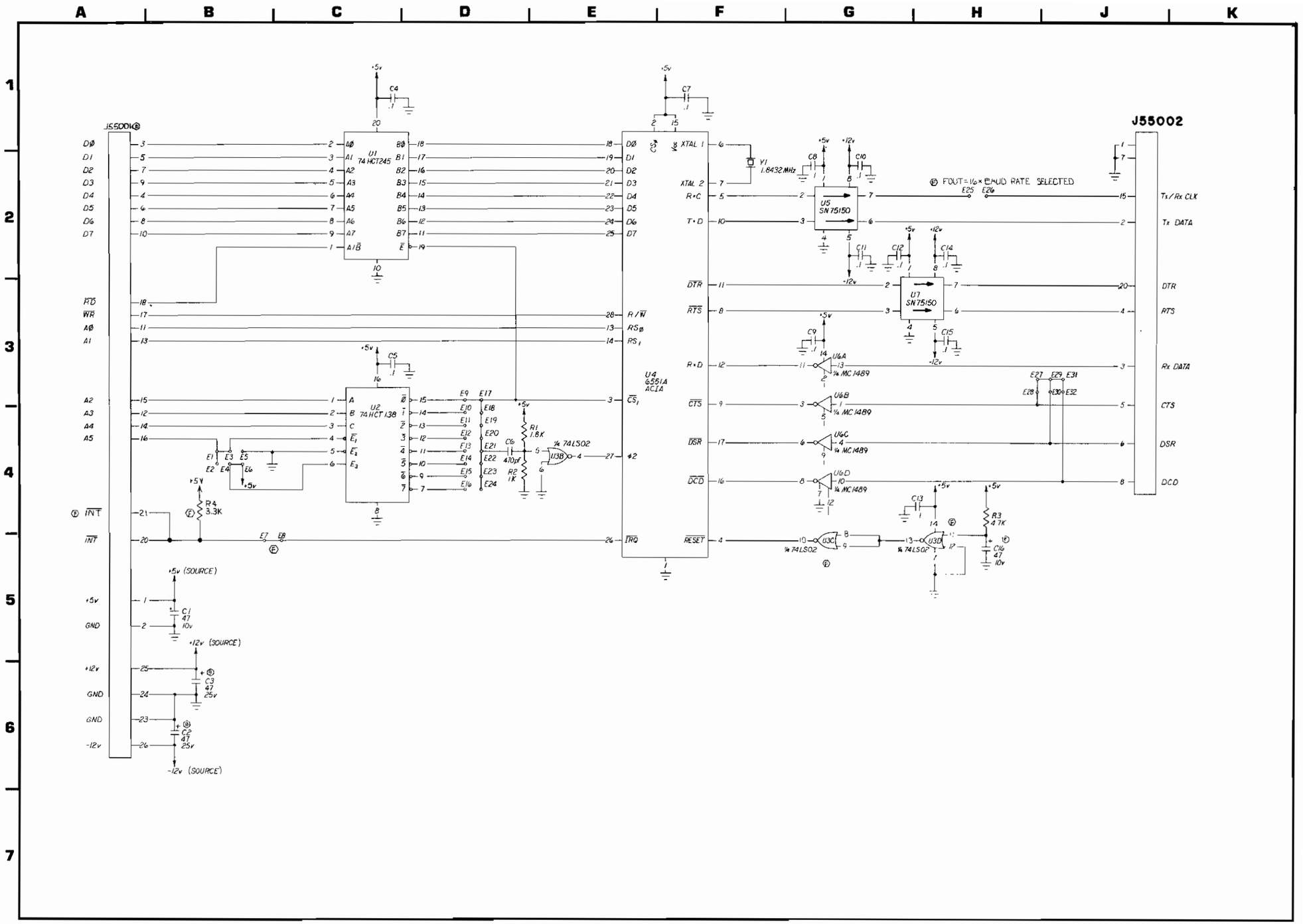


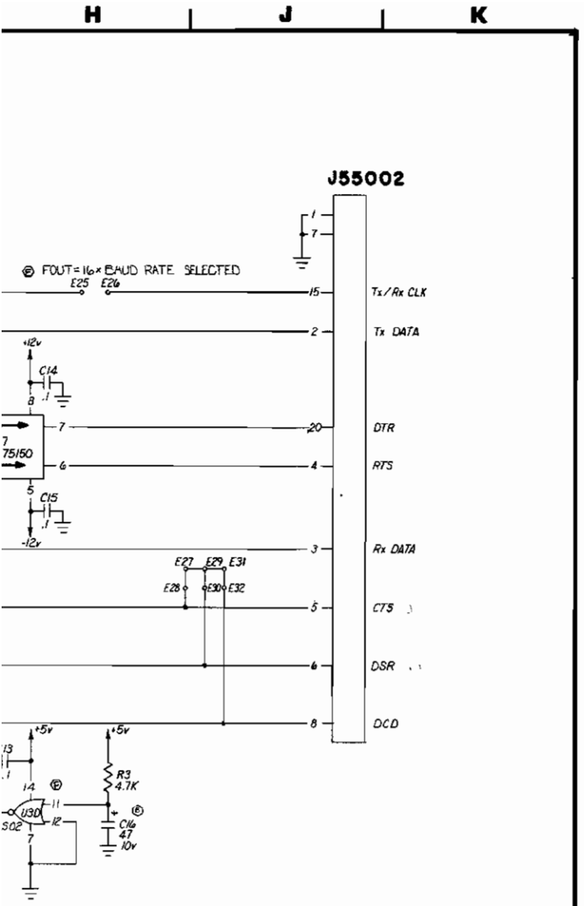


PC BOARD



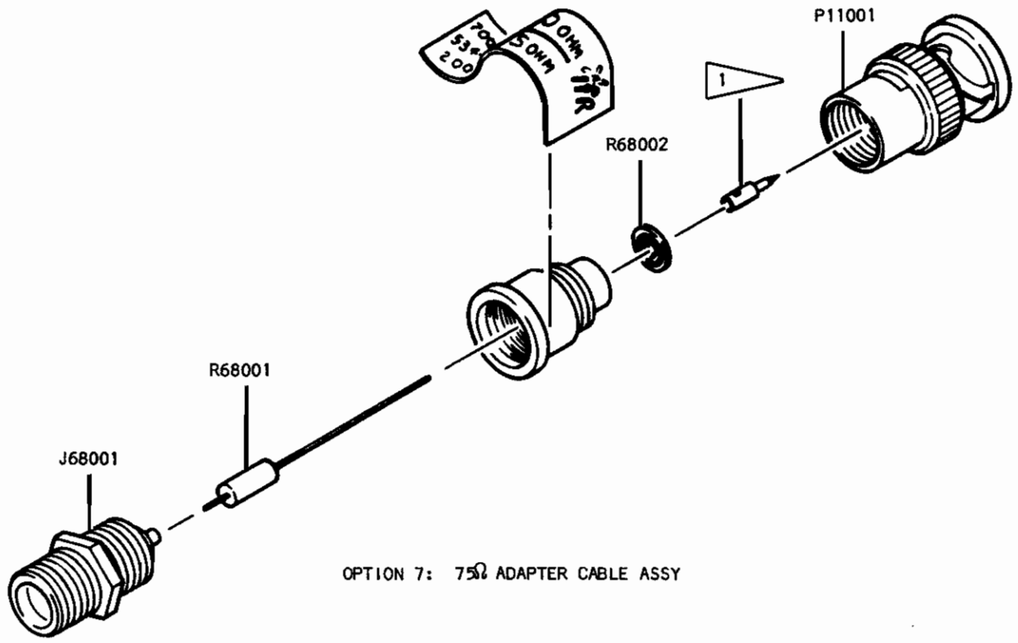
BOTTOM VIEW





NOTES:

1. ALL REF NOS ARE ASSIGNED TO A DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 55000 (E.G., R1 IS R55001).
2. RESISTORS ARE 1/4 W, 5% TOLERANCE (UNLESS NOTED).
3. RESISTANCE IS EXPRESSED IN OHMS.
4. CAPACITANCE IS IN MICROFARADS (UNLESS NOTED).



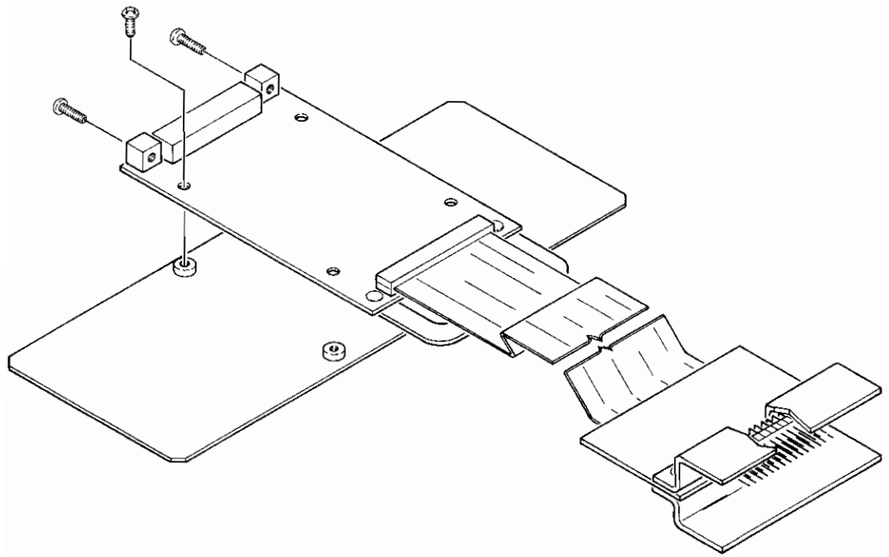
OPTION 7: 75Ω ADAPTER CABLE ASSY

NOTES:

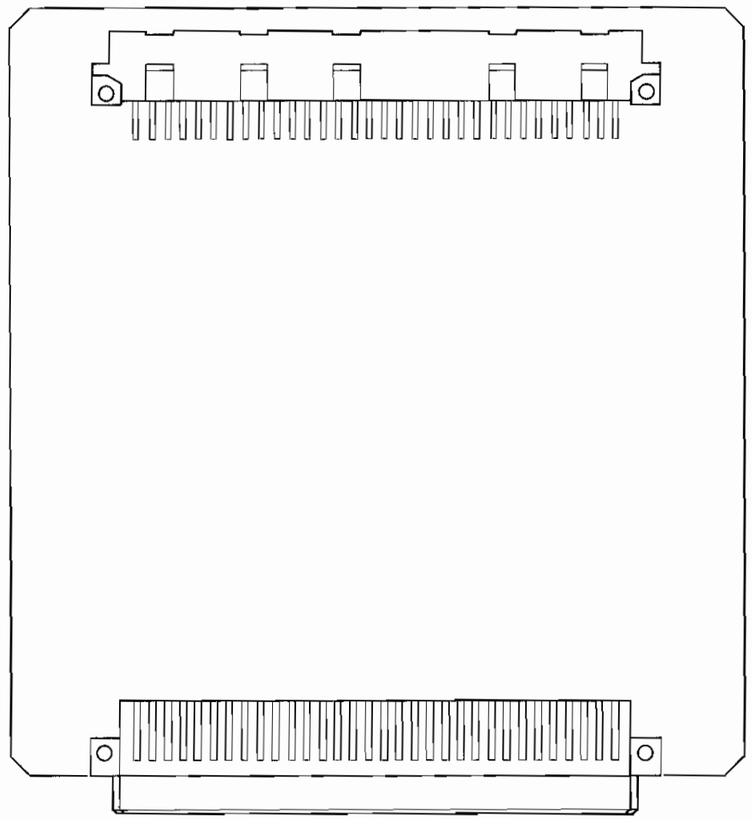
1. SUPPLIED WITH P11001.

Figure 5-28 Options 6 & 7: RS-232 PC Board and 0-75Ω Adapter (D-0000-5312-500-F)

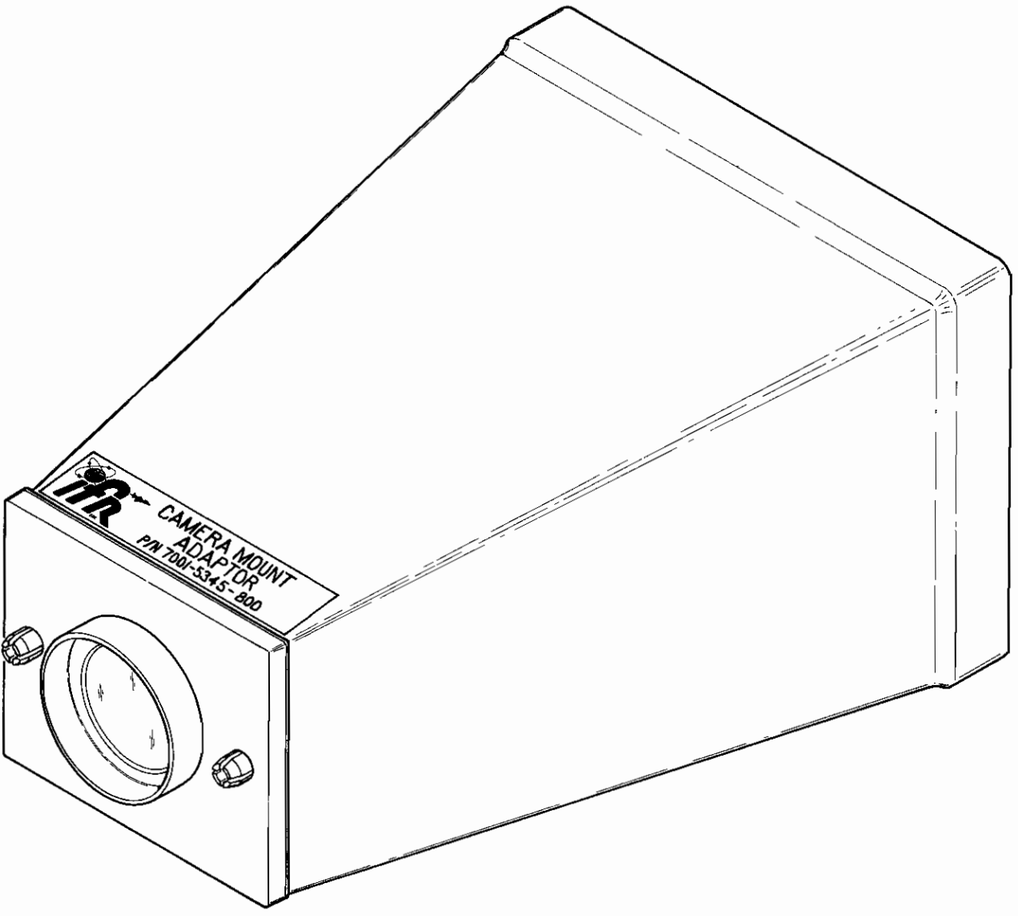
Figure 5-29 Option 8: Quasi-Peak Filter
(To be Supplied at a Later Date)



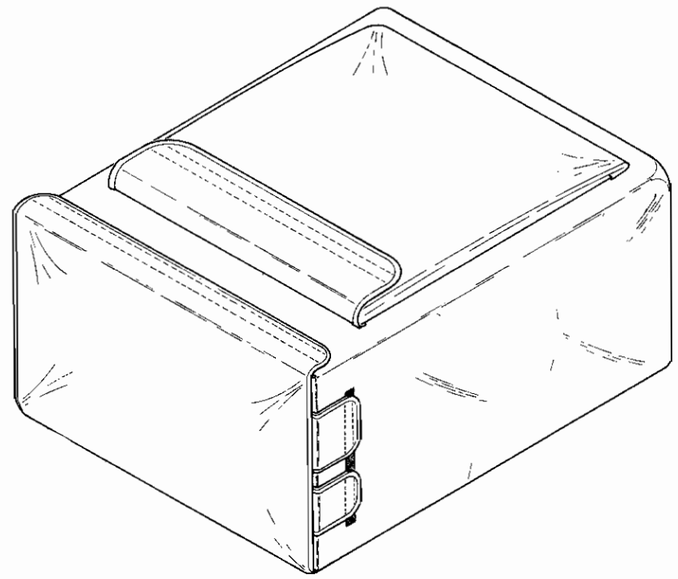
OPTION 9(a): RF EXTENDER PC BOARD



OPTION 9(b): DIGITAL EXTENDER PC BOARD



OPTION 10: CAMERA MOUNT



OPTION 11: CARRYING CASE ASSY

Figure 5-30 Options 9, 10 and 11: Extender Boards, Camera Mount and Carrying Case

APPENDICES

APPENDIX A - A-7550 PERFORMANCE SPECIFICATIONS

A-1 FREQUENCY

Frequency Range:	100 kHz to 1 GHz in 100 Hz steps.
Frequency Display Span:	1 kHz/DIV to 100 MHz/DIV in 1-2-5 sequence. In "0", the analyzer is a fixed-tuned receiver.
Frequency Display Linearity:	Frequency error between any two points on the display is less than ±5% of the indicated frequency separation.
Digital Frequency Readout:	Indicates center frequency at the frequency display span.
Accuracy:	Calibrator acccuracy, and ±3% of frequency display span selected.
Resolution:	
Bandwidth Ranges (at 3 dB):	300 Hz, 3 kHz, 30 kHz, 300 kHz and 3 MHz.
Accuracy:	±30% of bandwidth selected.
Filter Shape Factor:	60 dB/3 dB ratio < 4.5:1.
Video Filter:	Post-detection filter used to average displayed noise. 30 kHz and 300 Hz bandwidths selectable.
Residual FM (typical):	<30 Hz RMS peak at scan/DIV settings below 200 kHz/DIV.
Noise Sidebands (typical):	>65 dB below peak cw signal at 5X resolution bandwidth setting from cw signal.

A-2 AMPLITUDE

Measurement Range:	-120 dBm to +30 dBm.
Displayed Dynamic Range:	70 dB in 10 dB/DIV log scale. 16 dB in 2 dB/DIV log scale. 8 divisions with linear amplitude scale.
Amplitude Scale Linearity:	10 dB/DIV log - ±0.15 dB/dB, but not more than ±2.5 dB over 70 dB dynamic range. 2 dB/DIV log - ±0.4 dB/2 dB, but not more than ±1.5 dB over 16 dB dynamic range. Linear - demodulation linearity ±10%.
Amplitude Accuracy:	
Frequency Response:	±2 dB over 10 MHz to 1000 MHz range.
Amplitude Variation between Bandwidth:	±1 dB; except ±2 dB for 300 Hz.

A-3 INPUT

Impedance:	50Ω nominal, 75Ω optional.
Attenuator:	60 dB range in 10 dB steps.
Accuracy:	±0.5 dB/10 dB step.
Maximum Input Levels:	4 volts DC or +30 dBm with maximum input attenuation. +20 dBm for all other conditions.

A-4 OUTPUT

Calibrator:	
Frequency:	100 MHz ±2500 Hz, crystal controlled.
Amplitude:	-30 dBm ±1 dBm.
Sweep Out:	0 to 5V ramp (nominal).
Video Out:	0 to 800 mV riding on DC level.

A-5 GENERAL CHARACTERISTICS

Dimensions:	33.3 cm (13.1") wide, 18.5 cm (7.3") high, 49.8 cm (19.6") deep.
Weight (approximate):	12.6 kg (28 lbs.) without options.
Temperature Range:	0° + 50° C.
Power Requirements:	
Line:	106 to 266 VAC, 50 to 400 Hz at 55 watts typical (no options).
External D.C.:	12 to 30 VDC nominal 4 Amps at 12V typical (no options). 2 Amps at 28V typical (no options).

A-6 TRACKING GENERATOR (OPTIONAL)

Frequency Range:	100 kHz to 1 GHz
Output Level:	0 dBm to -75 dBm in 1 dB steps
Flatness:	±2 dB
Residual FM:	<100 Hz RMS peak
Output Impedance:	50Ω nominal (75Ω optional)
Spurious	Harmonics 20 dBc or lower. Non-harmonics 40 dBc or lower.

A-7 10.7 MHz RECEIVER (OPTIONAL)

Range: 100 kHz to 1 GHz

Center Frequency Resolution: 100 Hz

Sensitivity: 2 µV typical

Selectivity: (at 3 dB)

Mode	Receiver Bandwidth
FM 2	200 kHz
FM 1	15 kHz
SSB	6 kHz
AM 1	6 kHz
AM 2	15 kHz

Adjacent Channel Rejection:

Receiver Bandwidth (at 3 dB)	40 dB DOWN AT
200 kHz	±300 kHz
15 kHz	±27 kHz
6 kHz	±12 kHz

A-8 QUASI-PEAK DETECTOR (OPTIONAL)

(To Be Supplied)

APPENDIX B - TEST EQUIPMENT REQUIREMENTS

B-1 GENERAL

This appendix contains a list of test equipment suitable for performing the maintenance procedures in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted for the recommended models. Note that the equipment listed in this appendix may exceed the minimum specification requirements for some of these procedures.

B-2 RECOMMENDED TEST EQUIPMENT

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Oscilloscope	Tektronix 465B	DC to 100 MHz 5 mV/div vertical trace 2 nS/div sweep rate Dual Trace
Spectrum Analyzer	Tektronix 7613 Frame Tektronix 7L13/U Spectrum Analyzer	Variable Persistence Storage Oscilloscope Frequency Range: 1 kHz to 2.5 GHz Resolution Bandwidth: 30 Hz to 3 MHz
Digital Multimeter	Fluke Model 8010A	3½ digit, ±0.1% basic DC accuracy
RF Power Meter with Power Detector	Boonton RF Microwattmeter Model 42 BD	Frequency Range: 200 kHz to 18 GHz Power Range: 1.0 nW to 10 mW Accuracy: ±0.25% fs ±0.15 dB >10 nW
	Boonton Power Sensor Model 41-4A	Frequency Range: 200 kHz to 7 GHz Power Range: 1 nW to 10 mW Accuracy: ±0.3 dB >10 nW
Power Supply	B&K 1601	Regulation: .1% or 1 mV Ripple: 5 mV Voltage Range: 0-50 VDC @ 0-2 A

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
Function Generator	Wavetek 182A	Frequency Range: .004 Hz to 4 MHz Functions: Sine, Triangle & Square High Level Output: 20 Vp-p (10 Vp-p into 50Ω)
RF Signal Generator	Hewlett Packard 8640B	Frequency Range: 1 to 1000 MHz Resolution: 0.1 to 100 Hz Accuracy: 2×10^{-6} RF Output: +20 to -130 dBm
Modulation Meter	Boonton Model 82AD	Frequency Range: 10 MHz to 1.2 GHz Accuracy: FM: ±2% of reading from 30 Hz to 100 kHz Accuracy: AM: ±2% of reading from 10 Hz to 90% AM and 5% of reading below 10% and above 90%; from 30 Hz to 100 kHz Resolution: 0.1% of full scale for FM and AM
Electronic Counter Wattmeter	Hewlett-Packard Model 5315A Sierra 174A-1	Frequency Range: 0 to 100 MHz Sensitivity: 10 mV RMS Frequency Range: 25 to 1000 MHz VSWR: 25-512 MHz: 1.10 max 512-1000 MHz: 1.20 max Accuracy Indent Power: 25-512 MHz: ±5% of full scale 512-1000 MHz: ±7% of full scale

TYPE	MANUFACTURER & MODEL	SPECIFICATIONS
1 dB Step Attenuator	Weinshet Model 9621	Frequency: 20-80 MHz, 1.0-1.2 GHz Impedance: 50Ω Accuracy: 1 dB ±.14 dB
10 dB Step Attenuator	Weinshet Model 9682-1	Attenuation Range: 0-127 dB Accuracy: ±.25 dB or 1.25% from .5 MHz to 1 GHz whichever is greater
Power Supply	LAMBDA LK-351-FM	Regulation: .015% or 1 mV Ripple: 500 µV Voltage Range: 0-36 VDC @ 25.0 A
Distortion Analyzer	Sound Technology Model 1700B	Frequency Range: 10 Hz to 110 kHz Accuracy: .002% distortion AC Voltage Accuracy: 2%

APPENDIX C - PREVENTIVE MAINTENANCE RECOMMENDATIONS

Preventive maintenance on A-7550 test sets primarily consists of cleaning and visual inspection of components. External cleaning of the test set is recommended as often as necessary. Internal cleaning should be performed on a more limited basis, preferably when the set is in a disassembled state for routine calibration, troubleshooting or repair. Test set disassembly for the sole purpose of internal cleaning is not recommended.

C-1 EXTERNAL CLEANING

1. Clean front panel and case with a soft lint-free cloth moistened with rubbing alcohol.

2. To remove tar or oil from outside case, safety solvent may be used.

CAUTION

DO NOT ALLOW SAFETY SOLVENT TO CONTACT FRONT PANEL CONTROL AREA. SOLVENT CAN CAUSE DAMAGE TO FRONT PANEL CONTROLS, MARKINGS ETC.

C-2 INTERNAL CLEANING AND INSPECTION

NOTE

The following procedures require removing the case from test set.

CAUTION

DELIBERATELY MOVING (HOWEVER SLIGHT) DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

DO NOT OPEN INTERNAL MODULES FOR SOLE PURPOSE OF CLEANING.

1. Remove dust with hand-controlled dry air jet of 15 psi (1.054 kg/cm^2) and wipe internal chassis parts and frame with soft lint-free cloth moistened with alcohol.

1. (Continued)

WARNING

DO NOT USE COMPRESSED AIR IN EXCESS OF 15 PSI. USE EXTREME CARE WHEN USING COMPRESSED AIR IN THE VICINITY OF CRT, IN ORDER TO MINIMIZE POSSIBILITY OF CRT IMPLOSION. OBSERVE FOLLOWING PRECAUTIONS:

a. MANUALLY REMOVE ANY LARGE DIRT/DUST PARTICLES CRT, AS OPPOSED TO USING COMPRESSED AIR.

b. DO NOT USE COMPRESSED AIR IN A DIRTY, CLUTTERED ENVIRONMENT. REMOVE ANY DEBRIS OR SMALL OBJECTS IN THE IMMEDIATE WORK AREA THAT MAY BECOME AIRBORNE DUE TO PRESSURIZED AIRFLOW.

c. IF POSSIBLE, USE AN AIR HOSE NOZZLE EQUIPPED WITH A SPRING LOADED ON/OFF VALVE, AS OPPOSED TO ONE THAT REMAINS OPEN OR CLOSED CONTINUOUSLY.

d. MAKE SURE COMPRESSED AIR HOSE IS FILTERED, TO PREVENT POSSIBLE OIL OR WATER DROPLETS FROM STRIKING CRT AT HIGH SPEEDS.

2. Inspect CHASSIS for:

a. Tightness of subassemblies and chassis mounted connectors.

b. Corrosion or damage to metal surfaces.

3. Inspect CAPACITORS for:

a. Loose mounting, deformities or obvious physical damage.

b. Leakage or corrosion around leads.

4. Inspect CONNECTORS for:

a. Loose or broken parts, cracked insulation and bad contacts. (DO NOT disassemble connectors needlessly within test set.)

5. Inspect POTENTIOMETER CONTROLS for:

a. Free rotation. If rotation feels rough, check control with an ohmmeter.

6. Inspect readily accessible PRINTED CIRCUIT BOARDS for:

a. Corrosion or damage to connectors.

6. (Continued)

   b. Damage to all mounted components including crystals and I.C.'s.

   c. Accumulation of dirt, dust or other foreign material.

7. Inspect RESISTORS for:

   a. Cracked, broken, charred or blistered bodies.

   b. Loose or corroded solder connections.

8. Inspect SEMICONDUCTORS for:

   a. Cracked, broken, charred or discolored bodies.

   b. Seals around leads being in place and in good condition.

9. Inspect TOGGLE SWITCHES for:

   a. Loose levers or terminals and switch body contact to frame.

   b. Bent or loose line switch contacts.

10. Inspect TRANSFORMER for:

    a. Signs of excessive heating.

    b. Broken or charred insulation and loose mounting hardware.

11. Inspect WIRING for:

    a. Broken or loose ends and connections.

    b. Proper dress relative to other chassis parts.

NOTE

All laced wiring should be tight with ends securely tied.

APPENDIX D - SPECIAL ACCESSORY TEST EQUIPMENT

D-1 GENERAL

This appendix contains recommendations for constructing special equipment necessary for performing certain test procedures in this manual.

D-2 BATTERY LOAD SIMULATOR

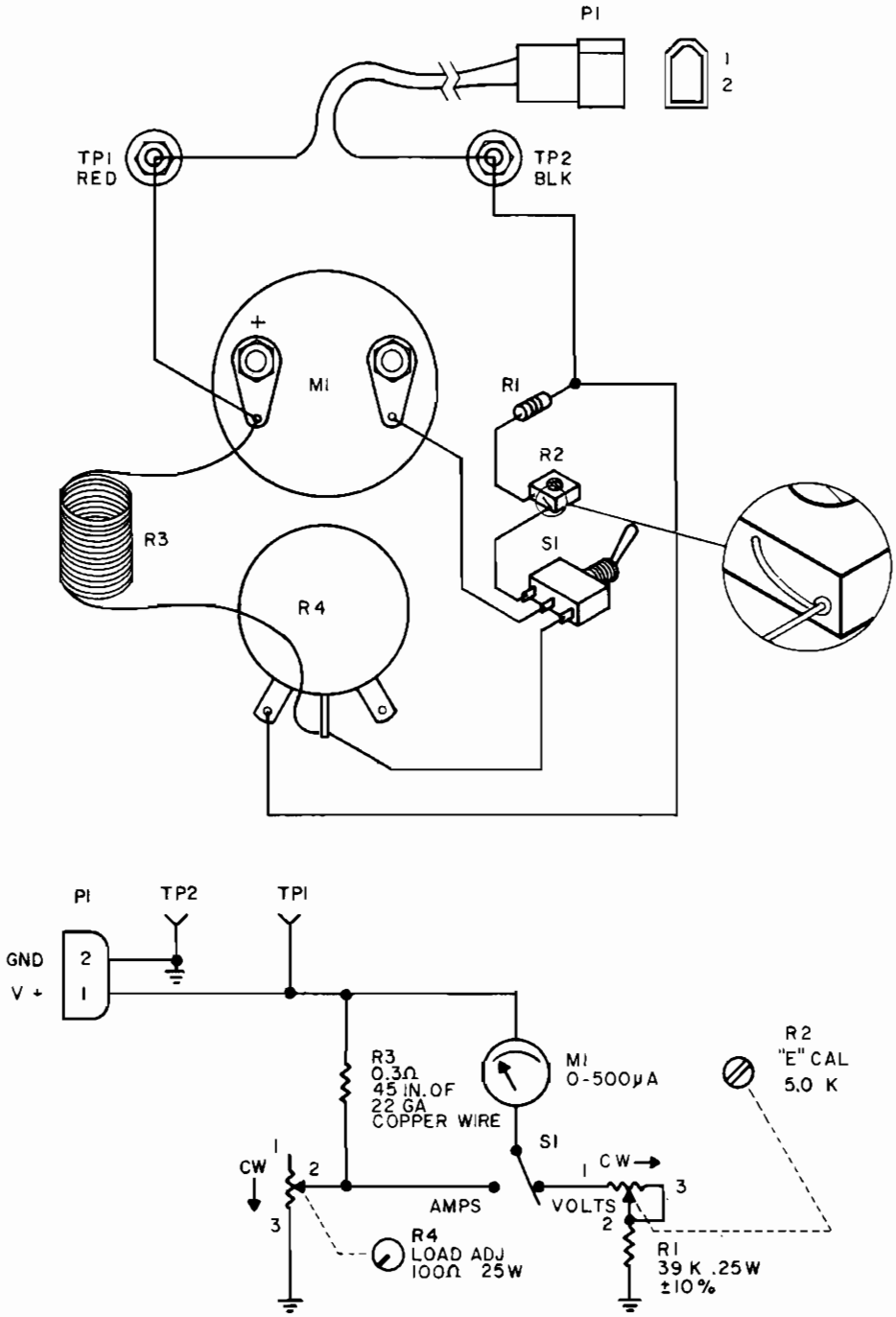
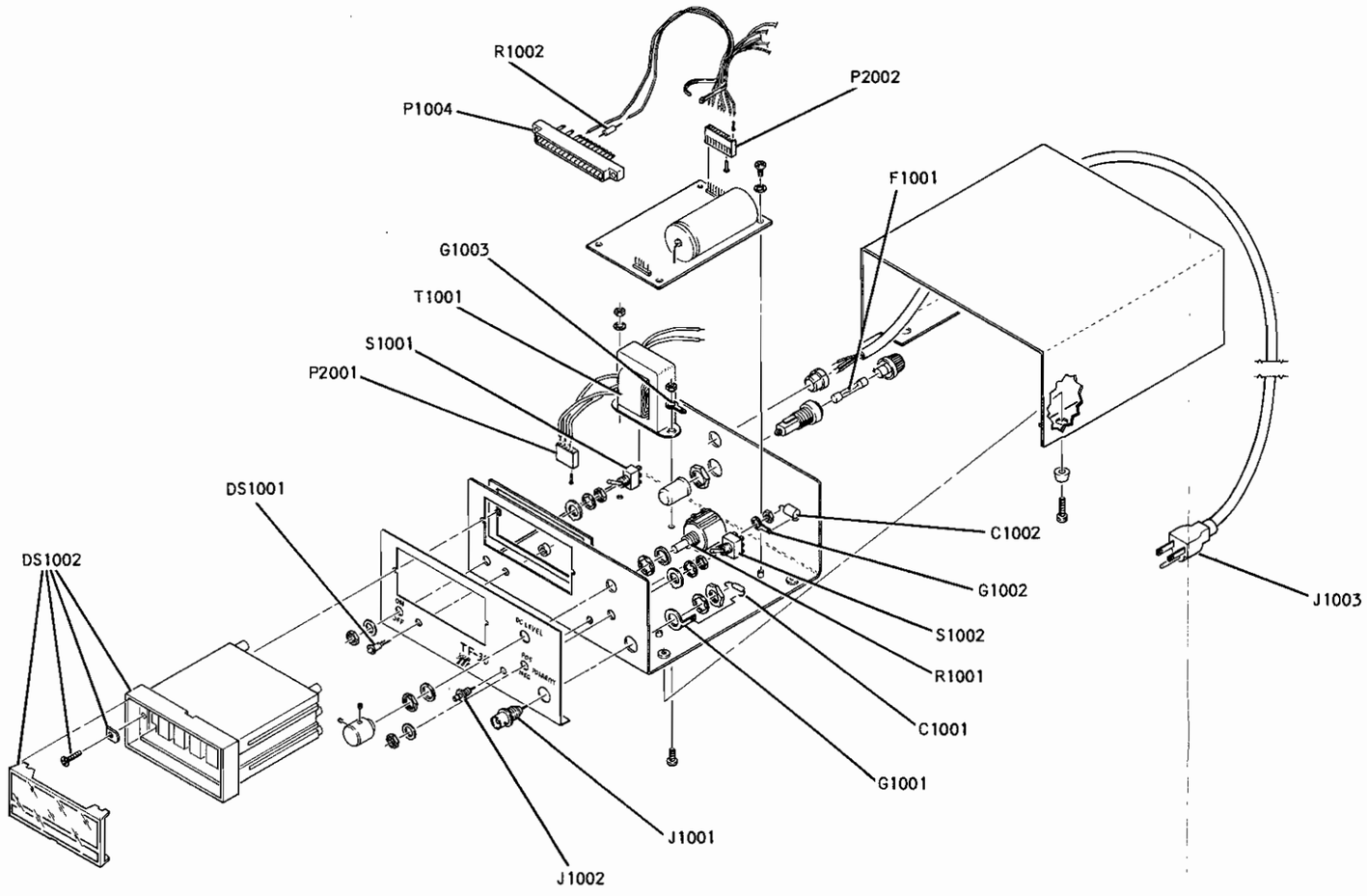


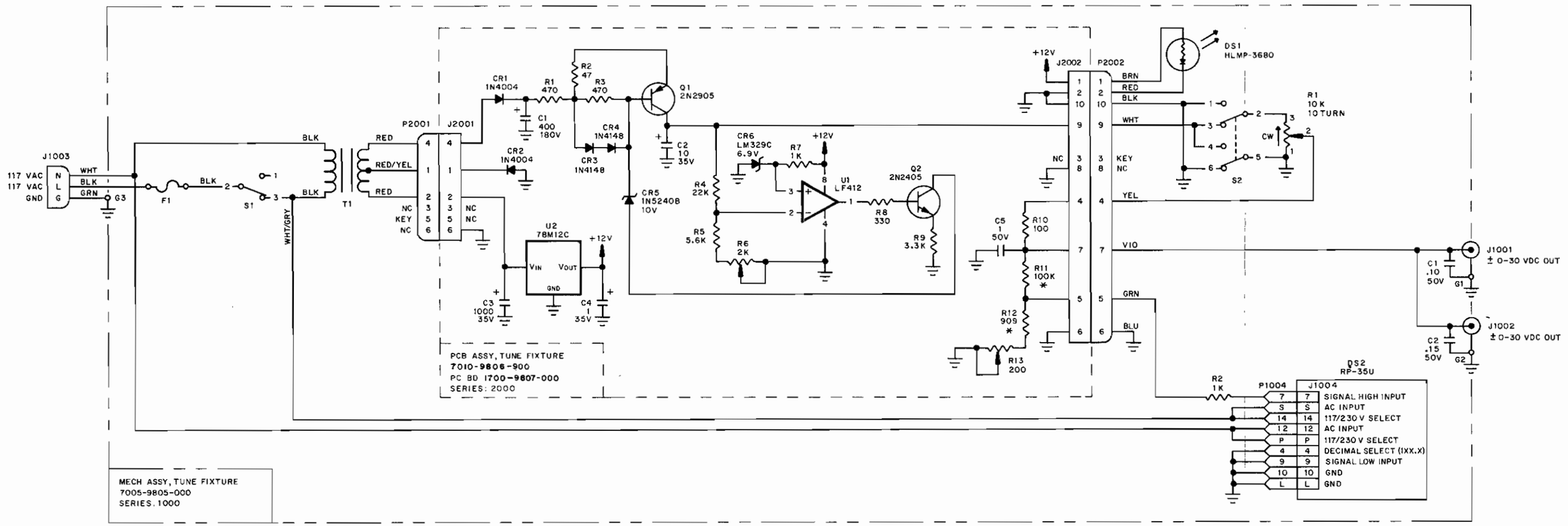
Figure D-1 Circuit Schematic and Diagram of Battery Load Simulator

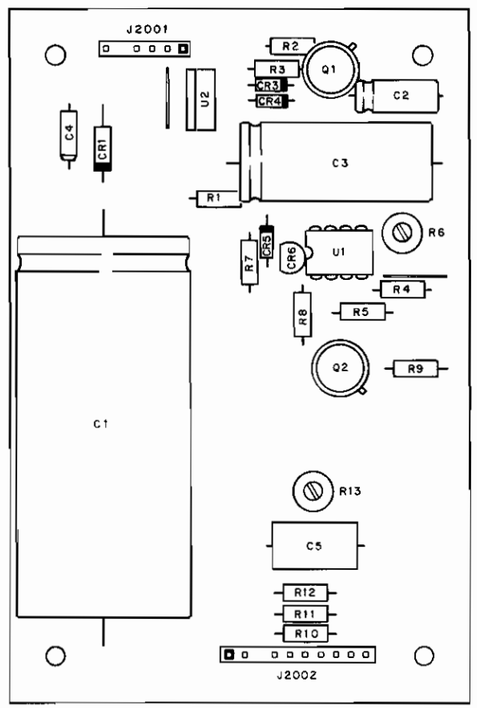
D-3 TF-30 TUNE FIXTURE



REF DES	DESCRIPTION	IFR PART NO.	QTY
	TUNE FIXTURE ASSEMBLY		
J1001	CONNECTOR, BNC	2113-0000-020	1
J1002	CONNECTOR, SMB	2123-0000-038	1
J1003	CABLE ASSY, AC POWER	6041-0000-001	1
P1004	CONNECTOR, CARD EDGE	2122-0000-018	1
P2001	CONNECTOR, WAFER	2115-0000-006	1
P2002	CONNECTOR, WAFER	2115-0000-013	1
C1001	CAPACITOR .10 µF, 50 V	1521-0000-008	1
C1002	CAPACITOR .15 µF, 50 V	1646-1540-098	1
DS1001	LED GRN	4950-0300-200	1
DS1002	DISPLAY, DIGITAL VOLTMETER	4600-0000-006	1
F1001	FUSE, FAST BLO 1 A, 250 V		1
G1001	LUG, GND 3/8"	2850-0000-025	1
G1002	LUG, GND 3/8"	2850-0000-041	1
G1003	LUG, GND #4 INT TOOTH	2850-0000-014	1
R1001	RESISTOR, VAR 10 K	4770-8810-300	1
R1002	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
S1001	SWITCH, TOGGLE	5114-0000-001	1
S1002	SWITCH, TOGGLE	5114-0000-004	1
T1001	TRANSFORMER	5604-0000-002	1
	TUNE FIXTURE, PC BD	7010-9806-900	1
J2001	CONNECTOR, WAFER	2115-1001-006	1
J2002	CONNECTOR, WAFER	2115-0000-016	1
C2001	CAPACITOR 400 µF, 180 V	1580-4010-800	1
C2002	CAPACITOR 10 µF, 35 V	1580-1000-350	1
C2003	CAPACITOR 1000 µF, 35 V	1580-1020-358	1
C2004	CAPACITOR 1 µF, 35 V	1507-0105-118	1
C2005	CAPACITOR 1 µF, 50 V	1502-0105-007	1
CR2001	DIODE, RECT IN4004	4815-0000-002	1
CR2002	DIODE, RECT IN4004	4815-0000-002	1
CR2003	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2004	DIODE, SIGNAL IN4148	4815-0000-003	1
CR2005	DIODE, ZENER 10 V	4818-0000-001	1
CR2006	DIODE, ZENER 6.9 V	4818-0000-015	1
Q2001	TRANSISTOR 2N2905	4801-0000-004	1
Q2002	TRANSISTOR 2M2405	4801-0000-002	1
R2001	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2002	RESISTOR 5%, 1/4 W, 47 OHM	4702-0470-003	1
R2003	RESISTOR 5%, 1/4 W, 470 OHM	4702-0471-003	1
R2004	RESISTOR 5%, 1/4 W, 22 K	4702-0223-003	1
R2005	RESISTOR 5%, 1/4 W, 5.6 K	4702-0562-003	1
R2006	RESISTOR, VAR 2 K	4752-0202-002	1
R2007	RESISTOR 5%, 1/4 W, 1 K	4702-0102-003	1
R2008	RESISTOR 5%, 1/4 W, 330 OHM	4702-0331-003	1
R2009	RESISTOR 5%, 1/4 W, 3.3 K	4702-0332-003	1
R2010	RESISTOR 5%, 1/4 W, 100 OHM	4702-0101-003	1
R2011	RESISTOR 1%, 1/4 W, 100.00 OHM	4706-1003-001	1
R2012	RESISTOR 1%, 1/4 W, 909.00 OHM	4706-9090-001	1
R2013	RESISTOR, VAR 200 OHM	4752-0201-002	1
U2001	IC, DUAL J-FET OP AMP LF412	3135-0000-054	1
U2002	IC, REGULATOR 78M12C	5750-0000-010	1
	WIRE, BUS 22 GA	1050-0000-073	

Figure D-2 TF-30 Tune Fixture Assembly (Sheet 1 of 2)





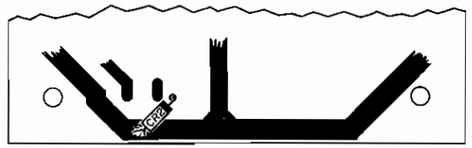


Figure D-2 TF-30 Tune Fixture Assembly (Sheet 2 of 2)

D-4 REMOVABLE 20 dB TEST POINT

FABRICATE 20 dB TEST POINT AS FOLLOWS:

1. SOLDER RESISTOR TO FIRST SMB CONNECTOR.

2. SOLDER RF SHIELD TO FIRST SMB CONNECTOR.

3. USING ACCESS HOLE, SOLDER RESISTOR TO SECOND SMB CONNECTOR.

4. SOLDER SECOND SMB CONNECTOR TO RF SHIELD.

5. SOLDER BUS WIRE TO FIRST SMB CONNECTOR.

6. TRIM BUS WIRE TO LENGTH REQUIRED TO CONTACT TEST POINT BEING ACCESSED.

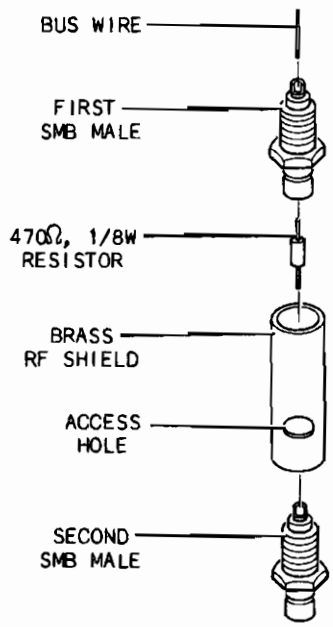


Figure D-3 20 dB Test Point

APPENDIX E - ABBREVIATIONS AND REFERENCE DESIGNATORS

E-1 TEXT ABBREVIATIONS

A	- Ampere (Amp)
AC	- Alternating Current
ADC (A/D)	- Analog-to-Digital Converter
AGC	- Automatc Gain Control
AM	- Amplitude
AMP	- Amplifier, Amplitude, Ampere
A/N	- Alphanumeric
Assy	- Assembly
ATTEN	- Attenuator, Attenuation
AUTO CAL	- Automatic Calibration
BATT	- Battery
BCUR	- Buffered Cursor
Bd	- Board
BW	- Bandwidth
CAL	- Calibration
CAL OUT	- Calibration Output
cm	- Centimeter
COAX	- Coaxial Cable
COMP	- Compare
CPU	- Central Processing Unit
CRT	- Cathode Ray Tube
CTC	- Counter-Timer Circuit
CW	- Continuous Wave
DAC (D/A)	- Digital-to-Analog Converter
dB	- Decibels
dBc	- Decibels relative to a carrier
dBm	- Decibels relative to milliamps
dBmV	- Decibels relative to millivolts
dBµV	- Decibels relative to microvolts
DC	- Direct Current
DIV (Div)	- Division(s)
ECL	- Emitter Coupler Logic
e.g.	- for example
EMC	- Electro-Magnetic compatibility
EPROM	- Eraseable Programmable Read-only Memory
EXT AMP	- External Amplifier
F	- Farad
FET	- Field-effect Transistor
FIFO	- First-in First-out
FM	- Frequency Modulation
GEN	- Generator
GHz	- GigaHertz
GPIB	- General Purpose Interface Bus

Hz	- Hertz
IC	- Integrated Circuit
i.e.	- that is
IEEE	- Institute of Electrical and Electronic Engineers
IEEE-488	- An IEEE communications standard
IF	- Intermediate Frequency
IORQ	- Input-output request
K	- kilo - 1,000
kg	- kilogram
kHz	- kiloHertz
LIN	- Linear
LO	- Local Oscillator
LOG AMP	- Logarithmic Amplifier
LPF	- Low-pass Filter
LSB	- Least Significant Bit
MHz	- Megahertz
MOD	- Modulo
MREQ	- Memory request
MSB	- Most Significant Bit
nS (nSec)	- nanosecond
nW	- nanowatt
PC	- Printed Circuit
pF	- picoFarad
p-p	- peak-to-peak
PROM	- Programmable read-only memory
psi	- pounds per square inch
PWR	- power
Q	- Logical output level of a flip-flop
RAM	- Random Access Memory
RCVR	- Receiver
REF	- Reference
REF CAL OUT	- Reference Calibration Output
REF FREQ	- Reference Frequency
RES B/W	- Resolution Bandwidth
RF	- Radio Frequency
RFSH	- Refresh
RMS	- Root mean square
ROM	- Read-only Memory
RS-232	- A data communications standard
S/N	- Serial Number
SSB	- Single Side Band
SYN/SYNTH	- Synthesizer
TC	- Time Constant
TSR	- Time Sharing Receiver
TTL	- Transistor-to-Transistor Logic

V	- Voltage, Volts
VAC	- Volts, Alternating Current
VCO	- Voltage Controlled Oscillator
VDC	- Volts, Direct Current
VERT	- Vertical
VRMS	- Volts, Root Mean Square
*VRS T.M.	- Vertical Raster Scan
VSWR	- Voltage Standing-wave ratio
µV	- Microvolt

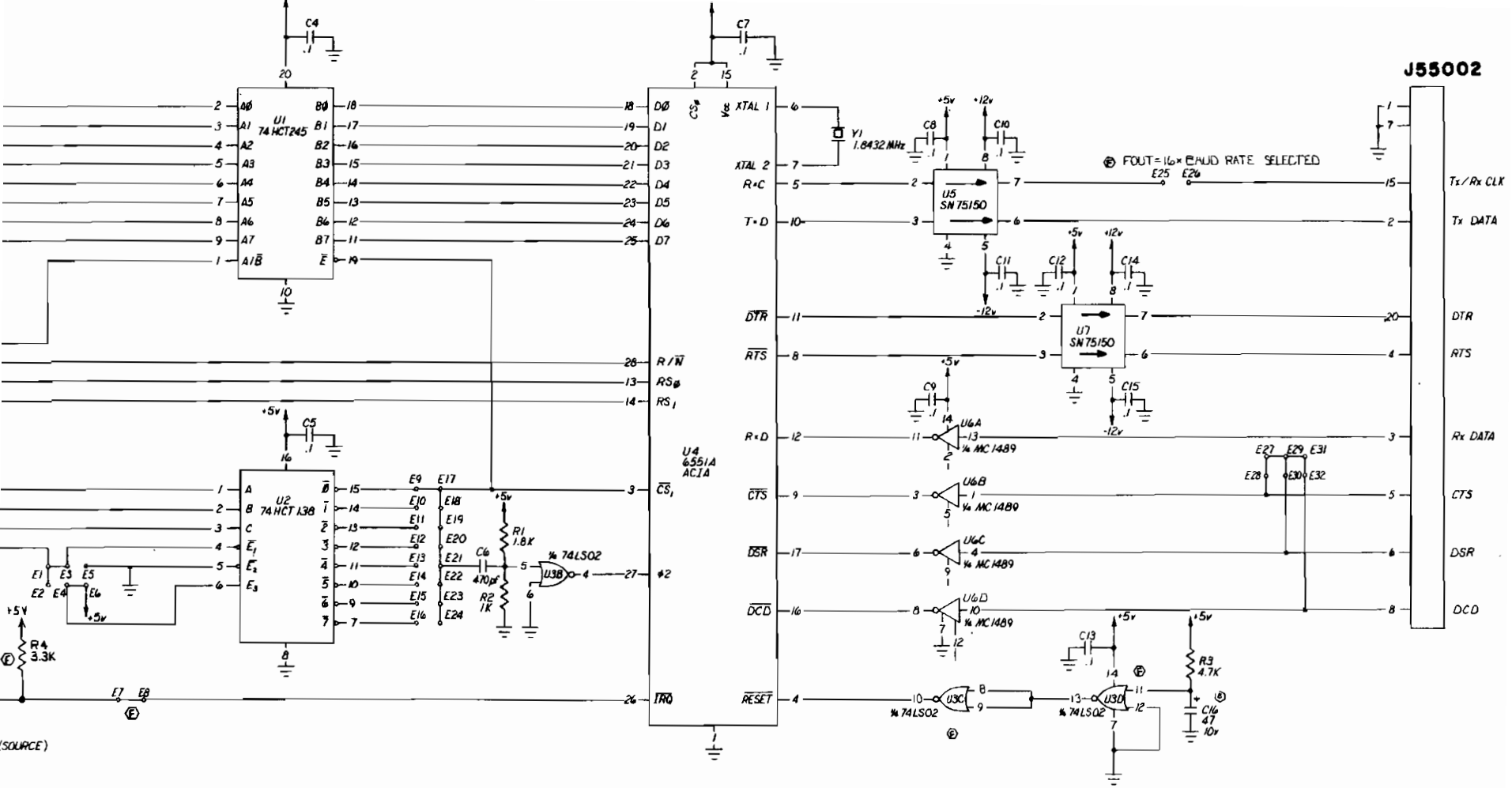
E-2 REFERENCE DESIGNATORS

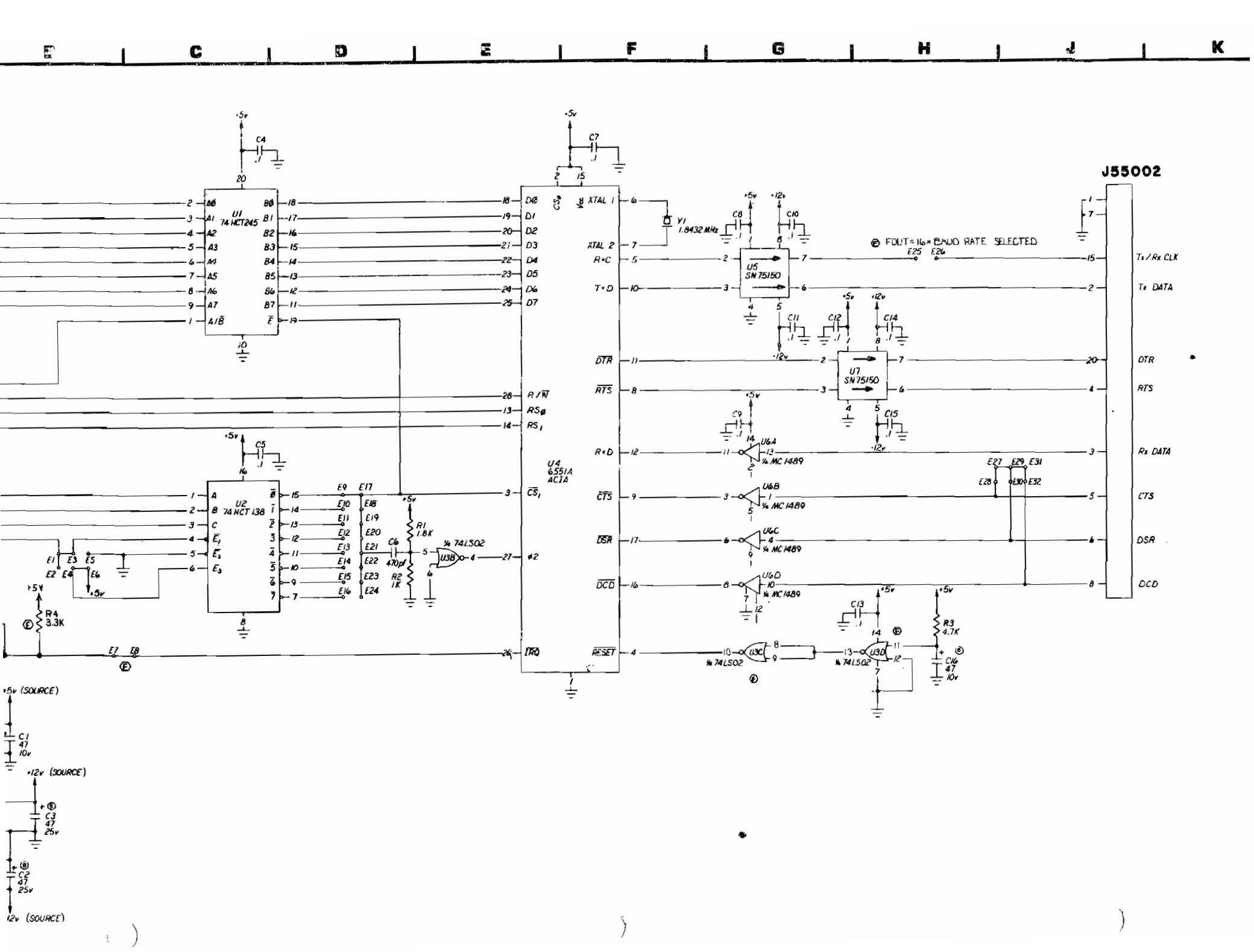
AT	Attenuator, Pad, Isolator
B	Motor, FAN
BR	Bridge Rectifier
BT	Battery
C	Capacitor
CR	Diode, Varactor
CX	Copax Cable
DET	Detector
DS	Lamp, Alphanumeric Display, LED, etc.
E	Connection, Inseparable, Elect.
F	Fuse
FL	Filter, VFeedthrough Cap
G	Ground
Hy	Circulator
J	Jack (fixed half of connector pair)
JTB	Jumper Terminal Block
K	Relay
L	Inductor, Ferrite Bead
M	Meter
MXR	Mixer
P	Plug (Moveable half of connector pair)
PC	Printed Circuti Board
Q	Transistor
R	Resistor
RN	Resistor Network
RT	Thermistor
S	Switch
SP	Speaker
T	Transformer
TP	Test Point
U	Opto-isolator, I.C., Voltage Regulator, Incapsulated Circuit (i.e., Circuit Combiner)
X	Socket
Y	Crystal
YFL	XTAL Filter
Z	Tune Pole, Tuneable Band Pass Filter

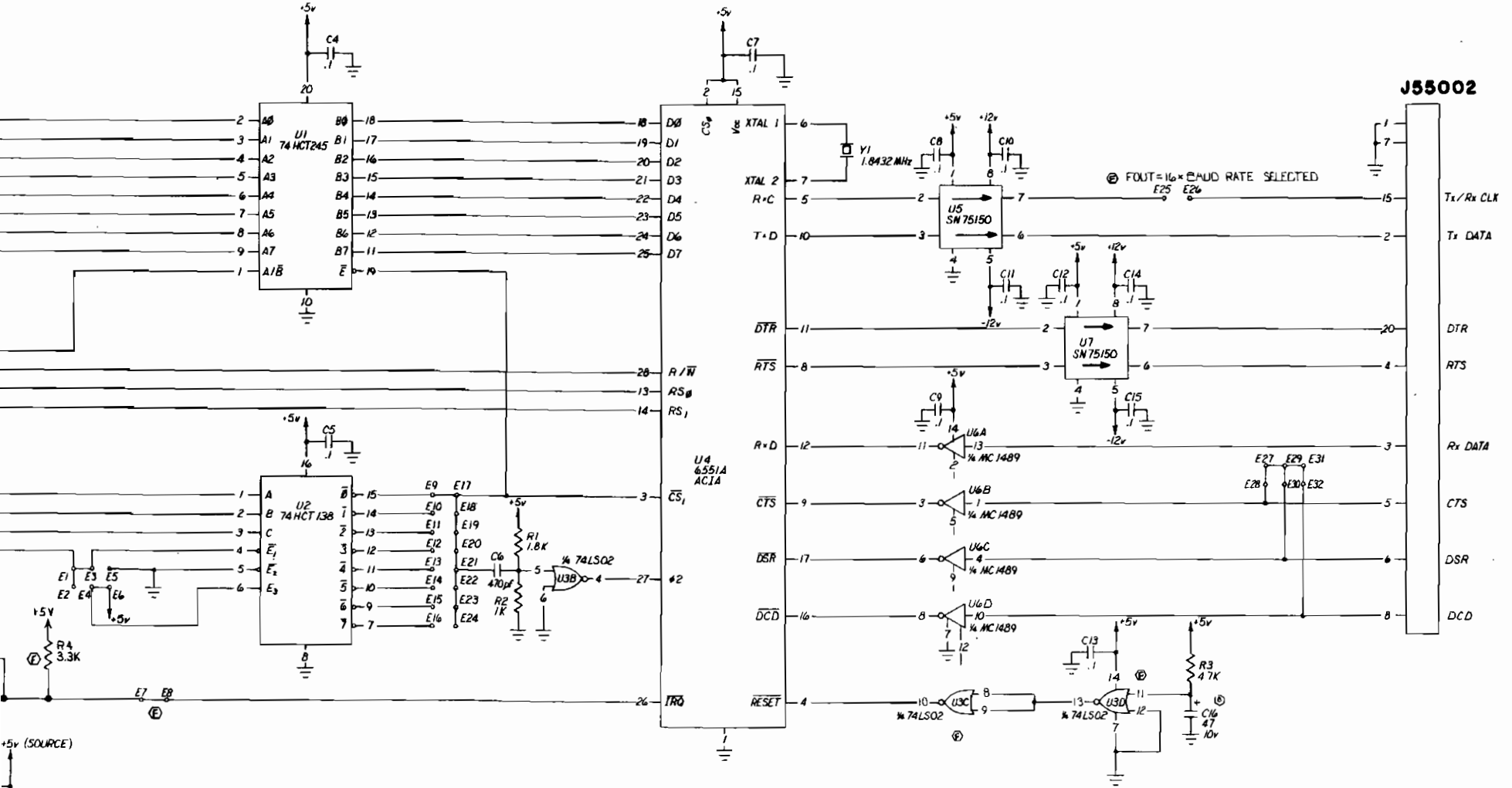
*IFR SYSTEMS, INC. TRADEMARK

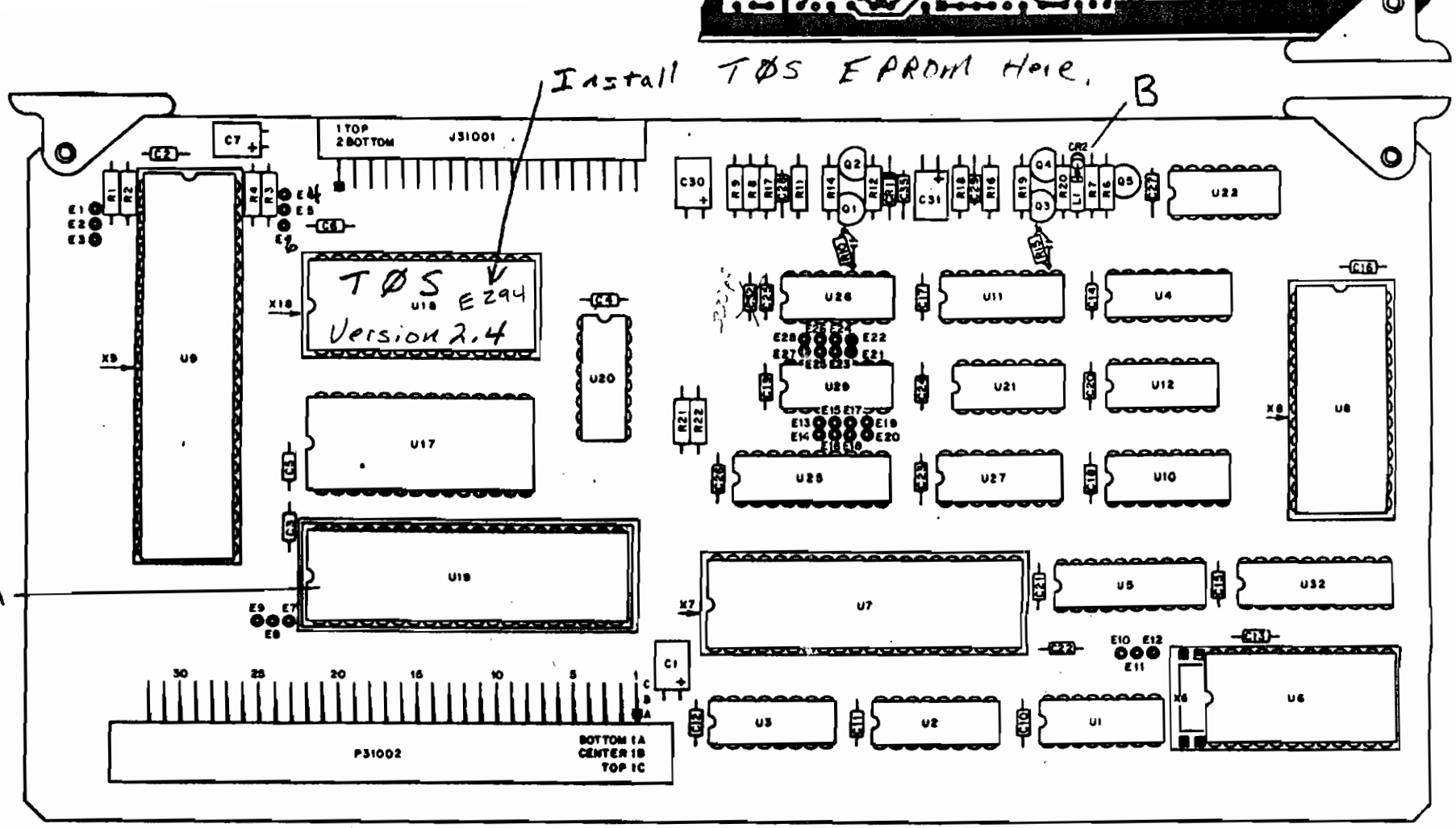
APPENDIX F - dBm TO MICROVOLT CONVERSION CHART

dBm	µV	dBm	µV	dBm	µV
0	224,000	-47	1,000	-94	4.47
-1	200,000	-48	891	-95	3.99
-2	178,000	-49	795	-96	3.55
-3	159,000	-50	709	-97	3.17
-4	141,000	-51	633	-98	2.82
-5	126,000	-52	563	-99	2.52
-6	112,000	-53	501	-100	2.24
-7	100,000	-54	447	-101	2.00
-8	89,100	-55	399	-102	1.78
-9	79,500	-56	355	-103	1.59
-10	70,900	-57	317	-104	1.41
-11	63,300	-58	282	-105	1.26
-12	56,300	-59	252	-106	1.12
-13	50,100	-60	224	-107	1.00
-14	44,700	-61	200	-108	0.891
-15	39,900	-62	178	-109	0.795
-16	35,500	-63	159	-110	0.709
-17	31,700	-64	141	-111	0.633
-18	28,200	-65	126	-112	0.563
-19	25,200	-66	112	-113	0.501
-20	22,400	-67	100	-114	0.447
-21	20,000	-68	89.1	-115	0.399
-22	17,800	-69	79.5	-116	0.355
-23	15,900	-70	70.9	-117	0.317
-24	14,100	-71	63.3	-118	0.282
-25	12,600	-72	56.3	-119	0.252
-26	11,200	-73	50.1	-120	0.224
-27	10,000	-74	44.7	-121	0.200
-28	8,900	-75	39.9	-122	0.178
-29	7,950	-76	35.5	-123	0.159
-30	7,090	-77	31.7	-124	0.141
-31	6,330	-78	28.2	-125	0.126
-32	5,630	-79	25.2	-126	0.112
-33	5,010	-80	22.4	-127	0.100
-34	4,470	-81	20.0	-128	0.0891
-35	3,990	-82	17.8	-129	0.0795
-36	3,550	-83	15.9	-130	0.0709
-37	3,170	-84	14.1	-131	0.0633
-38	2,820	-85	12.6	-132	0.0563
-39	2,520	-86	11.2	-133	0.0501
-40	2,240	-87	10.0	-134	0.0447
-41	2,000	-88	8.91	-135	0.0399
-42	1,780	-89	7.95	-136	0.0355
-43	1,590	-90	7.09	-137	0.0317
-44	1,410	-91	6.33	-138	0.0282
-45	1,260	-92	5.63	-139	0.0252
-46	1,120	-93	5.01	-140	0.0224


J55002
U1 74 HCT245
U2 74 HCT 138
U4 6551A ACIA
U5 SN 75150
U7 SN 75150
U6A 1/4 MC 1489
U6B 1/4 MC 1489
U6C 1/4 MC 1489
U6D 1/4 MC 1489
U3B 1/4 74LS02
U3C 1/4 74LS02
U3A 1/4 74LS02
Y1 1.8432 MHz
R1 1.8K
R2 1K
R3 4.7K
R4 3.3K
C6 470pf
C16 47 10v
FOUT=16× BAUD RATE SELECTED
Tx/Rx CLK
Tx DATA
DTR
RTS
Rx DATA
CTS
DSR
DCD
+5v
+12v
-12v
(SOURCE)


J55002
U1 74 HCT245
U2 74 HCT 138
U4 6551A ACIA
U5 SN 75150
U7 SN 75150
U6A ¼ MC 1489
U6B ¼ MC 1489
U6C ¼ MC 1489
U6D ¼ MC 1489
U3A ¼ 74LS02
U3B ¼ 74LS02
U3C ¼ 74LS02
U3D ¼ 74LS02
Y1 1.8432 MHz
R1 1.8K
R2 1K
R3 4.7K
R4 3.3K
C1 47 10v
C2 47 25v
C3 47 25v
C16 47 10v
C6 470pf
E FOUT = 16 × BAUD RATE SELECTED
+5v (SOURCE)
+12v (SOURCE)
-12v (SOURCE)
Tx / Rx CLK
Tx DATA
DTR
RTS
Rx DATA
CTS
DSR
DCD


J55002
U1 74HCT245
U2 74HCT138
U3 74LS02
U4 6551A ACIA
U5 SN75150
U7 SN75150
U6 MC1489
Y1 1.8432 MHz
R1 1.8K
R2 1K
R3 4.7K
R4 3.3K
C6 470pf
FOUT = 16 × BAUD RATE SELECTED
E25 E26
Tx/Rx CLK
Tx DATA
DTR
RTS
Rx DATA
CTS
DSR
DCD
+5v (SOURCE)
+12v (SOURCE)
-12v (SOURCE)

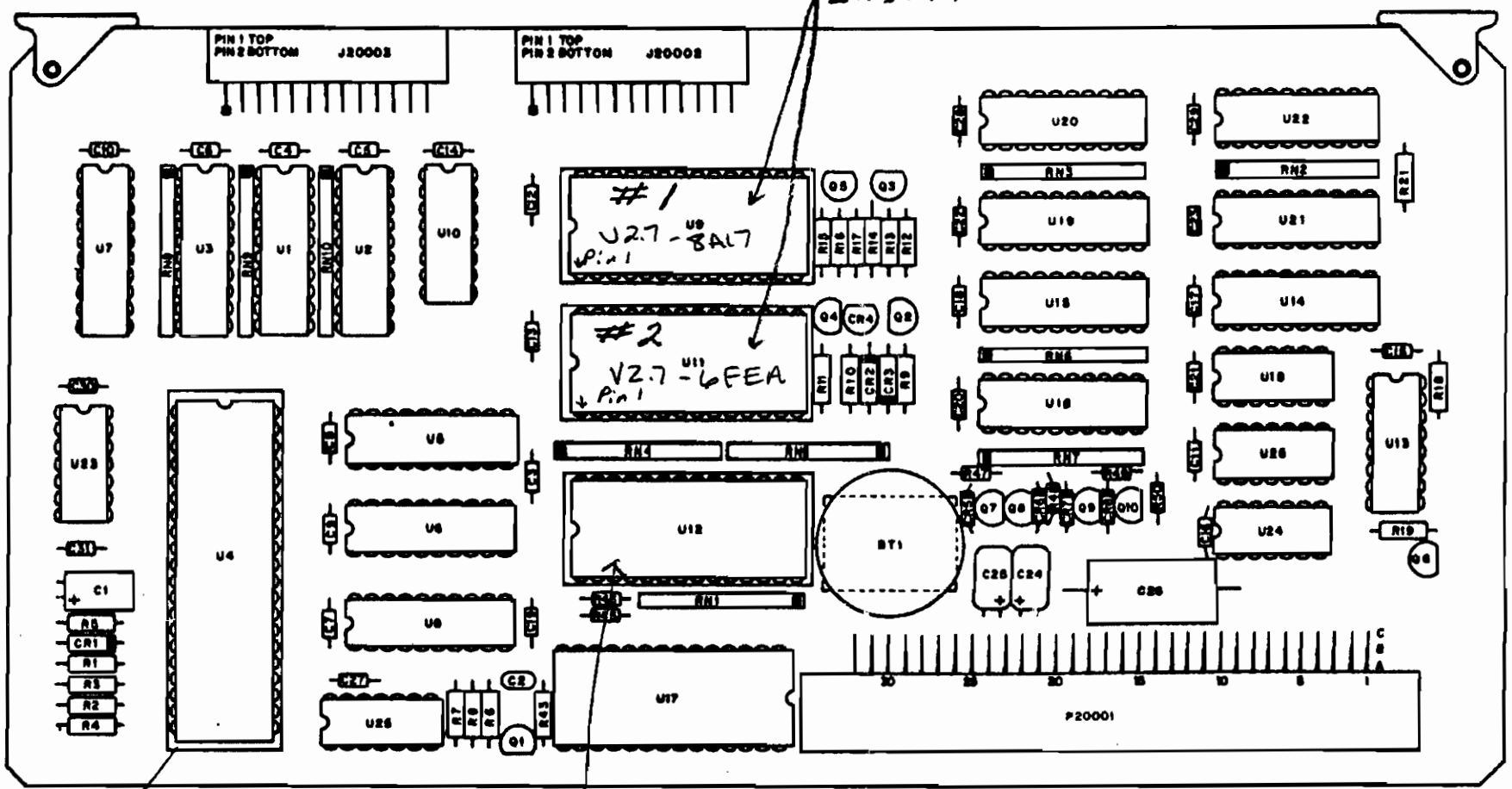


VIDEO PROCESSOR PC BD

7010-5334-200 C-2

1700-5326-500

REV. A



Control Processor PC Bd
1700-5326-600 7010-5334-400 D
REV A

Remove And Install This RAM IC
(Erases RAM Memory)

Turn Unit On, Then Off 3 Times -
Unit Will Lock Up First 2 Times -
Run RF Atten Up And Down After 3rd
Turn On - Unit Now Ready For Use

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