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OPERATION / MAINTENANCE MANUAL

STANDARD DIGITAL INTERFACE SYSTEM

STD-7000

PUBLISHED BY
IFR AMERICAS, INC.

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WARNING:

HIGH VOLTAGE EQUIPMENT

THIS EQUIPMENT CONTAINS CERTAIN CIRCUITS AND/OR COMPONENTS OF EXTREMELY HIGH VOLTAGE POTENTIALS, CAPABLE OF CAUSING SERIOUS BODILY INJURY OR DEATH. WHEN PERFORMING ANY OF THE PROCEDURES CONTAINED IN THIS MANUAL, HEED ALL APPLICABLE SAFETY PRECAUTIONS.

RESCUE OF SHOCK VICTIMS

1. DO NOT ATTEMPT TO PULL OR GRAB THE VICTIM
2. IF POSSIBLE, TURN OFF THE ELECTRICAL POWER.
3. IF YOU CANNOT TURN OFF ELECTRICAL POWER, PUSH, PULL OR LIFT THE VICTIM TO SAFETY USING A WOODEN POLE, A ROPE OR SOME OTHER DRY INSULATING MATERIAL.

FIRST AID

1. AS SOON AS VICTIM IS FREE OF CONTACT WITH SOURCE OF ELECTRICAL SHOCK, MOVE VICTIM A SHORT DISTANCE AWAY FROM SHOCK HAZARD.
2. SEND FOR DOCTOR AND/OR AMBULANCE.
3. KEEP VICTIM WARM, QUIET AND FLAT ON HIS/HER BACK.
4. IF BREATHING HAS STOPPED , ADMINISTER ARTIFICIAL RESUSCITATION. STOP ALL SERIOUS BLEEDING.

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CAUTION:

INTEGRATED CIRCUITS AND SOLID STATE DEVICES SUCH AS MOS FET'S, ESPECIALLY CMOS TYPES, ARE SUSCEPTIBLE TO DAMAGE BY ELECTROSTATIC DISCHARGES RECEIVED FROM IMPROPER HANDLING, THE USE OF UNGROUNDED TOOLS, AND IMPROPER STORAGE AND PACKAGING. ANY MAINTENANCE TO THIS UNIT MUST BE PERFORMED WITH THE FOLLOWING PRECAUTIONS:

1. BEFORE USING IN A CIRCUIT, KEEP ALL LEADS SHORTED TOGETHER EITHER BY THE USE OF VENDOR-SUPPLIED SHORTING SPRINGS OR BY INSERTING LEADS INTO A CONDUCTIVE MATERIAL.

2. WHEN REMOVING DEVICES FROM THEIR CONTAINERS, GROUND THE HAND BEING USED WITH A CONDUCTIVE WRISTBAND.

3. TIPS OF SOLDERING IRONS AND/OR ANY TOOLS USED MUST BE GROUNDED.

4. DEVICES MUST NEVER BE INSERTED INTO NOR REMOVED FROM CIRCUITS WITH POWER ON.

5. PC BOARD, WHEN TAKEN OUT OF THE SET, MUST BE LAID ON A GROUNDED CONDUCTIVE MAT OR STORED IN A CONDUCTIVE STORAGE BAG.

6. PC BOARDS, IF BEING SHIPPED TO THE FACTORY FOR REPAIR, MUST BE PACKAGED IN A CONDUCTIVE BAG AND PLACED IN A WELL-CUSHIONED SHIPPING BOX.

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INTRODUCTION - STD-7000 STANDARD DIGITAL INTERFACE SYSTEM

This manual contains operation and maintenance instructions for the STD-7000 Bus Controller and its optional Operator Terminal designated as the Standard Digital Interface (with keypad) System (SDIS).

The information provided in this manual will familiarize the operator/technician with the STD-7000 to:

1. Understand general operating capabilities of each unit and how both are to be implemented into a functional test system.

2. Identify and understand function of all equipment controls.

3. Properly interface STD-7000 to its Operator Terminal and prepare for further interface to accessory test equipment and UUT.

4. Power-up STD-7000/Operator Terminal and understand all phases of start-up operations.

5. Certify, test, repair or replace any major assembly or module within the STD-7000 Bus Controller.

6. Sufficiently understand the circuitry and principles of operation of the optional Operator Terminal and Keypad.

7. Maintain the operation of each unit in the Standard Digital Interface System to comply with expected performance standards as depicted in the "specifications" for each unit.

8. Understand the principles of operation as they relate to the overall operation of the system, as well as to individual circuits.

Due to the diverse range of applications for which this equipment can be used, this manual does not contain detailed operating instructions for any specific application. After thoroughly familiarizing oneself with all contents of this manual and sequentially performing all required installation/operation procedures, operator should refer to appropriate System Operation Manual for detailed operating instructions.

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The information in this manual applies to each unit in the Standard Digital Interface System (SDIS), which includes the STD-7000 Bus Controller Unit, ESP 6515 CRT Display Terminal, CRT Interface, Numeric Keypad and associated interface cabling. The information is relative to the mechanical and electrical characteristics of the Standard Digital Interface System (SDIS). This manual contains requirements for evaluating the SDIS during annual certification or at any time performance is in doubt. Even though its history indicates a high reliability rate, the SDIS may require "in depth" maintenance, such as prudent testing, troubleshooting and or extensive repair. With this in mind, the material and procedures in this manual will be helpful to the technician during the maintenance process from problem isolation to final repair.

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CHAPTER ONE

STD-7000 STANDARD DIGITAL INTERFACE SYSTEM

OPERATION MANUAL

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SECTION 1 - DESCRIPTION

1. General

The Standard Digital Interface System (SDIS) is comprised of the STD-7000 Bus Controller and Operator Terminal (CRT Display, CRT Interface and Numeric Keypad).

These components make up a standard hardware configuration common to several different ARINC compatible avionics test systems. The primary function of the configuration is to generate and receive ARINC 429/453 buses and display the contents of those buses on a CRT, thereby permitting an operator to verify the integrity of the system under test. A prime design goal of the SDIS is to provide a clear and simple format for monitoring and controlling ARINC bus activity from and to the unit under test (UUT), while allowing the operator to interpret and manipulate data with a minimum of effort.

2. Functional

Until programmed for a specific application and implemented within a test system thru an appropriate interface, the capabilities of the SDIS are limited to normal power-up functions. This manual therefore describes the capabilities of the SDIS on a general level only, as they exist within any ARINC 700 series test system. Detailed operation of the system, when programmed for specific applications, are described within separate System Operation Manuals.

A. STD-7000 Bus Controller

The STD-7000 is a programmable ARINC bus controller designed to control serial bus communication within ARINC 700 series avionics test systems. The controller contains the following bus provisions:

(1) Six (6) programmable high/low speed ARINC 429 I/O buses and three (3) programmable very high speed ARINC 453 I/O buses.

(2) One (1) IFR I/O bus used for interface of auxiliary IFR test equipment.

(3) One (1) IEEE Standard 488-1978 bus for interface of an external ATE Controller.

(4) One (1) EIA RS232C bus for interface of Operator Terminal.

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In addition to the STD-7000's primary function as a bus controller, the unit also has the capability of controlling and activating a UUT through an interface device, while monitoring selected discrete signals to determine performance.

B. Operator Terminal

The Operator Terminal, consisting of a CRT display terminal, CRT Interface and 16-Key numeric keypad, provides operator with ability to interact with test system. The display terminal permits operator to observe all pertinent bus status and control information, while the keypad enables control information to be entered into the system.

NOTE: The STD-7000's IEEE-488-1978 bus provision enables the test system to be interfaced with an external ATE Controller, permitting automatic/remote system control. Within this configuration, use of Operator Terminal is optional.

3. Functional Block Diagram

The "STD-7000 Functional Block Diagram" (refer to 1-1-1, Figure 1) depicts the Standard Digital Interface System implemented within a typical ARINC 700 series test system.

4. Software Implementation

To perform a given task, the STD-7000 must first be programmed with appropriate application software. In so doing, the STD-7000 is said to acquire a "personality", which enables it to execute program instructions according to the dictates of the application software. Two methods of software implementation are available to the user:

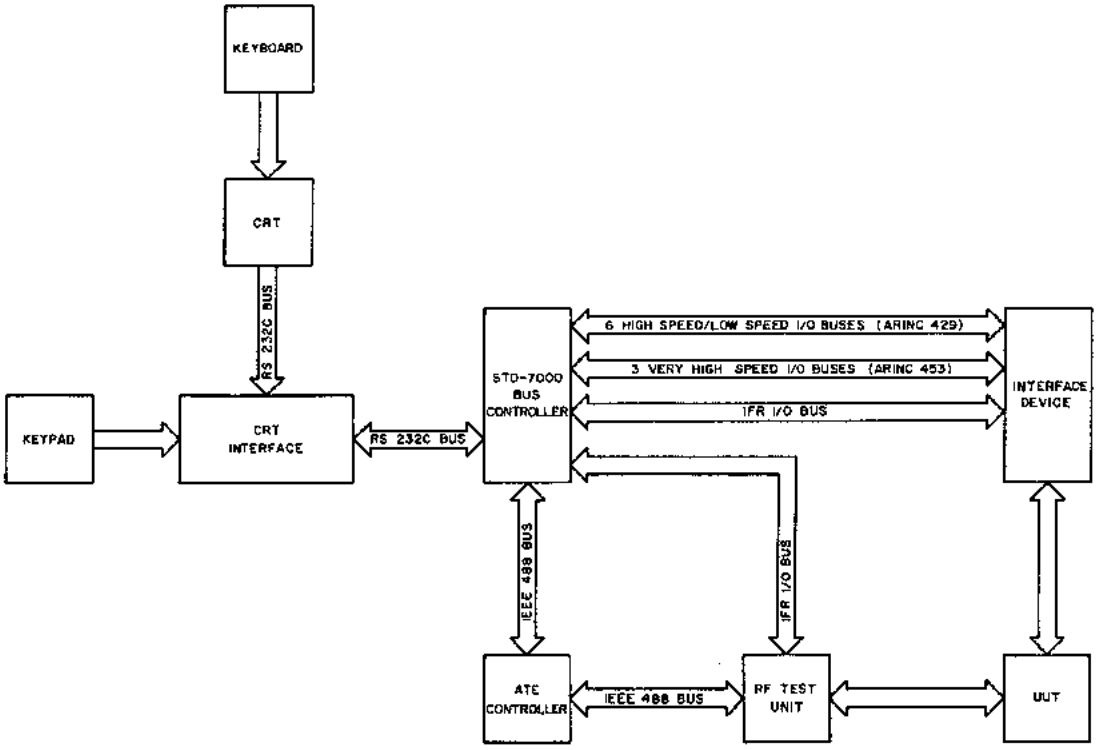
A. Magnetic (or "Personality") Tape

The STD-7000 is equipped with a magnetic tape drive which will accept certified mini-cassette tapes. The user is supplied with a prepared tape, containing desired application software, ready for loading into RAM memory.

B. PROM Card Memory (Optional)

At user's option, application software can be supplied on a PROM card.

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STD-7000 Functional Block Diagram
Figure 1

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5. Mechanical (Refer to 1-1-1, Figure 2)

The STD-7000 Bus Controller is comprised of the following major assemblies and associated modules:

A. Front Panel

Power Switch
Tape Transport (with ejector)
Numeric Keypad Mount
Reset Switch

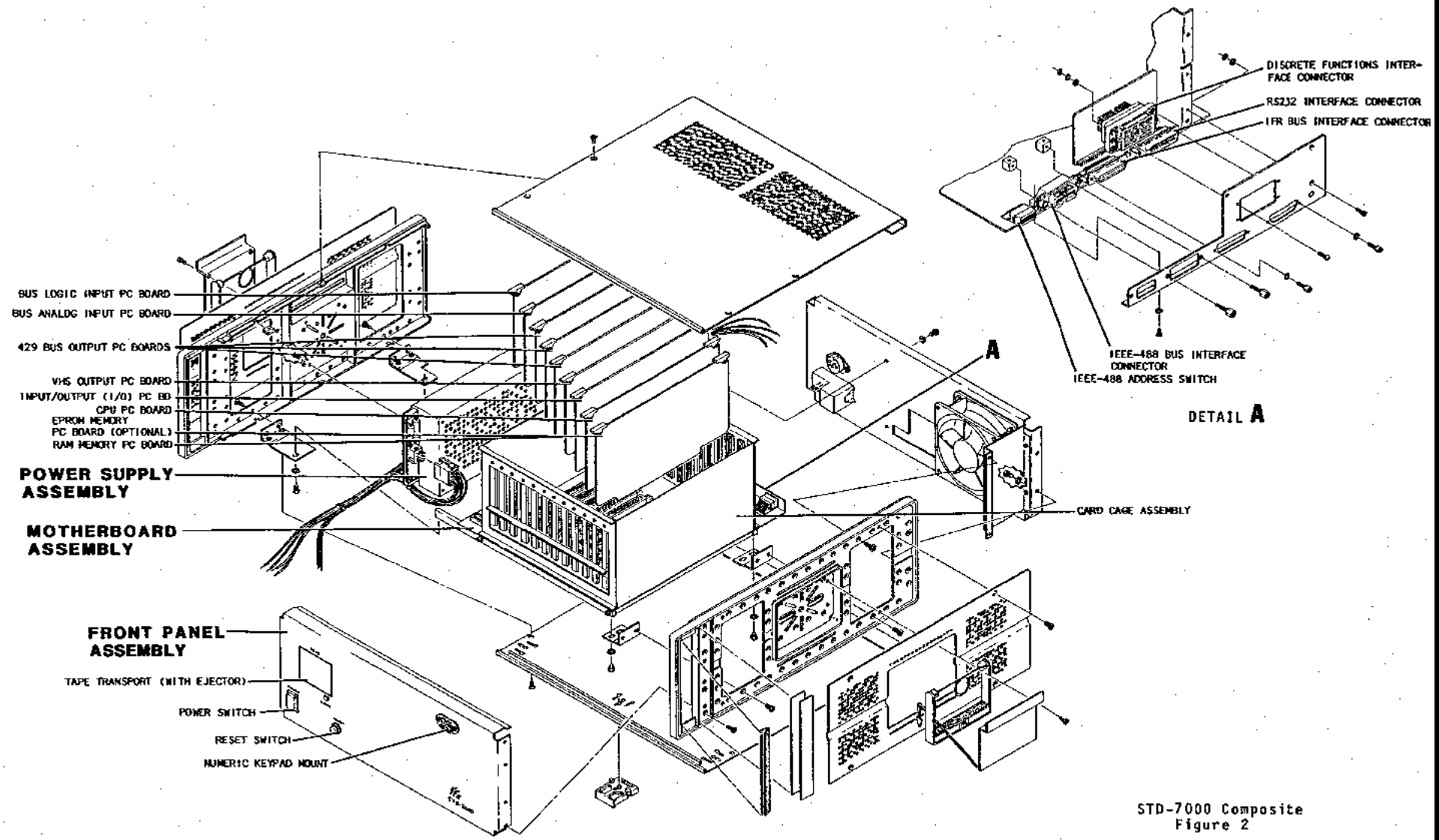
B. Motherboard Assembly

Card Cage Assembly
EPROM Memory PC Board (optional) (removable PC Board)
RAM Memory PC Board (removable PC Board)
429 Bus Output PC Boards (removable PC Board)
Bus Analog Input PC Board (removable PC Board)
IFR Bus Interface Connector
RS-232 Interface Connector
CPU PC Board (removable PC Board)
Input/Output (I/O) PC Bd (removable PC Board)
VHS Output PC Board (removable PC Board)
Bus Logic Input PC Board (removable PC Board)
IEEE-488 Address Switch
IEEE-488 Bus Interface Connector
Discrete Functions Interface Connector

C. Power Supply Assembly

NOTE: Two different types of Power Supply Modules are currently being used in the STD-7000 Bus Controller. In this manual, the IFR, Inc. Power Supply (Voltage Regulator) is described without any restrictions, however, information concerning the Sierracin Power Supply is restricted by its manufacturer to the +5 Volt calibration and removal/installation procedures.

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STD-7000 Composite
Figure 2

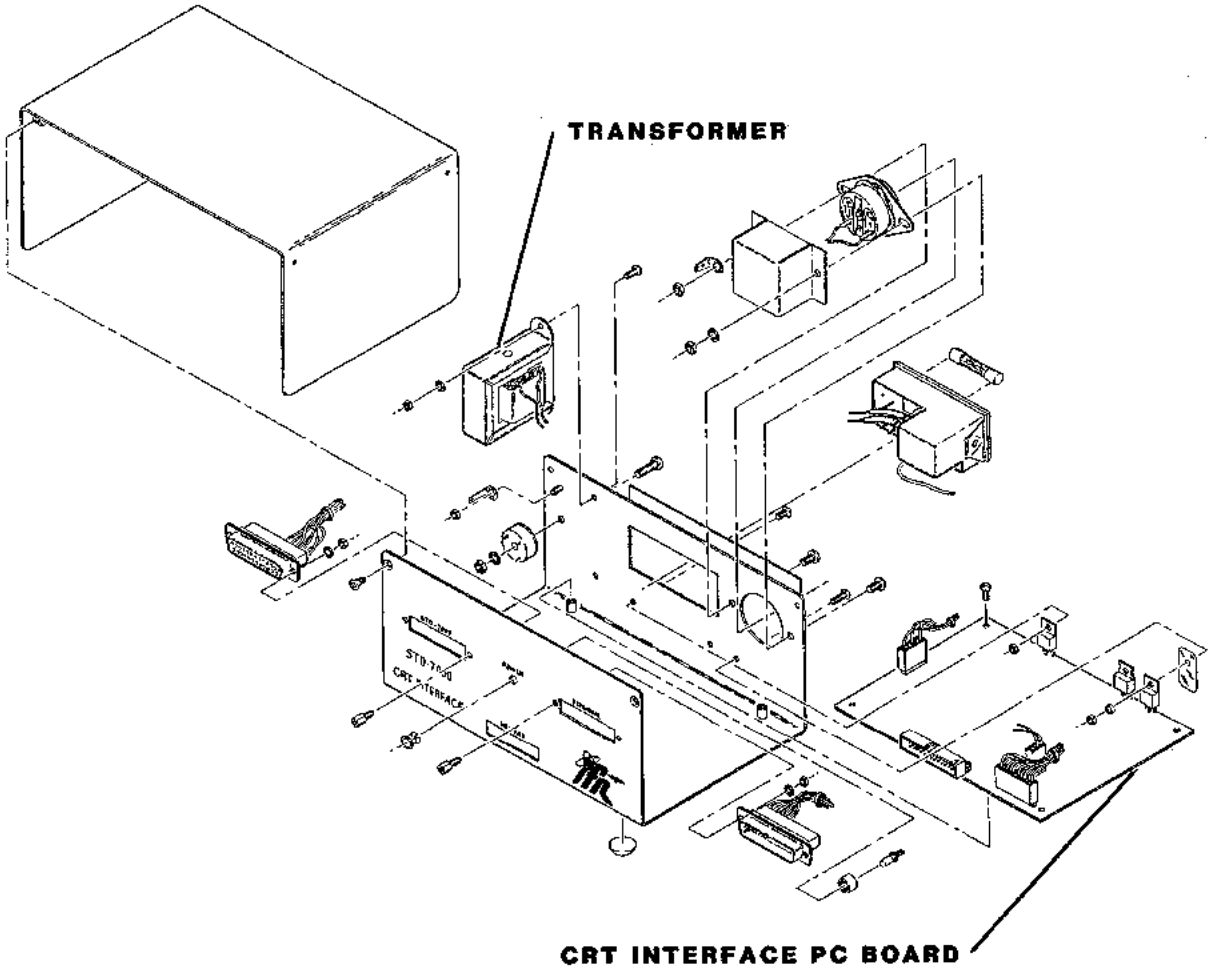
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6. Operator Terminal

The Operator Terminal CRT Interface consists of an ESP 6515 CRT Display Terminal and a KP-72480 Numeric Keypad. For maintenance information on the CRT, the technician should consult the appropriate CRT manufacturer's maintenance manual.



CRT Interface Composite
Figure 3

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SECTION 2 - OPERATION

1. Installation

A. General

This section contains instructions for interfacing the STD-7000 Controller with an Operator Terminal and preparing the STD-7000 and installation site for interface to accessory test equipment and UUT.

NOTE: As illustrated in the STD-7000 Functional Block Diagram (refer to 1-1-1, Figure 1), accessory test equipment for most ARINC 700 series test systems will consist primarily of a Discrete Functions Interface Device and an RF Test Unit. Instructions for interfacing these units to STD-7000 are contained in the appropriate System Operation Manual.

Also included in this section are recommendations regarding installation/operating safety, equipment inspection, power requirements, required installation tools and bench/rack installations.

(1) Safety Precautions

Listed below are several important safety precautions which must be observed during all phases of system installation and operation. IFR Inc. assumes no liability for customer's failure to comply with any of the safety precautions outlined in this manual.

(a) Complying With Instructions

Installation/operating personnel should not attempt to install/operate system without reading and complying with all instructions contained in in this manual. All procedures contained in this manual must be performed in exact sequence and manner described.

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(b) Grounding Requirements

To minimize shock hazard, all equipment chassis and cabinets must be connected to an electrical ground. For this purpose, all IFR test sets are equipped with a standard three-prong power cable which must be connected to a properly grounded three-prong wall receptacle. It is the customer's responsibility to:

1 Have a qualified electrician check wall receptacle(s) for proper grounding.

2 Replace any standard two-prong wall receptacle(s) with properly grounded three-prong receptacle(s).

WARNING: DUE TO POTENTIAL SAFETY HAZARDS, USE OF THREE-PRONG TO TWO-PRONG ADAPTOR PLUG(S) IS NOT RECOMMENDED.

(c) Operating Safety

Due to presence of potentially lethal voltages within test equipment, operating personnel must not remove test equipment covers at any time. Component replacement and internal adjustments must be made by qualified maintenance personnel only.

(d) Observing "CAUTION" and "WARNING" Labels

Extreme care should be exercised when performing any operations preceded by a "CAUTION" or "WARNING" label. "CAUTION" labels appear where possibility of damage to equipment exists, while "WARNING" notes are used to denote a condition where a shock hazard exists, exposing personnel to possible bodily injury.

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(2) Equipment Inspection

All IFR test sets are carefully inspected for material defects and are subjected to a thorough performance check prior to leaving factory. All sets are shipped to customer in excellent mechanical/electrical condition. Upon receipt of shipment, receiving personnel should:

(a) Account for presence of all equipment and accessories as listed on packing slip.

(b) Inspect all equipment for visible or concealed damage which may have occurred in transit. (If damage is apparent, see Receiving Inspection/ Unpacking sticker affixed to shipping container for Damage Claim procedure.)

(3) Power Requirements

All IFR test sets are normally factory wired to accept available external power service at installation site. Prior to making any electrical connections, installation personnel must check equipment power rating against power service rating, making sure both are same.

NOTE: Equipment power rating information can be found on Model/Serial No. nameplate, located on rear panel of test instruments or in 1-3-1.

If existing power service does not conform to equipment requirements, customer should contact IFR factory for instructions concerning equipment power supply modifications.

(4) Installation Equipment

All electrical connections are easily made by hand, without use of any special tools.

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(5) Bench/Rack Installation

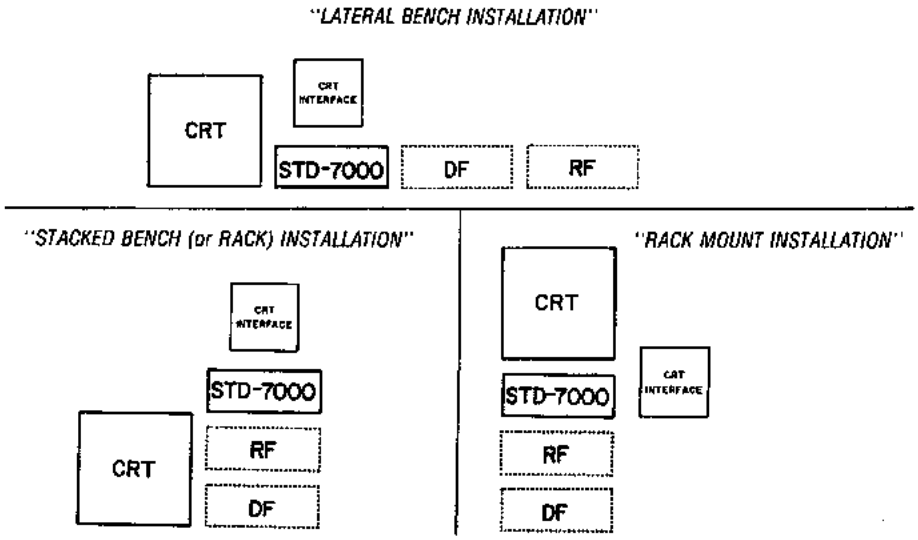
The STD-7000 Controller, Operator Terminal and accessory test equipment can be installed in either a bench-top or rack-mount fashion. All IFR test sets are normally shipped from factory with plastic feet installed for a bench-top installation. Instruments equipped for rack-mount installation must be special ordered from factory.

NOTE: Conversion from bench to rack-mount installation is possible by ordering appropriate rack mounting kits from IFR factory (one kit per instrument required):

Equipment	Rack Mounting Kit (IFR Part Number)
STD-7000	1001-0000-002
CRT Display Terminal	1405-0001-000

Rack Mounting Kits
Table 1

Shown below are the recommended installation configurations for the STD-7000, Operator Terminal and accessory equipment:



Recommended Installation Configuration
Figure 1

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B. System Interface

(1) System Interface Procedure (Refer to 1-2-1, Figure 2)

(a) Position STD-7000, Display Terminal Interface and CRT Terminal on bench or within rack, leaving appropriate space for interface of accessory test equipment.

(b) Connect Cable 1 from STD-7000 CRT Power Connector (J202) to CRT Interface Power Input Connector (J15001).

(c) Connect Cable 2 from CRT Interface Power Output Connector (J15005) to CRT Terminal.

(d) Connect Cable 3 from CRT Interface Terminal Connector (J15004) to CRT Terminal.

(e) Connect Keypad to CRT Interface Keypad Connector (J15002).

(f) Connect Cable 4 from STD-7000 RS-232C Connector (J414) to CRT Interface STD-7000 Connector (J15003).

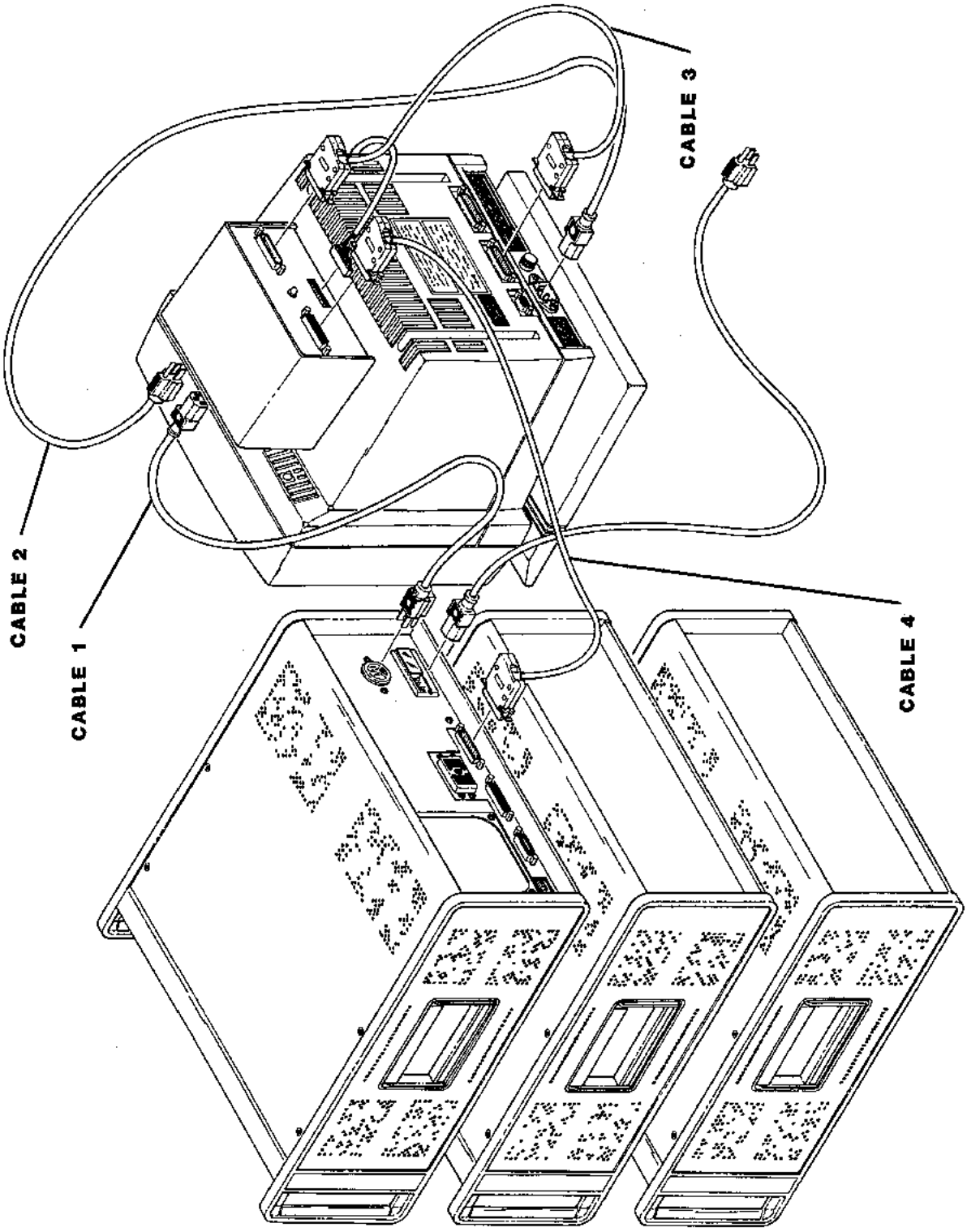
(g) Connect Keyboard to CRT Terminal.

(h) Plug female end of supplied STD-7000 AC power cable into male power receptacle (J201) on rear panel of STD-7000.

(i) Plug male end of STD-7000 AC power cord into standard three-prong grounded wall receptacle.

Interface procedure is now complete. Do not activate STD-7000 AC power switch at this time; familiarization with all information contained in 1-2-2 and 1-2-3 is required before power-up sequence is performed.

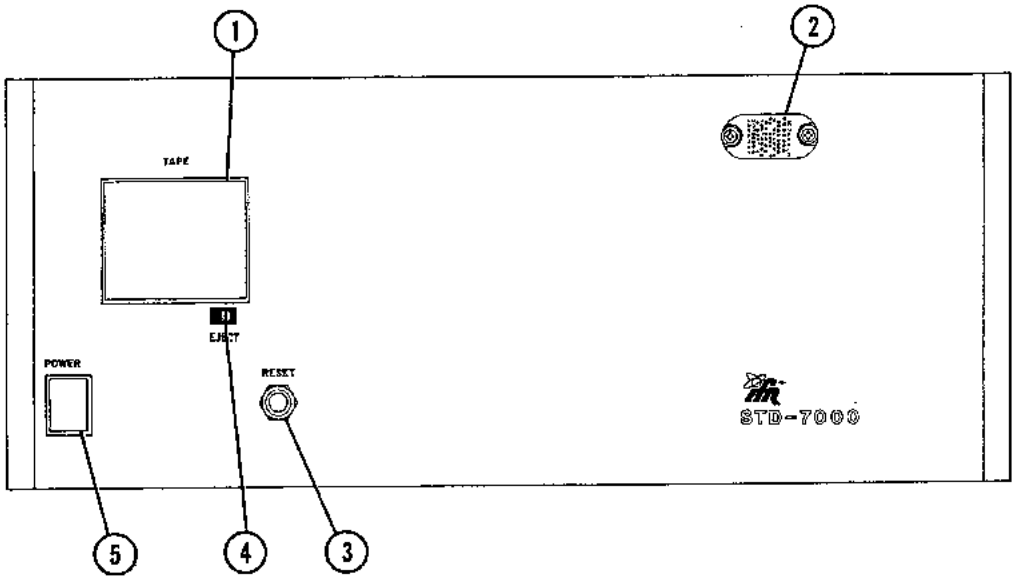
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System Interface Diagram
Figure 2

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2. Description of Controls, Connectors, and Indicators



STD-7000 Front Panel
Figure 3

A. STD-7000 Front Panel

(1) Magnetic Tape Transport

Tape drive compartment for program (personality) tape cassettes. Tape drive will accept only Certified Digital Mini-cassettes.

(2) Keypad Mount

Mounting attachment used in securing model KP-72480 Keypad to STD-7000 front panel for operating convenience.

(3) Reset Switch

Returns all program test sequences and variables to initial operating conditions in event a program restart is desired.

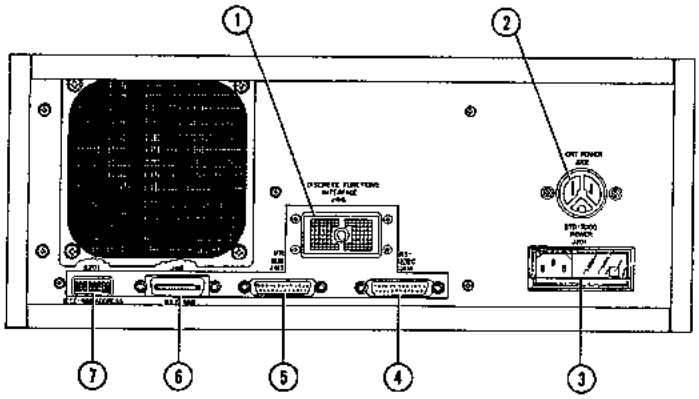
(4) Tape Cassette Eject Button

Provides access to tape drive compartment for tape loading or ejection.

(5) AC Power Switch

Pushbutton switch which supplies/interrupts external AC power to STD-7000. (Switch is illuminated when power is set to ON.)

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STD-7000 Rear Panel
Figure 4

B. Rear Panel

(1) Discrete Functions Interface Connector

96-pin female connector for interface of Discrete Functions Control Unit to STD-7000.

(2) CRT Power Receptacle

Standard 3-prong power receptacle for interface of CRT Interface.

(3) STD-7000 Power Receptacle/Line Fuse Compartment

Contains standard three-prong power receptacle for STD-7000 AC power cord and 2 Amp line fuse.

(4) RS232C Interface Connector

25-pin EIA RS232C compatible female connector for interface of CRT Interface.

(5) IFR Bus Interface Connector

25-pin female connector for interface of auxiliary IFR test equipment.

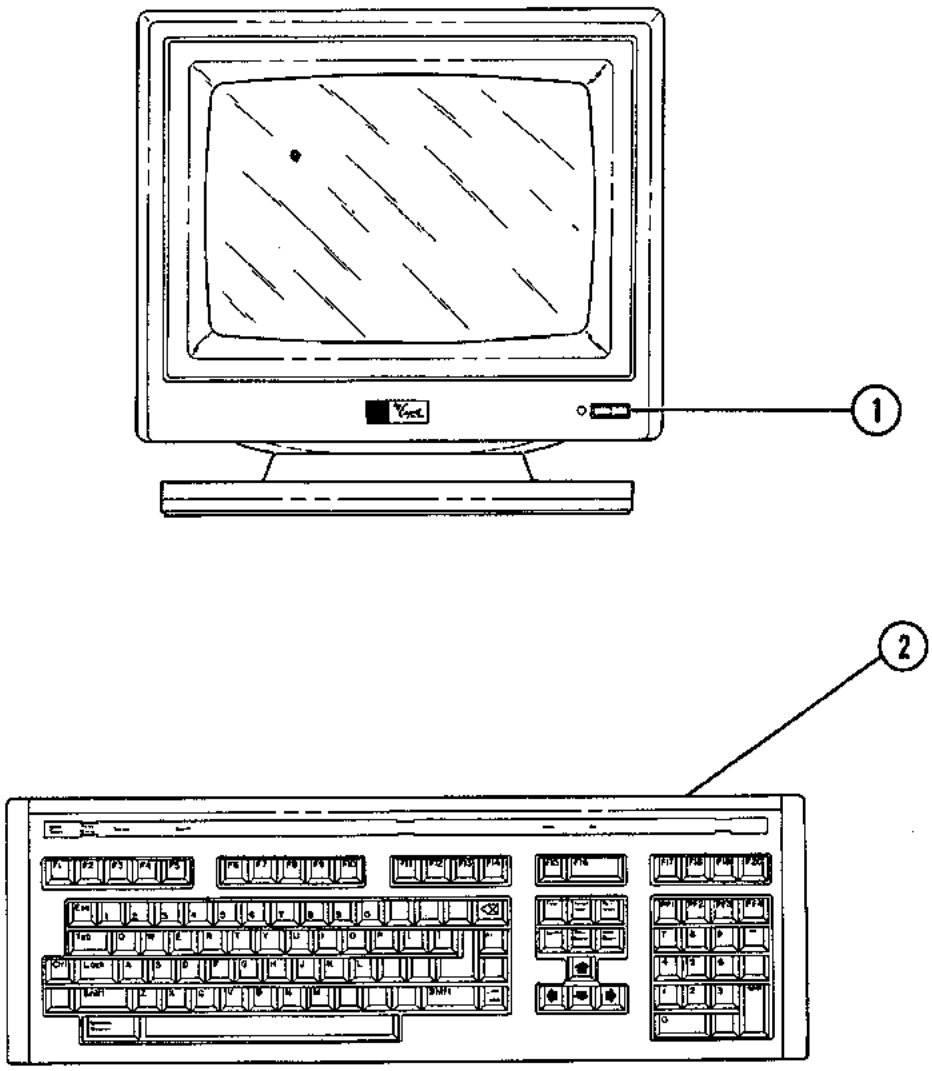
(6) IEEE-488 Bus Interface Connector

24-pin female connector conforming to IEEE Standard 488-1978 for interface of general purpose programmable instrumentation.

(7) IEEE-488 Address Switch

Eight segment DIP switch used for setting both IEEE-488 bus address and operating mode of STD-7000.

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CRT Display Terminal (Front View)
Figure 5

C. ESP-6515 CRT Display Terminal

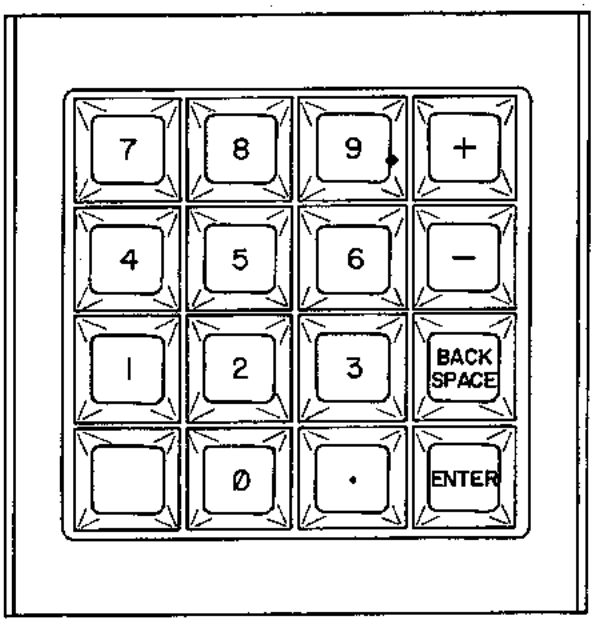
(1) CRT Power Switch

Pushbutton switch which supplies/interrupts AC power to CRT Terminal.

(2) CRT Keyboard

(Refer to Manufacturer Reference Manual for key identification and description.)

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16-Key Numeric Keypad (Top View)
Figure 6

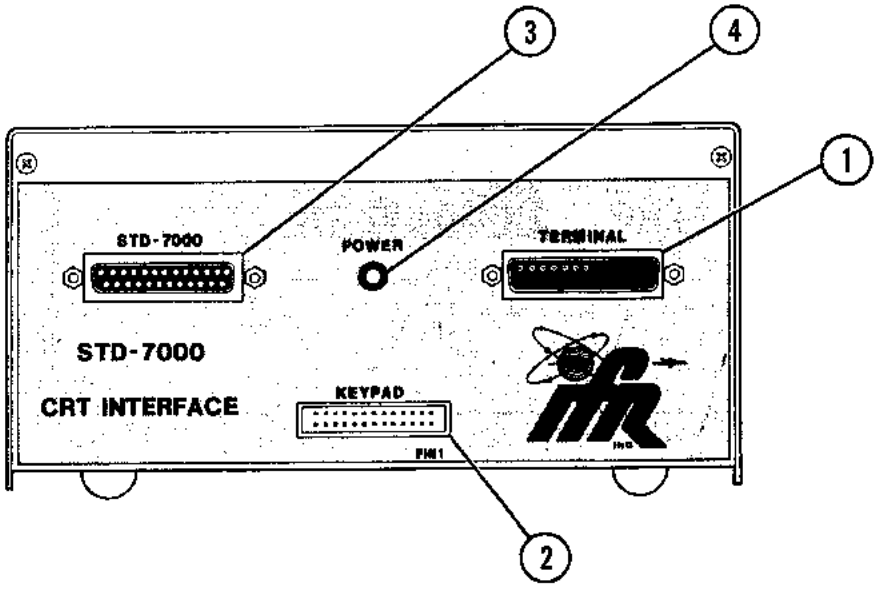
D. Numeric Keypad

All data entry operations are performed with the 16-key numeric keypad. All keypad entries are displayed on CRT Terminal, where each can be checked for proper input format prior to being entered into STD-7000 memory.

(1) Basic Keypad Operations

Function	Required Keystrokes
ENTERING DATA INTO MEMORY	1. Key in numeric data into appropriate data field. 2. Press "ENTER" key.
ERROR CORRECTION (For data keyed in, but not yet entered into memory)	1. Press "BACKSPACE" key to erase any displayed data preceding CRT cursor.
ERROR CORRECTION (For data entered into memory)	1. Procedure same as outlined for "ENTERING DATA INTO MEMORY."

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CRT Interface Front Panel
Figure 7

E. CRT Interface Front Panel

(1) Terminal Connector

Input/Output Connector for CRT Terminal.

(2) Keypad Connector

26 PIN Connector for STD-7000 Keypad.

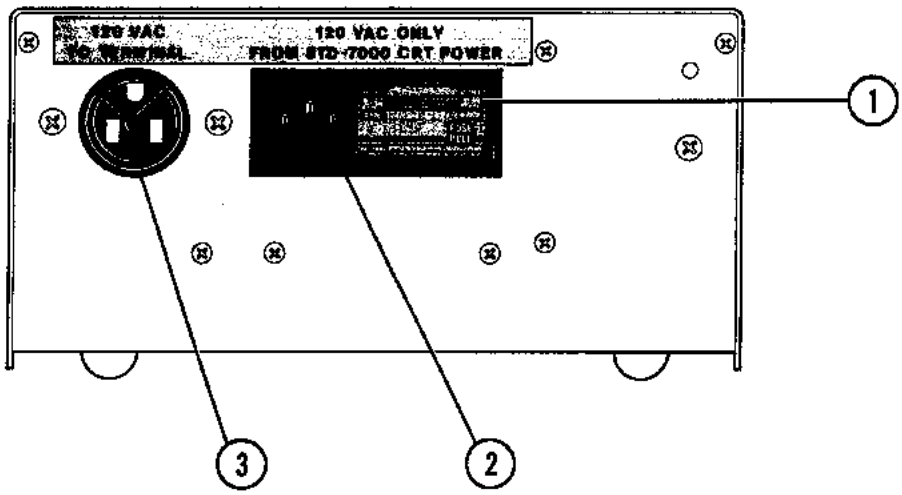
(3) STD-7000 Connector

Input/Output Connector for STD-7000.

(4) Power Indicator Lamp

Illuminates when power is applied to the CRT Interface.

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CRT Interface Rear Panel
Figure 8

F. CRT Interface Rear Panel

(1) Fuse

1.5 Amp - 125 Volt

(2) Power Input Connector

Input Connector for STD-7000.

(3) Power Output Connector

Output Connector for CRT Terminal.

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3. General Operating Procedures

A. Power-Up Behavior

Power-up behavior concerns the operating characteristics of the SDIS from the time power is first applied to the system until the initial personality display is presented on the CRT. These operating characteristics include several different power-up sequences or start-up routines contained in STD-7000 firmware, which are operator selectable through the IEEE-488 address switch. Described below are four resident start-up routines available for use:

(1) Automatic Start-Up Routine

This routine is intended for use within manual operating systems (equipped for magnetic tape and/or PROM card operation), where operator control is implemented through a CRT terminal/keypad combination. This routine automatically performs all necessary start-up operations required to obtain an initial personality display.

(2) Diagnostic Test Program

The diagnostic test program contains several important self-test routines used in maintaining and troubleshooting the STD-7000.

CAUTION: THESE ROUTINES ARE NOT INTENDED FOR OPERATOR USE. ALL DIAGNOSTIC TEST PROCEDURES SHOULD BE PERFORMED BY QUALIFIED MAINTENANCE PERSONNEL ONLY! (REFER TO 2-2-2).

(3) Tape Program

This routine automatically performs tape rewinding and program loading functions for STD-7000 units equipped only for magnetic tape operation. Use of this routine is intended for STD-7000 units operating under ATE control.

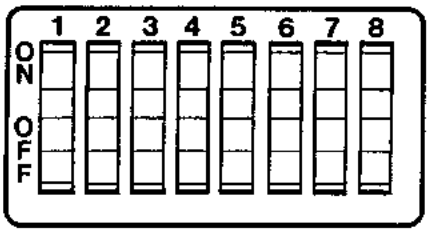
(4) PROM Program

Similar to the Tape Program described above, this routine is intended for STD-7000 units functioning under ATE control and equipped for optional PROM card operation. This routine will automatically access and display program information contained in PROM.

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B. IEEE-488 Address Switch Settings

The IEEE-488 address switch (1-2-3, Figure 9) is located in the lower left hand corner of STD-7000 rear panel (refer to 1-2-2, Figure 4). Each switch segment can be placed to an ON or OFF position.



STD-7000 IEEE-488 Address Switch Settings
Figure 9

C. IEEE-488 Address Switch Functions

(1) Selection of Start-Up Routines

To select one of the four start-up routines, only switch segments 7 and 8 are used (positioning of segments 1 thru 6 do not affect selection of a start-up routine). The following table specifies positioning required of segments 7 and 8 for selection of a given start-up routine:

START-UP ROUTINE	SEGMENT 7	SEGMENT 8
Automatic Start-up Routine	ON	ON
Diagnostic Menu	OFF	OFF
Tape Program	OFF	ON
PROM Program	ON	OFF

Segment Positioning
Table 2

(2) Selection of Bus Address

Switch segments 1 thru 6 are used to set bus address of STD-7000 when interfaced with IEEE-488 bus. (Specific switch settings for this purpose are contained in appropriate System Operation Manual, under section ATE System Operation.)

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Detailed discussion of Automatic Start-up Routine will follow in 1-2-3D. Operator should now set switch segments 7 and 8 to proper location.

D. Automatic Start-Up Routine

The automatic start-up routine performs virtually all power-up functions automatically from time operator activates STD-7000 power switch until an initial tape or PROM personality display appears on CRT. Depending on equipment configuration, required operator action (beyond activating power switch) is normally limited to two or fewer keypad entries.

The Automatic Start-Up Routine (refer to 1-2-3, Figure 10) depicts the sequential flow of start-up operations from the time power is applied until the initial personality display is presented. A detailed step by step description of those operations is listed below, including the explanation of all utility codes and instructions which may appear on CRT.

(1) INSERT PERSONALITY TAPE INTO TAPE DRIVE (unless unit is equipped for PROM card operation).

(2) ACTIVATE STD-7000 POWER SWITCH

Operator applies AC power to Standard Digital Interface System by pressing STD-7000 "POWER" switch.

(3) MEMORY DIAGNOSTIC

A few seconds after power is applied, a memory diagnostic is automatically performed to check all memory locations for proper operation. An eight character hex field (8000 XX XX++++*) will momentarily appear on CRT to indicate memory diagnostic is taking place.

NOTE: 8000 is a four digit hex field, representing the maximum RAM address available within system. This figure will vary from one unit to another, depending on options installed.

NOTE: Warm up time of CRT is approximately 10 seconds. If system is started up cold, memory diagnostic may be concluded prior to CRT warm-up and the hex field will not be visible.

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If a memory error is detected during memory diagnostic, start-up routine automatically jumps to Diagnostic Test Program. If this condition occurs, operator should consult authorized maintenance personnel before taking further action.

(4) PROM CARD MEMORY CHECK

Following a successful memory diagnostic, the STD-7000 performs a self-check to determine if an optional PROM memory card is installed. The STD-7000 unit is equipped for magnetic tape and/or PROM card operation. If STD-7000 contains both operation capabilities, the personality software contained on tape may or may not be the same as that contained in PROM.

(a) If PROM card memory is available, CRT will automatically display a RESET MENU as shown below. (refer to 1-2-3E for definition and use of menu format.)

RESET MENU

1. EXECUTE TAPE PROGRAM
2. LOAD AND EXECUTE TAPE PROGRAM
3. EXECUTE PROM PROGRAM

KEY IN:___

Through an appropriate keypad entry, operator can instruct STD-7000 to execute one of the three operations listed on RESET MENU.

1 A key entry of 1 will immediately provide an initial personality display of tape program (if tape has been loaded).

2 A key entry of 2 will provide an initial personality display of tape program subsequent to program loading.

3 A key entry of 3 will immediately provide an initial personality display of PROM program.

(b) Without PROM card memory capability, the routine will proceed directly with tape rewinding and loading functions immediately after completion of memory diagnostic.

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(5) REWIND TAPE

As a prerequisite to program loading, all magnetic tape cassettes are automatically rewound to start position. CRT will display REWINDING TAPE when this operation is in progress. (Maximum duration: approx. 30 seconds.)

(6) LOAD TAPE

Program information contained on tape is entered into STD-7000 RAM memory. (Maximum duration: approx. 90 seconds.)

(7) RESET OPERATION

Under normal operating conditions, "RESET" switch is used primarily to:

(a) Return all test parameters and sequences to their initial conditions.

(b) Restart a program after a program error occurs.

Pressing RESET switch after an initial personality display has been achieved, will cause automatic start-up routine to reinitialize as follows:

(a) Under magnetic tape operation

The following RESET MENU will automatically appear on CRT:

RESET MENU

1. EXECUTE TAPE PROGRAM
2. LOAD AND EXECUTE TAPE PROGRAM

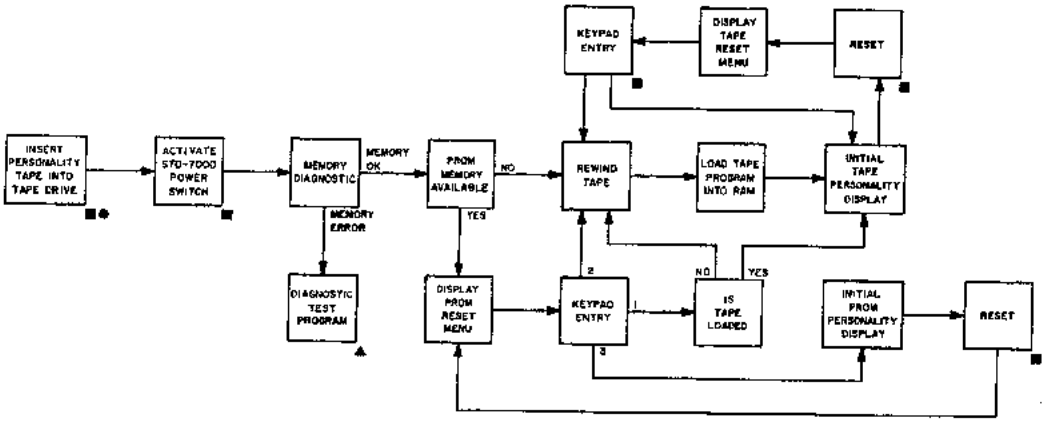
KEY IN:___

NOTE: Through an appropriate keypad entry, operator can load tape (if necessary) and restart tape program.

(b) Under PROM card operation

CRT will automatically display same RESET MENU described in paragraph (4)(a), and operator again has option of executing tape or PROM programs.

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■ STEPS REQUIRING OPERATOR ACTION.

● UNLESS UNIT IS EQUIPPED ONLY FOR PROM CARD OPERATION.

▲ CAUTION! TO BE PERFORMED BY QUALIFIED MAINTENANCE PERSONNEL ONLY.

Automatic Start-Up Routine (Sequence of Operation)
Figure 10

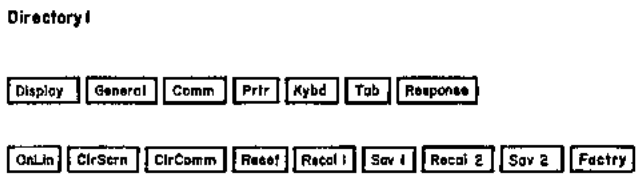
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E. Set-Up Mode

Set-Up Mode provides the operator a selection of terminal features to enable and save for future use.

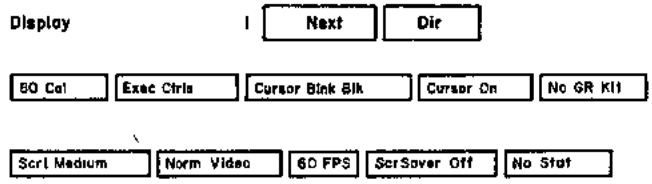
(1) Set-Up Mode Procedure

STEP	PROCEDURE
1	Press F3 key on Keyboard to display Directory Menu.

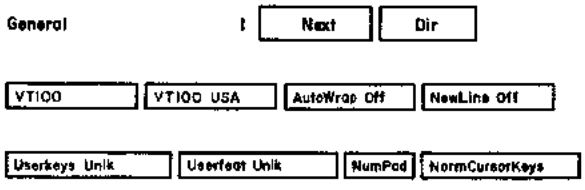


Directory Menu
Figure 11

2	Utilize keyboard keys and adjust if necessary for the following menus and features (refer to CRT Reference Manual for keyboard key identification and use):



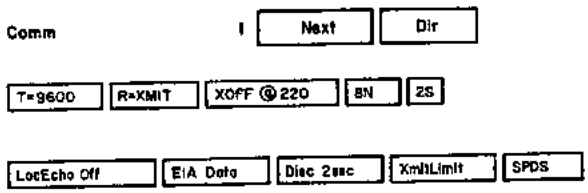
Display Menu
Figure 12



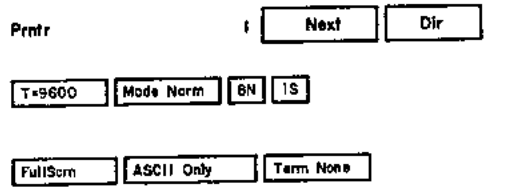
General Menu
Figure 13

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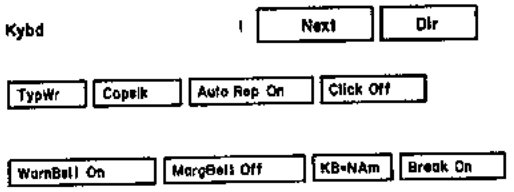
STEP PROCEDURE



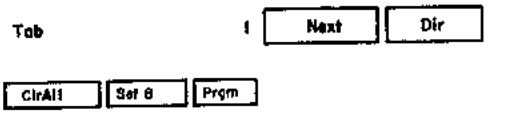
Comm Menu
Figure 14



Printer Menu
Figure 15



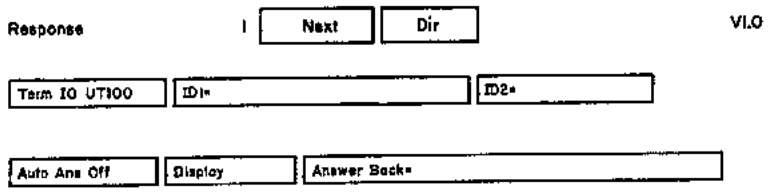
Keyboard Menu
Figure 16



Tab Menu
Figure 17

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STEP PROCEDURE



Response Menu
Figure 18

NOTE: Refer to Directory Menu and utilize SAV 1 function.

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F. Personality Display

(1) Menu Format

Two important objectives of the SDIS are:

(a) To display bus information in a simple and easily understood format.

(b) To permit data entry with a minimum of key strokes.

The menu format within the SDIS is structured so all data fields of a given bus are displayed on a CRT screen, with each field assigned a number. To change a field, the operator uses a numeric keypad to key in the number assigned to that field. This causes the CRT cursor to move to that field, permitting the operator to key in the desired new data.

(2) Reset vs. Personality Menus

Menus can be categorized into two basic groups:

1 Reset Menus

Reset menus (contained in STD-7000 firmware) are used only in performing start-up and/or maintenance operations. Examples of reset menus referenced in earlier sections are:

Diagnostic Test Program (1-2-3A)

Tape Reset Menu (1-2-3D)

PROM Reset Menu (1-2-3D)

2 Personality Menus

Personality menus (contained on magnetic tape or in PROM) reflect test information relative to specific application for which system is being utilized.

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(3) Personality Menus

Two basic types of menus (common to all personality displays, regardless of application) are used to display bus information within the STD-7000:

(a) Master Menu (Initial Personality Display)

This type of menu is displayed on Power-Up (subsequent to program loading) and when operator desires a change in the type of bus being displayed. Its only purpose is to serve as an index to other more detailed function control menus, which the operator will use to monitor bus activity. A typical master menu is shown in 1-2-3, Figure 19.

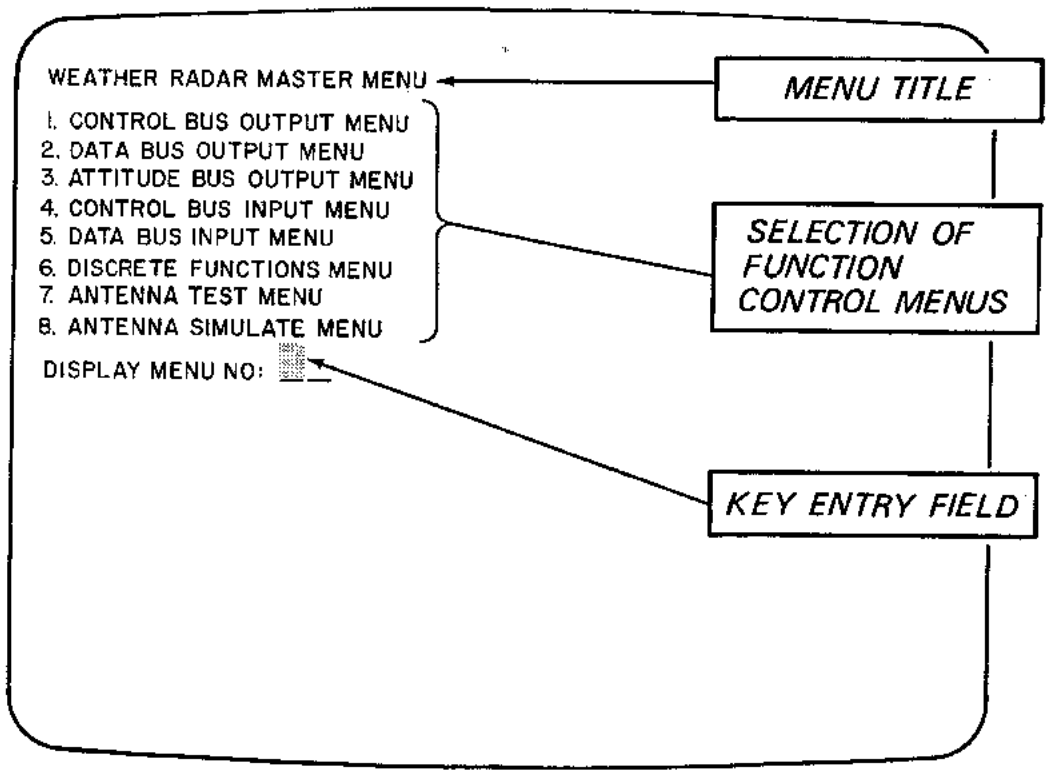
NOTE: All examples of menu displays shown on the ensuing pages, pertain to the WRX-7708 Weather Radar Test Program. Although specific menu content will vary from one test application to another, all menus exhibit the same common characteristics identified in the following menu displays.

(b) Function Control Menus

The Function Control menu is used to display specific status and control data pertinent to the test procedure being performed. All test parameters are formatted into clearly defined data fields, permitting simultaneous observation of all bus communication. A function control menu is selected for display by keying in the appropriate numerical code for that menu, as presented on the master menu. A typical function control menu is shown in 1-2-3, Figure 20.

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(4) Master Menu



Master Menu (Typical Display)
Figure 19

(a) Menu Title

Specifies the test application for which the Master Menu is being used.

(b) Selection of Function Control Menus

Provides the operator with a listing of function control menus available for display. Each function control menu is preceded by a number which is used to select that particular menu for display.

(c) Key Entry Field

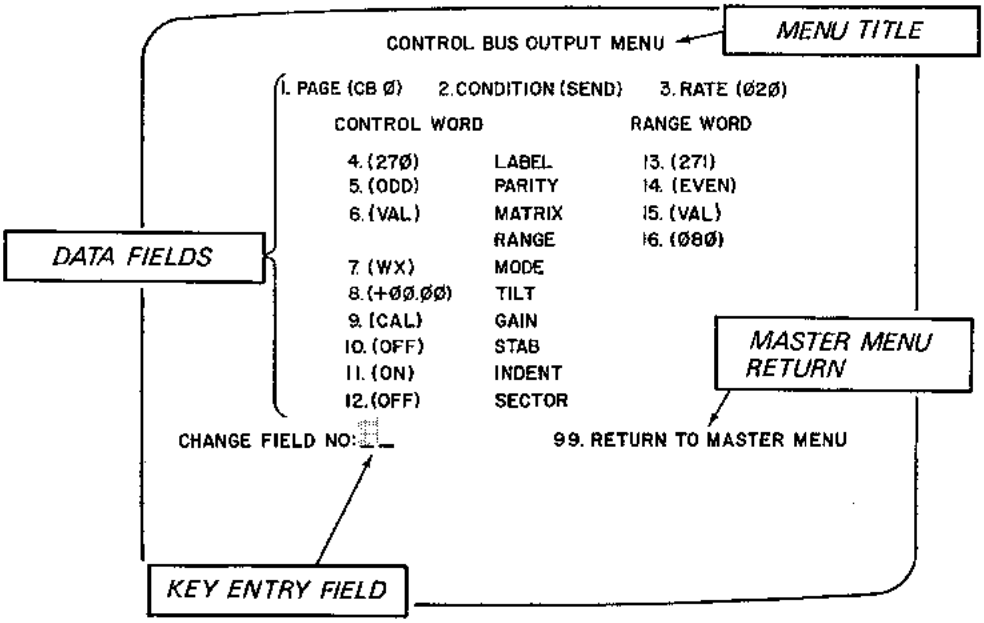
Entry position for number corresponding to (CRT Cursor) function control menu to be displayed.

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STEP	PROCEDURE
1.	Determine the function control menu to be displayed.
2.	Using numeric keypad, enter the number corresponding to the desired function control menu.
3.	Press ENTER key. Control Bus Output Menu will now be displayed (refer to 1-2-3, Figure 20).

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(5) Function Control Menu



Function Control Menu (Typical Display)
Figure 20

(a) Menu Title

Specifies the function control menu being displayed.

(b) Master Menu Return

A key entry of 99 allows the operator to return to the Master Menu from any function control menu.

(c) Key Entry Field (CRT Cursor)

Entry position for changing data fields or returning to Master Menu.

(d) Data Fields

A listing of specific test parameters, the values of which reflect prevailing test conditions and performance of the UUT.

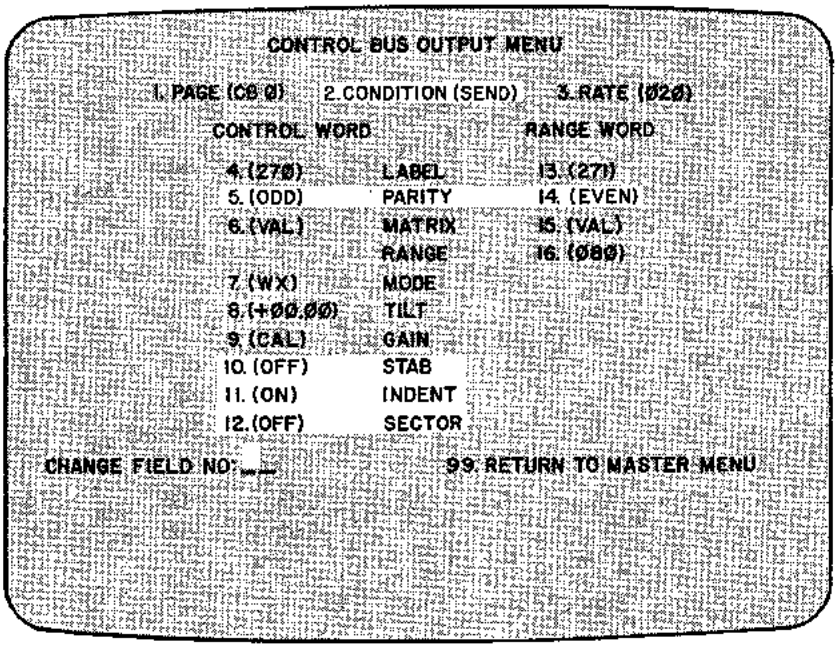
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(6) Data Fields (Identification and Manipulation)

Four basic types of data fields are used in most function control menus:

(a) Binary Data Fields

A binary data field is characterized as having only two states. Examples of binary data fields are highlighted in 1-2-3, Figure 21.



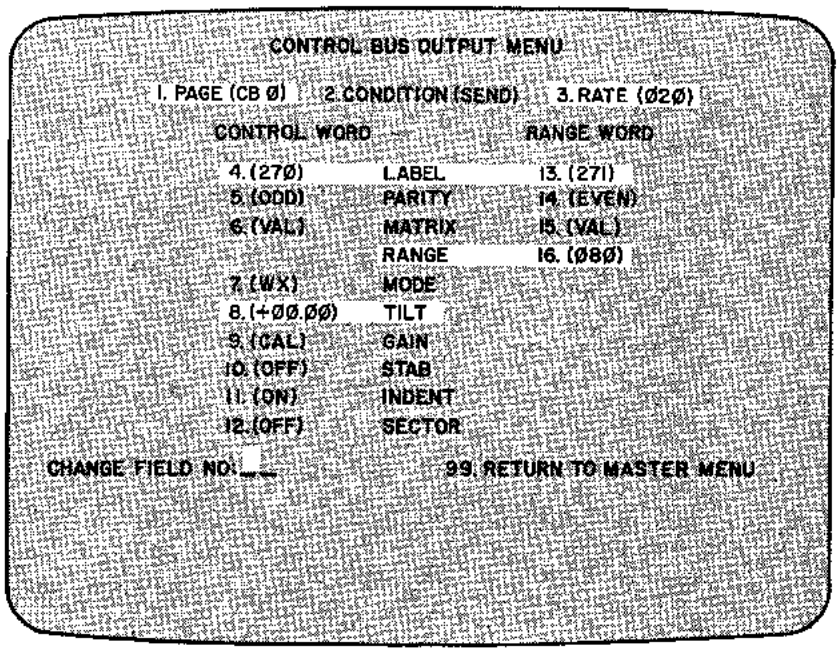
Function Control Menu (Binary Data Fields)
Figure 21

STEP	PROCEDURE
1.	Determine data field to be changed.
2.	Enter number of data field and press ENTER key. 1. The field will now automatically change to its opposite state.

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(b) Numeric Data Fields

Numeric fields contain numeric data only. Examples of numeric fields are highlighted in 1-2-3, Figure 22.



Function Control Menu (Numeric Data Fields)
Figure 22

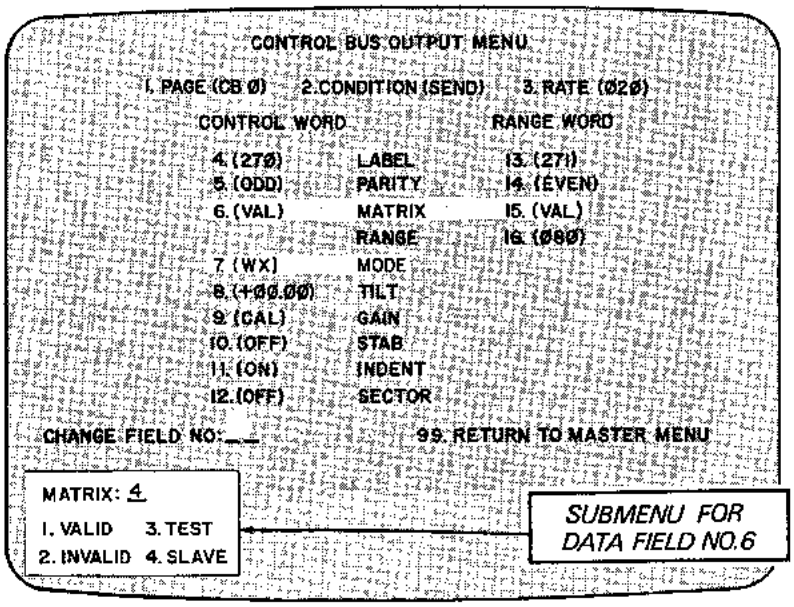
STEP	PROCEDURE
1.	Determine the data field to be changed.
2.	Enter number of data field and press ENTER key. NOTE: This will position CRT cursor within selected data field and all numeric data previously contained in the field will be erased.
3.	Key in desired new numeric data and press ENTER key). NOTE: Desired numeric data will now appear within data field.

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(c) Alpha Data Fields

Alpha fields are fields that may contain one of several words. Examples of alpha fields are highlighted in 1-2-3, Figure 23.

When an alpha field is changed, a submenu specifically for that field is displayed in the lower left corner of the CRT display. A submenu provides a choice of parameter conditions which can be entered within the selected alpha field.



Function Control Menu (Alpha Data Fields)
Figure 23

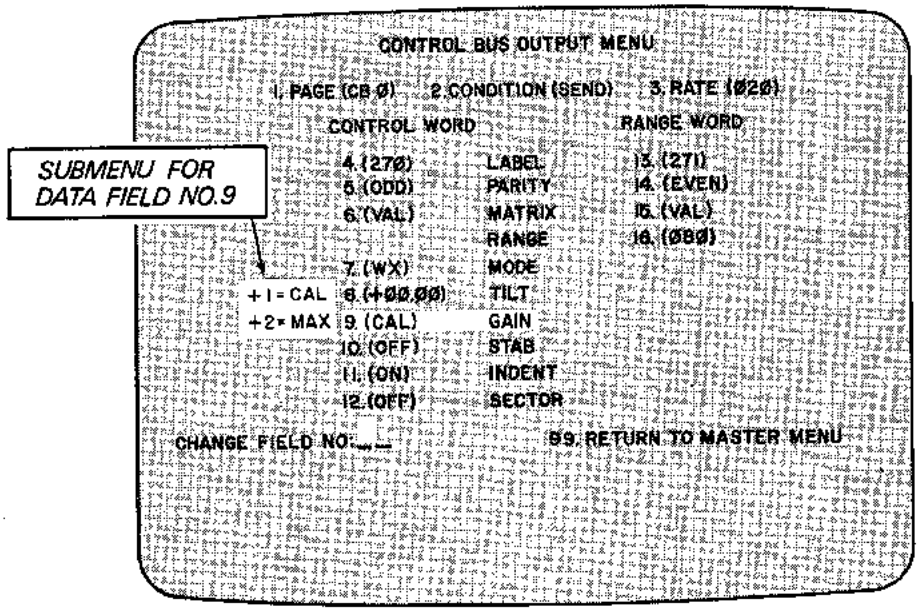
STEP	PROCEDURE
1.	Determine data field to be changed.
2.	Enter number of data field and press ENTER key. NOTE: A submenu for the selected data field will now appear in lower left corner of CRT display.
3.	From the choices provided on the submenu, determine which new parameter condition is to be entered into selected data field.
4.	Enter number corresponding to selected condition and press ENTER key.

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(d) Alphanumeric Data Fields

An alphanumeric data field is one that contains either words or numbers. An alphanumeric field is highlighted in 1-2-3, Figure 24.

When an alphanumeric field is changed, a submenu specifically for that field is displayed on the CRT.



Function Control Menu (Alphanumeric Data Fields)
Figure 24

STEP	PROCEDURE
1.	Determine data field to be changed.
2.	Enter number of data field and press ENTER key. NOTE: A submenu for the selected data field will appear on the CRT display (specific location of submenu on CRT display may vary).

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STEP	PROCEDURE
3.	The operator has two choices for entering new data: 1. Select one of several conditions provided on submenu and press ENTER key. 2. Enter numeric data subject to proper range and limits for the test parameter.

(7) Data Entry Format

All STD-7000 application programs feature an inherent error-checking capability which will aid operator in minimizing data entry errors. Any data keyed into a given data field must conform to specific format and/or value requirements for that particular field. Data not conforming to required input format is considered invalid, and as such will not be accepted. This becomes evident when operator attempts to enter invalid data by pressing ENTER key and the display automatically erases the invalid entry and the CRT cursor repositions itself at initial entry point of the field, awaiting a new and valid entry.

EXAMPLE #1: Test parameter LABEL requires all data entries to be in octal coding within a range of Ø to 377 and with no digit being larger than 7.

ENTRY	RESULT
426	INVALID; entry exceeds range limit of 377.
35.6	INVALID; decimal point not acceptable.
346	VALID; entry conforms to all input requirements.
285	INVALID; middle digit is greater than 7.

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EXAMPLE #2: Test parameter TILT requires an entry representing tilt angle of radar antenna. Numeric entry must be a multiple of .25 within a range of 15.75 and each entry must be preceded by a designation of polarity (+ or -).

ENTRY	RESULT
-15.02	INVALID; entry is not a multiple of .25.
+63.25	INVALID; entry exceeds maximum acceptable tilt angle of 15.75.
+14.75	VALID; entry conforms to all input requirements.

NOTE: Operator should refer to appropriate System Operation Manual for explanation of input formats required by data fields within that particular application.

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SECTION 1 - SERVICING

1. Preventive Maintenance

This section contains routine maintenance instructions for cleaning and inspecting the STD-7000 Bus Controller.

A. External Cleaning

(1) Clean front panel with a soft lint-free cloth. If soiled area is difficult to remove, dampen cloth with water. Use liguid detergent only if necessary.

(2) Remove Cooling Fan Filter from rear panel and remove dust with dry air jet. If dirt is difficult to remove, wash filter in warm soapy water and dry with dry air jet.

(3) Remove grease, fungus and/or ground-in dirt from surfaces with a soft lint-free cloth dampened (not wet) with denatured alcohol.

(4) Remove dust and dirt from connectors with a soft bristled brush.

(5) Clean wire leads with soft lint-free cloth.

(6) Paint exposed metal surface to avoid rust or corrosion.

B. Internal Cleaning

(1) Remove internal dust with hand controlled dry air jet of no more than 15 psig (1.054 kg/cm^2) and wipe internal case assembly parts and frame with soft lint-free cloth moistened with alcohol.

CAUTION: DELIBERATE OR ACCIDENTAL MOVING (HOWEVER SLIGHT) OF DISCRETE COMPONENTS ON CIRCUIT BOARDS, ETC. SHOULD BE AVOIDED.

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C. Visual Inspection

(1) Card Cage Assembly:

(a) Inspect tightness of subassemblies and all mounted equipment (including vertically installed PC Boards).

(b) Inspect for corrosion or obvious damage to metal surfaces.

(2) Circuit Boards:

(a) Inspect for corrosion or damage to connectors.

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1. Theory of Operation

A. Introduction

This section contains Theory of Operation for the major circuits within the STD-7000 Bus Controller. The circuit theory is presented on two levels and is organized as follows:

(1) Simplified Theory of Operation

Provides a simplified description of how each module interacts within the STD-7000 Bus Controller system. This description is based on the STD-7000 Simplified Interconnect Block Diagram (2-2-1, Figure 1), STD-7000 Detailed Block Diagram (2-2-1, Figure 3) and the STD-7000 Organizational Chart (2-2-1, Figure 2).

(2) Module Level Theory of Operation

Detailed description of the individual module circuit theory and functions relating to normal operation of the STD-7000. All module descriptions are based on the STD-7000 Detailed Block Diagram (2-2-1, Figure 3) and associated circuit schematics located in 2-2-7.

B. General

The STD-7000 Bus Controller is a programmable ARINC Bus Controller capable of controlling serial bus communications. All components within the unit are solid state. The primary function of this unit is to generate and receive ARINC 429/453 buses and display the contents of those buses on an optional CRT Display Terminal. In addition to its primary function as a bus controller, the STD-7000 also controls and activates a UUT through an interface device while monitoring selected discrete signals to determine UUT performance. The STD-7000 consists of a Power Supply, Cooling Fan, Mini-Tape Cassette Transport Assembly and a Card Cage Assembly with provisions for twelve plug-in PC boards. The basic module functions are described as follows:

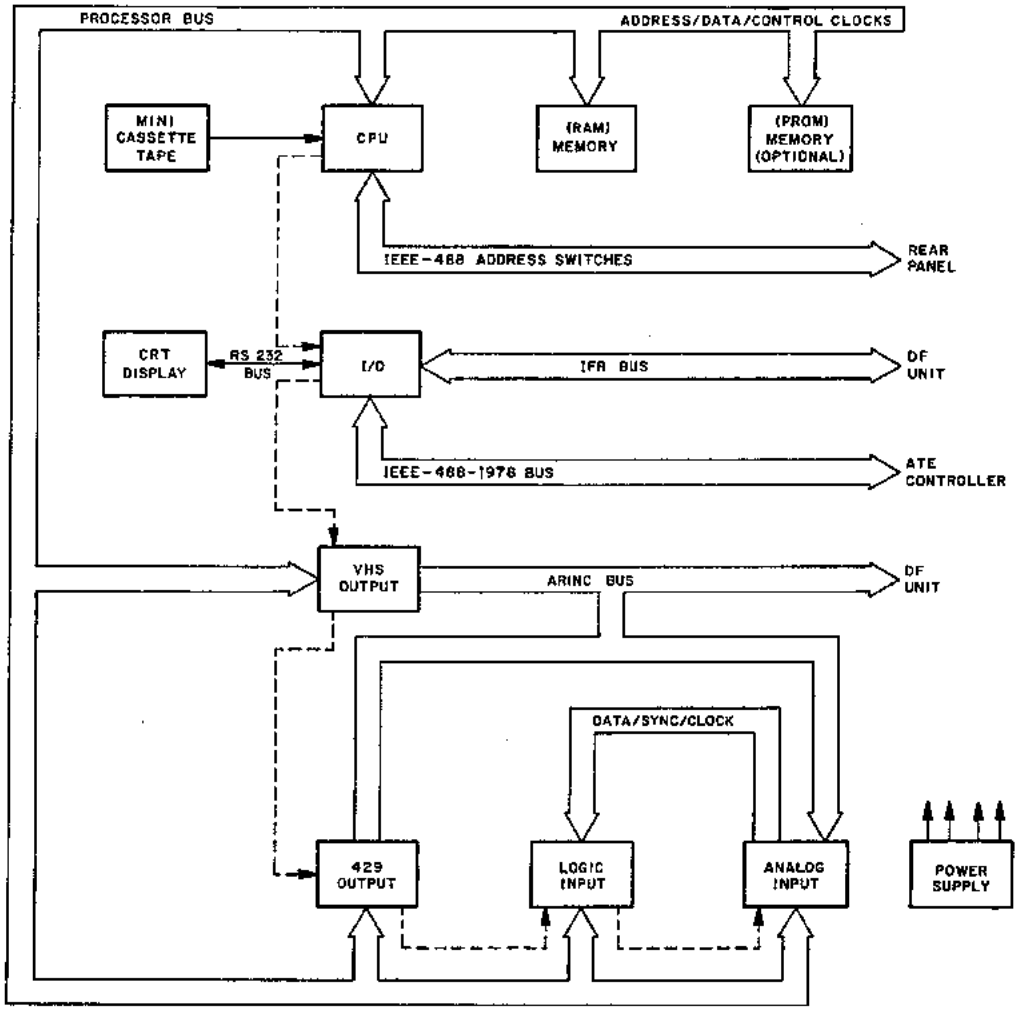
(1) Power Supply

Converts the AC input voltage to four DC voltages (+5 VDC, -5 VDC, +12 VDC and -12 VDC) which are distributed to the Mini-Cassette Transport and Card Cage Assemblies. AC power is available at the STD-7000 Rear Panel CRT Power Receptacle (J202) for use as a source of power for the operation of other equipment.

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(2) Cooling Fan

Provides cooling for internal components within STD-7000 Card Cage with external dust covers installed.

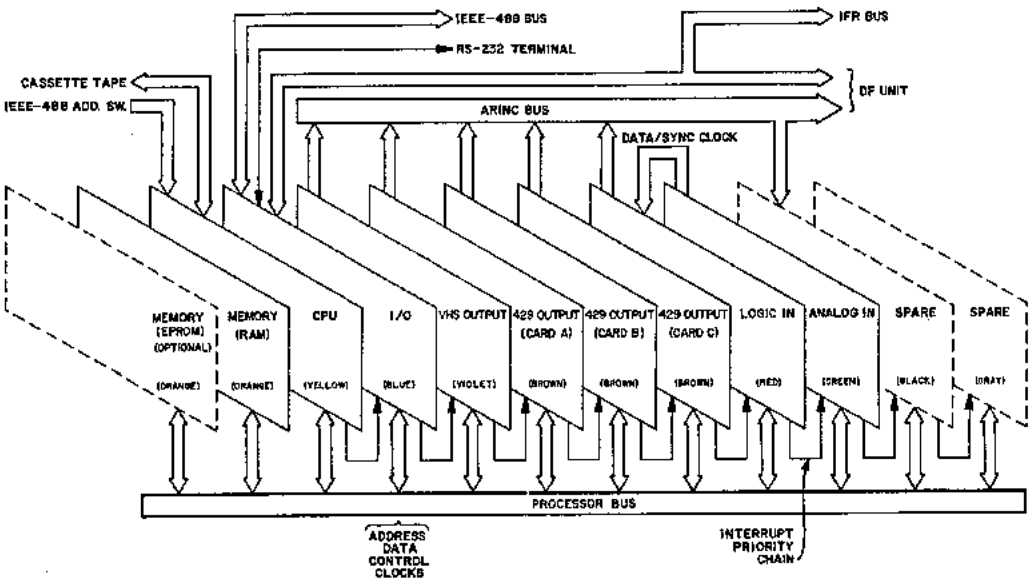


STD-7000 Simplified Interconnect Block Diagram
Figure 1

(3) Mini-Cassette Transport

Used as one source of STD-7000 software implementation. Once a prepared, certified, mini-cassette tape containing the desired application software is installed in the tape transport and the desired start-up routine has been selected, by positioning the IEEE-488 Address Switch (segments 7 and 8), the tape is ready and may be loaded into RAM memory. Once the tape is loaded in memory, the STD-7000 assumes a personality which enables it to execute program instructions according to instructions contained in the software. The tape transport also allows off-line storage of personality tapes as well as other non-pertinent data.

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STD-7000 Organizational Chart
Figure 2

(4) Card Cage Assembly

Consists of a Card Cage and Motherboard Assembly which contains the IFR Bus, ARINC Buses, IEEE-488 Bus, IEEE-488 Address Switch, Cassette Tape Transport Interface, RS-232C (CRT Display) Interface, Cooling Fan power source and DF (Discrete Functions) interconnect. The Motherboard contains provisions for twelve vertically installed, plug-in PC boards or cards (refer to 2-2-1, Figure 2). The cards may be installed in any slot within the card cage with the exception of the CPU and I/O cards. To prevent damage to the CPU and its peripherals, these two cards must occupy their assigned positions. For proper system operation, all slots between the CPU Card and last card in system (normally the Analog Input Card) must be occupied. The following cards are within the Card Cage Assembly:

(a) 16K EPROM Card

This optional card is primarily prepared for use in units under ATE control. When this card is installed, the Microprocessor will automatically access and display program information contained in PROM, if selected.

(b) 16K RAM Card

Used in conjunction with the Mini-Cassette personality tape to program the STD-7000 for a specific software application.

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(c) CPU Card

Contains the brain for controlling all the interface circuits and executes the program instructions which determine the usage of all I/O devices and CPU support devices.

(d) I/O (Input/Output) Card

Provides interface for the RS232C Bus (CRT Display Terminal), IFR Bus (Discrete Functions Unit or other IFR, Inc., compatible equipment) and the IEEE-488 Bus (GPIB).

(e) VHS Output Card

Provides interface for three VHS Buses, each having either a high or low speed VHS Bus output. The VHS Output Card maintains control over the VHS Buses with the CPU having the option of selecting either a high or low speed bus operation.

(f) 429 Output Card

Provides interface for two identical 429 Bus outputs to the ARINC Bus.

NOTE: Three 429 Output Cards are in use. Each card is jumpered for CPU identification.

(g) Logic Input Card

Deformats and buffers VHS (342) and 429 Bus inputs from the Analog Input Card.

(h) Analog Input Card

Provides multiplexing and line receiving of VHS and 429 Buses from the ARINC Bus.

C. Simplified Theory of Operation (Refer to 2-2-1, Figure 4)

(1) STD-7000

(a) Microprocessor Operation

The CPU or Microprocessor Card is the controller of the STD-7000. The CPU manipulates and controls all data to and from the appropriate buses at the expected time intervals, allowing successful STD-7000 operation. The Microprocessor is located on the CPU PC Board and

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communicates with the rest of the STD-7000 through a 100-pin connector on the Motherboard. The Microprocessor has sixteen address lines, eight data lines, seven control lines (including one read and one write strobe). On initial power-up, the Micro-processor performs a functional test of each card installed in the card cage. Upon completion of this functional check, the Microprocessor checks the Card Cage for the presence of an EPROM Card. If the EPROM Card is present, its program will automatically be executed, if selected, in accordance with the information contained in ROM. If the Microprocessor does not sense an EPROM Card, it will then load the program contained on magnetic tape, into RAM. After tape loading, the Microprocessor executes the tape program which determines the usage of the I/O devices and CPU support devices.

(b) Memory Operation

The STD-7000 contains provisions for a 16K RAM PC Board and/or the optional 16K EPROM PC Board. The CPU Card contains an additional 4K bytes of EPROM and 8K bytes of RAM. (Refer to Appendix E for RAM/PROM address locations)

(c) Card Cage Operation

The Card Cage contains the nucleus of the STD-7000. In the case of weather radar, a choice of two memory cards (RAM or PROM), a CPU Card, I/O Card, VHS OUTPUT Card, three 429 OUTPUT Cards, a Logic Input Card, and an Analog Input Card are used. Each card has been assigned a color coded slot within the Card Cage that produces the best operational characteristics for that particular card. The Processor Bus, which allows signal transfer of Address, Data and Control Clock input and/or output information (necessary for correct operation of each specified card), is located on the Motherboard. The Motherboard also contains the ARINC Bus, used for all 429 and 453 (VHS) Bus activities during communications with a UUT, via the DF unit. The Interrupt Priority Chain provides each card direct communication with the CPU, mostly consisting of command completion signals to provide

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the CPU freedom from a constant monitoring profile. This allows other functions in the protocol structure to be accomplished simultaneously. The 429 Bus data originates from one of three 429 Output Cards (depending upon how the access jumpers are installed) and the VHS Bus data originates on the VHS Bus Output Card. Both buses use the Logic and Analog Input Cards for interpretation, multiplexing and deformatting of signals. Received data is available to CPU from either or both Input Cards, when requested.

(2) CRT Interface

The CRT Interface filters the control codes from the STD-7000 and converts the control codes to the appropriate ANSII control codes for use with any standard ANSII terminal.

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CHAPTER TWO

STD-7000 STANDARD DIGITAL INTERFACE SYSTEM

MAINTENANCE MANUAL

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SECTION 5 - STORAGE

1. Please note the following storage precautions.

   A. No particular storage requirements are necessary during extended periods in which the Test Set will not be utilized.

   B. The following common sense practices should be done, however:

      (1) Disconnect the Test Set from any electrical power source.

      (2) Disconnect and store the AC power cable and any other accessories with the Test Set.

      (3) Cover the Test Set to prevent dust and debris covering and entering the Test Set.

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SECTION 4 - SHIPPING

1. The following information applies to shipping and repacking procedures for the STD-7000.

   A. Shipping Information

      IFR test sets returned to factory for calibration, service or repair must be repackaged and shipped subject to the following conditions:

      (1) Do not return any products to factory without first receiving authorization from IFR Customer Service Department.

      CONTACT: Customer Service Dept.
      IFR SYSTEMS, INC.
      10200 West York Street
      Wichita, Kansas 67215

      Telephone: (800)-835-2350
      TWX: 910-741-6952

      (2) All test sets must be tagged with:

      (a) Owner's Identification and address
      (b) Nature of service or repair required
      (c) Model No.
      (d) Serial No.

      (3) Sets must be repackaged in original shipping containers using IFR packing molds. If original shipping containers and materials are not available, contact IFR Customer Service Dept. for shipping instructions.

      (4) All freight costs on non-warranty shipments are assumed by customer. (See Warranty Packet for freight charge policy on warranty claims.)

   B. Repacking Procedure (Refer to 1-4-1, Figure 1)

      (1) Make sure bottom packing mold is seated on floor of shipping container.

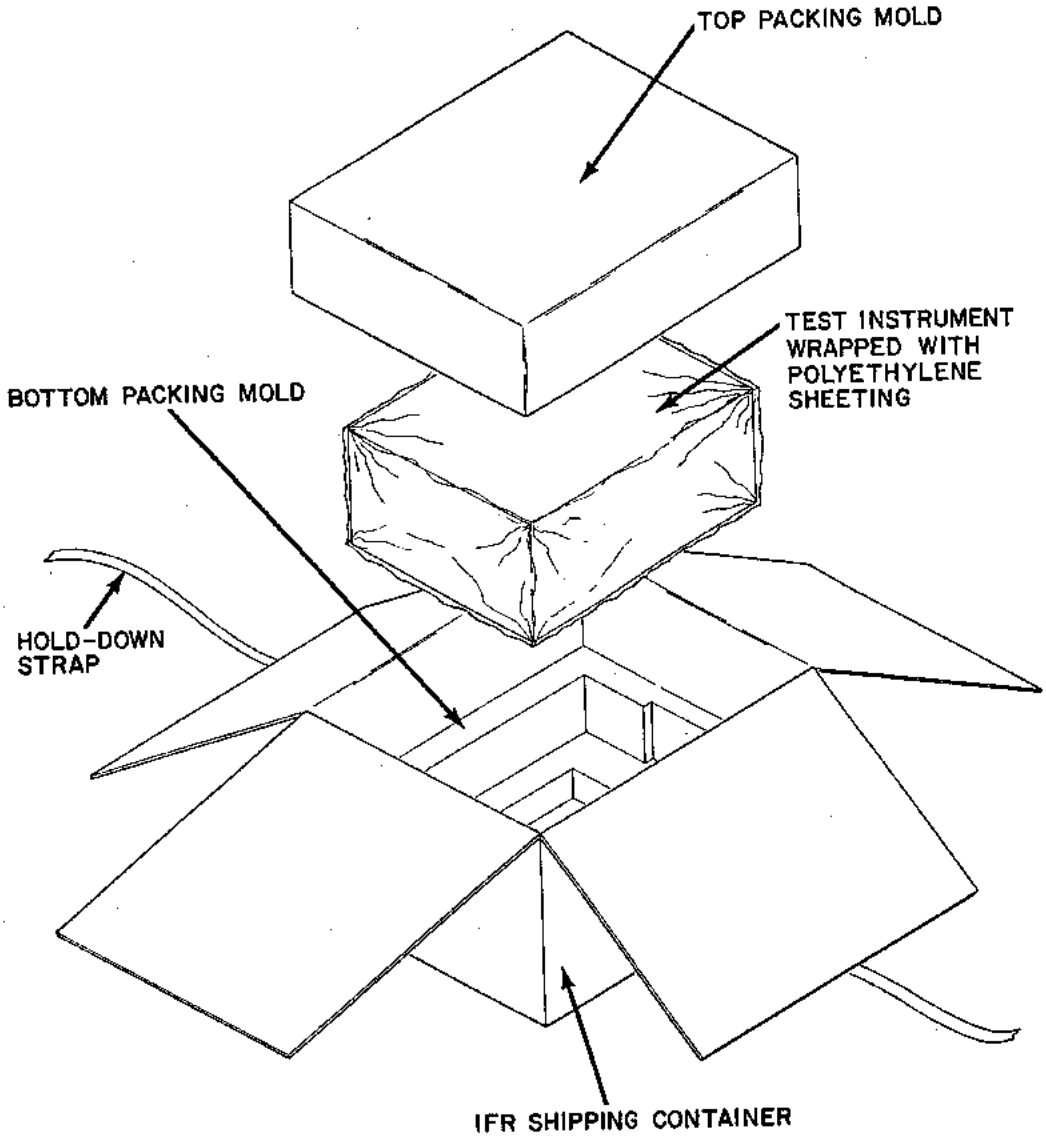
      (2) Carefully wrap test set with polyethylene sheeting to protect finish.

      (3) Place test set into shipping container, making sure set is securely seated in bottom packing mold.

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(4) Place top packing mold over top of set and press down until mold rests solidly on bottom packing mold.

(5) Close shipping container lids and seal with shipping tape or an industrial stapler. Tie all sides of container with break resistant rope, twine or equivalent.



Repacking Procedure
Figure 1

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(2) Model KP-72480 Keypad

Description: 16-key numeric Keypad; includes 10 numeric keys, two math operator keys (+,-), one decimal point key, one backspace key, one enter key and one shift key.

2. Following are the specifications for the CRT Interface:

A. Dimensions

(1) 8 X 8 X 4

B. Weight

(1) 8 lbs.

C. Power

(1) 105 to 205 volts AC
(STD-7000 switches if 240 VAC)

D. Operating Temperature

(1) 0 to 50 degrees C

E. Code Conventions

(1) Input - Ann Arbor Model 400E Control Codes.

(2) Output - ANSI Standard X3.64-1979 and X3.41-1974 Control Codes.

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D. Magnetic Tape Transport

Type:	Certified Cassette Transport
Read/Write Speed:	3 ips
Media:	Certified Digital Mini-Cassette
Data Rate:	2400 Baud
Formatted Data Density:	50K bytes per side
Number of Heads:	One
Tracks on Tape:	Two
Channels in Head:	One

NOTE: For further information concerning the CM-600 Mini-DEK (Digital Mini-Cassette Transport), address correspondence to:

BRAEMAR COMPUTER SERVICES, INC.
11400 Rupp Drive
Burnsville, Minnesota 55337
(612) 890-5135

E. Physical Characteristics

Dimensions	
Length:	16.125" (41cm)
Width:	16.31" (42cm)
Height:	6.75" (17cm)
Weight:	20 lbs Approx. (9,07Kg)
Power Requirements	
Voltage:	115 VAC (Standard) 230 VAC (Factory available by special order.)
Frequency:	60 Hz (Standard) 50 Hz (Factory available by special order.)

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Power Consumption:	100 Watts

Environmental Requirements

Temperature:	50° F to 113° F (Operating) -40° F to 160° F (Storage)
Humidity:	20% to 80% (Operating) 0% to 90% (Storage)

F. Optional Peripherals

(1) ESPRIT 6515 CRT Terminal

Screen:	14" (35.6 cm) diagonal, P31 (green) phosphor
Display Size:	7" (17.8 cm) X 9.4" (23.9 cm)
Character:	7 or 8 Bit; Odd, Even, 0, 1, or No Parity; 1 or 2 Stop Bits
Character Font:	7 x 9 dot matrix with 2 descenders ((80 col.) or 5 X 7 with 2 descenders (132 col.)
Dimensions:	Length: 13.0" (33 cm.) Width : 13.6" (34.6 cm.) Height: 13.8" (35 cm.) Weight: 21 lbs. (9.5 kg.)
Line Voltage:	97.75 to 132.25 VAC (115 V Nominal) or 195.5 to 264.5 VAC (230 V Nominal), Switch Selectable
Frequency:	47 to 63 Hz
Input Power:	50 Watts Maximum

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SECTION 3 - SPECIFICATIONS

1. Following are the specifications for the STD-7000 Standard Digital Interface System:

   A. Bus Characteristics

      (1) ARINC 429 (High & low speed I/O buses)

Number of Buses:	Six (6) programmable high speed and low speed I/O buses.
Low Speed Bit Rate:	Variable from 10 kHz to 15 kHz
High Speed Bit Rate:	100 kHz
Bus I/O Capabilities	
Output:	Selected or simultaneous operation of all 6 output buses; data content and transmission rate of each bus are individually programmable.
Input:	Selected operation of any one of six buses at any given time.
Buffering:	Buffering capability for a minimum of eight (8) ARINC 429 specified 32 bit words.
Message Transmission Rate:	Programmable from 0 to 255 messages per second, in minimum of 1 message per second increments.
Word Spacing:	Programmable in single bit increments.

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(2) ARINC 453 (Very high speed I/O buses)

Number of Buses:	Three (3)
Bit Rate:	1 MHz
Bus I/O Capabilities	
Output:	Selected or simultaneous operation of all 3 output buses; data content and transmission rate of each bus are identical.
Input:	Selected operation of any one of three buses at any given time.
Word Length:	Programmable from 1 to 2,048 bits.
Message Transmission Rate:	Programmable from 0 to 255 messages per second, in minimum of 1 message per second increments.

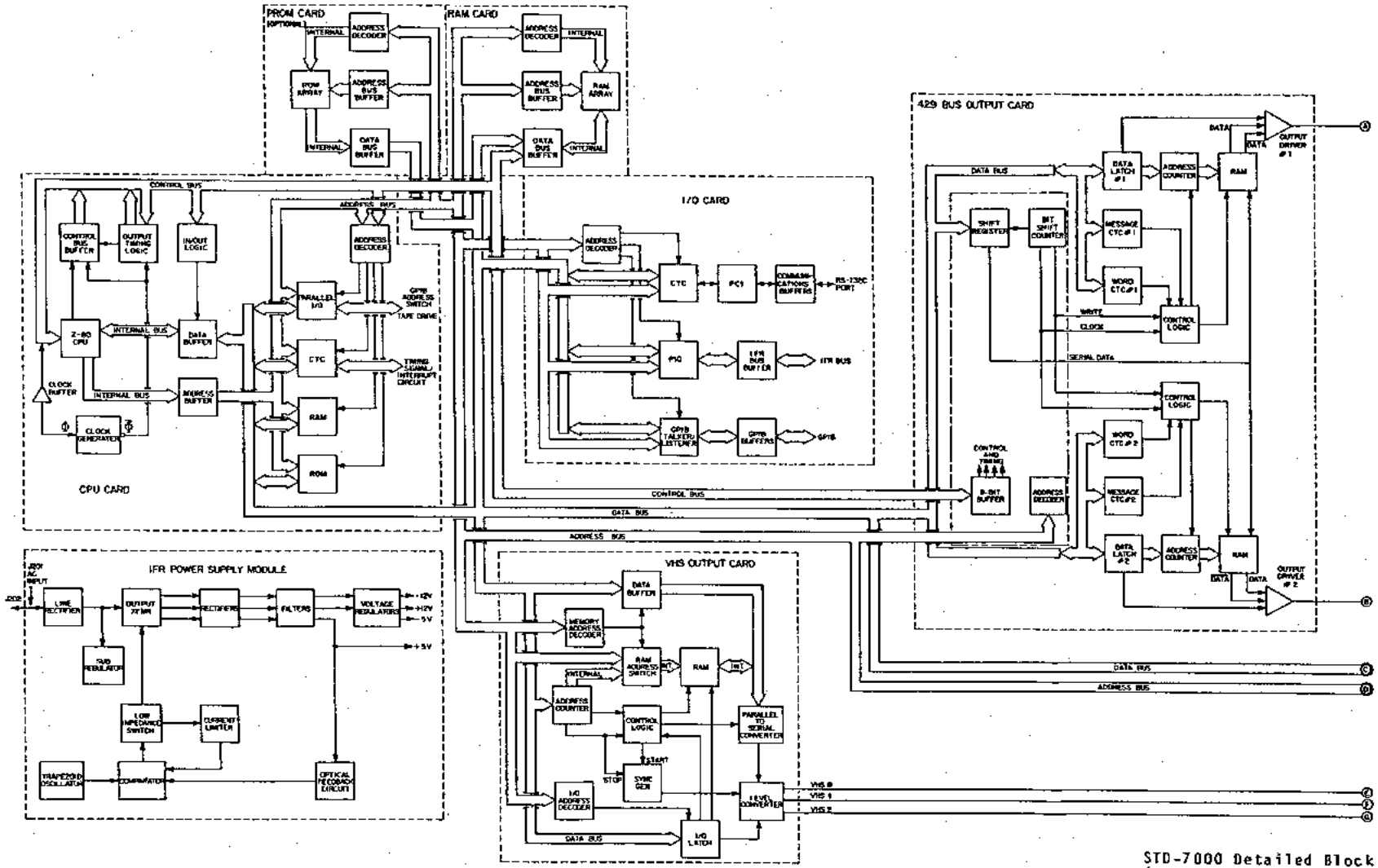
B. Rear Panel Interfaces

IEEE-488-1978:	One 24-pin GPIB connector as defined by IEEE Standard 488-1978.
EIA RS232C:	One 25-pin "D" type connector for optional CRT terminal.
IFR Auxiliary Bus:	One 25-pin "D" type connector for interfacing IFR test equipment.

C. Processor System

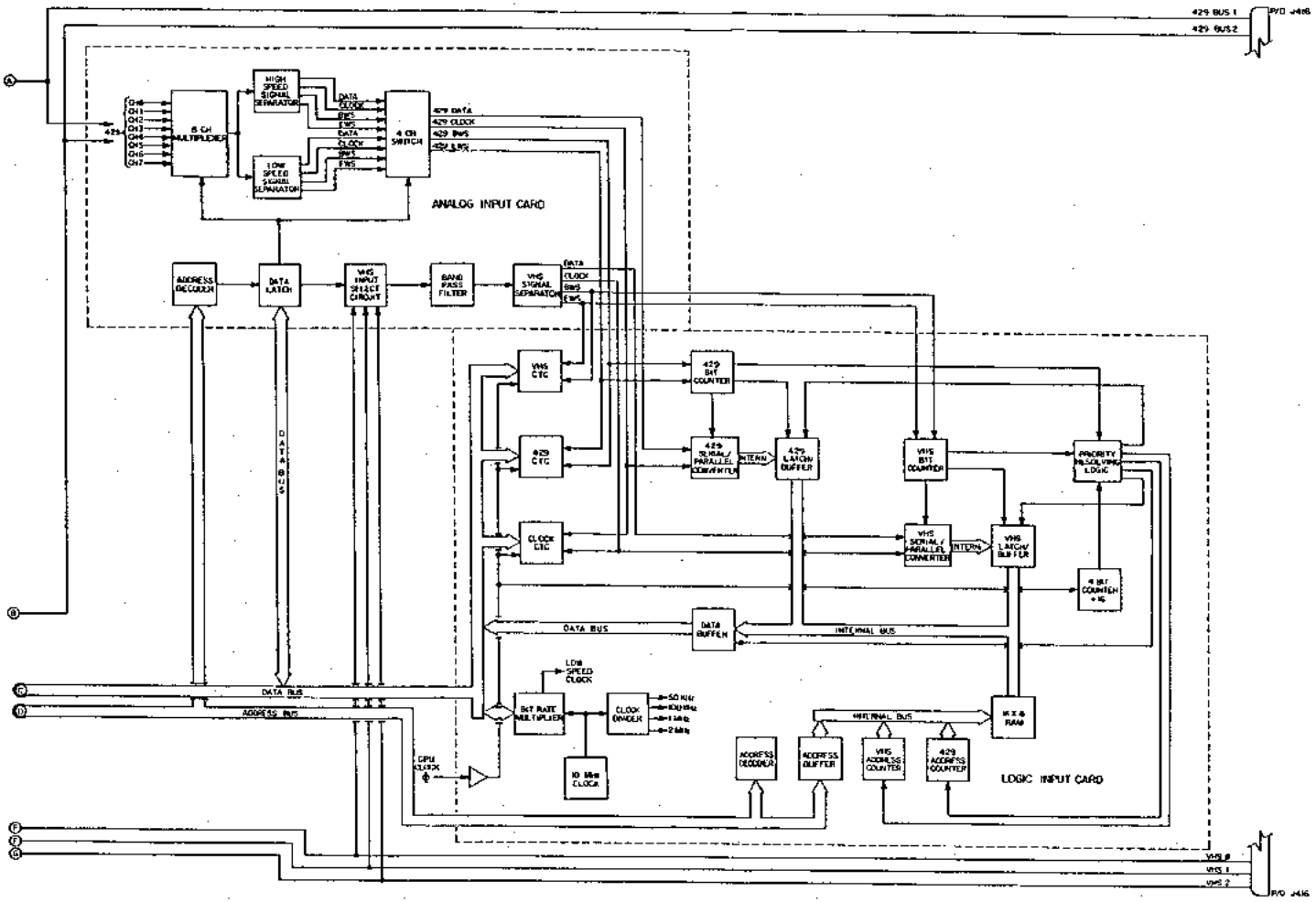
Microprocessor:	Z-80
Memory	
Max. Hardware:	40K RAM or 64K PROM
Max. Addressing:	64K RAM or 64K PROM

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STD-7000 Detailed Block Diagram
(Sheet 1 of 2)
Figure 3

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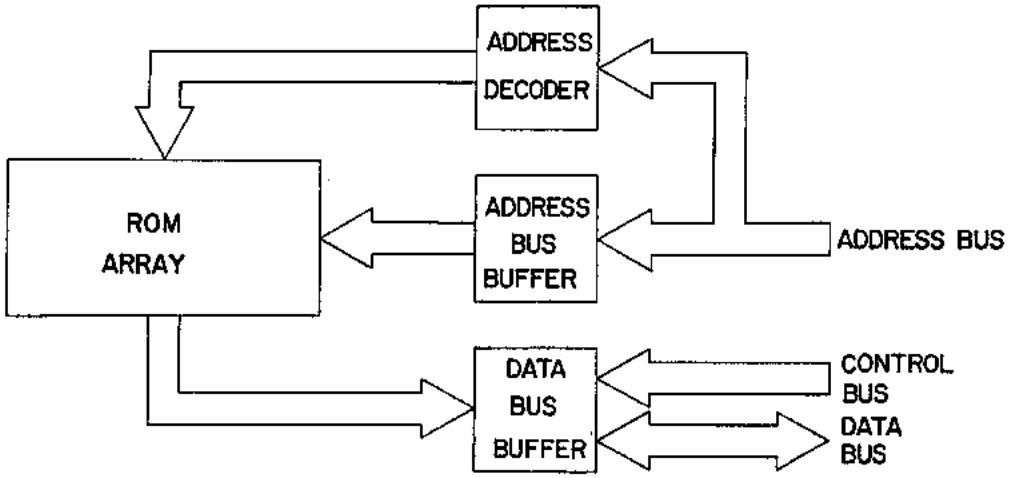


STD-7000 Detailed Block Diagram (Sheet 2 of 2)
Figure 3

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D. Module Level Theory of Operation

(1) EPROM Card - Optional (Refer to 2-2-1, Figure 4 and 2-2-7, Figure 85)



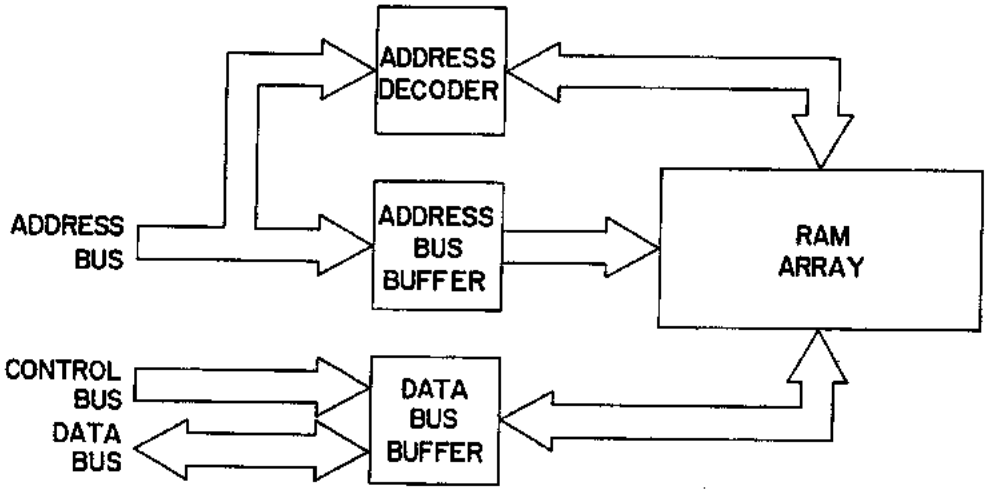
EPROM Card Block Diagram
Figure 4

The EPROM Card circuitry contains an Address Decoder, Address Buffer, Data Buffer and a 32K X 8 ROM Array.

The Address Decoder (X1219 thru X1223 plus X1225) is used to decode the address present on the Address Bus. X1219 selects either the high half or low half of the 32K Memory, as interpreted by jumpers which are provided to program the location of each half (16K each). X1220 and X1221 operate identically to X1222 and X1223. X1220 and X1222 decode and select any one 2K block of memory when required. The 2K block of memory jumpers (1-8) permit any 2K block of memory to be defeated, therefore freeing a 2K block of memory for use by another PC board within the system. X1221 and X1223 will enable the selected block of memory and their outputs join at X1225 to produce a Data Strobe that will occur if the selected 2K block of memory has its associated jumper installed. The Address Buffers (X1218 and X1224) isolate the Address Bus from the bank of 16 memory IC's. The Data Buffer (X1217) gates data to and from the Data Bus and also isolates the Data Bus from the band of 16 memory IC's. The 32K X 8 ROM Array (X1201 thru X1216) contains sixteen 2K X 8 EPROMs (P/N2716), each of which must be jumpered to +5V for proper operation.

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(2) RAM (Random Access Memory) Card (Refer to 2-2-1, Figure 5 and 2-2-7, Figure 86)



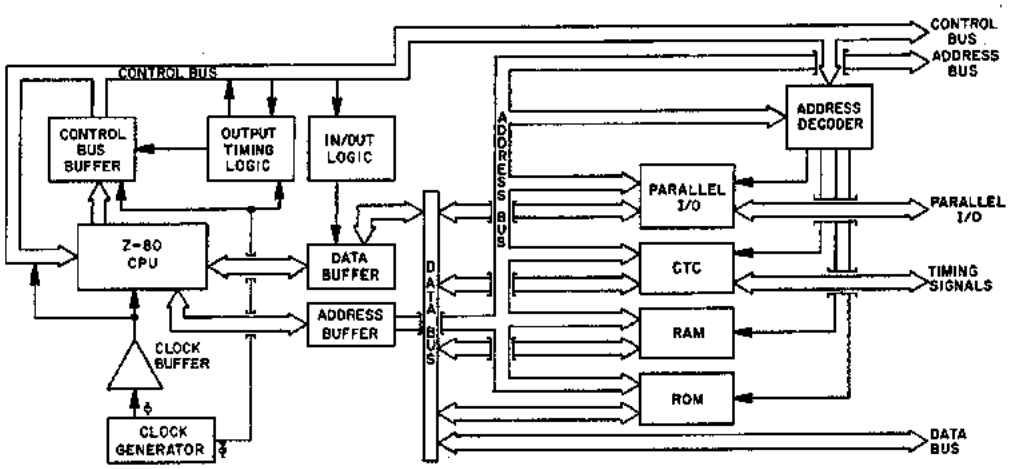
RAM Card Block Diagram
Figure 5

The RAM Card circuitry contains an Address Decoder, Address Bus Buffer, Data Bus Buffer and a 16K X 8 RAM Array.

The Address Decoder (X1102, X1103, X1106A and X1106B) decodes the address present on the Address Bus. The address information is used to select the appropriate 1K X 8-Bit Block of RAM. X1101 decodes the base address for the RAM PC Board which is jumper programmable to allow the installation of identical PC Boards on the same bus circuit without any address conflict. The 16K X 8 RAM Array consists of thirty-two, 1K X 4-Bit memory IC's (X1107 through X1138). Two IC's are used to form a 1K X 8-Bit Block of memory, thus sixteen 1K X 8-Bit Blocks are configured to represent a 16K X 8-Bit RAM. The address Bus Buffer (X1104) and the Data Bus Buffer (X1139) provide buffering between the bus lines and the thirty-two memory IC's.

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(3) CPU Card (Refer to 2-2-1, Figure 6 and 2-2-7, Figure 87)



CPU Card Block Diagram
Figure 6

The architecture of the CPU Card is structured around a Z-80 Central Processing Unit (CPU). This card contains 4K Bytes of EPROM, 8K Bytes of RAM, four 8-Bit parallel I/O ports, a Counter Timer Controller (CTC), the IEEE-488 Address Switch and Mini-cassette Tape Transport Interfaces otherwise known as Parallel Input/Outputs (PIO's).

The Clock Generator (9.9 MHz Square Wave Oscillator) is formed by X805B, X805E, X805F, X807 along with X801 and its associated components. The 9.9 MHz output of the oscillator is applied to a ÷4 Counter which produces a 2.475 MHz Square Wave Clock Signal (Φ). This square wave signal is then routed to the Clock Buffer (driver) and Clock Inverter (X805B) which inverts the square wave clock signal producing a $\overline{\Phi}$ signal for application to the Control Bus Buffer and Output Timing Logic. The Clock Buffer (X803, X802 and associated components) provides the necessary line driving for the Φ signal.

The 8-Bit Z-80 Microprocessor (X802) systematically repeats the cycle of retrieving (fetching) instructions from either the RAM or EPROM memory. It issues commands based on the information contained in these instructions to act on data, its peripherals, and/or itself (refer to Zilog 1981 Data Book for Z-80 CPU Timing information). The Control Bus Buffer (X821) provides buffering of the control signals between the CPU and Control Bus. The Address Buffer (X808 and X809), like the Control Bus Buffer, provides buffering

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between the CPU and Address Bus. The Data Bus Buffer (X820) gates data from the Data Bus to the CPU during an input (read) cycle or gates data from the CPU to the Data Bus during an output (write) cycle. The direction of this buffer is controlled by the In/Out Logic (X801A, X801B and X804B) which operates as an OR gate. This way, the state of its output is determined by the states of the $\overline{RD}$ and $\overline{M1}$ lines. The gate output will indicate an "in" condition during a read ($\overline{RD}$ active) or instruction fetch ($\overline{M1}$ active). An output condition indication is present at all other times.

The Output Timing Logic (X803C, X804A, X804D, X805A, X805D, X806 and Q801) controls the $\overline{WAIT}$ and $\overline{IORQ}$ lines and is provided to insure the I/O devices have sufficient time to respond to commands issued by the CPU. The Address Decoder (X818, X830 and X836) decodes the present address information on the Address Bus and selects the addressed circuit for communication with the CPU. Decoder X830 decodes address $0000_{(H)}$ thru $0FFF_{(H)}$ which is used to select EPROM operation. Decoder X818 decodes address $2000_{(H)}$ thru $3FFF_{(H)}$ which is used to select RAM operations, and Decoder X836 decodes $20_{(H)}$ thru $2B_{(H)}$ which is used to select the CTC and/or the Parallel I/O ports.

The EPROMs (X819 and X831) contain the CPU execution instructions and together contain 4K Bytes of EPROM collectively. Each EPROM may be completely erased by exposing them to an ultra violet light source.

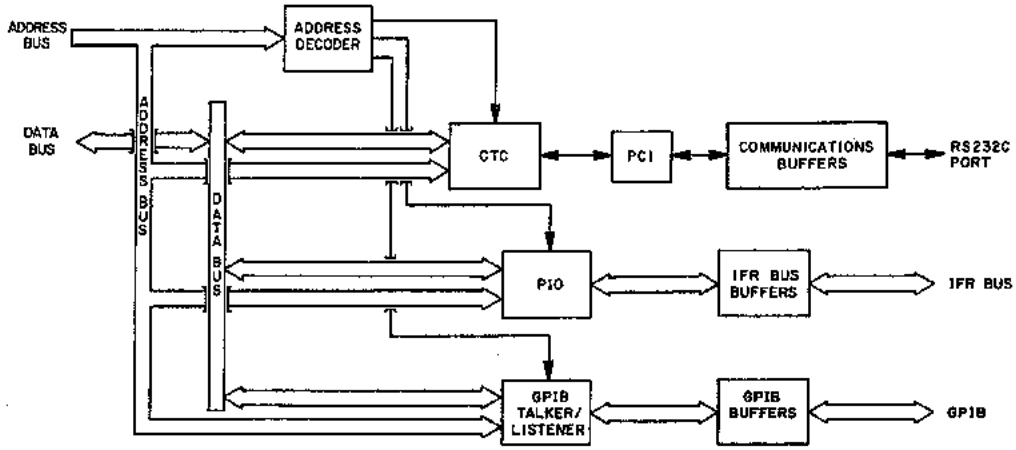
The RAM (X810 through X817 and X822 through X829) is used to store instructions, as well as data, from the Mini-cassette Tape Transport and scratchpad data information.

The Parallel I/O (X834 and X835) is software programmable and contains a handshaking feature (refer to Zilog 1981 Data Book for timing and programmable functions).

The CTC (Counter Timer Controller) has four programmable counter/timer circuits and prescalers that are used for general purpose timing applications (refer to Zilog 1981 Data Book for timing and programmable functions).

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(4) I/O (Input/Output) Card (Refer to 2-2-1, Figure 7 and 2-2-7, Figure 88).



I/O Card Block Diagram
Figure 7

The primary purpose of the Input/Output (I/O) Card is to interface the CRT Display Terminal (RS-232C), IFR Bus and IEEE-488 (GPIB) with the STD-7000 Bus Controller circuitry.

The Address Decoder (X1001 and X1005) decodes the I/O Address present on the Address Bus. Once an I/O address is decoded, the appropriate I/O circuitry (i.e. CTC, PIO or GPIB Talker/Listener) is enabled and directed to transfer data between itself and the CPU.

A Counter/Timer Controller (CTC) (X1009) generates the RS232C Baud Rate for use by the CRT Display Terminal. An additional responsibility for this CTC is to interrupt the CPU, either when the RS232C Transmitter has completed the transmission of a character or when an RS232C character has been received. These interrupts alert the CPU to either fetch the received character or supply the next character to be transmitted (refer to Zilog 1981 Data Book for timing and other data pertaining to the Z-80 CPU). The Programmable Communications Interface (PCI) (X1008) performs the RS232C coding and decoding functions (refer to INTEL 1980 Component Data Catalog for timing and other data pertaining to the 8251A component). The Communications Buffers (X1017 and X1018) provide buffering between the PCI and RS232C port. These buffers include a Line Receiver (X1017) and a Line Driver (X1018).

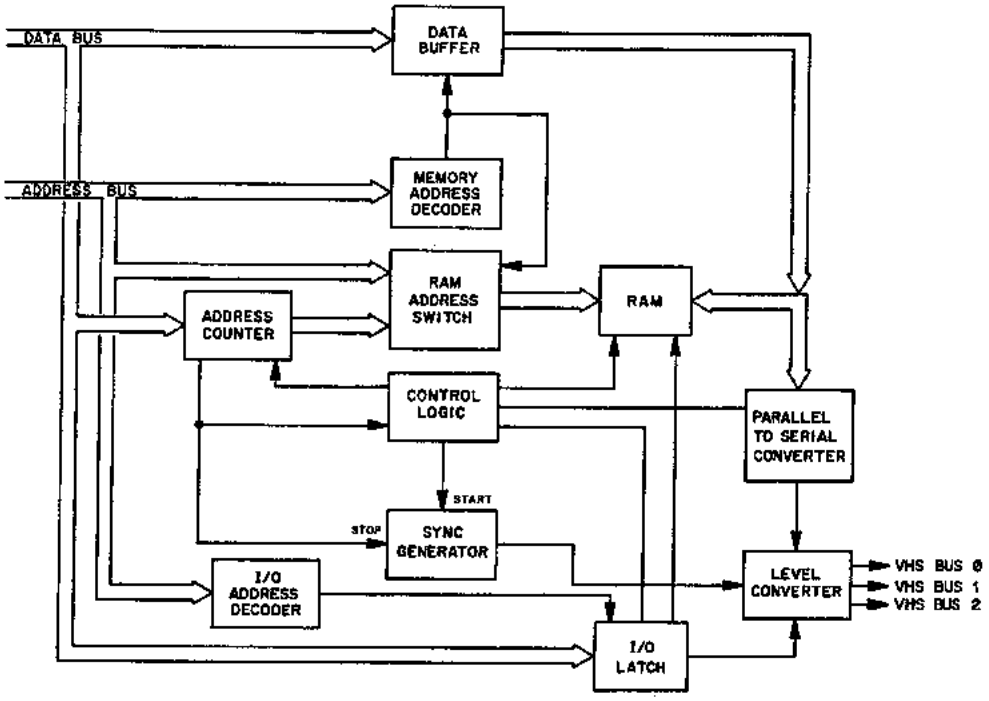
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A Parallel Input/Output (PIO) (X1007) circuit controls each IFR Bus function. The IFR Bus transmits data to and receives data from other compatible IFR, Inc. test equipment (refer to Zilog 1981 Data Book for timing and other electrical parameters of the Z-80 PIO).

The IFR Bus Buffer consists of a Single Direction Buffer (X1015) which is used to buffer the eight address lines on the IFR Bus and a Bidirectional Buffer (X1016) for buffering data lines.

The GPIB Talker/Listener (X1006) controls all GPIB transactions, including the serial to parallel/ parallel to serial conversions. In addition to these requirements, the GPIB Talker/Listener performs other GPIB protocol requirements, when necessary (refer to INTEL 1980 Component Data Catalog for additional information pertaining to the 8291 component). The GPIB Buffers consist of three Bi-directional Buffers (X1010 through X1012) and a Uni-directional Buffer (X1013). Each has a requirement to provide buffering between the GPIB and the GPIB Talker/Listener.

(5) VHS Output Card (Refer to 2-2-1, Figure 8 and 2-2-7, Figure 89)



VHS Output Card Block Diagram
Figure 8

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The VHS Output Card generates and sends Manchester II Bi-phase encoded VHS data to the Unit Under Test (UUT). This card has the capability of driving up to three VHS Output Buses with each bus capable of storing up to four word messages. Each word message may be up to 2000 bits in length and, as with word repetition rate, the word length is software controlled.

The RAM Memory Address Decoder (X728) controls the RAM Select (RAM SEL) line which will be low anytime a memory address between F8ØØ and FFFF appears on the Address Bus. When this line is active, the Data Buffer gates data to the RAM and additionally, the RAM Address Switch activates and allows the application of information on the Processor Address Bus to the RAM. On the other hand, when the RAM SEL line is inactive, the RAM is placed in a READ mode (read from RAM) and the Address Switch places the output of each of the Counters onto the RAM's Address Bus. An I/O Address Decoder (X727) decodes the addresses of the I/O Latch, Address Counter, and the CTC, within the Control Logic Network. The I/O Latch (X723) provides temporary storage for control data which is used to control the word length, word select, and VHS Bus Select. The Address Counter is a programmable up counter that generates the address for the RAM when the RAM SEL line is inactive. Software selection of the number of bits to be transmitted is accomplished by presetting this counter, via the Data Bus. The CTC within the Control Logic Network produces the start signal and also interrupts the microprocessor after receiving a Stop Sync signal (refer to Z-80 CTC Data Sheet for timing and programming data). An 8-Bit wide Address Switch (X725 and X726) selects between the output of the Address Counter and the output of the Processor Address Bus, and places the selected output into the RAM. The 8-Bit X 1024-Bit RAM (X715 and X716) contains 10 Address lines, eight of which are driven by the Address Switch and two are driven by the I/O Latch. Two of these lines select one of four words stored in 256 Byte boundaries within the 1K RAM. When the RAM is selected by the RAM Memory Address Decoder, the Data Buffer (X703) gates data from the Data Bus to the RAM. This action allows the Processor to write to this memory. When not selected, the Data Buffer remains in a tri-state configuration. A parallel to Serial Converter (X704) reads the RAM by converting an 8-Bit Byte into 8 Serial Bits of 1 µSec each. The Shift Register output of this converter is the NRZ Serial Data Stream minus the presence of any synchronization pulses. The NRZ data is converted to Manchester II Bi-phase encoded data by X710D (located

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within the Level Converter circuitry). X709A, X709C and X710A gate the serial data and/or sync signals into Latches (X711A and X711B), where the data is synchronized with a 2 MHz Clock signal. The latch outputs are applied to Level Converters (X720, X721 and X730) which allow TTL levels to drive the Output Transformers (T701, T702 and T703). Transformer output signals are controlled by Relays (K701, K702 and K703). These relays are driven by the I/O latch which commands them to either enable or disable VHS channels Ø, 1 or 2.

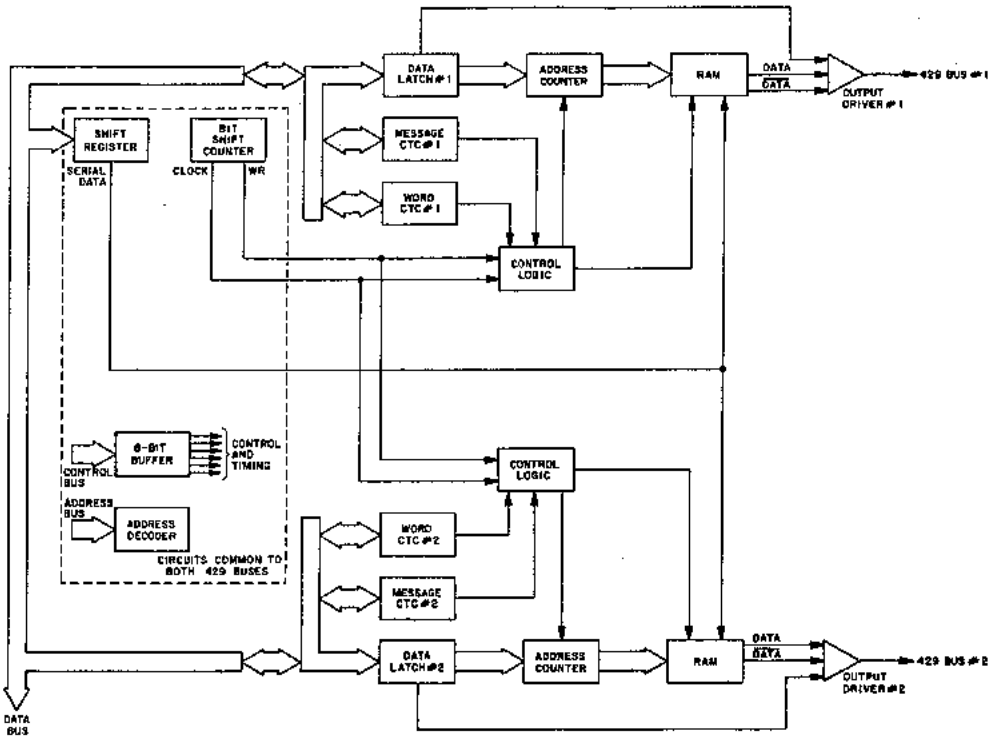
The Start Sync and End Sync signals are produced by the Sync Generator and are temporarily stored in two Flip-Flops (X708B and X718B). When the Line START from the CTC (in the Control Logic Network) becomes active, the start signal is synchronized with a 1 MHz clock signal within X708A. When either X708A or X718B is set, the Counter (X719) is enabled by X709B.

The Counter counts up to its terminal count (3 µSec) and the Flip-Flops are reset. The (Q2) output of the counter and the output of the Start Sync Flip-Flop are routed to an exclusive OR Gate (X710B). When the Start Sync Line is active, the counter output (Q2) is inverted producing a Start Sync signal (1.5 µSec high followed by 1.5 µSec low). When the Start Sync Line is inactive, a Stop Sync (End Sync) signal is assumed and X710B passes the output of the Counter (Q2) unaltered to the Level Converter. Flip-Flop (X718A) turns the Level Converter on at the beginning and off at the end of the VHS word-message.

The Control Logic starts the word transmission, clocks the Address Counter and loads the parallel to Serial Converter with the next byte from the RAM. A ÷16 Frequency Divider (X712 causes the Address Counter to clock at 8 µSec intervals. The programmable inputs are used to yield a 1-Bit resolution of the word length (the Address Counter can only address 8-Bit Bytes). The Load signal for the Parallel to Serial Converter is produced by X707, X709C and X722D.

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(6) 429 Bus Output Card (Refer to 2-2-1, Figure 9 and 2-2-7, Figure 90)



429 Bus Output Card Block Diagram
Figure 9

A 429 Bus is a 3-State Serial Bus defined as having a positive voltage represent a logic 1 indication, a negative voltage represent a logic 0, and a zero volt or ground potential existing for ½ bit cell time (the time element required between bits). A 429 Bus message may consist of several words. The number of words, as well as the message repetition rate are software programmable.

The 429 Bus Output Card is configured with two 429 Buses (#1 and #2 on the same card). Design and operation of each is identical, therefore only Bus #1 is described in the following paragraphs. Both buses use the same common use circuitry consisting of an 8-Bit Octal Buffer, Address Decoder, a Shift Register and Bit Shift Counter. Since their outputs and effects on the system are identical, it should be understood that in any particular situation (other than normal), either 429 Output Card may be substituted for the other simply by changing jumper configuration as shown in Section 9. Since the common use circuitry applies to both buses, they are discussed first.

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(a) Common Use Circuits (Refer to 2-2-1, Figure 9)

An 8-bit Octal Buffer (X937) buffers all Control Bus signals. Q909 and Q910 provide additional buffering for the microprocessor clock signal (Φ). The Address Decoder (X935 and X936) enables any device that has an address present on the Address Bus. Decoder X935 is jumper programmable, meaning that installed jumpers determine which block on the STD-7000 Memory Map (see Appendix H) is used for a particular 429 Bus Output PC Board. The use of jumper programming eliminates any address conflicts and allows the use of more than one 429 Bus Output Card in the STD-7000. Decoder X936 enables the following devices when their applicable address is on the Address Bus:

Message CTC #1	Message CTC#2
Word CTC #1	Word CTC #2
Data Latch #1	Data Latch #2
Output Driver #1	Output Driver #2
Shift Register	
8-Bit Shift Counter	

The 8-Bit Shift Counter (X931A, X931B, X932, X929C and X929D) completes multiple operations when enabled. Flip-Flop X931B initiates (starts) and terminates (stops) the counting process. It is set (started) when a byte is loaded into the Shift Register and stopped (reset) when the Counter (X932) reaches its terminal count. Flip-Flop X931A synchronizes the start of Counter X932 with the microprocessor clock signal. At this time, the Counter counts up sixteen counts, with a shift occurring at every other clock cycle, yielding eight shifts. The least significant counter bit is applied to X929C and X929D which together produce memory timing signals. The write pulse is produced by X929D, and X929C produces an address increment pulse immediately following the write pulse. This address increment pulse will advance the RAM Address Counter (X910 and X911). The 8-Bit Shift Register (X934) converts parallel information to a Serial Data Stream before it is committed to a section of memory. In other words, the byte to be written into memory is placed into the Shift Register which converts it to Serial Data, and when clocked by the Bit Shift Counter, sends the Serial Data Stream to the appropriate block of memory.

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(b) 429 Bus Output Circuit (Refer to 2-2-1, Figure 9)

The Message Repetition Rate and the number of words per message are controlled by the Message CTC (X901). The Word Length and between word gap are controlled by the Word CTC (X902). The Word CTC also informs the Message CTC when the transmission of a word has been completed. This action permits the Message CTC a means of keeping track of how many words remain to be sent (reference the Z-80 CTC Data Sheet for timing and other pertinent data pertaining to either CTC device). The output of Flip-Flop X923A is sent to the CMOS Switch (X912), NAND Gate X922B and NAND Gate X922D.

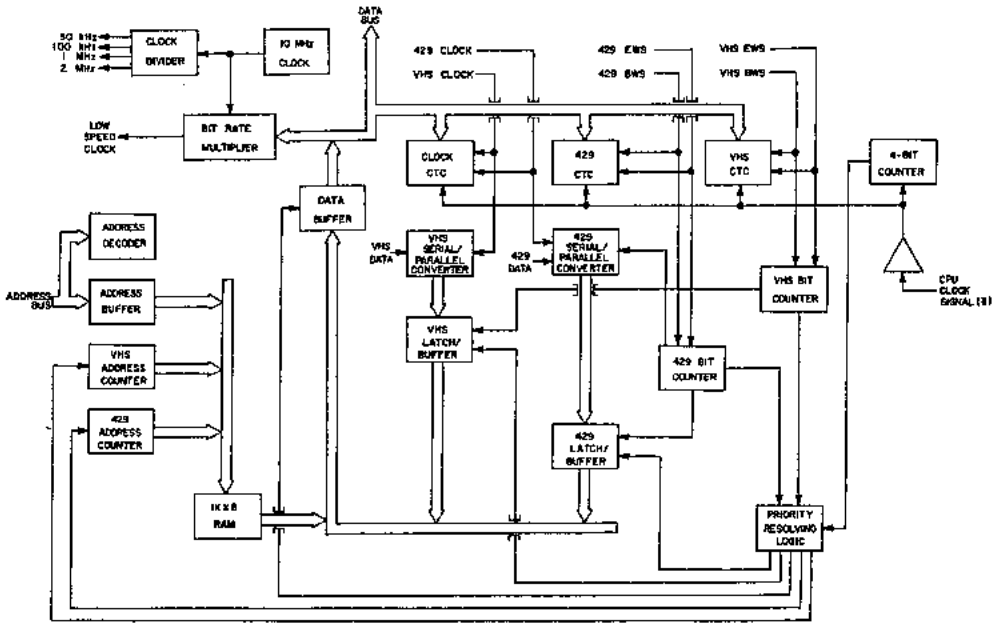
The CMOS Switch gates the selected Baud Rate to the Address Counters. NAND Gate X922B gates selected pulses to the Word CTC, and NAND Gate X922D gates the selected Baud Rate to NOR Gates X907A and X907D. The latter gates the data from the memory block with the Baud Rate Clock pulse before applying the data to the Output Driver. When the count of the pulses into the Word CTC reaches the word length, the Word CTC resets Flip-Flops X923A and X923B and also signals the Message CTC that a word has been sent. The Word CTC will then insert the between word gap and reset Flip-Flop X923B once again to complete the cycle. After all the words have been sent, the Word CTC resets X918C and X918D which stops the transmission of the message.

The Address Counter (X910 and X911) increments the RAM Address each time a pulse is received from X912 of the Control Logic. This counter may be preset to select any word in the memory. The RAM (X906) is a 1024-Bit X 1-Bit memory that stores data to be transmitted. During a memory Read operation, data is clocked out to X904A and X904D. The Serial Data Stream is written into the RAM by the Shift Register during a memory write operation.

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The Output Driver (X933B, X933C, X916A, X916B, X916C, X916D, X921, Q901, Q902, Q903, X904, K901 and associated circuitry) is used for low speed operation. The CMOS Switches (X933B and X933C) add an additional 470pF of capacitance during low speed operation to reduce the slew rate. The Unity Gain Buffers (915B and 916A) pro-vide a low impedance path for the Summing Amps (X915A and X916B). Q901, Q902, Q903 and Q904 buffer the output of the Summing Amps before it is sent to Relay K901. X921B controls Relay K901 when signals are received from the Microprocessor Bus. When X921B is set, Relay K901 is energized, placing the selected bus circuits on line.

(7) Bus Input Logic Card (Refer to 2-2-1, Figure 10 and 2-2-7, Figure 91)



Bus Input Logic Card Block Diagram
Figure 10

The Bus Input Logic Card converts the VHS (453) or 429 Bus Serial Data to Parallel Data and stores this data in a 1K X 8 Buffer Ram (capable of being read by the Microprocessor). This card also produces and contains clock circuits for the Bus Input Analog Card.

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The Address Decoder Circuit (X629 and a gate each of X614 and X615) selects one of the following devices when either of their addresses is present on the Address Bus:

VHS Z-80 CTC
429 Z-80 CTC
CLOCK Z-80 CTC
Bit Rate Multiplier

NOTE: Only one of these devices is selected and permitted to communicate with the microprocessor at any given time.

The 429 Z-80 CTC (X626) performs the same functions for the 429 Buses as the VHS Z-80 CTC (X613) performs for the VHS Buses (for electrical timing and programming information, refer to Z-80 CTC Data Sheet). The 429 and VHS Z-80 CTC's perform the following three functions:

1. Interrupt microprocessor when EWS (End Word Sync) is present.

2. Count words over a given amount of time.

3. Control the number of words per message.

The Clock CTC (X627) counts the number of bits per word for both the VHS and 429 Buses. The Bit Rate Multiplier (X623, X624, X625, X639 and X640) produces the Low Speed VHS Clock Signal. The Data Latch (X639) is loaded with the bit rate (from the Data Bus), when selected by the Address Decoder. The data output of the Data Latch and a 10 MHz Clock signal from the 10 MHz Oscillator are sent to two 4-Bit Rate Multipliers (X625 and X640). The 10 MHz Oscillator (Y601 and three gates of X611) produces a 10 MHz Square Wave with a duty cycle of approximately 50%. Each Bit Rate Multiplier output is between 0 and 9.9 MHz, in 100 kHz steps, as determined and controlled by BCD data stored in the Data Latch. The signal (0 to 9.9 MHz) is sent to the divide-by-five (÷5) stage of X624, decreasing it to between 0 and 1.98 MHz which can be read at pin 9. This output signal is then applied to a divide-by-one hundred (÷100, formed by ½ of X623 and X624) to further decrease it to between 0 and 19.8 kHz. This signal is the Low Speed VHS Clock.

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The 10 MHz Clock Square Wave Signal (from the 10 MHz Oscillator) is also sent to the Clock Divider (X612, ½ of X613 and X624). The 10 MHz Clock signal enters at pin 12 on ½ of X612 (configured as a ÷5/÷2 Counter) where it is decreased to 2 MHz (available at pin 10) and further decreased to 1 MHz (available at pin 13) before being returned to the other half of X612 (configured as a ÷10 counter) to produce 100 kHz (available at pin 3). This 100 kHz Square Wave is sent to the ÷2 stage of X624 where it is further decreased to 50 kHz (available at pin 13). Each output signal, 2 MHz, 1 MHz, 100 kHz and 50.0 kHz is used by the Bus Input Analog Card.

The VHS Bus Serial to Parallel Converter (X621) shifts each VHS bit into an internal 8-Bit Register, and once all eight bits are loaded, they are transferred in parallel to the VHS Latch/Buffer (X636). This cycle will repeat itself until all data is transferred, however all data stored in the VHS Latch/Buffer must be transferred before the next eight bits can be latched.

The VHS Counter (X604, X608 and X609) is synchronized with the BWS (Beginning Word Sync) so that after every eight bits, the VHS Bit Counter generates a strobe causing the VHS Latch Buffer to store the contents of the 8-Bit Shift Register. Additionally, the counter signals the Priority Resolving Logic Network that a byte needs to be transferred from the VHS Buffer/Latch to the 1K X 8 RAM.

The 429 Bus Serial to Parallel Converter (X638) shifts each 429 bit into an internal 8-bit Register. Once all eight bits are loaded, they are transferred in parallel to the 429 Latch/Buffer (X637). This cycle will repeat itself until all data is transferred, however all data stored in the 429 Latch Buffer must be transferred before the next eight bits can be latched.

The Data Buffer (X630) gates data from the 1K X 8 RAM to the Processor Bus when directed by the Priority Resolving Logic Network. The 1K X 8 RAM (X633 and X634) stores the data bytes received from the respective latch until the entire word is received. This data is retrieved by the microprocessor when the CPU is interrupted by the EWS (End Word Sync). The VHS and 429 Bus Data are kept in separate memory by the RAM address locations assigned to each.

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The VHS Bus Address Counter (X617, X618 and X631) and 429 Bus Address Counter (X619, X620 and X632) operate in the same manner. An 8-Bit Counter (X617 and X618, or X619 and X620) is incremented each time a byte has been transferred from the VHS or 429 Bus Latch/Buffer. The address from the Address Counter is gated to the 1K X 8 RAM by X631. The Address Buffer (X630) gates the address from the Processor Address Bus to the 1K X 8 RAM's Address Bus when required.

The 4-Bit Counter (X601 and X602) controls the Priority Resolving Logic Network. This counter divides its output into time slots which are derived from the CPU Clock signal. The time slots determine which circuit has access to the 1K X 8 RAM.

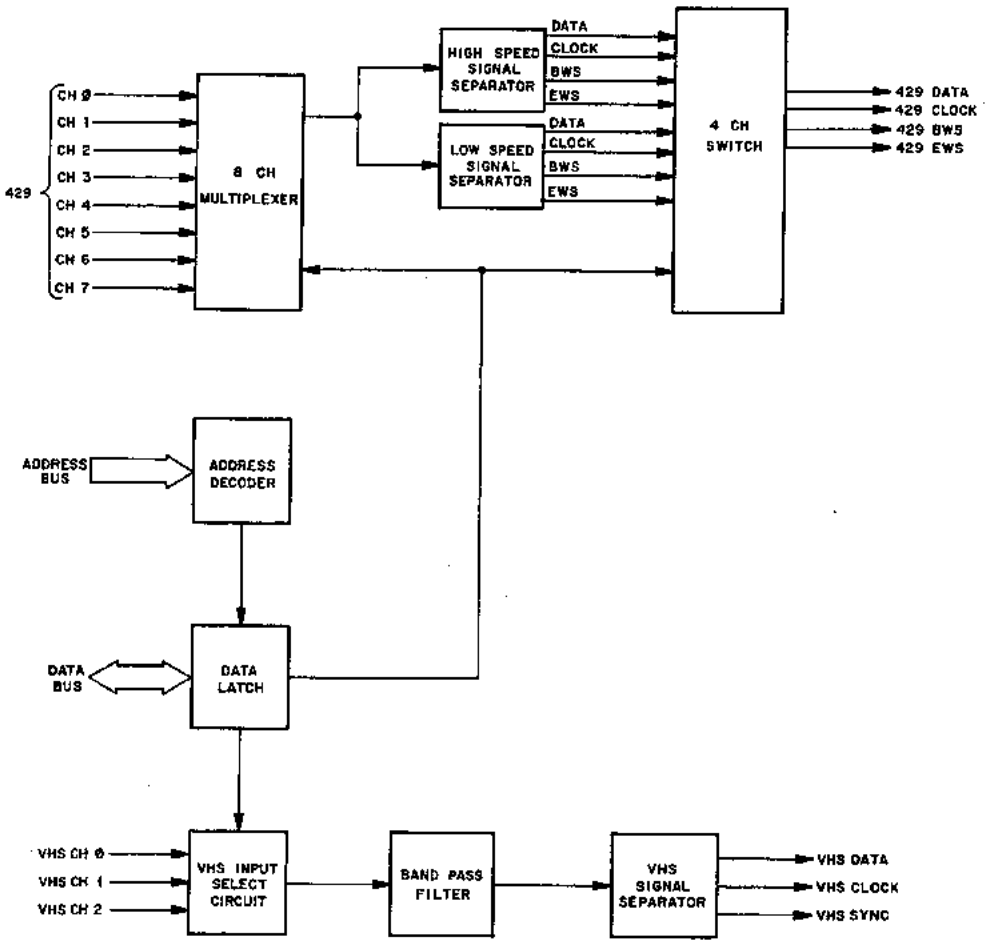
The Priority Resolving Logic Network (X603 thru X606, X614, X615 and Q601) controls and sets priorities for use of the Memory, Data and/or Address Buses. X603 stores the output of the VHS Bit Counter (X604 stores the output of the 429 Bit Counter) and at the same time, synchronizes this signal with one of the outputs of the 4-Bit Counter. Once the 4-Bit Counter pulse is present, X603 transfers the data from the VHS Latch/Buffer to the 1K X 8 RAM. In the case of 429 Bus, X604 transfers the 429 Data from the 429 Latch/Buffer to the 1K X 8 RAM. To make this type of transfer, X603 or X604 completes the following:

1. Gates the address from the Address Counter to the 1K X 8 RAM.
2. Gates data from the VHS Latch/Buffer to the 1K X 8 RAM.
3. Causes X606, X614 and X615 to generate a memory write pulse.

After the above items are performed, the VHS or 429 Address Counter increments and X603 (VHS) or X604 (429 Bus) resets. X606, X614 and X615 generate memory control signals and, if necessary, a processor wait state. $\overline{Q601}$ drives the WAIT line on the Processor Bus.

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(8) Bus Input Analog Card (Refer to 2-2-1, Figure 11 and 2-2-7, Figure 92)



Bus Input Analog Card Block Diagram
Figure 11

The Bus Analog Input Card selects the appropriate bus, controls all line receiving, and provides signal separation for data, clock, beginning word sync (BWS) and end word sync (EWS), for each bus.

An Address Decoder (X504 and certain circuits of X501, X502 and X503) clocks the Data Latch (X505) when the Data Latch address appears on the Address Bus. The Data Latch stores information strictly for use by the Bus Input Analog Card to control an 8-Channel Multiplexer, 4-Channel Switch and the VHS Input Select Circuit. The 8-Channel Multiplexer (X507) selects which 429 Bus channel is to be received.

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The multiplexer select information is provided by three bits from the Data Latch and its output is sent to either the High or Low Speed Signal Separators.

The High Speed Signal Separator is functionally identical to the Low Speed Signal Separator, with the only difference being the speed of operation. Therefore, only the High Speed Signal Separator will be discussed in the remainder of this paragraph. The High Speed Signal Separator consists of a line receiver (X508C and X508D), to reduce noise levels, and a Flip-Flop (X509A and X509B) that produces a serial data stream based on information received from the Line Receiver. Gate X502B is active only during the first half of a bit cell time. Its information is used by X513 to produce the Serial Clock signal and by X512B, which detects the start and stop of the serial data stream. X512B drives X514 to produce the beginning and end of message sync signals. The Serial Data, Serial Clock, End of Word Sync and Beginning of Word Sync signals are separately sent to the 4-Channel Switch.

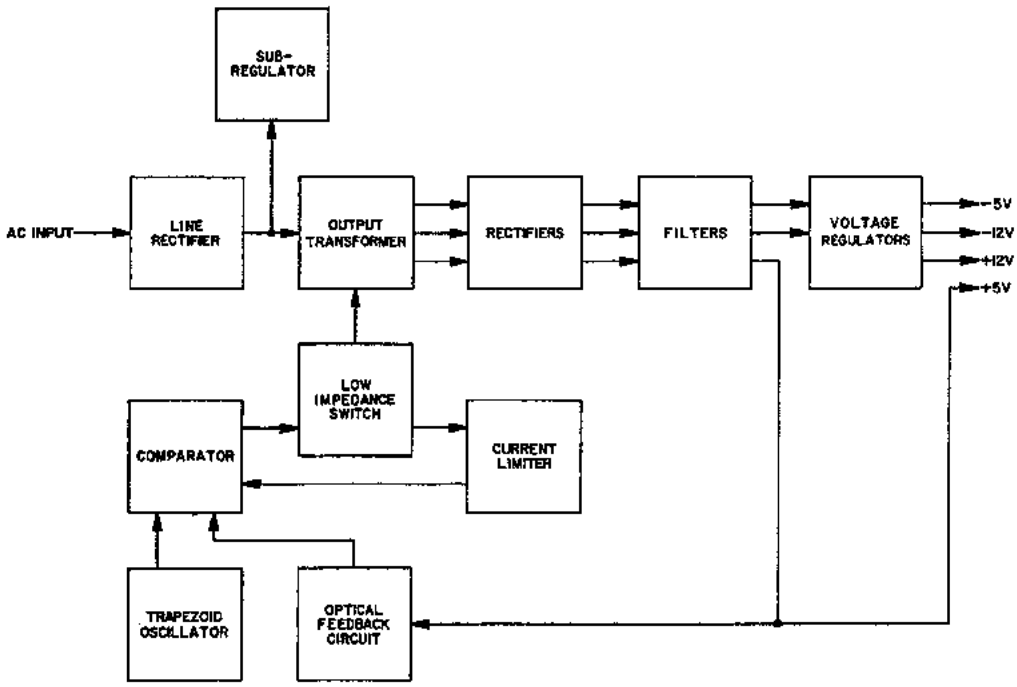
The 4-Channel Switch (X506) selects the VHS speed by choosing either the output of the High Speed Signal Separator or the output of the Low Speed Signal Separator. Two bits from the Data Latch determine which signal separator output is to be used. The 4-Channel Switch selection is sent to the Bus Input Logic PC Board.

The VHS Input Select Circuit (X515) buffers the select information from the Data Latch to Relays K501, K502 and K503. When selected, each relay connects one VHS Bus to a Bandpass Filter. Due to the circuit configuration, only one relay can be energized at any given time. The Bandpass Filter (X517, T501, Q501 and Q502) provides active filtering and line receiving for the selected VHS Bus. Buffer X517 drives the Dual Comparator (X518) of the VHS Signal Separator Circuit. The VHS Signal Separator Circuit consists of a Dual Comparator (X518), a Flip-Flop (two gates of X519), two Single-Shot Multivibrators (X520) and a Data Detection Circuit (X521, X522, X523, X524 and a gate each from X501 and X503). The Dual Comparator produces two outputs which set a Flip-Flop (two gates of X519). During the positive transition of the VHS Bus output, pin 9 of X519 is set high and during the negative transition, pin 11 of X519 is set high.

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This complementary data is fed to two Single-Shot Multivibrators (X520A and X520B), each having an output pulse width of 1/8 Bit Cell time. Both outputs are combined to produce the VHS clock information present at pin 6 of X519. X524 detects the Beginning of Word Sync (BWS). One single-shot of X523 enables the Data Detection Circuit by placing a signal at X522 and also enables the End of Word Sync Detector (X525). Pin 8 of X522 goes low when the clock and Beginning of Word Sync signals are present. When pin 8 is active, X521 produces an output which enables two gates of X522 to allow the received data to latch into X523. The output of X523 is the VHS Bus Serial Data.

(9) Power Supply (Refer to 2-2-1, Figure 12 and 2-2-7, Figure 93)



IFR Universal Power Supply Block Diagram
Figure 12

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The STD-7000 Bus Controller may be equipped with either of two different types of Power Supply Assemblies. Earlier STD-7000 models (prior to Serial Number 1041) contain Sierracin (model 5CXMP) Power Supply Modules. Information concerning the Sierracin (model 5CXMP) Power Supply, is restricted by the manufacturer. If any problems are encountered requiring maintenance or repair of this type power supply, it is recommended that the customer contact Sierracin Customer Service (213) 998-9873 and request assistance. The Power Supply Module used in later STD-7000 models (1041 and subsequent) is described in the following paragraphs. Either Power Supply converts the supplied AC voltage to four DC voltages (+5 VDC, -5 VDC, +12 VDC and -12 VDC) which are distributed throughout the bus controller. The power supply also supplies the +12 VDC for cooling fan operation.

The external AC power (line AC voltage) is rectified and filtered by the Line Rectifier (BR9901, C9901, C9902, C9903, C9904, C9905, C9906, R9901, R9902, T9901 and TR9901). The resultant high DC potential (140-370 VDC) is routed to the Sub Regulator (Q9901, CR9910, CR9906 and associated components) and to the primary windings of the Output Transformer (T9902).

The Sub-regulator consists of a Current Limiter (Q9901, CR9906 and associated components) and a Shunt Regulator (Zener Diode, CR9910). The Current Limiter maintains a safe operating level for the Zener Diode (CR9910). The Sub-Regulator provides a source of power for the operation of a Trapezoid Oscillator (X9905, CR9911 and associated com-ponents), Comparator (X9906, Q9902 and Q9903), Low Impedance Switch (Q9904) and part of the Optical Feedback Circuit.

The Trapezoid Oscillator signal is sent directly to the Comparator, which produces the variable duty cycle rectangular wave required to drive the Low Impedance Switch. This switch controls current flow through the primary windings of the Output Transformer (T9902) by comparing the Trapezoid Wave with the DC feedback from the Optical Feedback Circuit. This way, when the Trapezoid Waveform rises higher than the DC feedback, the output of the Comparator goes high and conversely, when the instantaneous voltage on the Trapezoid Wave falls below the DC feedback, the output of the Comparator goes low. In other words, the Comparator produces a rectangular waveform of which its duty cycle is inversely proportional to its DC input.

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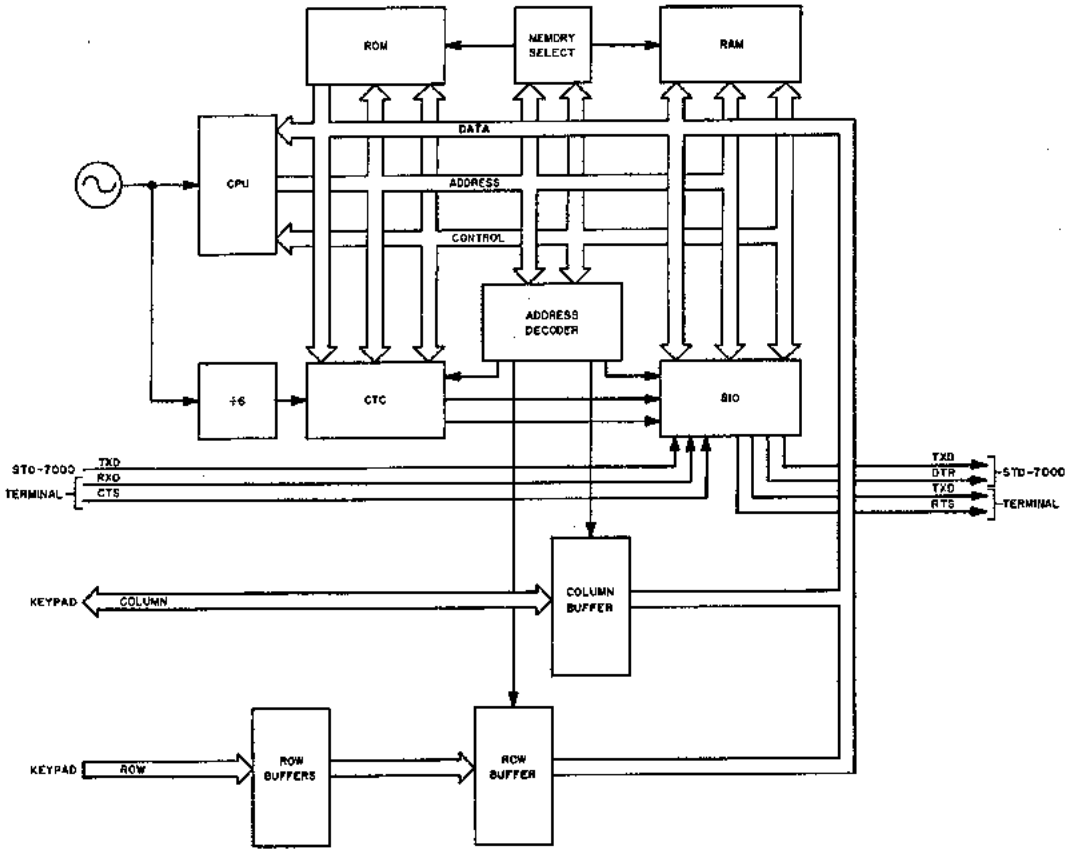
In addition to its primary windings, the Output Transformer has three secondary windings corresponding to the +12V, -12V and +5V outputs of the Power Supply. The secondary winding output voltages are proportional to the duty cycle at which the primary windings are switched. These transformer secondary winding output voltages are rectified by Rectifiers (CR9917, CR9918, CR9919 and CR9920), producing a DC voltage with a large amount of ripple. This ripple is filtered by Filters (C9909, C9912, C9918, C9919 and L9901 through L9904) before being sent to Voltage Regulators (X9901 through X9904).

Voltage Regulator X9901 regulates the -12V supply and X9902 regulates the -5V supply. At the same time, X9903 and X9904 regulate two separate +12V sources. The +5V output is regulated by the DC Optical Feed Back Circuit which also performs as the duty cycle regulator for the primary windings of the Output Transformer. This is accomplished by using an Operational Amplifier (X9908) to compare a sample of the +5V, from the filter output, with a reference voltage derived from Zener Diodes (CR9914 and CR9915). The Operational Amplifier drives an Optical Coupler (U9901) to the extent necessary to make the amplifier's input voltages equal (+5V from filter output equal to +5V reference voltage). The optical isolation is necessary to isolate the input circuits from the output circuits.

The Current Limiter serves a dual purpose; one as an Average Current Limiter (CR9912, X9907 and associated components) and the other as a Peak Current Limiter (Q9905). The Average Current Limiter (X9907) compares the peak voltage from Current Sense Resistors (R9923 through R9925) with a preset voltage value determined by R9919 and R9921. When a large current drain is detected, the output signal of X9907 causes comparator X9906 to stop operating, discontinuing the operation of the Low Impedance Switch. The Peak Current Limiter operates much faster than the Average Current Limiter so Q9905 is activated when the peak current exceeds a predetermined level. This action turns Q9902 OFF and Q9903 ON to remove the current spike, by discontinuing operation of the Low Impedance Switch.

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(10) CRT Interface (Refer to 2-2-1, Figure 13 and 2-2-7, Figure 94)



CRT Interface Block Diagram
Figure 13

The CPU (U16004) controls all the functions of the CRT Interface. The System ROM (U16007) contains the operating software. The System RAM (U16008) is used for temporary information storage. The Counter/Timer (U16012) is used to select the Baud Rates. The Serial I/O Device (U16011) provides communication between the STD-7000, Terminal and CPU (U16004).

(a) Baud Rate

The CPU (U16004) operates at 1.8432 MHz clock rate. The CPU frequency is divided down by six by the Binary Synchronous Up/Down Counter (U16003) to 307.2 MHz and fed to the Z80 CTC (U16012) to select the Baud Rate.

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(b) Memory Selection

The three to eight Line Decoder (U16009) uses the Refresh Line, Memory Request Line and Address Line A15 to select the System RAM (U16008) or System ROM (U16007). The three to eight Line Decoder (U16010) is used to select Z80 CTC (U16012) or the Serial I/O Device (U16011) and to check the Row and Column Lines for the Keypad.

(c) Keypad Circuit

The Keypad Circuit is composed of RN1, RN3 and a series of transistors used to buffer the lines and feed the Row Lines to the Row Buffer (U16006) and the Column Lines to the Column Buffer (U16005). The Row and Column Lines are normally high. When a button is pushed, one Row Line and one Column Line will go low and the CPU (U16004) will enter a routine to determine which button was pushed.

NOTE: The CPU (U16004) is programmed to periodically check the Column Buffer (U16005) for an indication that a key has been pushed.

As data enters the CRT Interface from the STD-7000, the data is stored in the RAM (U16008) and converted by the CPU (U16004) to standard ANSII Control Codes for use in the Video Terminal. Data from the Video Terminal goes directly to the STD-7000.

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2. Performance Evaluation

A. General

This section contains step-by-step procedures to be used as a method of assessing the performance of the Standard Digital Interface System (SDIS). These procedures should be accomplished when the operating condition of the SDIS is in question or when functional certification is required. When completed, these procedures will verify ARINC bus transmission and reception of valid data, high and low speed characteristics and proper electrical characteristics of each bus. Each procedure is designed to be performed using the SDIS (STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad), correctly interfaced in accordance with procedures described in 1-2-1, and do not require the removal of any external panels or covers.

In this section, information concerning the ESP 6515 CRT Display Terminal and KP-72480 Numeric Keypad is limited to support requirements for the STD-7000 Bus Controller.

Each procedure in this section assumes the technician is familiar with the operating procedures described 1-2-3, therefore no description of key-in operating sequences is provided, except when a requirement for a special function exists.

(1) Test Equipment Requirements

Appendix B at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this section. Any other equipment meeting the specifications listed in Appendix B may be substituted in place of the recommended models.

NOTE: For certain procedures in this section, the equipment listed in Appendix B may exceed the minimum required specifications; for this reason, minimum use specifications appear at the beginning of all individual procedures where special accessory equipment is required.

(2) Safety Precautions

Listed below are several important safety precautions which must be observed during all phases of SDIS operation. IFR Systems, Inc. assumes no liability for customer's failure to comply with any of the safety precautions outlined in this manual.

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(a) Complying With Instructions

All personnel should not attempt to interface and/or operate SDIS without reading and complying with instructions in Chapter 1. Each procedure contained in this manual and Chapter 1 must be performed in exact sequence and manner described.

(b) Grounding Requirements

To minimize shock hazards, all equipment chassis and cabinets must be connected to an electrical ground. For this purpose, all IFR Systems, Inc., test sets are equipped with a standard three-prong power cable plug which must be connected to a properly grounded three-prong wall, bench or floor receptacle.

WARNING: DUE TO POTENTIAL SAFETY HAZARDS, USE OF THREE-PRONG TO TWO-PRONG ADAPTER PLUG(S) IS NOT RECOMMENDED.

(c) Operating Safety

Due to the presence of potentially lethal voltages within the STD-7000 and accessory test equipment, maintenance personnel must not remove test equipment covers at any time unit is connected to a power source. Component replacement and internal adjustments must be made by qualified maintenance personnel only.

(d) CAUTION And WARNING Labels

Extreme care should be exercised when performing any operation or procedure preceded by a CAUTION or WARNING label. The CAUTION label appears where the possibility of damage to equipment exists, while the WARNING label is used to denote a condition where a danger exists, exposing personnel to possible bodily injury or death.

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B. Performance Evaluation Procedures

(1) Control Bus Performance Evaluation

SPECIAL ACCESSORY EQUIPMENT REQ'D:

1 Oscilloscope (0-100 MHz Bandwidth, Dual Trace with Delta Time).

1 Mini-cassette personality Tape (version 2.4 or subsequent).

2 Jumper Wires (26 gauge, approximately four inches in length and adaptable to STD-7000 Rear Panel Connector J416 pin holes).

NOTE: Interface STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad in accordance with instructions located in 1-2-1.

NOTE: If the Control Bus Performance Evaluation is to be accomplished consecutively, following either the attitude Bus or Data Bus Performance Evaluation, begin with Step 7, otherwise begin with Step 1.

STEP	PROCEDURE
1.	Insure compliance with SDIS interface instructions as described in 1-2-1.
2.	Position IEEE-488 Address Switch, segments 7 and 8, to select desired Start-Up Routine as described in 1-2-1.
3.	Position CRT Display Terminal Power Switch to ON.
4.	Insert personality cassette tape (2.4 or subsequent) into tape drive (unless STD-7000 is equipped for PROM operation).
5.	Apply AC power to STD-7000 and check for a blinking cursor on CRT Terminal Display.

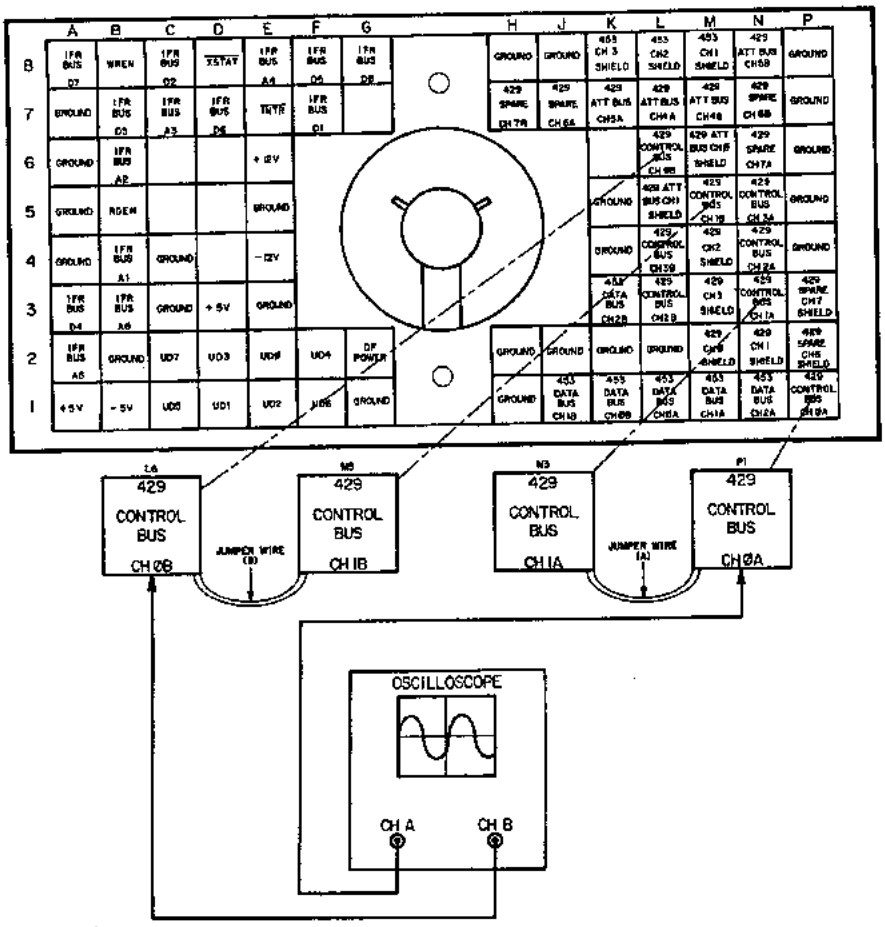
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STEP PROCEDURE

6. Momentarily depress STD-7000 RESET Button.

CAUTION: IF THE AUTOMATIC START-UP ROUTINE WAS SELECTED IN STEP 2, A MEMORY DIAGNOSTIC IS AUTOMATICALLY PERFORMED TO CHECK ALL MEMORY LOCATIONS FOR PROPER OPERATION. IF A MEMORY ERROR IS DETECTED DURING THIS MEMORY DIAGNOSTIC, THE START-UP ROUTINE AUTOMATICALLY CHANGES TO DIAGNOSTIC TEST PROGRAM. IF THIS CONDITION OCCURS, QUALIFIED MAINTENANCE PERSONNEL SHOULD REFER TO 2-2-4B BEFORE CONTINUING.

7 Connect Jumper Wire (A) between Pins P1 and N3 of STD-7000 Rear Panel Connector J416 (refer to 2-2-2, Figure 14).

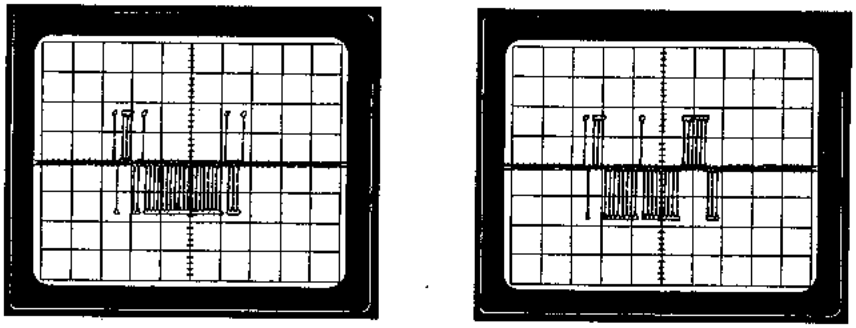


Control Bus (Channels Ø and 1) Evaluation Set-Up Diagram

Figure 14

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STEP	PROCEDURE
8.	Connect Jumper Wire (B) between Pins L6 and M5 of J416 (refer to 2-2-2, Figure 14).
9.	Connect Oscilloscope Channel A, X1 Probe to Pin P1 of J416 (refer to 2-2-2, Figure 14).
10.	Connect Oscilloscope Channel B, X1 Probe to Pin L6 of J416 (refer to 2-2-2, Figure 14).
11.	Apply AC power to Oscilloscope, sum Channels A and B, invert Channel B and set for delayed sweep.
12.	After initialization (when WEATHER RADAR MASTER MENU is displayed on CRT Display), key-in and display CONTROL BUS OUTPUT PAGE (1).
13.	Change COND (Data Field 2) to (SEND).



Two-Word Data Message
Figure 15

14.	Change RATE (Data Field 3) to (1ØØ).
	NOTE: At this point, verify Data Field 1 indicates CBØ.
15.	Adjust Oscilloscope delayed sweep to observe 2-word data message as shown in 2-2-2, Figure 15, and verify data is within the following tolerances:

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STEP PROCEDURE

Bits each word	(32)
Rise Time	(1.5 µSec±.5 µSec)
Fall Time	(1.5 µSec±.5 µSec)
Bus Amplitude	(20 V±1 Vp-p)
Rate = 20	(period is 50 mS±1%)
Rate = 100	(period is 10 mS±1%)
Rate = 150	(period is 6.67 mS±1%)
Bit Period	(10 µSec±1%)

Two-Word Data
Table 1

NOTE: Rate period is measured as the time between two like words (i.e. RANGE WORD to RANGE WORD or CONTROL WORD to CONTROL WORD).

NOTE: Bit period is measured as time between leading edge of one bit to leading edge of next bit or trailing edge of one bit to trailing edge of next bit.

NOTE: Insure RATE (Data Field 3) remains (100) after completion of Step 15.

16. Adjust Oscilloscope to observe CONTROL WORD. Change CONTROL WORD Label (Data Field 4) to indicate each label shown in 2-2-2, Table 2 and verify label agrees octally on Bits 1 thru 8.

	BIT							
LABEL	1	2	3	4	5	6	7	8
000	0	0	0	0	0	0	0	0
377	1	1	1	1	1	1	1	1
252	1	0	1	0	1	0	1	0
125	0	1	0	1	0	1	0	1

CONTROL WORD Labels
Table 2

NOTE: Insure each bit indicates correct polarity.

NOTE: Return Data Field 4 to (ØØØ) before continuing.

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STEP PROCEDURE

17. Change Standard Digital Interface (SDI) (Data Field 5) to reflect each SDI number shown in 2-2-2, Table 3 and verify bits 9 and 10 indicate accordingly.

	BIT	
SDI	9	10
1	1	0
2	0	1
3	1	1
0	0	0

CONTROL WORD SDI Numbers
Table 3

18. Change Data Field 7 to indicate each MATRIX Sub Menu shown in 2-2-2, Table 4 and observe oscilloscope display for proper indications.

	BIT	
MATRIX SUBMENU	30	31
1. FAIL	0	0
2. INV	1	0
3. TST	0	1
4. VAL	1	1

CONTROL WORD Submenus
Table 4

19. Change PARITY (Data Field 6) and observe oscilloscope display Bit 32 changes to the opposite state.

20. Change CONTROL WORD Data Fields to following:

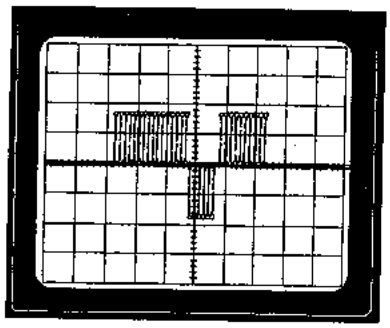
DATA FIELD		DATA FIELD	
4.	(377)	9.	(-16.ØØ)
5.	(3)	10.	(CAL)
6.	(EVEN)	11.	(ON)
7.	(SLV)	12.	(ON)
8.	(SETUP)	13.	(ON)

CONTROL WORD Data
Table 5

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STEP PROCEDURE

21. Verify all CONTROL WORD bits are high except Bits 17 thru 22 as shown in 2-2-2, Figure 16.



CONTROL WORD Data Bits
Figure 16

22. Change Data Field 9 to reflect each TILT position shown and observe oscilloscope display for proper indication as reflected in 2-2-2, Table 6.

TILT POSITION	BIT						
	17	18	19	20	21	22	23
(+00.25)	1	0	0	0	0	0	0
(+00.50)	0	1	0	0	0	0	0
(+01.00)	0	0	1	0	0	0	0
(+02.00)	0	0	0	1	0	0	0
(+04.00)	0	0	0	0	1	0	0
(+08.00)	0	0	0	0	0	1	0
(-16.00)	0	0	0	0	0	0	1

CONTROL WORD Tilt Positions
Table 6

23. Adjust Oscilloscope to observe RANGE WORD. Change RANGE WORD Label (Data Field 14) to indicate each label shown in 2-2-2, Table 2, and verify label agrees octally on Bits 1 thru 8.

NOTE: Verify each bit indicates correct polarity. Return Data Field 14 to (ØØØ) before continuing.

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STEP PROCEDURE

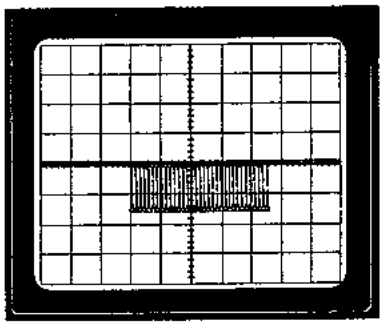
24. Change SDI (Data Field 15) to reflect each SDI number shown in 2-2-2, Table 3 and verify bits 9 and 10 indicate accordingly.

25. Change RANGE WORD Data Fields to following:

DATA FIELD	
14.	(ØØØ)
15.	(Ø)
16.	(Even)
17.	(VAL)
18.	(32Ø)

RANGE WORD Data
Table 7

26. Verify all RANGE WORD bits are LOW as shown in 2-2-2, Figure 17.



RANGE WORD Data Bits
Figure 17

27. Change Data Field 18 to indicate each set of MILES shown in 2-2-2, Table 8 and observe Oscilloscope display for proper indications.

	BIT					
MILES	24	25	26	27	28	29
(005)	1	0	0	0	0	0
(010)	0	1	0	0	0	0
(020)	0	0	1	0	0	0
(040)	0	0	0	1	0	0
(080)	0	0	0	0	1	0
(160)	0	0	0	0	0	1
(315)	1	1	1	1	1	1
(320)	0	0	0	0	0	0

RANGE WORD Miles
Table 8

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STEP PROCEDURE

28. Change Data Field 17 to indicate each MATRIX Sub-Menu shown in 2-2-2, Table 4, and observe Oscilloscope display for proper bit indications.

29. Change PARITY (Data Field 16) and observe Oscilloscope display bit 32 changes to opposite state.

30. Change COND (Data Field 2) to (OFF).

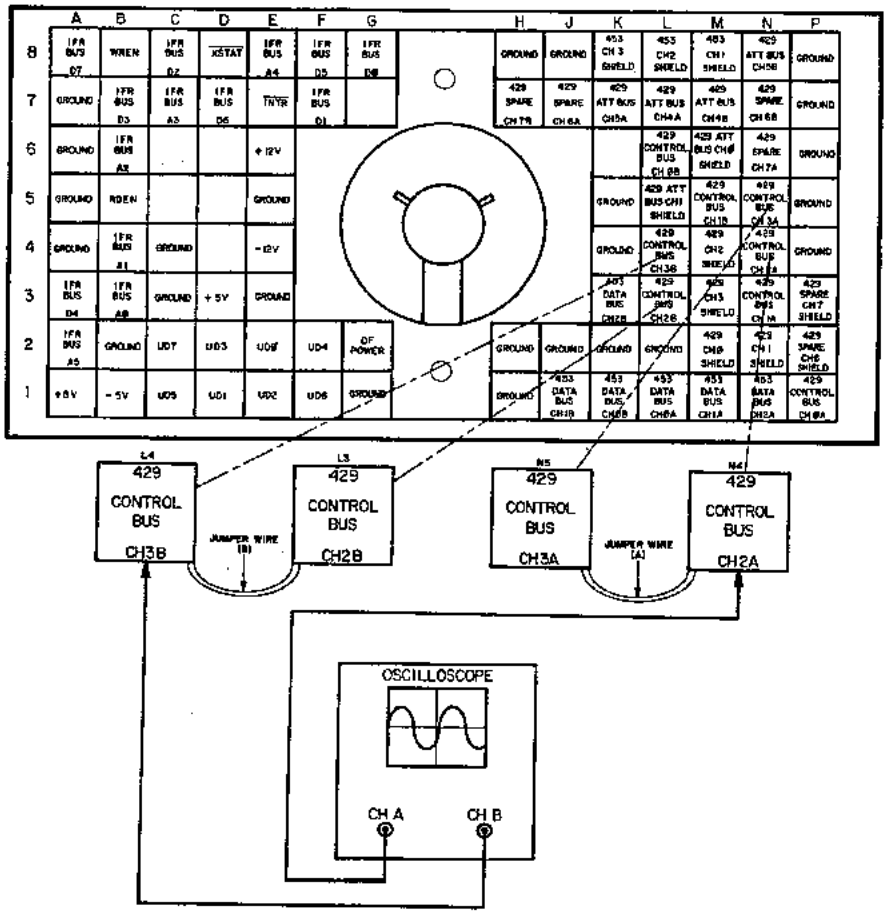
31. Change PAGE (Data Field 1) to (CB 1).

32. Change COND (Data Field 2) to (SEND).

33. Change RATE (Data Field 3) to (1ØØ).

34. Repeat Steps 15 through 30 for Control Bus 1.

35. Disconnect Oscilloscope probes and Jumper wires from connector J416.

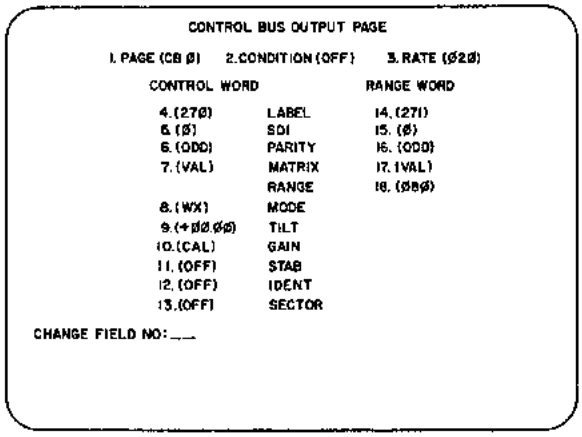


Control Bus (Channels 2 and 3) Evaluation Set-Up Diagram

Figure 18

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STEP	PROCEDURE
36.	Connect Jumper Wire A between Pins N4 and N5 of STD-7000 Rear Panel Connector J416 (refer to 2-2-2, Figure 18).
37.	Connect Jumper Wire B between Pins L3 and L4 of J416 (refer to 2-2-2, Figure 18).
38.	Connect Oscilloscope Channel A, X1 Probe to Pin N4 of J416 (refer to 2-2-2, Figure 18).
39.	Connect Oscilloscope Channel B, X1 Probe to Pin L4 of J416 (refer to 2-2-2, Figure 18).
40.	Change PAGE (Data Field 1) to (CB 2).
41.	Change COND (Data Field 2) to (SEND).
42.	Change RATE (Data Field 3) to (1ØØ).
43.	Repeat Steps 15 through 30 for Control Bus 2.
44.	Change PAGE (Data Field 1) to (CB 3).
45.	Change COND (Data Field 2) to (SEND).
46.	Change RATE (Data Field 3) to (1ØØ).
47.	Repeat Steps 15 through 30 for Control Bus 3.
48.	Disconnect Oscilloscope probes and Jumper wires from Connector J416.
49.	Restore Control Bus Output Page (CBØ) to its original state as shown in 2-2-2, Figure 19.



Control Bus Output Page (CB Ø)
Figure 19

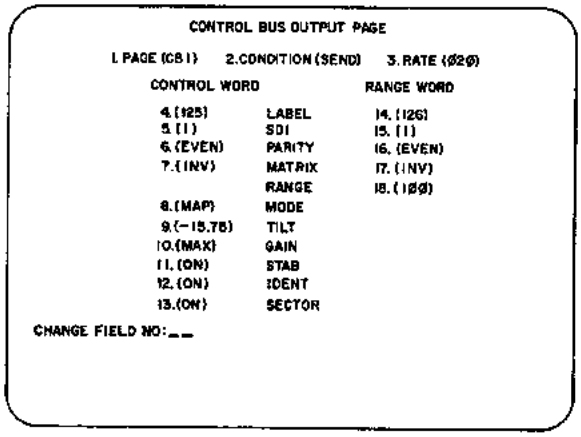
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STEP	PROCEDURE

50. Change PAGE (Data Field 1) to each Control Bus (1 through 3) and verify each COND (Data Field 2) indicates (OFF).

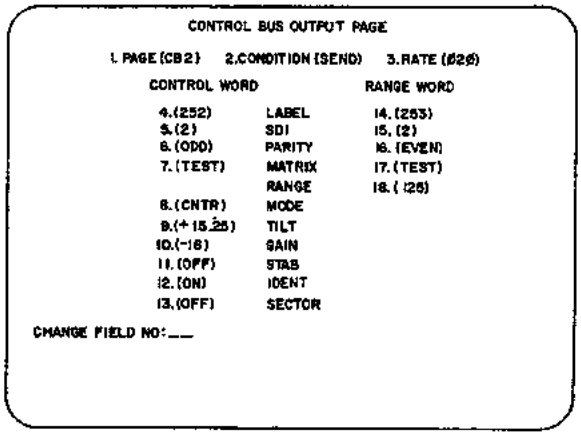
51. Change Control Bus Ø (CB Ø), COND (Data Field 2) to (SEND).

52. Change Control Bus Output Page to reflect data in 2-2-2, Figure 20.



Control Bus Output Page (CB 1)
Figure 20

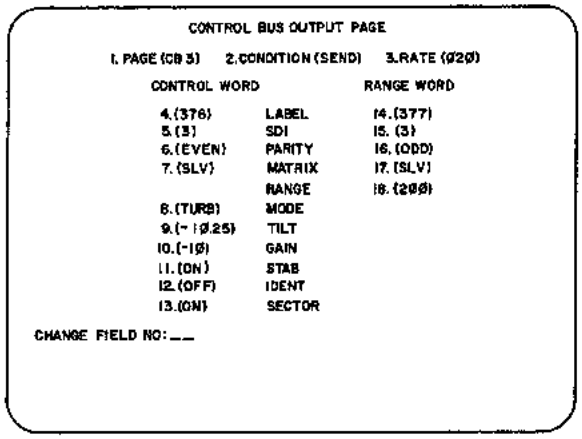
53. Beginning with Data Field 1, change Control Bus Output Page to reflect data indicated in 2-2-2, Figure 21.



Control Bus Output Page (CB 2)
Figure 21

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STEP PROCEDURE

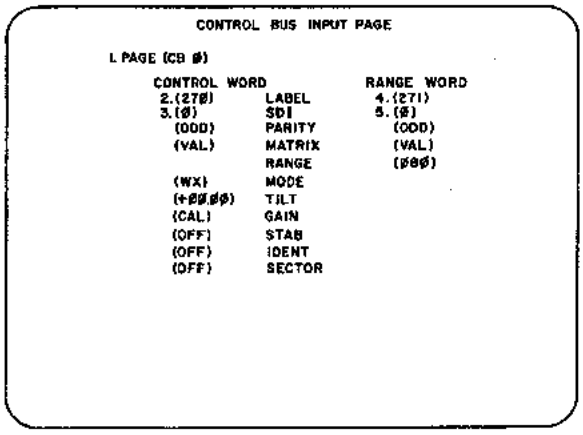


Control Bus Output Page (CB 3)
Figure 22

54. Beginning with Data Field 1, change Control Bus Output Page to reflect data indicated in 2-2-2, Figure 22.

55. Using Numeric Keypad, select CONTROL BUS INPUT PAGE (4).

56. Verify, by observation, that PAGE CB Ø reflects data transmission indications shown in 2-2-2, Figure 23.



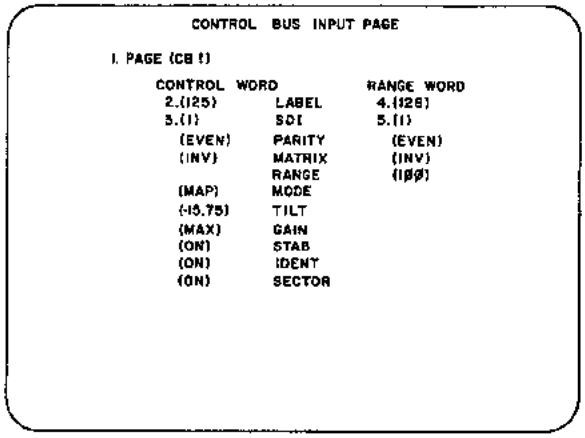
Control Bus Input Page (CB Ø)
Figure 23

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STEP PROCEDURE

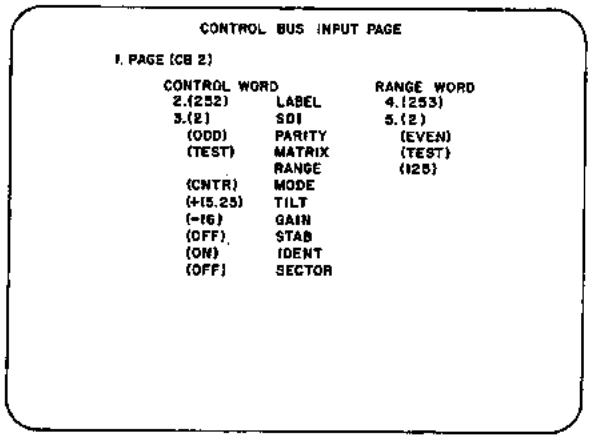
57. Select Control Bus 1 (CB 1), on CONTROL BUS INPUT PAGE (4) and verify transmitted data is the same as shown in 2-2-2, Figure 24.

NOTE: To receive desired data transmission in Steps 57 through 59, it will be necessary to Change Data Fields 1 through 5 of CONTROL BUS INPUT PAGE (4) to reflect identical data as Data Fields 1,4,5,14 and 15, respectively, of CONTROL BUS OUTPUT PAGE (1).



Control Bus Input Page (CB 1)
Figure 24

58. Select Control Bus 2 (CB 2), on CONTROL BUS INPUT PAGE (4) and verify transmitted data is the same as shown in 2-2-2, Figure 25.

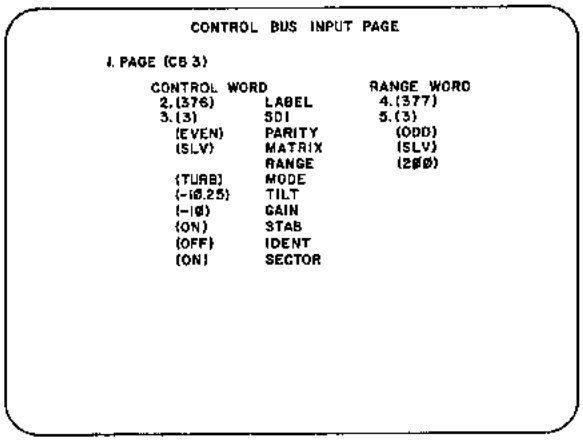


Control Bus Input Page (CB2)
Figure 25

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STEP PROCEDURE

59. Select Control Bus 3 (CB 3), on CONTROL BUS INPUT PAGE (4) and verify transmitted data is the same as shown in 2-2-2, Figure 26.



Control Bus Input Page (CB3)
Figure 26

60. Using Keypad, select CONTROL BUS OUTPUT PAGE (1).

61. Change each Control Bus page (Ø through 3), COND (Data Field 2) to (OFF).

62. Using Keypad, select CONTROL BUS INPUT PAGE (4).

63. Verify all data transmission has ceased on each Control Bus (CBØ through CB3) by selecting CONTROL BUS INPUT PAGE for each bus.

NOTE: Data Fields 1, 2 and 4 of CONTROL BUS INPUT PAGE (CBO through CB3) will retain last transmitted data until intentionally changed, RESET Button actuation or an interruption in external AC power.

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(2) Attitude Bus Performance Evaluation

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Oscilloscope (0-100 MHz Bandwidth, Dual Trace with Delta Time)

NOTE: Interface STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad in accordance with instructions described in 1-2-1.

NOTE: If the Attitude Bus Performance Evaluation is to be accomplished consecutively, following either the Control Bus or Data Bus Performance Evaluation, begin with Step 7, otherwise begin with Step 1.

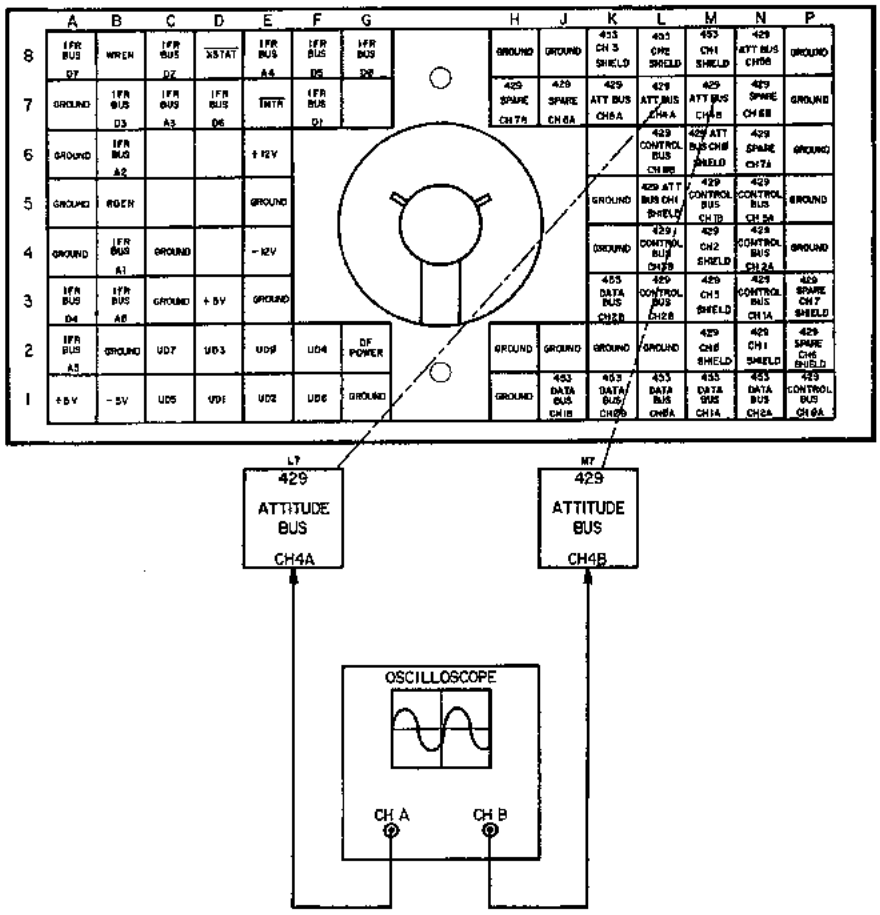
STEP	PROCEDURE
1.	Insure compliance with SDIS interface instructions as described in 1-2-1.
2.	Position IEEE-488 Address Switch, segments 7 and 8, to select desired Start-Up Routine as described in 1-2-3.
3.	Position CRT Display Terminal Power Switch to ON.
4.	Insert personality cassette tape (2.4 or subsequent) into tape drive (unless STD-7000 is equipped for PROM operation).
5.	Apply AC power to STD-7000 and check for a blinking cursor on CRT Terminal Display.
6.	Momentarily depress STD-7000 RESET Button.

CAUTION: IF THE AUTOMATIC START-UP ROUTINE WAS SELECTED IN STEP 2, A MEMORY DIAGNOSTIC IS AUTOMATICALLY PERFORMED TO CHECK ALL MEMORY LOCATIONS FOR PROPER OPERATION. IF A MEMORY ERROR IS DETECTED DURING THE MEMORY DIAGNOSTIC, THE START-UP ROUTINE WILL AUTOMATICALLY CHANGE TO DIAGNOSTIC TEST PROGRAM. IF THIS CONDITION OCCURS, QUALIFIED MAINTENANCE PERSONNEL SHOULD REFER TO 2-2-4B BEFORE CONTINUING.

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STEP PROCEDURE

7. Connect Oscilloscope Channel A, X1 Probe to Pin L7 of STD-7000 Rear Panel Connector J416 (refer to 2-2-2, Figure 27).



Attitude Bus (Channel Ø) Evaluation Set-Up Diagram

Figure 27

8. Connect Oscilloscope Channel B, X1 Probe to Pin M7 of J416 (refer to 2-2-2, Figure 27).

9. Apply AC power to Oscilloscope, sum Channels A and B, invert Channel B and set for Delayed Sweep.

10. Using Keypad, display ATTITUDE OUTPUT PAGE (3) on CRT Display Terminal.

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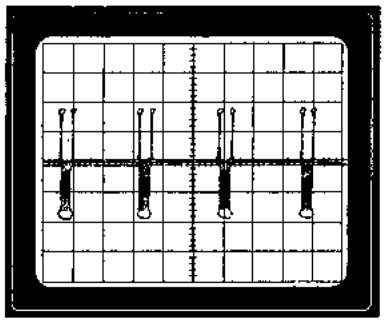
STEP PROCEDURE

11. Change COND (Data Field 2) to (SEND).

NOTE: Insure BUS NO. (Data Field 1) remains (Ø).

12. Change RATE (Data Field 3) to (Ø87).

13. Adjust Oscilloscope controls until four stable word traces are indicated as shown in 2-2-2, Figure 28.



Attitude Bus Four Word Trace
Figure 28

14. Select each word individually on Oscilloscope display screen and verify the data is within the following tolerances:

Bits each word	(32)
Rise Time	(10%-90%)
Fall Time	(90%-10%)
Bus Amplitude	(20±1 V)
Rate = 20	(period is 50 mS±1%)
Rate = 100	(period is 10 mS±1%)
Rate = 150	(period is 6.67 mS±1%)
Bit Period	(80.6±1 µSec)

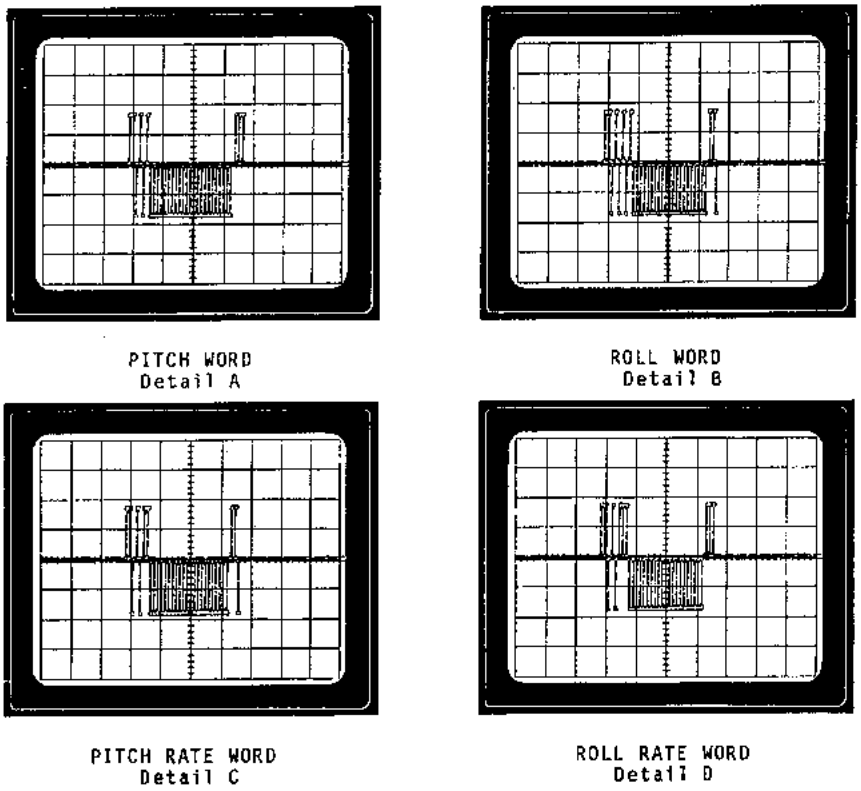
Four Word Trace Data
Table 9

NOTE: Rate period is measured as the time between two like words (i.e. PITCH WORD to PITCH WORD or ROLL WORD to ROLL WORD, etc.).

NOTE: Each word can easily be identified by comparing Oscilloscope trace with one of the sample traces in 2-2-2, Figure 29.

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STEP PROCEDURE



PITCH WORD
Detail A

ROLL WORD
Detail B

PITCH RATE WORD
Detail C

ROLL RATE WORD
Detail D

Attitude Bus Sample Traces
Figure 29

15. Change ATTITUDE OUTPUT PAGE to reflect data shown in 2-2-2, Figure 30.

ATTITUDE OUTPUT PAGE

1. BUS NO.(Ø) 2.CONDITION(SEND) 3.RATE (Ø67)

PITCH		ROLL
4.(ØØØ)	LABEL	9.(ØØØ)
5.(FAIL)	MATRIX	10.(FAIL)
6.(ODD)	PARITY	11.(EVEN)
7.(89.99)	LIMIT	12.(89.99)
8.(+ØØ.ØØ)	DATA	13.(+ØØ.ØØ)
PITCH RATE		ROLL RATE
14.(ØØØ)	LABEL	18.(ØØØ)
15.(FAIL)	MATRIX	19.(FAIL)
16.(EVEN)	PARITY	20.(EVEN)
17.(+ØØØ)	RATE	21.(+ØØØ)

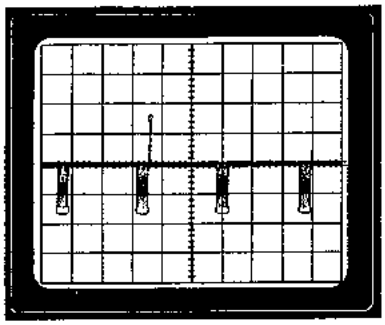
CHANGE FIELD NO:___

Attitude Output Page (Bus No. Ø)
Figure 30

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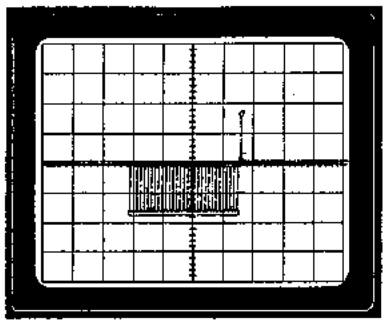
STEP PROCEDURE

16. Adjust Oscilloscope controls until four stable word traces are displayed as shown in 2-2-2, Figure 31.



Attitude Output Page Word Identification Trace
Figure 31

17. Adjust Oscilloscope Delay Display and Delay Sweep Controls to display PITCH word as shown in 2-2-2, Figure 32.



Pitch Word
Figure 32

MATRIX SUBMENU	BIT 30	BIT 31
1. FAIL	0	0
2. INV	1	0
3. TST	0	1
4. VAL	1	1

PITCH WORD Matrix Submenus
Table 10

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STEP PROCEDURE

NOTE: PITCH word is identified by locating the word with one high bit (Bit 32) as shown in 2-2-2, Figure 32.

18. Change Data Field 5 through each MATRIX Submenu listed in 2-2-2, Table 10. Observe and verify the operation of Bits 30 and 31.

NOTE: After completion of Step 18, return MATRIX (Data Field 5) sub-menu to (FAIL).

19. Change DATA (Data Field 8) to each angle shown in Data column of 2-2-2, Table 11. Check that Bits 15 through 29 comply as shown.

	BIT														
DATA	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
(+59.99)	1	0	1	0	1	0	1	0	1	0	1	0	1	0	0
(-60.00)	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
(+89.98)	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0
(-89.98)	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1

PITCH WORD Data
Table 11

NOTE: When entering a DATA angle (Data Field 8 or 13), a .01 loss will be realized after key-in sequence except when keying in (+ØØ.ØØ).

EXAMPLE: To indicate (-6Ø.ØØ), key-in (-6Ø.Ø1).

Return DATA angle to (+ØØ.ØØ) after completion of Step 19.

20. Change LABEL (Data Field 4) to indicate numbers shown in Label column in 2-2-2, Table 12. Verify Bits 1 through 8 comply with bit pattern shown.

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STEP PROCEDURE

LABEL	BIT 1	2	3	4	5	6	7	8
(377)	1	1	1	1	1	1	1	1
(252)	1	0	1	0	1	0	1	0
(125)	0	1	0	1	0	1	0	1

PITCH WORD Labels
Table 12

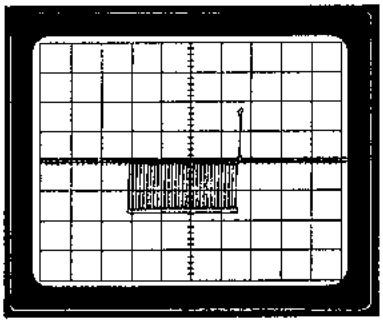
NOTE: Return LABEL to (ØØØ) after completion of Step 20.

NOTE: Bits 9 through 14 are not used in PITCH word and therefore will remain low at all times.

21. Change PARITY (Data Field 6) to (EVEN) and note that all PITCH word bits are low at this time.

22. Change PARITY (Data Field 11) to (ODD).

23. Adjust Oscilloscope Delay Display and Delay Sweep Controls to display ROLL word as shown in 2-2-2, Figure 33.



Roll Word
Figure 33

NOTE: ROLL word is identified by locating the word with one high bit (Bit 32) as shown in 2-2-2, Figure 33.

24. Change Data Field 10 through each MATRIX Submenu listed in 2-2-2, Table 10. Observe and verify the operation of Bits 30 and 31.

NOTE: After completion of Step 24, return MATRIX (Data Field 1Ø) sub-menu to (FAIL).

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STEP PROCEDURE

25. Change DATA (Data Field 13) to each angle shown in DATA column of 2-2-2, Table 11. Check that Bits 15 through 29 comply as shown.

NOTE: When entering a DATA angle (Data Field 8 or 13), a .01 loss will be realized after key-in sequence. For example input situation, see Step 19.

NOTE: Return DATA angle to (+ØØ.ØØ) after completion of Step 25.

26. Change LABEL (Data Field 9) to indicate numbers shown in label column of 2-2-2, Table 12. Verify Bits 1 through 8 comply with bit pattern shown.

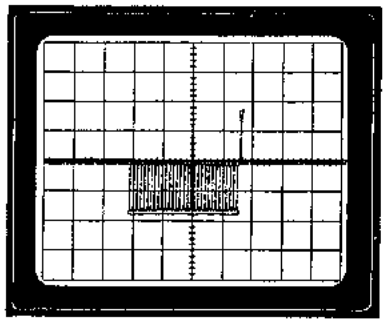
NOTE: Return LABEL to (ØØØ) after completion of Step 26.

NOTE: Bits 9 through 14 are not used in ROLL word and will remain low at all times.

27. Change PARITY (Data Field 11) to (EVEN) and note that all ROLL word bits are low at this point.

28. Change PARITY (Data Field 16) to (ODD).

29. Adjust Oscilloscope Delay Display and Delay Sweep Controls to display PITCH RATE word as shown in 2-2-2, Figure 34.



Pitch Rate Word
Figure 34

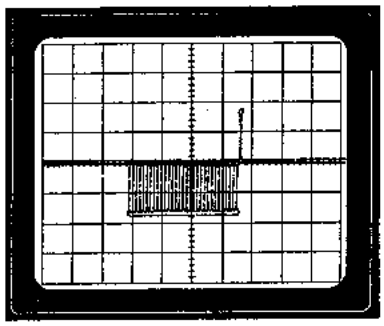
NOTE: PITCH RATE word is identified by locating the word with one high bit (Bit 32) as shown in 2-2-2, Figure 34.

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STEP	PROCEDURE
30.	Change Data Field 15 through each MATRIX Sub-menus listed in 2-2-2, Table 10. Observe and verify correction operation of Bits 30 and 31.
	NOTE: After completion of Step 30, return MATRIX (Data Field 15) Sub-menu to (FAIL).
31.	Change DATA (Data Field 8) to indicate (+89.98).
	NOTE: Enter (+89.99) to display (+89.98).
32.	Change RATE (Data Field 17) to indicate (-ØØ1). Bits 21 through 29 will remain high until DATA (Data Field 8) times out and consequently returns RATE (Data Field 17) to (+ØØØ). At the completion of this event, Bits 21 through 29 will return low.
	NOTE: Return Data Field 8 to (+ØØ.ØØ) after completion of Step 32.
33.	Change LABEL (Data Field 14) to indicate numbers shown in Label Column of 2-2-2, Table 12. Verify Bits 1 through 8 comply with bit pattern shown.
	NOTE: Return LABEL to (ØØØ) after completion of Step 33.
	NOTE: Bits 9 through 20 are not used in PITCH RATE word and will remain low at all times.
34.	Change PARITY (Data Field 16) to (EVEN) and note that all PITCH RATE word bits are low at this time.
35.	Change PARITY (Data Field 2Ø) to (ODD).
36.	Adjust Oscilloscope Delay Display and Delay Sweep Controls to display ROLL RATE word as shown in 2-2-2, Figure 35.

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STEP PROCEDURE



Roll Rate Word
Figure 35

NOTE: ROLL RATE word is identified as the only word with a high bit (Bit 32) as shown in 2-2-2, Figure 35.

37. Change MATRIX (Data Field 19) through each sub-menu listed in 2-2-2, Table 10. Observe and verify correct operation of Bits 30 and 31.

NOTE: After completion of Step 30, return Matrix (Data Field 19) sub-menu to (FAIL).

38. Change DATA (Data Field 13) to indicate (+89.98).

NOTE: Enter (+89.99) to display (+89.98).

39. Change RATE (Data Field 21) to indicate (-ØØ1). Bits 21 through 29 will remain high until DATA (Data Field 13) times out and consequently returns RATE (Data Field 21) to (+ØØØ). At this point, Bits 21 through 29 will return low.

NOTE: Return Data Field 13 to (+ØØ.ØØ) after completion of Step 39.

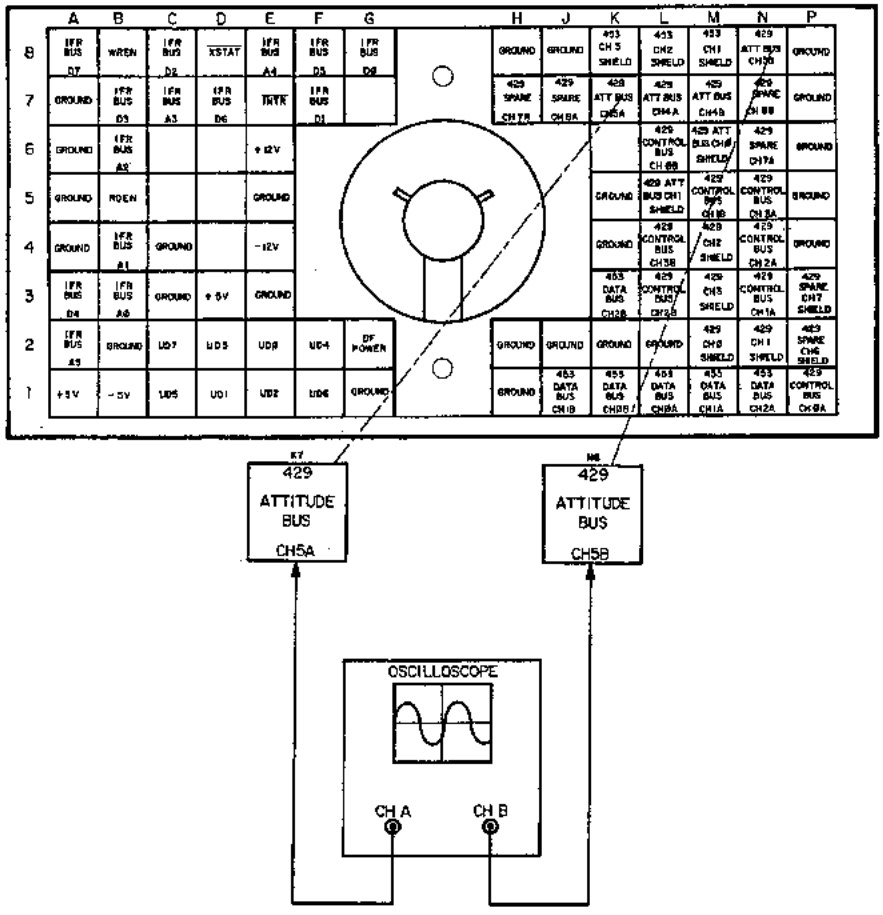
40. Change LABEL (Data Field 18) to indicate numbers shown in Label Column of 2-2-2, Table 12. Verify Bits 1 through 8 comply with bit pattern shown.

NOTE: Return LABEL to (ØØØ) after completion of Step 40.

NOTE: Bits 9 through 20 are not used in ROLL RATE word and will remain low at all times.

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STEP	PROCEDURE
41.	Change PARITY (Data Field 20) to (EVEN) and note that all ROLL RATE word bits are low at this point.
42.	Change COND (Data Field 2) to (OFF). Note that all Oscilloscope traces disappear.
43.	Disconnect Oscilloscope Probes from STD-7000 Rear Panel Connector J416.
44.	Connect Oscilloscope Channel A, X1 Probe to Pin K6 of J416 (refer to 2-2-2, Figure 36).
45.	Connect Oscilloscope Channel B, X1 Probe to Pin N8 of J416 (refer to 2-2-2, Figure 36).

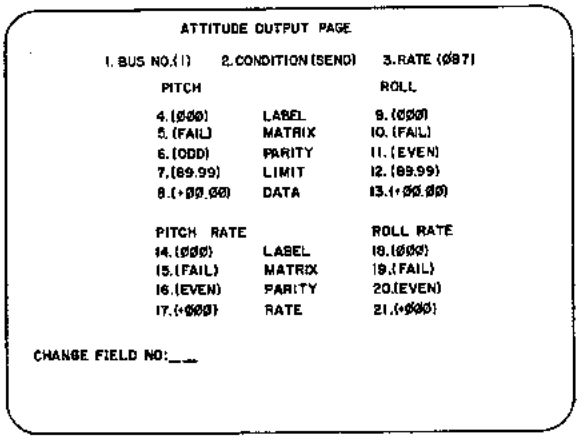


Attitude Bus (Channel 1) Evaluation Set-Up Diagram

Figure 36

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STEP	PROCEDURE
46.	Using Keypad, change BUS NO (Data Field 1) to (1). This action selects Bus number 1.
47.	Change COND (Data Field 2) to (SEND).
48.	Repeat Steps 12 through 14.
49.	Insure ATTITUDE OUTPUT PAGE reflects data shown in 2-2-2, Figure 37.



Attitude Output Page (Bus No. 1)
Figure 37

50.	Repeat Steps 16 through 43.

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(3) Data Bus Performance Evaluation

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Oscilloscope (0-100 MHz Bandwidth, Dual Trace with Delta Time).

NOTE: Interface STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad in accordance with instructions described in 1-2-1.

NOTE: If the Data Bus Performance Evaluation is to be accomplished consecutively, following either the Control Bus or Attitude Bus Performance Evaluation, begin with Step 7, otherwise begin with Step 1.

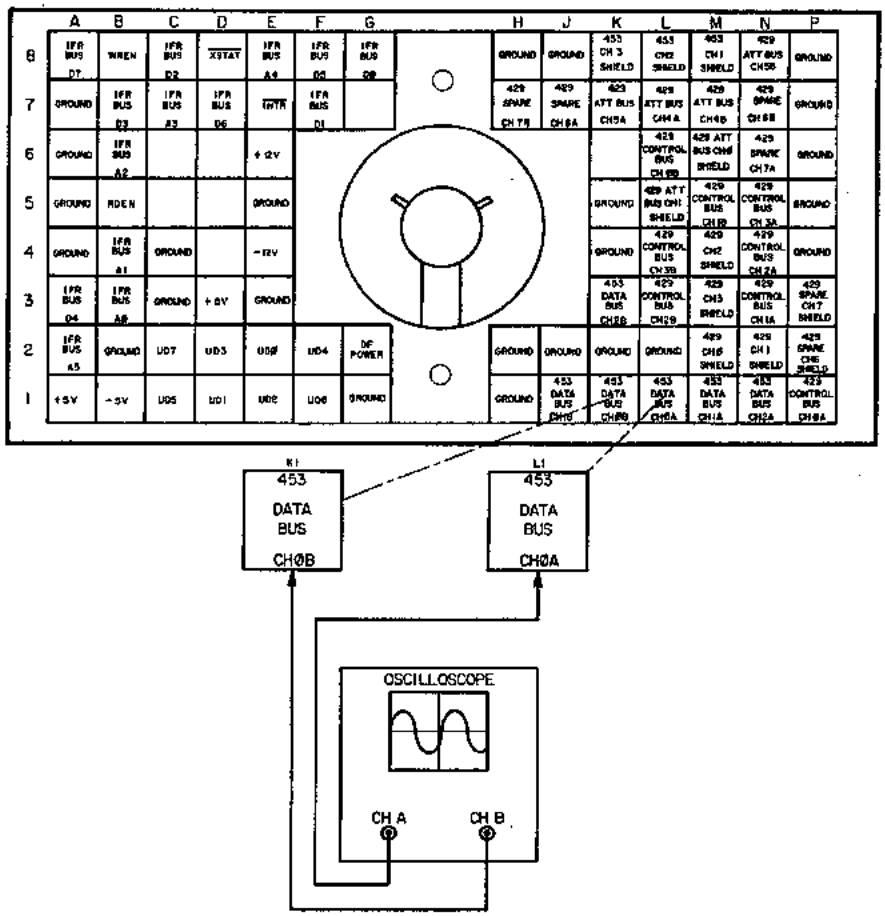
STEP	PROCEDURE
1.	Insure compliance with SDIS interface instructions as described in 1-2-1.
2.	Position IEEE-488 Address Switch, segments 7 and 8, to select desired Start-Up Routine as described in 1-2-1.
3.	Position CRT Display Terminal Power Switch to ON.
4.	Insert personality cassette tape (2.4 or subsequent) into tape drive (unless STD-7000 is equipped for PROM operation).
5.	Apply AC power to STD-7000 and check for a blinking cursor on CRT Terminal Display.
6.	Momentarily depress STD-7000 RESET Button.

CAUTION: IF THE AUTOMATIC START-UP ROUTINE WAS SELECTED IN STEP 2, A MEMORY DIAGNOSTIC IS AUTOMATICALLY PERFORMED TO CHECK ALL MEMORY LOCATIONS FOR PROPER OPERATION. IF A MEMORY ERROR IS DETECTED DURING THE MEMORY DIAGNOSTIC, THE START-UP ROUTINE WILL AUTOMATICALLY CHANGE TO DIAGNOSTIC TEST PROGRAM. IF THIS CONDITION OCCURS, QUALIFIED MAINTENANCE PERSONNEL SHOULD REFER TO 2-2-48 BEFORE CONTINUING.

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STEP PROCEDURE

7. Connect Oscilloscope Channel A, X1 Probe to Pin L1 of STD-7000 Rear Panel Connector J416 (refer to 2-2-2, Figure 38).



DATA Bus (Channel 1) Evaluation Set-Up Diagram
Figure 38

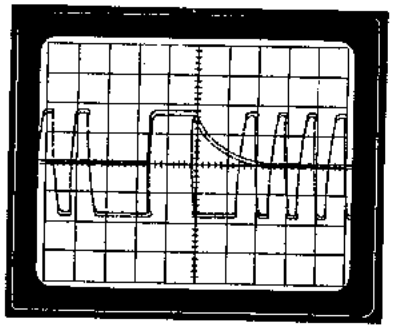
8. Connect Oscilloscope Channel B, X1 Probe to Pin K1 of J416 (refer to 2-2-2, Figure 38).

9. Apply AC Power to Oscilloscope, sum Channels A and B, invert Channel B and set for Delayed Sweep.

10. Using Keypad, display DATA BUS OUTPUT PAGE (2) on CRT Display Terminal.

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STEP	PROCEDURE
11.	Change SEND (Data Field 2) to (1,–,–).
12.	Change LABEL (Data Field 4) to (377).
13.	Change RATE (Data Field 3) to (255).
14.	Adjust Oscilloscope to display Start Sync (beginning of data) and verify waveform to be 1.5 µSec High, then 1.5 µSec Low.
15.	Adjust Oscilloscope to display End Sync (end of message) and verify waveform to be 1.5 µSec Low, then 1.5 µSec High.



Start and End Sync Overlap
Figure 39

16. Using Oscilloscope Delta Time Controls, count number of bits between start sync and end sync. There should be 1600 bits, that is, 1.606 mS from start sync to end Sync.

    NOTE: To count bits, overlap start sync and end sync of same mesage as shown in 2-2-2, Figure 39.

17. Measure bit Rise Time and verify it to be 100±10 nSec.

18. Measure bit Fall Time and verify it to be 100±10 nSec.

19. With Oscilloscope set at 2V/DIV, verify Bus Amplitude of 10±1 Vp-p.

20. Change PATTERN (Data Field 25) to (CROSS HATCH) while observing FORMAT (Data Field 1). FORMAT should change from (STD) to (X/Y).

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STEP PROCEDURE

21. Using Keypad, display DATA BUS INPUT PAGE (5).

22. Change LABEL (Data Field 3) to (377).

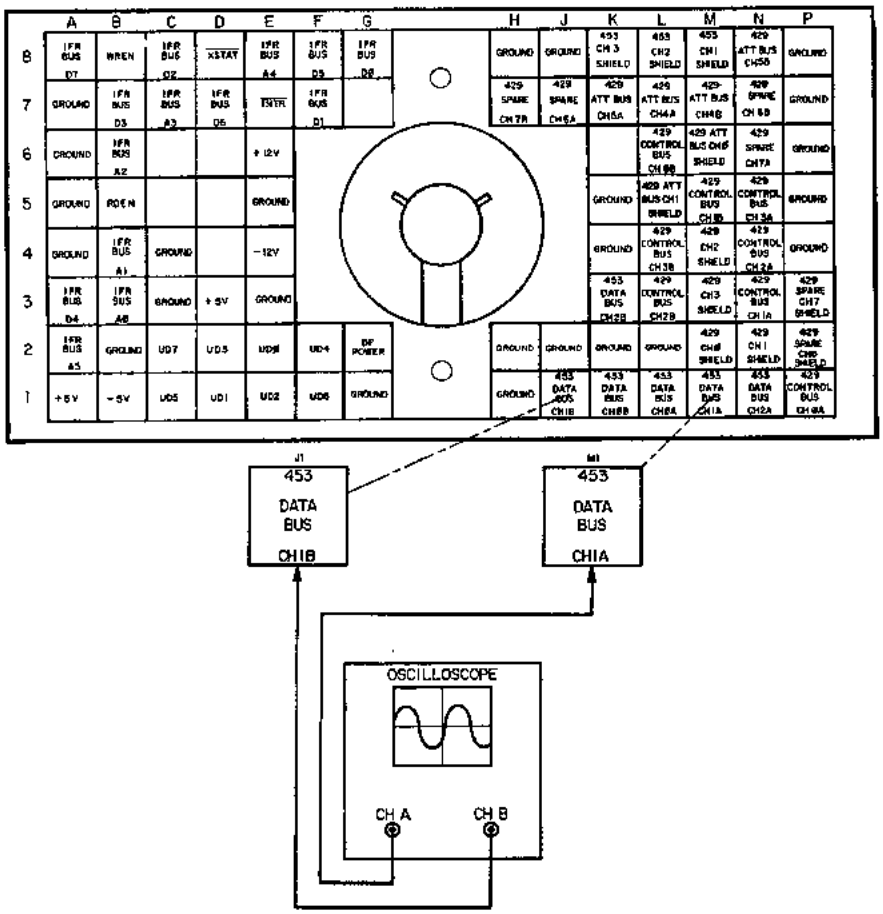
23. Verify data reception on BUS #1 only. To accomplish this, change BUS (Data Field 1) to (2) and then to (3). On Buses (2) and (3), Data Fields 1 through 6 should reflect the same data as BUS (1), however no other data should be indicated.

24. Change LABEL (Data Field 3) to (252) and note data reception ceases on BUS (1).

    NOTE: Restore LABEL to (377) upon completion of Step 24.

25. Using Keypad, display DATA BUS OUTPUT PAGE (2).

26. Change SEND (Data Field 2) to (–,–,–).



Data Bus (Channel 2) Evaluation Set-Up Diagram
Figure 40

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STEP PROCEDURE

27. Disconnect Oscilloscope Channel A Probe from Pin L1 and connect to Pin M1 (refer to 2-2-2, Figure 40).

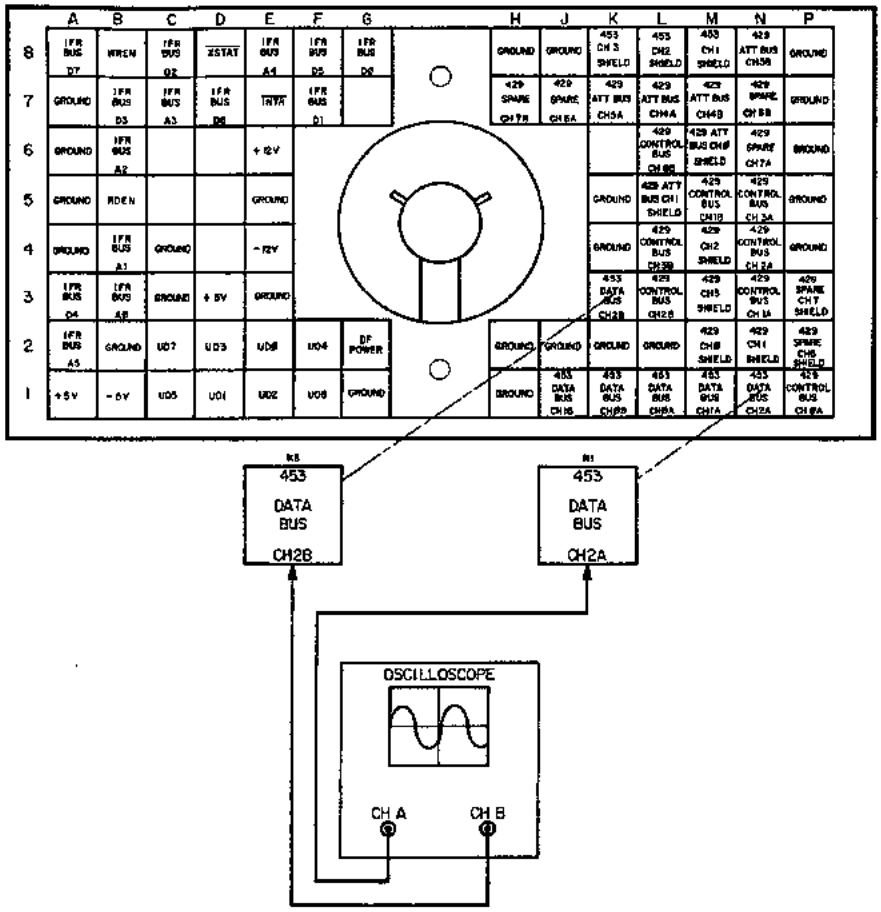
28. Disconnect Oscilloscope Channel B Probe from Pin K1 and connect to Pin J1 (refer to 2-2-2, Figure 40).

29. Change SEND (Data Field 2) to (—,2,—).

30. Repeat Steps 14 through 21 for Bus #2.

31. Change BUS (Data Field 1) to (2).

32. Verify data reception on BUS #2 only. To accomplish this, change BUS (Data Field 1) to (1) and then to (3). On Buses (1) and (3), Data Fields 1 through 6 should reflect the same data as Bus (2), however no other data should be indicated.



Data Bus (Channel 3) Evaluation Set-Up Diagram
Figure 41

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STEP	PROCEDURE
33.	Change LABEL (Data Field 3) to (125) and note data reception ceases on Bus (2). NOTE: Restore LABEL to (377) upon completion of Step 33.
34.	Using Keypad, display DATA BUS OUTPUT PAGE (2).
35.	Change SEND (Data Field 2) to (–,–,–).
36.	Disconnect Oscilloscope Channel A Probe from Pin M1 and connect to Pin N1 (refer to 2-2-2, Figure 41).
37.	Disconnect Oscilloscope Channel B Probe from Pin J1 and connect to Pin K3 (refer to 2-2-2, Figure 41).
38.	Change SEND (Data Field 2) to (–,–,3).
39.	Repeat Steps 14 through 21 for Bus (3).
40.	Change BUS (Data Field 1) to (3).
41.	Verify data reception on BUS (3) only. To accomplish this, change BUS (Data Field 1) to (1) and then to (2). On Buses (1) and (2), Data Fields 1 through 6 should reflect the same data as Bus (3), however no other data should be indicated.
42.	Change LABEL (Data Field 3) to (ØØØ) and note data reception ceases on Bus (3). NOTE: Restore LABEL to (377) upon completion of Step 42.
43.	Using Keypad, display DATA BUS OUTPUT PAGE (2).
44.	Change SEND (Data Field 2) to (–,–,–).
45.	Disconnect Oscilloscope Channel A and B Probes from STD-7000 Rear Panel Connector J416.
46.	Change SEND (Data Field 2) to (1,2,3). NOTE: Insure PATTERN (Data Field 25) indicates (BAR).
47.	Using Keypad, display DATA BUS INPUT PAGE (5).

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STEP PROCEDURE

48. Change BUS (Data Field 1) to (1).

49. Change START BIN (Data Field 6) to reflect the numbers in the Start Bin Column of 2-2-2, Table 13and verify BIN A through H change to coincide with levels indicated.

NOTE: START BIN (Data Field 6) will not accept inputs above (5Ø4).

	BIT							
START BIN	A	B	C	D	E	F	G	H
(057)	0	0	0	0	0	0	0	0
(065)	1	1	1	1	1	1	1	1
(122)	1	1	1	1	1	1	1	2
(129)	2	2	2	2	2	2	2	2
(186)	2	2	2	2	2	2	2	3
(193)	3	3	3	3	3	3	3	3
(250)	3	3	3	3	3	3	3	4
(257)	4	4	4	4	4	4	4	4
(314)	4	4	4	4	4	4	4	5
(321)	5	5	5	5	5	5	5	5
(378)	5	5	5	5	5	5	5	6
(385)	6	6	6	6	6	6	6	6
(442)	6	6	6	6	6	6	6	7
(449)	7	7	7	7	7	7	7	7

Data Bus Start Bin Inputs
Table 13

50. Change BUS (Data Field 1) to (2) and repeat Step 49.

51. Change BUS (Data Field 1) to (3) and repeat Step 49.

52. Using Keypad, display DATA BUS OUTPUT PAGE (2).

53. Change SEND (Data Field 2) to (–,–,–).

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3. Calibration

A. General

This section contains the calibration requirements for the STD-7000 Bus Controller. Currently, this requirement is limited to a +5 V calibration adjustment of the Power Supply Module. The Power Supply +5 V Calibration Adjustment should be performed when:

1. STD-7000 fails to meet the electrical requirements in 2-2-2.

2. STD-7000 Power Supply is found to be defective during troubleshooting and consequently replaced.

   NOTE: Normally, a new Power Supply Module is delivered calibrated; however, it is recommended that the outputs of the new power supply be checked before use.

3. Recommended twelve month calibration interval is due.

3.C. contains a tape write procedure for use when a new or existing mini-cassette personality tape requires a rewrite.

A tape rewrite requirement may exist when:

1. Additional tapes are desired.

2. As a result of complying with the Troubleshooting Flowcharts in 2-2-4.

(1) Accessory Test Equipment Requirements

Appendix B at the rear of this manual contains a comprehensive list of test equipment suitable for performing any of the procedures in this manual. Any other equipment meeting the specifications listed in Appendix B may be substituted in place of the recommended models.

(2) Disassembly Requirements

To perform the calibration procedure in this section, the Top Cover (2) (2-2-5, Figure 69) must be removed from the STD-7000. (Refer to 2-2-5 for top cover removal instructions.)

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(3) Safety Precautions

As with any piece of electronics equipment, extreme caution should be taken when troubleshooting or working with live circuits. Even though high voltage potentials only exist within the STD-7000 Power Supply, the presence of potentially lethal voltages within accessory test equipment may also exist within the STD-7000 through test probes. Maintenance personnel must not remove accessory test equipment covers anytime unit is connected to a power source. Component replacement and internal adjustments must be made by qualified maintenance personnel. When performing maintenance on the STD-7000, be sure to observe the following precautions:

WARNING: DO NOT REMOVE POWER SUPPLY FROM STD-7000 AND/OR REMOVE POWER SUPPLY COVER WITH EXTERNAL AC POWER CONNECTED. AFTER EXTERNAL AC POWER IS REMOVED, WAIT A MINIMUM OF 5 MINUTES BEFORE HANDLING, TO ALLOW HIGH VOLTAGE CONTROL CIRCUIT TO DISSIPATE.

WARNING: THE REAR PANEL CORCOM CONNECTOR AND POWER SUPPLY ASSEMBLY CARRY 120 OR 240 VAC AS LONG AS POWER CORD IS CONNECTED TO THE STD-7000 AND EXTERNAL AC POWER SOURCE. DO NOT CONTACT THESE OR ANY ASSOCIATED COMPONENTS DURING MAINTENANCE OPERATIONS.

WARNING: REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING MAINTENANCE ON "LIVE" CIRCUITS.

WARNING: WHEN WORKING WITH LIVE CIRCUITS, KEEP ONE HAND IN POCKET OR BEHIND BACK, TO AVOID SERIOUS SHOCK.

WARNING: USE ONLY INSULATED TOOLS WHEN WORKING WITH LIVE CIRCUITS.

WARNING: FOR ADDED INSULATION, PLACE RUBBER BENCH MAT UNDERNEATH ALL POWERED BENCH EQUIPMENT, AS WELL AS A RUBBER MAT UNDERNEATH TECHNICIAN.

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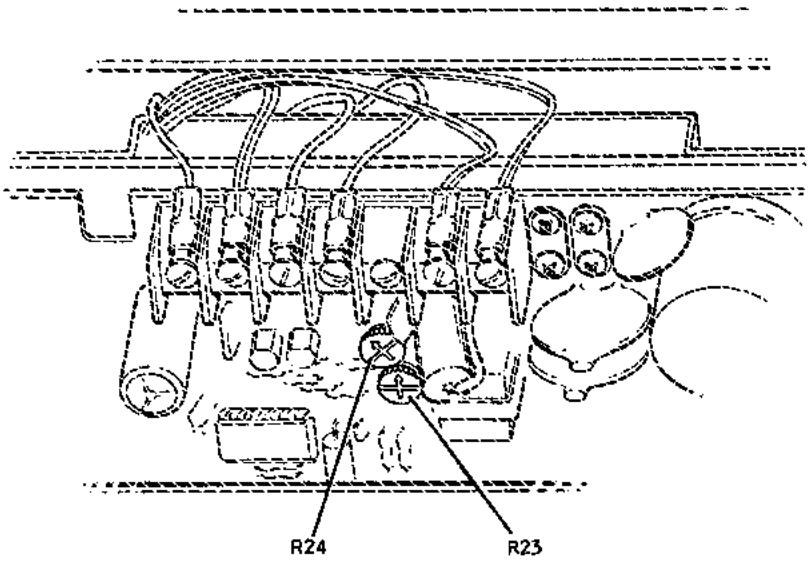
B. Calibration Procedures

(1) SIERRACIN Power Supply +5V Adjustment

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter (100KΩ/V)

1 Small Slotted Non-conductive Screwdriver or Adjustment Tool

TEST SET-UP DIAGRAM:



+5 V Adjustment Point (Sierracin)
Figure 42

STEP	PROCEDURE
1.	Remove STD-7000 top dust cover (2) (2-2-5, Figure 69) per instructions in 2-2-5.
2.	Verify proper operating voltage is selected on STD-7000 by checking orientation of Programmable PC Board, within CORCOM (VS & F) Connector, to the AC line voltage available.
3.	Connect Digital Voltmeter to either Power Supply Connector #1 or 2 (orange wires) of 7 screw side on terminal block (refer to 2-2-5, Table 14 for terminal block illustration).

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STEP	PROCEDURE
4.	Depress AC Power Switch (5) to ON position. Note illumination of AC Power Switch Button, as well as four red LEDs on Power Supply PC board. Allow 5 minute warmup before continuing.
5.	Looking down into STD-7000 (toward Power Supply Module), locate R23 (+5 V Adj) adjustment screw on Power Supply PC Board (Refer to 2-2-3, Figure 42).
	WARNING: DO NOT REPOSITION R24 LIMIT ADJUSTMENT SCREW. REPOSITIONING OF THIS SCREW (DEPENDING ON WHICH WAY SCREW IS TURNED) COULD CAUSE AN ELECTRICAL FIRE, OVER VOLTAGE SITUATION, OR UNDER CURRENT OPERATION OF POWER SUPPLY.
6.	Adjust R23 as necessary until Digital Voltmeter indicates +5V (±0.2V).
7.	Disconnect Digital Voltmeter.
8.	Replace top dust cover.

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(2) IFR Universal Power Supply +5V Adjustment

SPECIAL ACCESSORY EQUIPMENT REQ'D: 1 Digital Voltmeter (100KΩ/V)

1 Small Slotted Non-conductive Screwdriver or Adjustment Tool

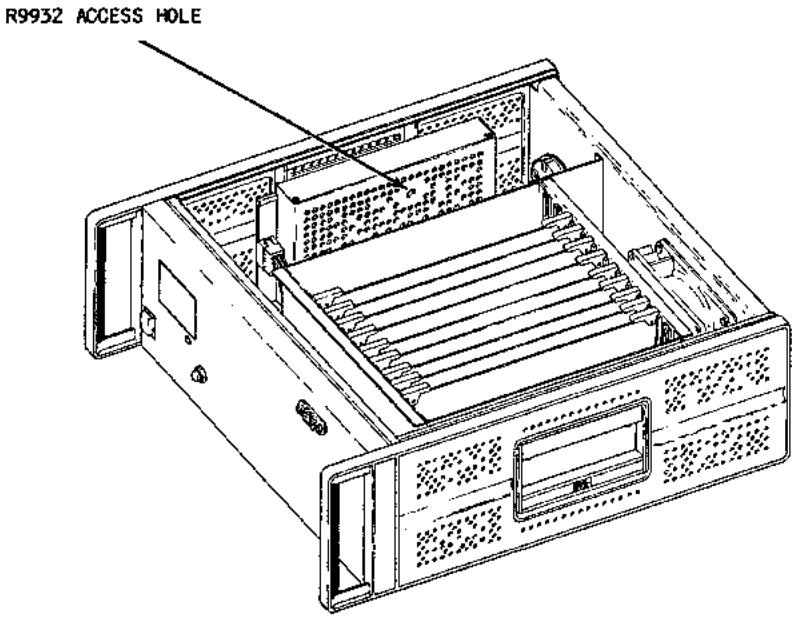
WARNING: DO NOT USE METAL SCREWDRIVER FOR POWER SUPPLY ADJUSTMENT. METAL TIP OF SCREWDRIVER COULD COME IN CONTACT WITH HIGH VOLTAGE CONTROL CIRCUIT (SEE STEP 5).

TEST SET-UP DIAGRAM: None

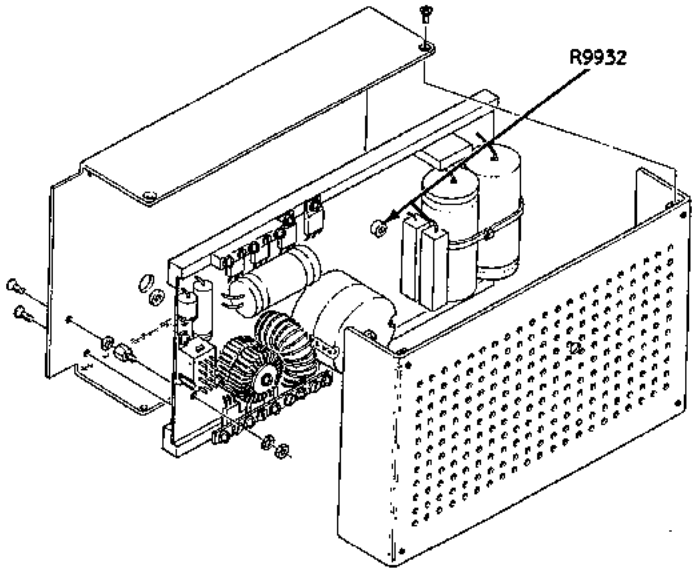
STEP	PROCEDURE
1.	Remove STD-7000 top (2) and bottom (25) dust covers (2-2-5, Figure 69) per instructions in 2-2-5.
2.	Verify proper operating voltage is selected on STD-7000 by checking orientation of Programmable PC Board, within CORCOM (VS & F) Connector, to the AC line voltage available.
3.	Connect Digital Voltmeter to either pin 1 or 2 of J405 thru J412 (Technician's choice).
4.	Depress AC Power Switch (5) to ON position (note illumination of AC Power Switch Button) and allow 5 minute warm-up before continuing.
5.	Adjust R9932 (refer to 2-2-3, Figure 43/44 as necessary until Digital Voltmeter indicates +5 V (±0.2V).
6.	Disconnect Digital Voltmeter leads.
7.	Replace top and bottom dust covers.

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STEP PROCEDURE



R9932 Adjustment Point Access Hole
(IFR Universal Power Supply Only)
Figure 43



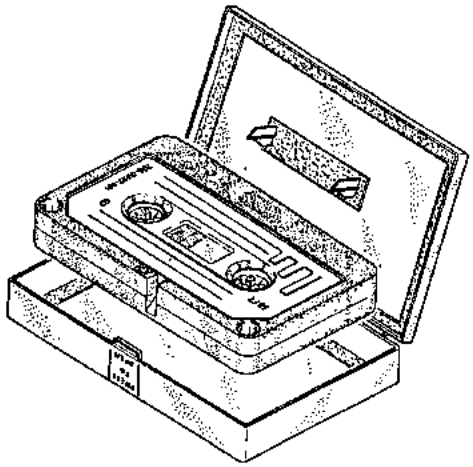
R9932 Adjustment Point (IFR Universal
Power Supply Cover Removed)
Figure 44

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C. STD-7000 Personality Tape Duplication

The following procedure is intended for use by maintenance personnel when a requirement to write or rewrite an STD-7000 personality tape exists.

CAUTION: TO PRECLUDE IRREVERSIBLE DAMAGE TO TAPE, DO NOT TEST RAM AND WRITE TAPE CONSECUTIVELY.



Certified Mini-Data Cassette Tape
Figure 45

STEP	PROCEDURE
1.	Verify correct interface between STD-7000 and CRT Display. Insure STD-7000 Bus Controller is operating normally in accordance with 1-2-3.
2.	Position STD-7000 IEEE-488 Address Switch (7) (Segments 7 and 8) to OFF.
3.	Apply External AC Power to Rear Panel CORCOM Connector (3).
4.	Depress AC Power Switch (5) to illuminate switch button and apply AC power to unit.
5.	Momentarily depress RESET Switch (3) and observe Diagnostic Menu on CRT Display screen.
6.	Insert a known valid (loadable) cassette tape (version 2.4 or later) in Tape Drive (1).
7.	Using Numeric Keypad (1-2-2, Figure 6), select Menu Item 1 (1 = LOAD TAPE).

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STEP PROCEDURE

NOTE: Allow between 1½ to 2 minutes load time from completion of initial rewind, to the illumination of the letter L on the KEYIN Line. The letter L indicates completion of loading sequence.

8. Remove good tape from Tape Drive.

9. Insert new blank tape or old tape (to be rewritten) in tape drive.

CAUTION: BE SURE SIDE TO BE WRITTEN IS TOWARD REAR OF STD-7000.

10. Using Numeric Keypad, enter 4 (4 = WRITE TAPE Key).

11. While depressing the lower left (blank) key, enter 8 (8 = GO 4000). Tape should begin to rewind.

NOTE: If tape fails to rewind, reattempt sequence indicated in Step 10.

NOTE: Allow approximately 4 minutes to elapse between completion of tape rewind sequence and appearance of the letter V on KEYIN Line. The letter V indicates tape has been written and verified.

NOTE: If other side of cassette tape is to be written, momentarily depress RESET Switch (3), turn tape cassette over and repeat Step 10.

12. Reposition IEEE-488 Address Switch (7) segments 7 and 8 to ON.

13. Momentarily depress RESET Switch (3) to initiate Automatic Start-Up Routine. Select and enter 2 LOAD AND EXECUTE TAPE PROGRAM.

NOTE: During initial start-up, it may not be necessary to select and enter 2 (LOAD AND EXECUTE TAPE PROGRAM).

NOTE: When Master Menu appears on CRT Display, the tape side (to the rear of STD-7000) is then verified useable.

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STEP	PROCEDURE
	NOTE: If MEM (Memory) or CS (Check Sum) errors appear at any time during this procedure, refer to applicable troubleshooting flow chart(s) in 2-2-4.

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4. Troubleshooting Flowcharts

A. General

This section contains tabular flowcharts designed to aid the technician in troubleshooting the STD-7000 Bus Controller. These flowcharts will enable the technician to isolate a given malfunction down to an individual module or PC board assembly. Typically, the technician will refer to the flowcharts in this section to isolate a trouble symptom which may have been detected during normal operation or while performing the Performance Evaluation Procedures in 2-2-2.

(1) How To Use Tabular Flowcharts

Each of the flowcharts in this section are designed to isolate a specific trouble symptom down to a repairable/replaceable module or PC board. Once a trouble symptom has been identified, the technician should locate the proper troubleshooting flowchart and proceed, beginning with Step 1. Each step has a YES and NO block and the numbers in these blocks indicate the next step the technician must perform. The technician should continue compliance with the flowchart until the faulty module or PC board is identified and repair/replacement recommendations are indicated.

(2) Troubleshooting Hints

Before proceeding with extensive troubleshooting, it is advisable that the technician first make a few simple checks, which may be related to the cause of the malfunction. These checks may save the technician many hours of labor, which might needlessly be spent on extensive troubleshooting.

(a) GPIB Address Switches

Improper address switch position will cause improper indications during start up routines.

(b) Visual Inspection

Visually inspect any components within the STD-7000 which may have a relationship to the malfunction. In many instances, a malfunction may be caused by loose connections, broken wires, unsoldered connections, damaged components, bent connector pins, etc. Also look for signs of excessive heat as evidenced by burned or charred components.

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(c) Performance Evaluation

Before attempting any troubleshooting, make sure all appropriate performance evaluation procedures in 2-2-2 have been performed. In many cases, these procedures will isolate a trouble symptom to a particular module, thereby making any subsequent troubleshooting easier or unnecessary.

(3) Safety Precautions

As with any piece of electronic equipment, extreme caution should be taken when troubleshooting live circuits. The power supply module is the only module capable of generating lethal voltages within the STD-7000. Because of the possibility of stray voltage, it is recommended that extreme caution be exercised while working on the STD-7000 circuits while the exterior covers are removed and external AC power is connected to the rear panel CORCOM connector. Also, keep in mind that certain pieces of accessory test equipment contain extremely high voltage potentials, capable of causing serious Bodily Injury or Death. When performing the troubleshooting procedures in this section, be sure to observe the precautions listed in each piece of accessory test equipment's operations manual as well as the following:

WARNING: THE STD-7000 REAR PANEL CORCOM CONNECTOR, CRT POWER RECEPTACLE AND ASSOCIATED WIRING CARRY EITHER A 120 OR 240 VAC AS LONG AS EXTERNAL POWER CORD IS CONNECTED TO STD-7000 AND EXTERNAL POWER SOURCE. DO NOT CONTACT THESE OR OTHER ASSOCIATED COMPONENTS DURING TROUBLESHOOTING.

WARNING: REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY TROUBLESHOOTING PROCEDURES INVOLVING LIVE CIRCUITS.

WARNING: USE INSULATED TROUBLESHOOTING OR ADJUSTMENT TOOLS WHEN WORKING WITH LIVE CIRCUITS.

WARNING: HEED ALL WARNINGS AND CAUTIONS CONCERNING MAXIMUM VOLTAGES AND POWER INPUTS OF ACCESSORY TEST EQUIPMENT.

CAUTION: DO NOT REMOVE OR REPLACE ANY MODULE OR COMPONENT WHILE STD-7000 IS POWERED.

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(4) Test Equipment Requirements

Appendix B, at the rear of this manual, contains a comprehensive list of test equipment suitable for performing any of the troubleshooting procedures in this section. Any other test equipment meeting the specifications listed in Appendix B may be substituted in place of recommended models.

(5) Disassembly/Reassembly Requirements

To use the troubleshooting flowcharts in this section, the top and possibly the bottom dust covers require removal from the STD-7000.

Refer to 2-2-5 for cover removal(s), module or PC board removal and/or module disassembly/reassembly instructions.

(6) Start-Up Routine Errors

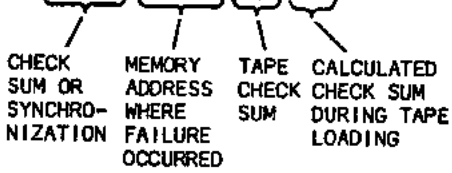
The eight-position IEEE-488 Address Switch located on the STD-7000 Rear Panel has two functions. One function is to select the desired bus address, using switch segments 1 thru 6 when STD-7000 is interfaced with IEEE-488 Bus, and the other function is to select one of four start-up routines described in 1-2-3. The automatic start-up routine performs virtually all powerup functions automatically from the time the STD-7000 Power Switch is activated until an initial tape or PROM personality display appears on CRT. Under this condition, during tape loading operations, the technician may encounter several error indications which halt the automatic sequence until the error is corrected. One such error most commonly encountered is the Check Sum or Sync error. An example indication with explanation is shown in 2-2-4, Figure 46.

NOTE: When the check sum (example 2) error is indicated, the technician can be confident and assume the problem lies with the magnetic cassette personality tape. Therefore the technician should obtain and use a known good replacement tape before initiating any further troubleshooting procedures. If new or different tape will not correct error condition, the technician should then proceed to 2.2.4.B(1).

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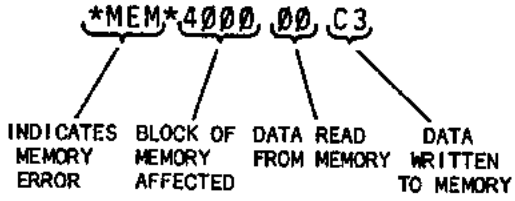
EXAMPLE 1: *SYNC*6CØØ BØ 74

EXAMPLE 2: *CS*6CØØ BØ 74



Example Check Sum (CS) and Synchronization (SYNC) Error Indications
Figure 46

If a memory error indication is detected during the memory diagnostic test, the start-up routine automatically indicates the STD-7000 Diagnostic Menu. If this condition should occur, proceed to 2-2-4B(2). An example of memory error indication and explanation is shown in 2-2-4, Figure 47.



Example Memory (MEM) Error Indication
Figure 47

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B. Start-Up Routine Failures

(1) Check Sum (CS) Error

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: NONE

STEP	DIRECTIONS	DECISION	YES	NO
1.	Check for proper installation and security of CPU (yellow), I/O (blue), RAM OR EPROM (if applicable) (orange) PC Boards within STD-7000 Card Cage.	Are all PC bds correctly installed and secured within the card cage?	2	3
2.	Interface STD-7000 with ESP 6515 CRT Display Terminal, Display Terminal Interface and Numeric Keypad in accordance with instructions in 1-2-1.		4	
3.	Remove and correctly install plug-in PC boards.		5	
4.	Install different personality mini-cassette tape (other than tape in Tape Transport at time of error).		5	
5.	Set IEEE-488 Address Switches (STD-7000 Rear Panel) to Diagnostic Start-Up Menu (segments 7 and 8 to OFF).		6	
6.	Depress AC Power Switch (5) to ON position and momentarily depress RESET Switch (3) (STD-7000 Front Panel).	Is STD-7000 Diagnostic Menu shown on CRT?	7	8
7.	Using Keypad, key-in 5 (5 = EXECUTE TAPE) and listen for audible indication of tape rewinding, followed by a tape loading sequence.	Did tape successfully load? NOTE: System Master Menu will automatically appear upon successful completion of tape loading.	9	
8.	Recheck IEEE-488 Address Switch segments for proper settings (7 and 8 OFF).		6	
9.	Original personality tape faulty. Refer to 2-2-3 for rewrite instructions.			

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STEP	DIRECTIONS	DECISION	YES	NO
	NOTE: Inspect original tape for obvious damage, if damage is apparent, obtain new tape.			
10.	Flip cassette personality tape to other side and attempt to load as described in Steps 6 and 7.	Did tape successfully load?	11	12
11.	Previously used cassette tape faulty. Refer to 2-2-3, for rewrite instructions. NOTE: Inspect original tape for obvious damage, if damage is apparent, obtain new tape.			
12.	Remove and replace X832 (Z-80 CTC) and X834 (Z-80 PIO) located on CPU PC Board (2-2-8, Figure 100). CAUTION: REMOVE ELECTRICAL POWER FROM STD-7000 BEFORE REMOVING PC BOARD.			
13.	Make another attempt to load personality tape into memory using Steps 5 thru 7.	Did tape successfully load?	14	15
14.	No defect noted.			
15.	Remove 16-wire, ribbon cable between Tape Drive and connector J419. Check continuity from pin to pin.	Did continuity check satisfactorily?	16	17
16.	Visually check 4.7K Resistors (R465, R466, R467 and R468), located on bottom side of Motherboard (2-2-8, Figure 96), for loose connections, worn sleeving, improper installation, etc.	Are resistors installed properly?	18	19
17.	Repair or replace faulty Ribbon Cable.			

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STEP	DIRECTIONS	DECISION	YES	NO
18.	Connect Oscilloscope Channel A Probe to pin 13 of J419 (2-2-8, Figure 96). Adjust Oscilloscope Controls to indicate High Logic Levels.	Is indicated High Logic Level 3.5 to 5V?	20	21
19.	Remove and replace or properly install affected resistor(s).			
20.	Adjust Oscilloscope Controls to indicate Low Logic levels.	Is indicated Low Logic Level Ø - Ø.5V?	22	21
21.	Tape Drive Assembly faulty. Refer to Braemar Computer Devices, CM-600 MINI-DEK Digital mini-cassette transport instruction and maintenance manual for repair instructions. If necessary, refer to 2-2-5 for tape drive removal instructions.			
22.	Adjust Oscilloscope Controls to Indicated Bit Cell Time.	Is Bit Cell Time between 160 to 170 µSec?	23	21
23.	Fault within circuitry of CPU PC Board. Repair or replace.			

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(2) Memory Error

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: NONE

STEP	DIRECTIONS	DECISION	YES	NO
1.	Insure external AC power has has been removed from STD-7000, then remove CPU RAM PC Boards (orange) from Card Cage and Inspect Connector J402 (Motherboard) for damage, corrosion or other foreign matter.	Is J402 damaged, corroded, or contaminated with foreign matter?	2	3
2.	Repair/Replace damaged connector or clean corrosion, foreign matter from connector pins.		3	
3.	Check CPU and RAM PC Boards for obvious damage (burn spots, cracks or missing ICs).	Did RAM PC Board check OK?	4	5
4.	Check CPU and RAM PC Boards 100-pin card edge plug for damage and/or corrosion.	Did Card edge plug check satisfactorily?	6	7
5.	Repair obvious damage or replace RAM PC Board with serviceable PC board.		4	
6.	Install RAM PC Board in its assigned slot (orange) within Card Cage.		8	
7.	Clean corrosion or other foreign matter from connector and/or repair damage or replace PC board, if necessary.		6	
8.	Check interface of STD-7000 with ESP 6515 Display Terminal verify connections are in accordance with Instructions in 1-2-1.		9	
9.	Set IEEE-488 Address Switches Switches (STD-7000 Rear Panel) to the Diagnostic Menu Start-up sequence (segments 7 and 8 OFF).		10	
10.	Depress POWER Switch (5) to apply AC power to STD-7000 and Display Terminal.		11	

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STEP	DIRECTIONS	DECISION	YES	NO
11.	Momentarily depress RESET Button (3).	Is STD-7000 Diagnostic Menu Indicated on CRT?	12	13
12.	Using Numeric Keypad, key in 9 (9 = TEST RAM). Observe an eight digit arbitrary number, similar to indication shown in 2-2-4, Figure 46, followed by a continuous series of asterisks.	Have five or more consecutive asterisks appeared on CRT Screen?	14	15
13.	Recheck position of IEEE-488 Switch Segments. (7 and 8 should be OFF.) NOTE: Check IEEE-488 Switch for proper installation (could be installed in reverse).		11	
14.	Momentarily depress RESET Button (3) (STD-7000 Front Panel).		16	
15.	Identify and note block of memory affected by using example in 2-2-4, Figure 47, and comparing it with memory error indicated.		17	
16.	Using Numeric Keypad, enter 2 (2 = VERIFY TAPE). After approximately 90 seconds a small v should appear to the right of the cursor.	Did small v appear to right of cursor?	18	17
17.	Momentarily depress RESET Button (3), eject tape, flip to other tape side and reinstall in Tape Transport.		18	
18.	Using Numeric Keypad, attempt to load tape into RAM by entering 5 (5 = EXECUTE TAPE).	Did tape load successfully within approximately 90 seconds?	19	20
19.	Original cassette tape or information encoded on original magnetic tape is altered. Suggest tape rewrite (refer to 2-2-3 for instructions).			

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STEP	DIRECTIONS	DECISION	YES	NO
	NOTE: If tape fails to re-write after two attempts, assume tape cassette has failed and obtain replacement.			
20.	Momentarily depress RESET Button (3).		21	
21.	Obtain and install different 2.4 version magnetic tape (other than tape causing malfunction).		22	
22.	Using Numeric Keypad, enter 5 (5 = EXECUTE TAPE).	Did tape successfully load within 90 seconds?	19	23
23.	Type of malfunction or error (Memory or CS) should be indicated on CRT screen. If CS error, go to 2-2-4B(1). If Memory error, go to 2-2-4B(2).	Does memory error identify similarly with memory error example shown in 2-2-4, Figure 46 or 2-2-4, Figure 47?	24	15
24.	Refer to Memory Map (Appendix E) for location of affected block of memory. Once identified, replace ICs corresponding to affected block of memory. CAUTION: REMOVE EXTERNAL AC POWER FROM STD-7000 BEFORE REMOVING ANY PC BOARD OR COMPONENTS.		14	

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C. CPU Card Failures

(1) CPU Card Inoperative

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove top dust cover from STD-7000 per instructions in 2-2-5.		2	
2.	Interface STD-7000 with ESP 6515 CRT Display Terminal, Display Terminal Interface and Numeric Keypad in accordance with instructions in 1-2-1.		3	
3.	Remove CPU Card (yellow) from Card Cage and place on 100 pin extender PC board. Reinstall in CPU slot of Card Cage.		4	
4.	Connect external AC power, depress AC Power Switch (5) to ON and momentarily depress RESET Switch (3).		5	
5.	Connect Oscilloscope X1 Probe Probe to Pin 14 of X807 (refer to CPU Card Circuit Schematic in 2-2-7, Figure 87, PC Board Layout Drawing in 2-2-8, Figure 100). Adjust Oscilloscope controls to observe 9.900 MHz.	Is an indication of 9.9 MHz indicated?	6	7
6.	Connect Oscilloscope X1 Probe to Pin 6 of Z-80 CPU (X802) and adjust Oscilloscope controls to observe 2.475 MHz with a high level voltage of 4.4 Volts or greater and a low level voltage of 0.5 Volt or less.	Is proper clock (Ω) signal indicated?	8	9
7.	Connect Oscilloscope X1 Probe to pin 13 of X805.	Is 9.9 MHz indicated?	10	11
8.		Is frequency (2.475 MHz) correct?	12	9

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STEP	DIRECTIONS	DECISION	YES	NO
9.	Connect Oscilloscope X1 Probe to pin 14 of X807.	Is 9.9 MHz signal indicated?	13	7
10.	Connect Oscilloscope X1 Probe to pin 10 of X805.	Is 9.9 MHz signal indicated?	14	15
11.	Replace 9.900 MHz Crystal (Y801) or X805.			
12.		Is voltage correct?	16	17
13.	Connect Oscilloscope X1 Probe to pin 2 of X807.	Is any signal present?	17	18
14.	Using normal troubleshooting procedures, locate and repair short or break in circuit between Y801 and pin 14 of X807.			
15.	Replace X805.			
16.	Replace socketed devices. NOTE: If card not repaired at this point, return card to IFR Systems, Inc., Customer Service for repair or replacement.			
17.	Using normal troubleshooting procedures, check for proper operation of transistors Q802 and/or Q803 and associated circuitry. Replace and/or repair as necessary.			
18.	Replace X807.			

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(2) CPU Card (Tape Related) Malfunction

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Insure all other tape associated modules (tape, tape drive, ribbon cable, motherboard circuit, etc.) are functioning properly before continuing.		2	
2.	Remove external AC power from STD-7000.		3	
3.	Remove Z-80 CTC (X832) and Z-80 PIO (X834) from CPU Card.		4	
4.	Install different (serviceable) ICs in place of X832 and X834. NOTE: The ICs mentioned above are socketed. Replacement IC's can be found on either the 429 Output Card (for Z-80 CTC), I/O Card (for Z-80 PIO) or if desired, swap CTC X832 with X835 (located on same card).		5	
5.	Reapply external AC power to STD-7000.	Does tape now function properly?	6	7
6.	Replace original Z-80 CTC (X832) and Z-80 PIO (X834) with serviceable IC's.			
7.	Malfunction requires extensive maintenance, therefore recommend return of CPU Card to factory for repair or replacement.			

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D. I/O Card Failures

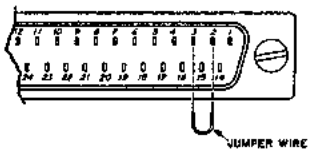
(1) No Terminal Display Operation

SPECIAL ACCESSORY TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

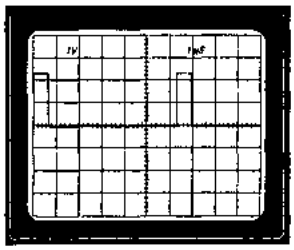
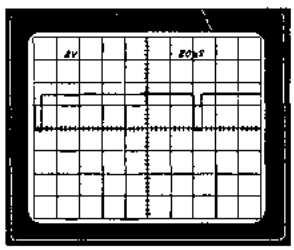
1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove top dust cover from STD-7000 per Instructions in 2-2-5.		2	
2.	Insure external AC power is removed from STD-7000.		3	
3.	Remove I/O card (blue) from STD-7000 Card Cage, install on 100-pin Extender PC board and install assembly in I/O card slot in Card Cage.		4	
4.	Verify eight segment DIP Switch on Terminal Logic PC Board (inside CRT housing access panel) is set as follows: Segments 1 thru 7 to OFF. Segment 8 to ON.		5	
5.	Position segments 7 and 8 of IEEE-488 Address Switch (7) to OFF (STD-7000 Rear Panel).		6	
6.	Connect external AC power to STD-7000 and depress AC Power Switch (5) to ON.		7	
7.	Install mini-cassette personality tape in tape transport and momentarily depress RESET Switch (3).	Is Diagnostic Menu indicated on CRT Display?	8	9
8.	No defect noted.			
9.	Disconnect RS232C plug from STD-7000 Rear Panel Connector J414.		10	

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STEP	DIRECTIONS	DECISION	YES	NO
10.	Jumper Pins 2 and 3 of RS232C plug from terminal as shown in 2-2-4, Figure 48.  RS232C Plug (Jumper Configuration) Figure 48		11	
11.	Depress each key of Numeric Keypad.	Does each number or symbol echo or repeat while key is depressed?	12	13
12.	CRT is operating properly. Remove jumper from RS232C Plug and reconnect plug to J414 on rear panel of STD-7000.		14	
13.	Fault located within CRT Display Terminal. Refer to CRT Manufacturer's (ESPRIT) Maintenance Manual for information concerning the CRT Display Terminal.			
14.	Connect Oscilloscope X1 Probe Probe to pin 7 of X1018.		15	
15.	Depress STD-7000 RESET Switch (3) and observe 9600 Baud Rate at RS232C levels.	Is the 9600 Baud Rate at RS232C levels indicated?	16	17
16.	Problem located between I/O Card Connector (J404) and STD-7000 Rear Panel Connector J414. Locate and repair as necessary.			
17.	Connect Oscilloscope X1 Probe to Pin 19 of X1008.		18	

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STEP	DIRECTIONS	DECISION	YES	NO
18.	Depress STD-7000 RESET Switch (3) and observe 9600 Baud Rate at TTL levels.	Is 9600 Baud Rate at TTL levels indicated?	19	20
19.	Replace X1018.			
20.	Connect Oscilloscope X1 Probe to Pin 9 of X1008.	Is 153.6 kHz clock signal indicated as shown in 2-2-4, Figure 49.  153.6 kHz Clock Signal Figure 49	21	22
21.	Connect Oscilloscope X1 Probe to Pin 11 of X1008.	Is there indication of a negative going pulse every 120 µS as shown in 2-2-4, Figure 50?  Negative Going Pulse Figure 50	23	24
22.	Replace X1009.			
23.	Replace X1008.			
24.	Replace X1001 and/or X1005.			

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(2) No Numeric Keypad Response

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove top dust cover from STD-7000 per Instructions in 2-2-5.		2	
2.	Insure external AC power is removed from STD-7000.		3	
3.	Remove I/O card (blue) from STD-7000 Card Cage, Install on 100-pin Extender PC board and install assembly in I/O card slot in Card Cage.		4	
4.	Verify eight segment DIP Switch on Terminal Logic PC Board inside CRT housing access panel is set as follows: Segments 1 thru 7 to OFF. Segment 8 to ON.		5	
5.	Position segments 7 and 8 of IEEE-488 Address Switches (7) to OFF (STD-7000 Rear Panel).		6	
6.	Connect external AC power to STD-7000 and depress AC Power Switch (5) to ON.		7	
7.	Install mini-cassette personality tape in tape transport and momentarily depress RESET Switch (3).	Is Diagnostic Menu Indicated on CRT Display?	8	9
8.	No defect noted.			
9.	Disconnect RS232C plug from STD-7000 Rear Panel Connector J414.		10	

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STEP	DIRECTIONS	DECISION	YES	NO
10.	Jumper Pins 2 and 3 of RS232C plug as shown in 2-2-4, Figure 48.			
11.	Depress each key of Numeric Keypad.	Does each number or symbol echo or repeat while key is depressed?	12	13
12.	CRT is operating properly. Remove jumper from RS232C Plug and reconnect plug to J414 on rear panel of STD-7000.		14	
13.	Fault located within CRT Display Terminal. Refer to CRT Manufacturer's (ESPRIT) Maintenance Manual for information concerning the CRT Display Terminal.			
14.	Connect Oscilloscope X1 Probe to pin 4 of X1017.		15	
15.	Continuously depress any numbered key (0 thru 9) on Numeric Keypad and observe 9600 Baud Rate at RS232C levels on Oscilloscope.	Is 9600 Baud Rate at RS232C levels indicated?	16	17
16.	Connect Oscilloscope X1 Probe to Pin 3 of X1008 and depress same numbered key as in Step 15.	Is 9600 Baud Rate at indicated TTL levels?	18	19
17.	Fault located in circuit between I/O Card Connector J404 and STD-7000 Rear Panel Connector J414. Using normal troubleshooting procedures, locate and repair short/break in circuit as necessary.			
18.	Replace X1008.			
19.	Replace X1017.			

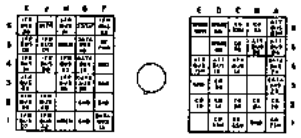
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(3) No IFR Bus Communication With Discrete Functions Unit

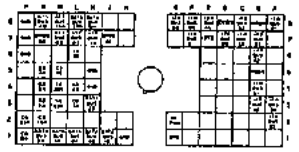
SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove external AC power from STD-7000 Power Supply by depressing AC Power Switch (5) to OFF.		2	
2.	Disconnect STD-7000 to DF Interface Cable and visually inspect each end plug for cracked, bent, broken and/or missing pins. NOTE: The DF plug and STD-7000 plug should resemble 2-2-4, Figure 51.	Do all cable end plug pins check satisfactorily?	3	4



DF PLUG (P801)



STD-7000 Plug (P201)

STD-7000 to DF Cable Ends
Figure 51

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STEP	DIRECTIONS	DECISION	YES	NO
3.	Remove I/O Card (blue) and Install on 100-pin Extender PC Board. Reinstall assembly in I/O Card slot.		5	
4.	Replace damaged or missing pins.			
5.	Position IEEE-488 Address Switch segments 7 and 8 to OFF.		6	
6.	Reapply external AC power to Power Supply by depressing AC Power Switch (5) to ON.		7	
7.	Insert mini-cassette personality tape in Tape Transport and momentarily depress RESET Switch (3).	Is STD-7000 Diagnostic Menu shown on CRT Screen?	8	9
8.	Using Numeric Keypad, select and enter 5 (5 = EXECUTE TAPE).	Did tape successfully load into RAM? NOTE: Appearance of System Master Menu indicates successful loading of tape.	10	11
9.		Is anything indicated on CRT Display Screen?	12	13
10.	Connect Oscilloscope X1 Probe at base of Q1001.	Is a logic "HIGH" indicated?	14	15
11.	Go to appropriate troubleshooting flowchart reflecting symptoms shown on CRT Screen.			
12.	Recheck IEEE-488 Address Switch segments 7 and 8 for proper positioning (segments 7 and 8 should be OFF).			
13.	Go to 2-2-4D(1).			
14.	Replace Q1001 after checking associated circuitry and determining no shorts are present.			

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STEP	DIRECTIONS	DECISION	YES	NO
15.	Replace the following IC's: X1002 - Type 7475 X1003 - Type 74LS04 X1001 - Type 74LS138 NOTE: Alphabetical listing corresponds to placement priority.			

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E. VHS Output Card Failures

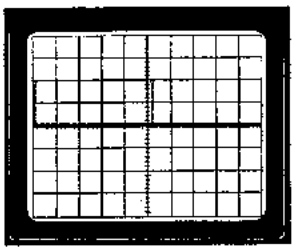
(1) No VHS Output Data

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

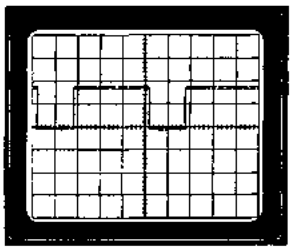
1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove Top Dust Cover (2) (2-2-5, Figure 69) per instructions in 2-2-5.		2	
2.	Remove VHS Output PC Board and install on 100-pin extender board. Install extender in the VHS Output Card position (J405) within card cage.		3	
3.	Insure STD-7000 and CRT are properly interfaced in accordance with 1-2-1.		4	
4.	Apply external AC power and power-up STD-7000 and CRT in accordance with 1-2-3.		5	
5.	Position IEEE-488 Address Switch Segments 7 and 8 to ON.		6	
6.	Momentarily depress RESET Switch (3) to cause automatic start-up routine sequence of rewinding cassette tape, loading information into RAM and producing Master Menu format on CRT.		7	
7.	Select Menu Item #2 (Data Bus Output Menu).		8	
8.	Change Data Field 2 SEND to indicate (1,2,3).		9	

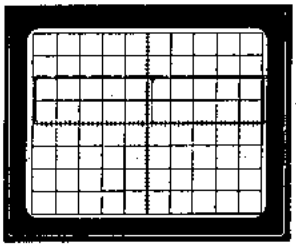
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STEP	DIRECTIONS	DECISION	YES	NO
9.	Change Data Field 3. RATE to (2ØØ).		10	
10.	Comply with Data Bus Performance Evaluation in 2-2-2 and verify data output on other two buses.	Do other buses have data output?	11	12
11.	Depending on faulty bus, connect Oscilloscope Probe to pins 1 and 14, in turn, of appropriate relay (K701, K702 or K703), and check for indication of data.	Is any data indicated?	13	14
12.	Connect Oscilloscope Probe to pin 11 of X708 and observe positive going pulse every 5 mS as shown in 2-2-4, Figure 52.  Positive Going Pulse Figure 52	Is a pulse, with proper timing, present?	15	16
13.	Using VHS Output Circuit Schematic in (2-2-7, Figure 89) troubleshoot appropriate pins of X729 pins associated with the faulty Bus Relay K701, K702 or K703.	Did X729 pins check OK?	17	18
14.	Depending on faulty bus, check voltage level on pin 2 of X720, X721 or X730 (refer to 2-2-7, Figure 89).	Is logic true or positive?	19	20

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STEP	DIRECTIONS	DECISION	YES	NO
15.	Connect Oscilloscope Probe to pin 2 of X717 and observe trace shown in 2-2-4, Figure 53.  Trace at Pin 2 of X717 Figure 53	Is waveform correct?	21	22
16.	Connect Oscilloscope Probe to pin 23 of X706.	Is a 50 kHz Squarewave observed?	23	24
17.	Replace affected relay.			
18.	Replace X729.			
19.	Depending on faulty bus, check for a data signal at pin 5 of X730, X720 or X721.	Is data signal present?	25	26
20.	Fault located within X723, X729 or the appropriate I.C. associated with the affected bus (X730, X721 or X720).			
21.	Connect Oscilloscope Probe to pin 11 or 3 of X711.	Is a 2 MHz Clock signal present?	27	24
22.		Is waveform logic low?	28	39
23.	Disconnect external AC power from STD-7000 and CRT.		30	
24.	Evidence indicates a short on another PC board within the VHS Bus circuitry.			

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STEP	DIRECTIONS	DECISION	YES	NO
	NOTE: To determine which card is causing the short, remove all cards (one at a time) except Logic Input PC Board (red) and VHS Output PC Board (violet). Turn AC power on after each removal and look at clock signal on VHS Output Card at pin 3 of X711.			
25.	Fault located between output of Driver X730, X720 or X721 (depending on faulty bus) and associated relay (K701, K702 or K703). Repair and or replace components as necessary.			
26.	Replace either X720, X721 or X730 (depending on which bus is faulty).			
27.	Troubleshoot and replace affected IC associated with faulty bus (X709, X711 or X710).			
28.	Connect Oscilloscope Probe to pin 11 of X718 and look for signal shown in 2-2-4, Figure 54.  Trace at Pin 11 of X718 Figure 54	Is signal present?	31	32
29.	Troubleshoot and replace X717, X710C and/or X708B as required.			

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STEP	DIRECTIONS	DECISION	YES	NO
30.	Using Ohmmeter, check continuity of the following circuits, in order listed: X705 X706 X708	Did circuits check OK?	33	34
31.	Replace X718.			
32.	Connect Oscilloscope Probe to pin 11 of X713.	Is indicated signal continuously low?	35	36
33.	Replace X727.			
34.	Repair circuit or replace faulty I.C.			
35.	Troubleshoot circuitry associated with X708A and B, X718A, X719, X709B, X710C and X717E. Repair or replace components as required.			
36.	Connect Oscilloscope Probe to pin 14 of X713.	Is a 2 MHz clock signal present?	37	24
37.	Troubleshoot circuits associated with X712, X713, X714, X718 and X706. Repair and/or replace components as required.			

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(2) Improper Number of VHS Bits

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove Top Dust Cover (2-2-4, Figure 69) (2) per instructions in 2-2-5.		2	
2.	Remove VHS Output PC Board and Install on 100-pin extender board. Install extender in the VHS Output Card position (J405) within card cage.		3	
3.	Insure STD-7000 and CRT are properly interfaced in accordance with 1-2-1.		4	
4.	Apply external AC power and power-up STD-7000 and CRT in accordance with 1-2-3.		5	
5.	Position IEEE-488 Address Switch Segments 7 and 8 to ON.		6	
6.	Momentarily depress RESET Switch (3) to cause automatic start-up routine sequence of rewinding cassette tape, loading information into RAM and producing Master Menu format on CRT.		7	
7.	Select Menu Item #2 (Data Bus Output Menu).		8	
8.	Change Data Field 2. SEND to indicate (1,2,3).		9	
9.	Change Data Field 3 RATE to (200).		10	
10.	Using normal troubleshooting techniques, check operation of X724, X712, X713 or X714. Replace faulty component.			

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(3) Improper Start/Stop Sync Generation

SPECIAL ACCESSORY TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove Top Dust Cover (2) (2-2-4, Figure 69) per Instructions in 2-2-5.		2	
2.	Remove VHS Output PC Board and Install on 100-pin extender board. Install extender in the VHS Output Card position (J405) within card cage.		3	
3.	Insure STD-7000 and CRT are properly interfaced in accordance with 1-2-3.		4	
4.	Apply external AC power and power-up STD-7000 and CRT in accordance with 1-2-3.		5	
5.	Position IEEE-488 Address Switch Segments 7 and 8 to ON.		6	
6.	Momentarily depress RESET Switch (3) to cause automatic start-up routine sequence of rewinding cassette tape, loading information into RAM and producing Master Menu format on CRT.		7	
7.	Select Menu Item #2 (Data Bus Output Menu).		8	
8.	Change Data Field 2. SEND to indicate (1,2,3).		9	
9.	Change Data Field 3 RATE to (200).		10	
10.	Troubleshoot circuitry associated with X708A, X710C, X717E, X718A, X719 and X709B. Repair and/or replace faulty circuit and/or component.			

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(4) Improper VHS Data

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove Top Dust Cover (2) (2-2-5, Figure 69) per instructions in 2-2-5.		2	
2.	Remove VHS Output PC Board and install on 100-pin extender board. Install extender in the VHS Output Card position (J405) within card cage. Replace X715 and X716.		3	
3.	Insure STD-7000 and CRT are properly interfaced in accordance with 1-2-1.		4	
4.	Apply external AC power and power-up STD-7000 and CRT in accordance with 1-2-3.		5	
5.	Position IEEE-488 Address Switch Segments 7 and 8 to ON.		6	
6.	Momentarily depress RESET Switch (3) to cause automatic start-up routine sequence of rewinding cassette tape, loading information into RAM and producing Master Menu format on CRT.		7	
7.	Select Menu Item #2 (Data Bus Output Menu).		8	
8.	Change Data Field 2. SEND to indicate (1,2,3).		9	
9.	Change Data Field 3 RATE to (200).		10	
10.	Has proper data been restored?		11	12

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STEP	DIRECTIONS	DECISION	YES	NO
11.	Malfunction cleared.			
12.	Fault is located in any I.C. or associated circuit shown on page 1 of 1 of the VHS Output PC Board Circuit Schematic (2-2-7, Figure 89) all troubleshooting techniques are exhausted, recommend return VHS Output PC Board to IFR Factory Customer Service for repair or replacement.			

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F. 429 Bus Output Card Failure

(1) No 429 Bus Output Data

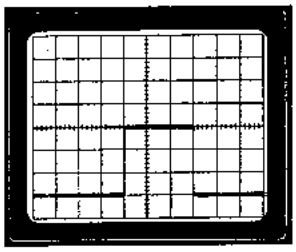
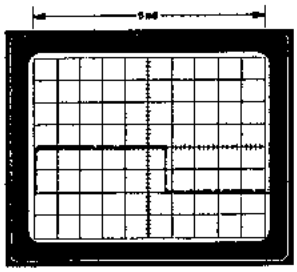
SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Digital Voltmeter

1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.		Does the other 429 Bus on PC board indicate a data output when requested?	2	41
2.	Place affected 429 Bus PC Board on a 100 pin extender and reinstall in assigned slot on Motherboard. CAUTION: REMOVE EXTERNAL AC POWER BEFORE REMOVING OR REPLACING ANY CARD WITHIN CARD CAGE.		3	
3.	Connect Oscilloscope Probe to pins 1 and 14 of malfunctioning Isolation relay (K901 or K902).	Is data transmission indicated?	4	5
4.	Connect Digital Voltmeter to pin 6 of affected Isolation Relay.	Is voltage 0 (±0.6) Volt?	6	7
5.	Connect Oscilloscope Probe to pins 3 and 11 of X907.	Is data transmission indicated?	8	9
6.	Repair short in Isolation Relay or remove and replace defective Isolation Relay.			
7.	Connect Digital Voltmeter probe to pin 8 of X926.	Is voltage indication 0 (±0.6) Volts?	10	11
8.	Fault located within Level Converter. Troubleshoot and repair as necessary.			

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STEP	DIRECTIONS	DECISION	YES	NO
9.	Connect Oscilloscope X1 Probe to pins 2 and/or 12 of X907.	Are 32 clock pulses observed as shown in 2-2-4, Figure 55.  Clock Pulse Figure 55	12	13
10.	Fault located within circuitry between pin 6 of K901 and pin 8 of X926. Repair as necessary.			
11.	Connect Digital Voltmeter probe to pin 9 of X926.	Is voltage indicated?	14	15
12.	Replace X907.			
13.	Connect Oscilloscope Probe to pin 6 of X923 and check for waveform with repetition rate every 5 mS.	Does waveform indicate correctly as shown in 2-2-4, Figure 56.  Repetition Rate Figure 56	16	17
14.	Remove and Replace X926.			
15.	Connect Digital Voltmeter to pin 9 of X921.	Is voltage indicated?	18	19

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STEP	DIRECTIONS	DECISION	YES	NO
16.	Connect Oscilloscope Probe to pin 7 of X912.	Is low speed clock signal indicated?	20	21
17.	Replace X901 and X902.		22	
18.	Fault located within circuitry between pin 9 of X926 and pin 9 of X921. Repair if necessary.			
19.	Replace X921.			
20.	Connect Oscilloscope Probe to pin 11 of X922.	Is correct Baud Rate indicated?	23	24
21.	Connect Oscilloscope Probe to pin 14 of X912.	Is a logic low indicated?	25	26
22.	Connect Oscilloscope Probe to pin 6 of X923.	Is waveform shown in 2-2-4, Figure 49 indicated?	27	28
23.	Connect Oscilloscope Probe to pin 12 of X907.	Is correct frequency indicated?	29	30
24.	Connect Oscilloscope Probe to pin 10 of X917.	Is the clock pulse present?	31	32
25.	Connect Oscilloscope Probe to pin 2 of X912.	Is a logic low indicated?	33	26
26.	Replace X905.			
27.	Malfunction cleared.			
28.	Use 429 Output Circuit Schematic (2-2-7, Figure 90) to troubleshoot the circuitry associated with and including I.C.'s indicated below: X917 X918 X923 X922	Were any faults indicated?	34	27
29.	Connect Oscilloscope Probe to pin 2 of X907.	Is correct frequency indicated?	35	36
30.	Fault located in circuit between pin 12 of X907 and pin 11 of X922. Repair as necessary.			

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STEP	DIRECTIONS	DECISION	YES	NO
31.	Fault located in circuit between pin 11 of X922 and pin 10 of X917. Repair as required.			
32.	Connect Oscilloscope Probe to pin 11 of X917.	Is low speed clock pulse present?	37	38
33.	Suspect fault within X912. NOTE: Before removing and replacing I.C., check for shorts in circuitry between pin 7 of X912 and associated components. Repair or replace as necessary.			
34.	Repair faulty circuit or replace faulty I.C. as required.			
35.	Replace X907.			
36.	Fault in circuit between pin 2 of X907 and pin 11 of X922. Repair as necessary.			
37.	Connect Oscilloscope Probe to pin 13 of X922.	Is low speed clock pulse present?	39	40
38.	Replace X917.			
39.	Replace X922.			
40.	Fault located within circuitry between pin 10 of X917 and pin 13 of X922.			
41.	Using 429 Bus Output Circuit Schematic (2-2-7, Figure 90) verify operation of X921 and X926.	Is I.C. operation satisfactory?	42	43
42.	Using 429 Bus Output Circuit Schematic (2-2-7, Figure 90) verify operation of X934, X936, X937, Q909 and Q910 and associated circuitry.	Did I.C.'s and/or circuitry check OK?	44	45
43.	Replace faulty I.C.			

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STEP	DIRECTIONS	DECISION	YES	NO
44.	Using 429 Bus Output Circuit Schematic (2-2-7, Figure 90) verify circuit operation involving X924, X929, X931 and X932.			
45.	Repair circuitry and/or replace affected I.C.			

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(2) Incorrect 429 Bus Output Data

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.		Does the other 429 Bus on PC board have valid data output?	2	3
2.	Connect Oscilloscope Probe to each address line of X906, in turn (AØ thru A9) and check for toggling and logic indication. NOTE: AØ thru A5 should be toggling. A6 thru A9 should be low.	Did any address line indicate improperly?	4	5
3.	Proceed to Step 42 of 2-2-4F(1).			
4.	Using normal troubleshooting procedures and the 429 Bus Output Circuit Schematic (2-2-7, Figure 90) check circuitry between the following IC's. X905 X910 X911 X917 X912 X918	Did circuitry and/or associated IC check satisfactorily?	6	7
5.	Replace X906, X907 and X917. NOTE: If malfunction not cleared at this point, remove and replace affected 429 Bus Output PC Board.			
6.	Malfunction cleared.			
7.	Repair affected circuit and/or replace faulty IC as required.			

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G. Logic Input Card Failures

(1) Clock Malfunctions

SPECIAL ACCESSORY TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

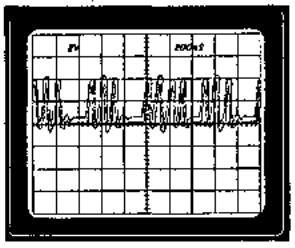
1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove STD-7000 Top Dust Cover as per instructions in 2-2-5.		2	
2.	Remove LOGIC INPUT Card (red) from Card Cage and place on 100-pin extender PC board. Install assembly in LOGIC INPUT Slot (J409) within Card Cage to allow access to logic input card components.		3	
3.	Interface STD-7000 with CRT Display Terminal in accordance with 1-2-1.		4	
4.	Position IEEE-488 Address Switch Segments 7 and 8 to OFF.		5	
5.	Apply external AC power to STD-7000 and CRT Display Terminal. Depress AC Power Switch (5) to power-up STD-7000 and CRT (if connected to J202).		6	
6.	Install mini-cassett personality tape in tape transport and momentarily depress RESET Switch (3).	Is STD-7000 Diagnostic Menu shown on CRT Screen?	7	8
7.	Using Numeric Keypad, enter 5 (5 = EXECUTE TAPE).	Did tape successfully load? NOTE: The appearance of System Master Menu on CRT Screen indicates successful tape loading.	9	10
8.	Recheck position of IEEE-488 Address Switch Segments 7 and 8. Both should be OFF.		9	

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STEP	DIRECTIONS	DECISION	YES	NO
	NOTE: If both segments are properly positioned, refer to 2-2-4D(1).			
9.		Which clock is inoperative? 2 MHz 1 MHz 100 kHz 50 kHz Low Speed VHS	 11 12 12 13 14	
10.	Go to appropriate trouble-shooting flowchart for indicated problem.			
11.	Connect Oscilloscope X1 Probe to pin 12 of X612.	Is a 10 MHz signal indicated?	15	16
12.	Replace X612.			
13.	Replace X624.			
14.	Connect Oscilloscope X1 Probe to pin 4 of X624.	Is a Low Speed Clock signal indication present?	17	30
15.	Connect Oscilloscope X1 Probe to pin 10 of X612.	Is 2 MHz Clock signal indicated?	18	19
16.	Connect Oscilloscope X1 Probe to pin 6 of X611.	Is a 10 MHz signal indicated?	20	21
17.	Connect Oscilloscope X1 Probe to pin 14 of X623.	Is Low Speed Signal present?	22	23
18.	Connect Oscilloscope X1 Probe to LOGIC INPUT Card Edge Connector pin 53.	Is 2 MHz Clock indicated?	24	25
20.	Replace X612.			
21.	Evidence indicates a short or break in pathwork circuitry between pin 6 of X611 and pin 12 of X612. Repair as necessary.			

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STEP	DIRECTIONS	DECISION	YES	NO
22.	Connect Oscilloscope X1 Probe to pin 5 of X611.	Is 10 MHz signal present?	26	27
23.	Connect Oscilloscope X1 Probe to pin 7 of X623.	Is signal present?	13	28
24.	No defect noted.			
25.	Evidence indicates a short or break in pathwork circuitry between pin 10 of X612 and LOGIC INPUT Card Edge Connector. Repair as necessary.			
26.	Replace X611.			
27.	Using Oscilloscope, check output of Y601.	Is Y601 producing 10 MHz?	26	29
28.	Replace X623.			
29.	Replace Y601.			
30.	Connect Oscilloscope X1 Probe to pin 12 of X624. Set Oscilloscope controls to 2V/200nS/DIV and observe trace indication in 2-2-4, Figure 57.  LS Clock Pulse Figure 57	Does waveform resemble 2-2-4, Figure 57.	13	31

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STEP	DIRECTIONS	DECISION	YES	NO
31.	Check the following pins of X625 for proper Logic Level Indication? Pin 2: L Pin 3: L Pin 14: L Pin 15: H	Are all Logic Levels correct?	32	33
32.	Replace X625.			
33.	Check the following pins of X640 for proper Logic Level Indication: Pin 2: H Pin 3: L Pin 14: L Pin 15: H	Are all Logic Levels correct?	34	35
34.	Replace X640.			
35.	Fault exists upstream of X639. Using normal troubleshooting techniques, attempt to isolate and repair.			

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(2) Wrong Low Speed Clock Frequency

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Remove STD-7000 Top Dust Cover as per instructions in 2-2-5.		2	
2.	Remove LOGIC INPUT Card (red) from Card Cage and place on 100-pin extender PC board. Install assembly in LOGIC INPUT Slot (J409) within Card Cage to allow access to LOGIC INPUT Card components.		3	
3.	Apply External AC power to STD-7000 and depress AC Power Switch (5) to ON.		4	
4.	Connect Oscilloscope X1 Probe to pin 6 of X625.	Does indicated waveform resemble 2-2-4, Figure 57?	5	6
5.	Replace X624.			
6.	Go to 2-2-4G(1) and enter at Step 31.			

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(3) Improper Logic Data or Logic Completely Inoperative

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Insure external AC power has been removed from STD-7000.		2	
2.	Remove Top Dust Cover from STD-7000 in accordance with instructions in 2-2-5.		3	
3.	Remove LOGIC INPUT Card (red).	Is logic completely inoperative?	4	12
4.	Remove either of three 429 Output Cards (brown).		5	
5.	Remove X613, X626 and X627 from LOGIC INPUT Card and replace each with technician's choice of X901, X902, X903 and X904 of selected 429 Output Card.		6	
6.	Reinstall LOGIC INPUT Card in assigned slot in Card Cage.		7	
7.	Install X613, X626 and X627 in open positions of selected 429 OUTPUT Card and reinstall 429 OUTPUT Card in assigned slot within Card Cage. NOTE: Insure no slots remain open between analog input (green) and CPU (yellow) cards.		8	
8.	Apply external AC power to STD-7000 and depress AC Power Switch (5) to ON.		9	
9.		Is logic still inoperative?	10	11

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STEP	DIRECTIONS	DECISION	YES	NO
10.	Remove external AC power from STD-7000. Remove LOGIC INPUT Card (red) and return to IFR Systems, Inc., Customer Service for repair and/or replacement.			
11.	Remove external AC power from STD-7000. Remove 429 OUTPUT Card containing original X613, X626 and X627. Replace X613, X626 and X627 PIO's with serviceable components.			
12.	Remove RAM Card (orange).		13	
13.	Remove any two RAM I.C.'s (X1107 thru X1122) from RAM Card.		14	
14.	Remove X633 and X634 from LOGIC INPUT Card and replace with previously removed RAMs (2114s) from RAM Card.		15	
15.	Install LOGIC INPUT Card in assigned slot within Card Cage.		16	
16.	Apply external AC power to STD-7000 and depress AC Power Switch (5) to ON.		17	
17.		Is Improper Logic Data still indicated?	10	18
18.	Original X633 and X634 RAMs are faulty. Replace with serviceable components.			

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H. Analog Input Card Failures

(1) No Receipt of 429 Bus Data

SPECIAL ACCESSORY TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Verify external AC power is removed from STD-7000.		2	
2.	Remove ANALOG INPUT Card (green) from Card Cage and install on 100-pin extender PC Board. Install assembly in ANALOG INPUT Card slot within Card Cage.		3	
3.	Verify STD-7000 and CRT Display Terminal are correctly interfaced in accordance with 1-2-1. Position IEEE-488 Address Switch Segments 7 and 8 to OFF.		4	
4.	Apply external AC power to STD-7000.		5	
5.	Place mini-cassette personality tape (version 2.4 or later) in Tape Transport.		6	
6.	Momentarily depress STD-7000 RESET Switch (3).	Is STD-7000 Diagnostic Menu indicated on CRT Screen?	7	3
7.	Using Numeric Keypad, enter 5 (5 = EXECUTE TAPE) and listen for audible indication of tape rewinding, followed by a tape loading sequence.	Did tape successfully load? NOTE: System Master Menu will automatically appear upon successful completion of tape loading.	8	9
8.	Using Numeric Keypad, enter 1 (CONTROL BUS OUTPUT PAGE).		10	
9.	Go to troubleshooting flowchart(s) pertaining to indicated problem (CS or MEM).			

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STEP	DIRECTIONS	DECISION	YES	NO
10.	Change Data Field 2 CONDITION to SEND) on all four pages (Ø thru 3) of Data Field 1.		11	
11.	Change Data Field 3 RATE to (Ø87) on all four pages (Ø thru 3) of Data Field 1.		12	
12.	While depressing blank (SHIFT) key of numeric Keypad, depress 4 key to indicate CONTROL BUS INPUT PAGE on CRT screen. Check each PAGE (Data Field 1) for data receipt).	Is data being received?	13	14
13.	While depressing blank (SHIFT) key, depress 3 key to indicate ATTITUDE BUS OUTPUT PAGE.		15	
14.	Go to appropriate 429 OUTPUT Card Troubleshooting Flowchart.			
15.	Change Data Field 2 COND to (SEND) on both buses (Ø and 1) of Data Field 1.		16	
16.	Change Data Field 3 RATE to (2ØØ) on both buses (Ø and 1) of Data Field 1.		17	
17.	Using Oscilloscope (with X1 Probe), check the ANALOG INPUT Card edge connector pins for associated 429 Bus data indications.	Is correct data available at card edge?		

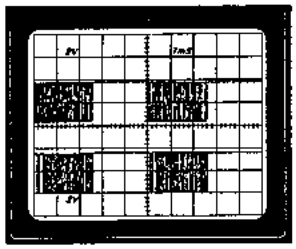
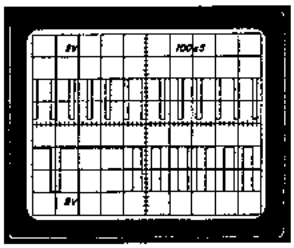
CONTROL BUS	X507 PIN	ANALOG INPUT CARD EDGE PIN
ØA	19	79
ØB	11	80
1A	20	81
1B	10	82
2A	21	83
2B	9	84
3A	22	85
3B	8	86

ATTITUDE BUS	X507 PIN	ANALOG INPUT CARD EDGE PIN
4A (ØA)	23	87
4B (ØB)	7	88
5A (1A)	24	89
5B (1B)	6	90

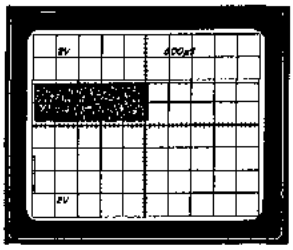
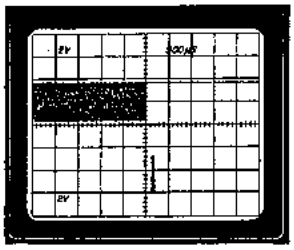
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STEP	DIRECTIONS	DECISION	YES	NO
18.	Using Oscilloscope (with X1 Probe), check the X507 pins in step 17 for associated 429 Bus Data indications.	Is correct data present?	20	21
19.	Go to appropriate 429 OUTPUT Card Failures Troubleshooting Flowchart.			
20.		Is problem or malfunction common to all 429 buses?	22	23
21.	Evidence indicates break or short in pathwork circuitry between X507 and card edge connector pins. Locate and repair as necessary.			
22.	Check affected pin of X507 (either pin 15, 16 or 17) for correct Binary signal.	Is signal correct?	24	25
23.	Connect Oscilloscope X1 Probe to pin 28 of X507.	Is data signal present?	26	27
24.	Replace X507.			
25.	Using Oscilloscope, check the following card edge pins for indication of data: CARD EDGE PIN / DATA BUS 7 D3 8 D7 9 D2 10 D6 11 D1 12 D5 13 DØ 14 D4	Is data indicated on each card edge pin?	28	29
26.	Connect Oscilloscope X1 Probe to pin 2 of X507.	Is data signal present?	30	24
27.	Connect Oscilloscope X1 Probe to pin 2 of X507.	Is data signal present?	24	22
28.	Connect Oscilloscope X1 Probe to pin 11 of X505.	Is a logic HIGH indicated?	31	32
29.	Problem or malfunction located elsewhere in STD-7000 System. Re-evaluate problem or malfunction. Choose Troubleshooting Flowchart best suited for malfunction.			
30.	Connect Oscilloscope X1 Probe to pin 1 of X506.	Is logic LOW indicated?	33	31

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STEP	DIRECTIONS	DECISION	YES	NO
31.	Replace X505.			
32.	Replace X504.			
33.	Connect Oscilloscope X1 Probe to pin 15 of X506.	Is logic LOW indicated?	34	31
34.	Connect Dual Trace Oscilloscope Channel A (X1) Probe to pin 7 (clock) of X506.		35	
35.	Connect Dual Trace Oscilloscope Channel B (X1) Probe to pin 4 (data) of X506. NOTE: Set Oscilloscope controls to 1mS/ 2V/DIV.	Does indicated waveform resemble waveform in 2-2-4, Figure 58?  X506 Dual Trace Figure 58	36	37
36.	Select timebase X10.	Does waveform resemble waveform in 2-2-4, Figure 59?  Timebase X10 Figure 59	38	37
37.		Is only clock signal incorrect?	39	40

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STEP	DIRECTIONS	DECISION	YES	NO
38.	Connect Oscilloscope Channel B Probe to pin 12 (BWS) of X506.	Is BWS present before clock transition as shown in 2-2-4, Figure 60?  BWS and Clock Signal Figure 60	45	46
39.	Troubleshoot, locate and repair shorted circuitry associated with X510 and/or replace X510 if necessary.			
40.		Is Data Signal present?	41	42
41.		Is Data Signal correct?	43	44
42.	Replace X506.			
43.	No defect noted.			
44.	Using normal troubleshooting techniques, troubleshoot X502 thru X508 and associated circuitry. Replace I.C.s or repair circuit as necessary.			
45.	Connect Oscilloscope Channel B Probe to pin 9 of X506.	Is EWS present after clock transition as shown in 2-2-4, Figure 61.  EWS and Clock Signal Figure 61	47	46

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STEP	DIRECTIONS	DECISION	YES	NO
46.	Using normal troubleshooting techniques, troubleshoot X511 and X512 and circuitry associated with each. Replace I.C.(s) or repair circuit as necessary.			
47.	Fault located on LOGIC INPUT Card. Go to 2-2-4G and choose appropriate Troubleshooting Flowchart.			

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(2) No Receipt of 453 (VHS) Data

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Oscilloscope (Dual Trace)

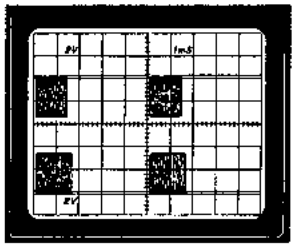
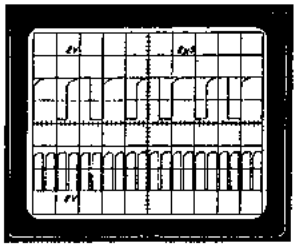
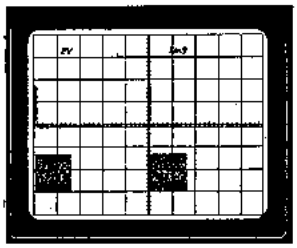
1 Extender PC Board (100 Pin)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Insure external AC power is removed from STD-7000.		2	
2.	Remove ANALOG INPUT Card (green) and install on 100-pin extender PC board. Install assembly in the ANALOG INPUT Card slot within Card Cage.		3	
3.	Position IEEE-488 Address Switch Segments 7 and 8 to OFF.		4	
4.	Insure STD-7000 and CRT Display Terminal are correctly interfaced in accordance with 1-2-1.		5	
5.	Apply external DC power to STD-7000.		6	
6.	Depress AC Power Switch (5) to ON and momentarily depress RESET Switch (3).			7
7.	Install mini-cassette personality tape (2.4 version or later) in Tape Transport and close Transport door.		8	
8.	Using Numeric Keypad, enter 5 (5 = EXECUTE TAPE).	Did tape successfully load? NOTE: The appearance of System Master Menu on CRT Screen indicates successful tape loading.	9	15
9.	Enter 2 to produce DATA BUS OUTPUT PAGE.		10	

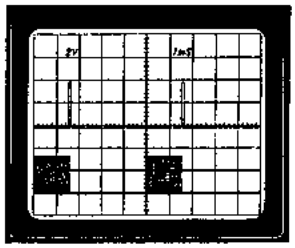
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STEP	DIRECTIONS	DECISION	YES	NO
10.	Change Data Field 2 SEND to (1,2,3).		11	
11.	Change Data Field 3 RATE to (200).		12	
12.	Using Oscilloscope X1 Probe, check the ANALOG INPUT Card Edge pins for corresponding 453 (VHS) data. CARD EDGE PIN / DATA BUS CHANNEL 73 / 1A 74 / 1B 75 / 2A 76 / 2B 77 / 3A 78 / 3B	Is the correct VHS (453) Data available?	13	14
13.		Is problem common to all VHS Buses?	16	17
14.	Go to 2-2-4E and choose appropriate Troubleshooting Flowchart.			
15.	Go to appropriate trouble-shooting flowchart for indicated problem.			
16.	Connect Dual Trace Oscilloscope Channel A X1 Probe to pin 5 (VHS Clock) of X521.		18	
17.		Is problem associated with DATA BUS 1 only?	19	
18.	Connect Oscilloscope Channel B X1 Probe to pin 8 (VHS DATA) of X523.	Are data and clock traces similar to 2-2-4, Figure 62? NOTE: See 2-2-4, Figure 63 for expanded trace of 2-2-4, Figure 62.	21	

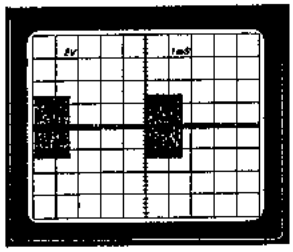
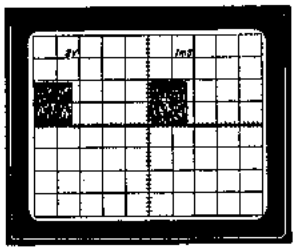
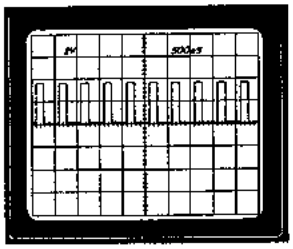
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STEP	DIRECTIONS	DECISION	YES	NO
	 VHS Data and Clock Traces Figure 62	 Expanded VHS Data and Clock Traces Figure 63		
19.	Connect Oscilloscope X1 Probe to pin 6 of Relay K501.	Is a logic LOW indicated?	23	24
20.		Is problem associated with DATA BUS 2 only?	25	26
21.	Connect Oscilloscope Channel B X1 Probe to pin 13 of X524.	Is VHS BWS indicated as shown in 2-2-4, Figure 64?  VHS BWS Figure 64	27	28
22.		Is VHS Clock signal incorrect?	29	30
23.	Replace Relay K501.			
24.	Connect Oscilloscope X1 Probe to pin 13 of X515.	Is a logic HIGH indicated?	31	32
25.	Connect Oscilloscope X1 Probe to pin 6 of Relay K502.	Is a logic LOW indicated?	33	34

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STEP	DIRECTIONS	DECISION	YES	NO
26.	Connect Oscilloscope X1 Probe to pin 6 of Relay K503.	Is a logic LOW indicated?	35	36
27.	Connect Oscilloscope Channel B X1 Probe to pin 5 of X525.	Is VHS EWS indicated as shown in 2-2-4, Figure 65?  VHS EWS Figure 65	42	28
28.	Replace X523 and X524.			
29.	Replace X521 and X522.			
30.		Is data signal indicated?	37	38
31.	Replace X515.			
32.	Replace X505.			
33.	Replace Relay K502.			
4.	Connect Oscilloscope X1 Probe to pin 5 of X515.	Is a logic LOW indicated?	31	32
35.	Replace Relay K503.			
36.	Connect Oscilloscope X1 Probe to pin 9 of X515.	Is a logic HIGH indicated?	31	32
37.		Is data correct?	21	39
38.	Replace X522 and X523.			

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STEP	DIRECTIONS	DECISION	YES	NO
39.	Connect Oscilloscope X1 Probe to pin 6 of X517.	Is waveform as shown in 2-2-4, Figure 66?  VHS Data Trace Figure 66	40	41
40.	Connect Oscilloscope X1 Probe to pin 6 of X519.  VHS Waveform Figure 67	Is waveform as shown in 2-2-4, Figure 67?  Expanded VHS Waveform Figure 68	42	43
41.	Fault located in the Analog Filtering Section of the ANALOG INPUT Card. (Refer to 2-2-7, Figure 91).			
42.	Fault located on LOGIC INPUT Card. Go to 2-2-4G for appropriate Troubleshooting Flowchart.			
43.	Fault located on Logic Conversion section of ANALOG INPUT Card. Troubleshoot using normal techniques.			

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I. Power Supply Troubleshooting Flowchart

(1) Power Supply

SPECIAL ACCESSORY
TEST EQUIPMENT REQ'D: 1 Digital Multimeter (100KΩ/V)

STEP	DIRECTIONS	DECISION	YES	NO
1.	Carefully disconnect P418 from Right Angle Connector J418 located on Motherboard.		2	
2.	Apply external AC power to STD-7000 Rear Panel CORCOM Receptacle.		3	
3.	Momentarily depress AC Power Switch (5) to apply external AC power to Power Supply Assembly.	Did the light within the switch illuminate the AC Power Switch Button?	4	5
4.		Is questionable voltage associated with: +5V? -5V? +12V? -12V? All voltages?	 6 19 21 23 12	
5.		Is cooling fan (8) operating? NOTE: See 1-2-2B for fan location.	7	8
6.	Using Digital Multimeter (100KΩ/V), measure and verify +5V±0.2V is indicated at pins 1 and 2 of P418 (Refer to 2-2-7, Figure 91).	Are voltages correct?	10	9
7.	Remove and replace light bulb(s) (type 328) by pulling gently on switch pushbutton (9) to remove it from Switch (1) to expose light bulbs. (Refer to 2-2-5, Figure 72.)			
8.	Check external AC power source, line cord receptacle connections and CORCOM fuse.		3	

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STEP	DIRECTIONS	DECISION	YES	NO
9.	Using Digital Multimeter (100Ω/V), measure and verify +5V±0.2V is indicated at pins 7 and 10 of P9901 (Refer to 2-2-7, Figure 91).	Are voltages correct?	11	12
10.	Depress AC Power Switch (5) to remove AC power from Motherboard.		13	
11.	Fault located within Cable Harness (7007-3781-3XX). Troubleshoot cable, Repair/ Replace as required.			
12.	Using Digital Voltmeter (100KΩ/V), verify voltage between pins 1 and 2 of P9901 are equal to the external ac line voltage input.	Are voltages equal?	14	11
13.	Remove all plug-in PC boards from Card Cage Assembly in accordance with 2-2-5B(2)(a)2. CAUTION: WHEN REMOVING AND/ OR INSTALLING ANY PC BOARD WITHIN THE CARD CAGE, REMOVE EXTERNAL AC POWER FROM STD-7000 TO PRECLUDE PERMANENT DAMAGE TO SYSTEM. TO DO THIS, SIMPLY DEPRESS AC POWER SWITCH (5) UNTIL AC POWER IS OFF.		15	
14.	Fault located within Power Supply Assembly. Using Power Supply Circuit Schematic (2-2-7, Figure 93) troubleshoot power supply circuit.			
15.	Depress AC Power Switch (5) to reapply external AC power to STD-7000.		16	
16.	Using Digital Multimeter (100KΩ/V), measure and verify voltages on the pins of J401 thru J412 (Refer to 2-2-7, Figure 80.)	Are all voltages correct?	17	18

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STEP	DIRECTIONS	DECISION	YES	NO
	<table><tr><th>Connector Pin No.</th><th>Voltage</th><th>Tolerance</th></tr><tr><td>1</td><td>+5.0</td><td>±0.2V</td></tr><tr><td>2</td><td>+5.0</td><td>±0.2V</td></tr><tr><td>5</td><td>-5.0</td><td>±0.2V</td></tr><tr><td>6</td><td>-5.0</td><td>±0.2V</td></tr><tr><td>95</td><td>-12.0</td><td>±0.2V</td></tr><tr><td>96</td><td>-12.0</td><td>±0.2V</td></tr><tr><td>99</td><td>+12.0</td><td>±0.2V</td></tr><tr><td>100</td><td>+12.0</td><td>±0.2V</td></tr></table>			
17.	Fault located within circuitry of one or more plug-in PC boards initially removed in Step 13. Re-install each PC board (one at a time) and determine which PC board is causing fault. CAUTION: WHEN REMOVING AND/OR INSTALLING ANY PC BOARD WITHIN THE CARD CAGE, REMOVE EXTERNAL AC POWER FROM STD-7000 TO PRECLUDE PERMANENT DAMAGE TO SYSTEM. TO DO THIS, SIMPLY DEPRESS AC POWER SWITCH (5) UNTIL AC POWER IS OFF. NOTE: When faulty PC board has been identified, repair or replace PC board before continuing with PC board installation.			
18.	Fault located on Motherboard Assembly circuit. Use normal troubleshooting procedures to isolate and evaluate fault location to determine whether to repair or replace Motherboard.			
19.	Using Digital Multimeter (100KΩ/V), measure and verify -5V±0.3V is indicated at pin 6 of P418 (Refer to 2-2-7, Figure 91).	Is voltage correct?	10	20
20.	Using Digital Multimeter (100KΩ/V), measure and verify -5V±0.3V is indicated at pin 12 of P9901 (Refer to 2-2-7, Figure 91).	Is voltage correct?	11	12

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STEP	DIRECTIONS	DECISION	YES	NO
21.	Using Digital Multimeter (100KΩ/V), measure and verify +12V±0.2V is indicated at pins 11 and 12 of P418 (Refer to 2-2-7, Figure 91).	Are voltages correct?	10	22
22.	Using Digital Multimeter (100KΩ/V), measure and verify +12V±0.2V is indicated at pins 6 and 9 of P9901 (Refer to 2-2-7, Figure 91).	Are voltages correct?	11	12
23.	Using Digital Multimeter (100KΩ/V), measure and verify -12V±0.5V is indicated at pin 18 of P418 (Refer to 2-2-7, Figure 90).	Is voltage correct?	10	24
24.	Using Digital Multimeter (100KΩ/V), measure and verify -12V±0.5V is indicated at pin 11 of P9901 Refer to 2-2-7, Figure 90).	Is voltage correct?	11	12

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5. Disassembly/Reassembly

A. Introduction

This section contains minimum instructions required to either remove and replace any internal module or completely disassemble/reassemble the STD-7000 Bus Controller, should it become necessary. Most of the module removal or disassembly procedures in this section are reflected in STD-7000 Composite Disassembly (2-2-5, Figure 69), however when further detail of module disassembly is required, it is shown on an individual assembly drawing for that particular module.

Reassembly of modules depend upon the extent of disassembly and should be performed in reverse sequence of the disassembly procedure used.

(1) Preliminary Considerations

(a) Tools required for disassembly/reassembly:

1 Wrenches

Open End: 1/4" and 5/8"

2 Other

Soldering Iron

3 Screwdrivers

Phillips and Spade (Slotted)

4 Nut Drivers

1/4" and 3/16" Nut Driver

(b) Preliminary Precautions

Comply with the following CAUTIONS during Disassembly/Reassembly:

CAUTION: TAG EACH WIRE AND CABLE PRIOR TO REMOVAL.

CAUTION: INSURE RIBBON CABLES ARE NOT STRETCHED OR TWISTED.

CAUTION: DO NOT PLACE UNDUE STRAIN ON ANY WIRE OR CABLE.

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CAUTION: DO NOT DISCARD LOOSE ITEMS (NUTS, SCREWS, WASHERS, ETC.).

CAUTION: SMALL COMPONENTS INSTALLED ON PC BOARDS ARE EASILY DAMAGED DURING HANDLING. SPECIAL CARE SHOULD BE EXERCISED DURING THIS PROCESS.

B. STD-7000 Disassembly/Reassembly

(1) Case Disassembly (Refer to 2-2-5 Figure 68)

(a) Top Cover (2) and Bottom Cover (19) Removal

1 Remove four screws (1) from Top Cover (2) and slide cover to rear to lift free.

2 Remove four screws (24) from Bottom Cover (19) and slide cover to rear to lift free.

NOTE: It is not necessary to remove Stacking Feet (22) prior to the removal of Bottom Cover (19).

(b) Left and Right Side Frame (13 and 31) Removal

CAUTION: POWER SUPPLY MOUNTING BRACKET (37) IS ATTACHED TO LEFT SIDE FRAME. CARE SHOULD BE TAKEN NOT TO PLACE UNDUE STRAIN ON POWER SUPPLY LEADS (43) DURING DISASSEMBLY.

1 Remove Top Cover (2) and Bottom Cover (19) per 5.B.(1)(a).

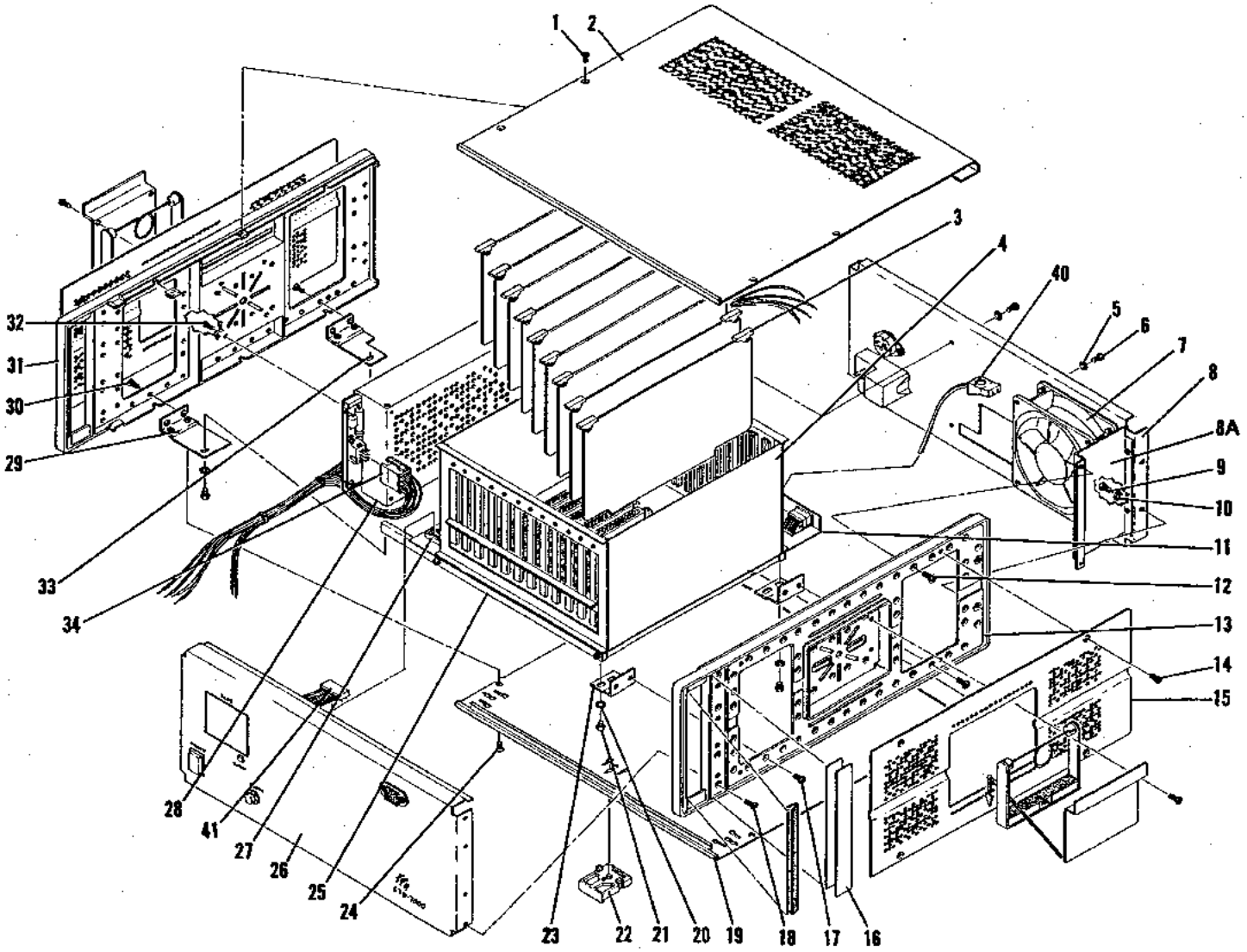
2 Remove four screws (14) that secures each Side Cover (15) to Side Frames (13 and 31), then remove Side Covers (15).

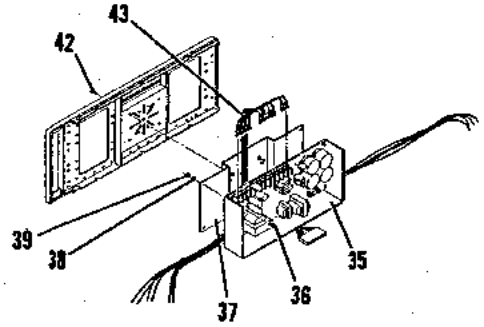
3 Remove two screws (17), from each of two Brackets (23) securing Right Side Frame (13) to Rail Assembly (25) or from each of two Brackets (29 and 33) securing Left Side Frame (31) to Rail Assembly (25).

4 Remove two screws (9) and two washers (10) securing either Side Frame (13 or 31) to Rear Panel (8).

5 Carefully pry adhesive-backed Side Strip (16) from either Side Frame (13 or 31) and remove four screws (18) securing Front Panel (26) to either Side Frame (13 or 31).

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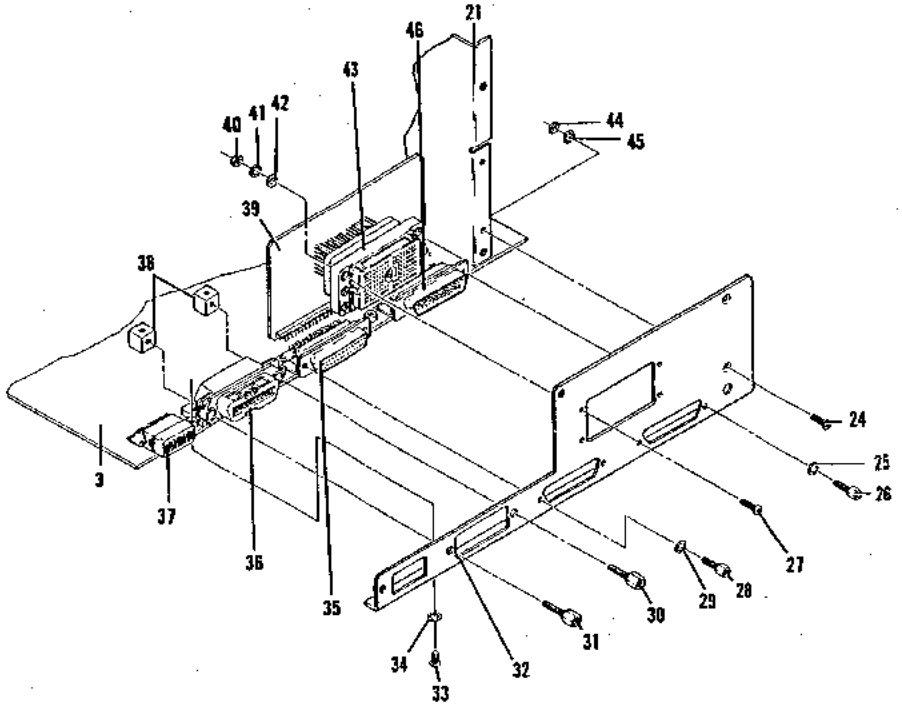


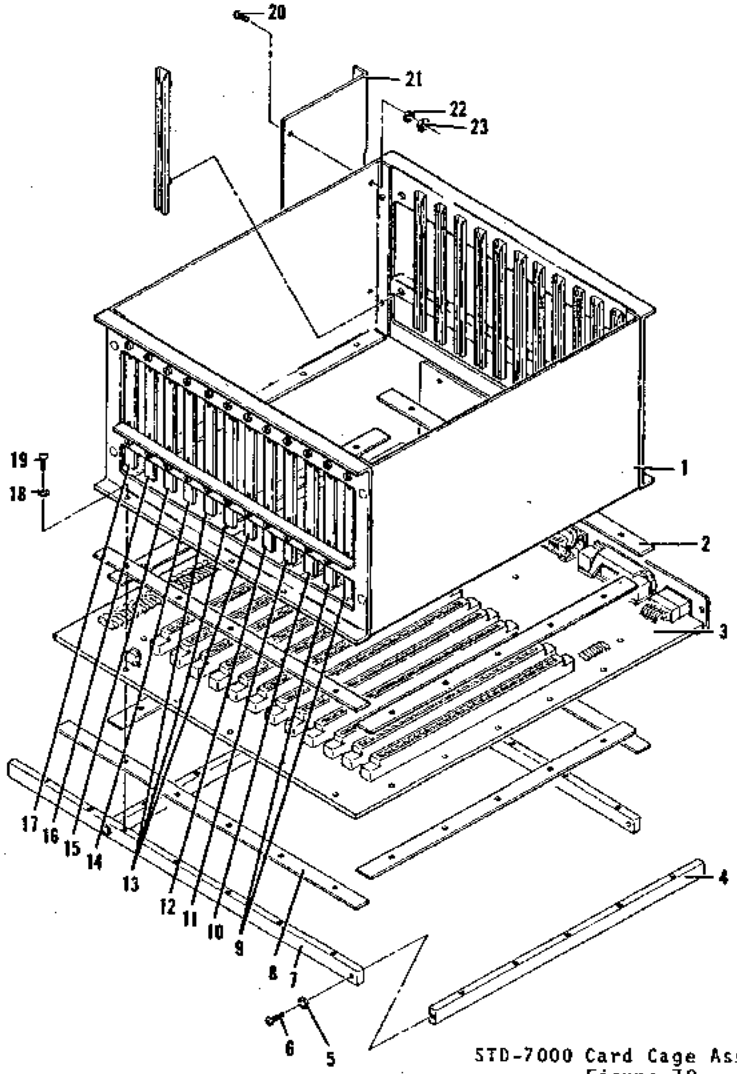


SIERRACIN POWER SUPPLY

STD-7000 Composite Assembly
Figure 69

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STD-7000 Card Cage Assembly
Figure 70

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(2) Card Cage Assembly (Refer to 2-2-5, Figure 69)

(a) Card Cage Assembly Removal

1 Remove Top Cover (2) and Bottom Cover (19) per 2-2-5B(1)(a).

2 Remove all vertically installed PC Boards (cards) from Card Cage Assembly (4) by simultaneously lifting both color-coded ejectors (3) until each card is free, then carefully remove each card.

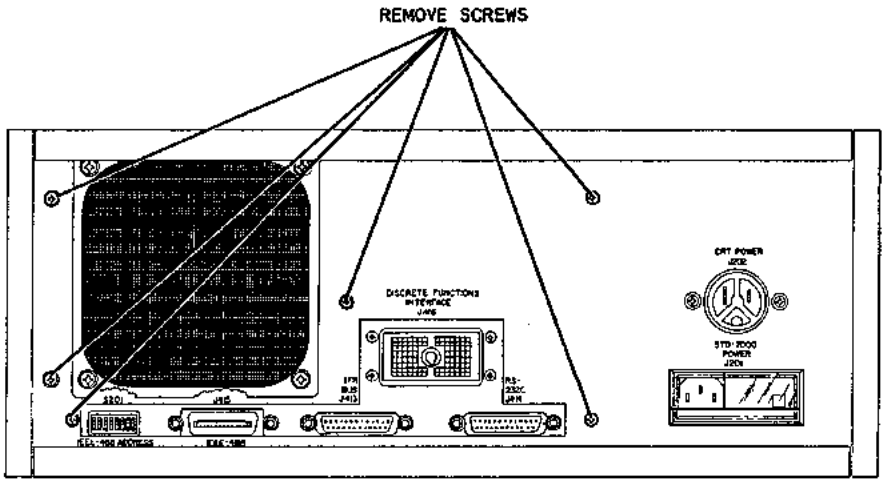
CAUTION: THE CPU (YELLOW) AND I/O (BLUE) PC BOARDS MUST BE INSTALLED IN THE ASSIGNED SLOTS WITHIN THE CARD CAGE ASSEMBLY TO PRECLUDE DAMAGE TO CPU.

NOTE: The remaining PC Boards are interchangeable for testing purposes, but should be returned to assigned positions prior to unit being returned to service.

3 Disconnect Power Supply Harness (43) at J18 on Motherboard (11).

4 Disconnect Tape Transport Ribbon Cable (41) at J19 on Motherboard (11).

5 Unplug Cooling Fan Electrical Connector (40) from Cooling Fan (7).



STD-7000 Rear Panel
Figure 71

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6 Remove six screws from Rear Panel Assembly as shown in 2-2-5, Figure 71.

7 Position STD-7000 so it rests on its Rear Panel Assembly (8) to allow access to both top and bottom openings.

8 While supporting Card Cage Assembly (4), remove four screws (21) and washers (20) securing Card Cage Rail Assembly (25) to Brackets (23, 29 and 33). Carefully lift Card Cage Assembly (4) through Bottom opening of STD-7000.

(b) Disassembly (Refer to 2-2-5, Figure 70)

1 Remove twenty screws (19) and washers (18) securing Card Cage (1), Insulators (2 and 8), and Motherboard (3) to Rails (4 and 7).

2 Remove four screws (6) and washers (5) securing Rails (4) to Rails (7).

3 Remove two screws (20), washers (22) and nuts (23) securing Bracket (21) to Card Cage (1).

4 Carefully remove each Card Guide (9 thru 17). (Refer to 2-2-5, Figure 70 as a guide during installation.)

(9) ORANGE	(12) VIOLET	(14) GREEN
(10) YELLOW	(13) BROWN	(16) GRAY
(11) BLUE	(14) RED	(17) BLACK

CAUTION: TAKE CARE NOT TO EXERT UNDUE FORCE OR STRAIN ON IEEE-488 DIP SWITCH (37), IEEE-488 INTERFACE CONNECTOR (36), IFR BUS INTERFACE CONNECTOR (35), RS232C INTERFACE CONNECTOR (47) OR DISCRETE FUNCTIONS INTERFACE CONNECTOR (43). AFTER CONNECTOR SUPPORT PANEL (32) REMOVAL, THE SOLDER CONNECTIONS OF THE AFORE-MENTIONED CONNECTORS ARE THE ONLY MEANS OF SUPPORT.

5 Remove two 1/4" shell nuts (30 and 31) securing IEE-488 Interface Connector, J415 (36) to Connector Support Panel (32).

NOTE: Two Mounting Blocks (38) will be free when 1/4" shell nuts (30 and 31) are removed.

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6 Remove four 3/16" shell nuts (26 or 28) and washers (25 or 29) securing IFR Bus Interface Connector, J413 (35) and RS232C Interface Connector, J414 (47) to Connector Support Panel (32).

7 Remove four screws (27), flat washers (42), lock washers (41) and hex nuts (40) securing Discrete Functions Interface Connector, J416 (43) to Connector Support Panel (32).

8 Remove four screws (33) and washers (34) securing Connector Support Panel (32) to Motherboard (3).

9 Remove two screws (24), washers (46) and hex nuts (45) securing baffle (44) to Connector Support Panel (32).

(3) Front Panel Assembly

(a) Front Panel Assembly Removal (Refer to 2-2-5, Figure 69)

1 Remove Top Cover (2) and Bottom Cover (19) per 2-2-5B(1)(a).

2 Disconnect Tape Transport Ribbon Cable (41) at J-19 (27).

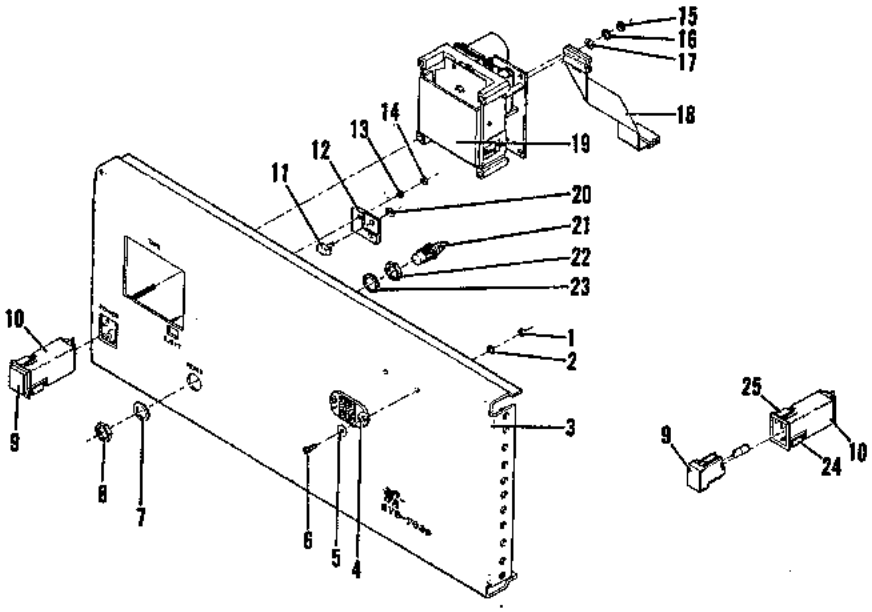
3 Unsolder five wires from STD-7000 AC Power Switch (10) (Refer to 2-2-5, Figure 72).

4 Unsolder two wires from Reset Button (21) (Refer to 2-2-5, Figure 72).

5 Remove two screws (21) and washers (20) from two forward Brackets (23 and 29) securing each side frame (13 and 31) to Rail Assembly (25).

6 Remove eight screws (18), four each securing each side frame (13 and 31) to Front Panel Assembly (26). Spread front of side frames to release Front Panel Assembly (26).

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Front Panel Assembly
Figure 72

(b) Disassembly (Refer to 2-2-5, Figure 72)

1 Remove STD-7000 Power Switch (10)

a Unsolder leads from switch (10).

b Pull gently on switch pushbutton (9) to remove it from switch (10).

c Loosen two screws (24) located inside switch (10), then rotate retainers (25) to clear front panel (3) and withdraw switch (10).

CAUTION: DURING REASSEMBLY, DO NOT OVER TIGHTEN THESE SCREWS OR POWER SWITCH OPERATION MAY BE IMPAIRED.

2 Remove Tape Transport (19)

a Disconnect Ribbon Cable (18) (2-2-5, Figure 72) at J19 (27) (2-2-5, Figure 69) on Mother Board (11) (2-2-5, Figure 69).

b Remove left side cover in accordance with 5.B.(1)(b)2.

c Remove four hex nuts (15), lock washers (16) and flat washers (17) securing Tape Transport (19) to Front Panel (3).

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3 Remove Magnetic Tape Eject Button (11)

a Remove to hex nuts (14) and flat washers (13) from retainer (12) securing Button (11) to front panel (3).

b Carefully remove clip (20) securing Button (11) to Retainer (12).

4 Remove Reset Button (21)

a Unsolder two leads from Button Assembly (21).

b Remove hex nut (8) and flat washer (7), then slide Reset Button (21) through hole in Front Panel (3).

NOTE: Hex nuts (8 and 22) and crush washer (23) are supplied with new Button (21).

5 Remove Keypad Mount (4)

a Remove two hex nuts (1), lock washers (2), screws (6) and flat washers (5) securing keypad mount (4) to Front Panel (3).

(4) Rear Panel Assembly

(a) Rear Panel Assembly (2-2-5, Figure 69)

1 Remove Top Cover (2) and Bottom Cover (19) per 2-2-5B(1)(a).

2 Unplug Cooling Fan Electrical Connector (40) from Cooling Fan (7).

3 Remove six screws from Rear Panel as shown in 2-2-5, Figure 73.

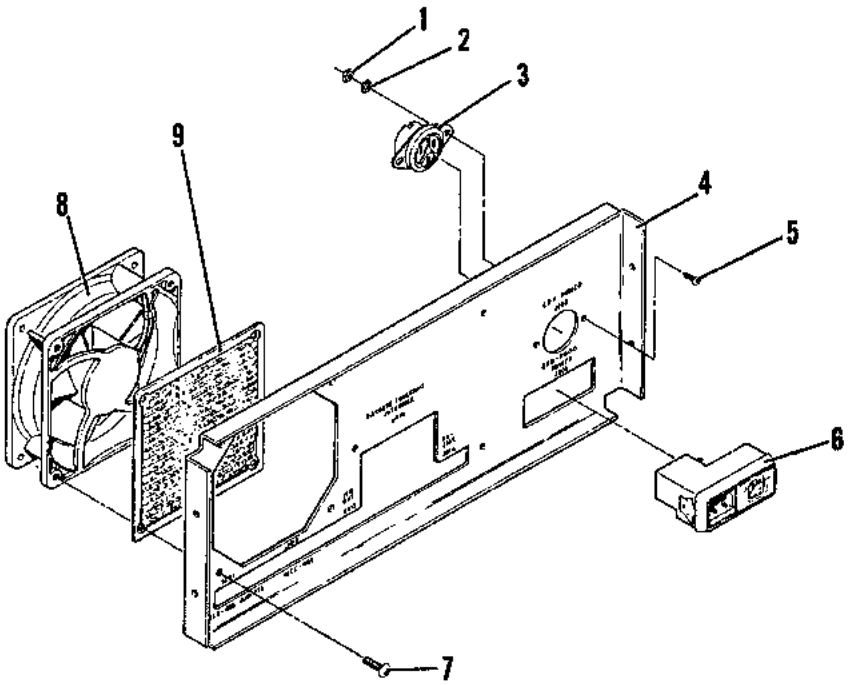
4 Remove side covers (15) per 2-2-5B(1)(b)2.

5 Loosen screws (21) securing Brackets (33 and rear 23) to Rail Assembly (25).

6 Remove four screws (9) and flat washers (10) securing Rear Panel (8) to side frames (13 and 31).

7 Gently spread Side Frames (13 and 31) and remove Rear Panel (8).

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Rear Panel Assembly
Figure 73

NOTE: Brackets (8A) (2-2-5, Figure 69) and (21) (2-2-5, Figure 70) are not normally removed with Rear Panel Assembly.

(b) Disassembly (Refer to 2-2-5, Figure 73)

1 Remove AC Power Cord Connector (6)

a Unsolder and tag two wires from AC Power Cord Connector (6).

b Depress both sides of retaining clip on one end of AC Power Cord Connector (6) and simultaneously press clip through Rear Panel Assembly (4).

c Repeat Step b. for opposite end of AC Power Cord Connector (6) and withdraw AC Power Cord Connector (6) from Rear Panel (4).

2 Remove CRT POWER Connector (3)

a Remove two screws (5), hex nuts (1) and lock washers (2) securing CRT Power Connector (3) to Rear Panel (4).

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b Unsolder and tag two wires from CRT Power Connector (3).

3 Remove Cooling Fan Assembly (8)

a Remove four screws (7) attaching cooling fan (8) and screen (9) to Rear Panel (4).

NOTE: Disconnect cooling fan plug (40) (2-2-5, Figure 69) if not already completed.

(5) DC Power Supply Assembly (28) (35) (Refer to 2-2-5, Figure 69)

(a) Sierracin (Model 5CXMP) (35) or IFR, Inc. Power Supply (28) Removal

1 Remove Top Cover (2) per 2-2-5B(1)(a).

2 Remove four screws (14) securing left side cover (15) to left side frame (31).

3 Disconnect and tag leads (43) from Sierracin (Model 5CXMP) Power Supply Terminal Block or squeeze both releases while simultaneously pulling plug from connector (34) (2-2-5, Figure 69) on IFR Power Supply.

NOTE: During reassembly, use Table 14 below to identify lead (43) positions.

PIN	FUNCTION	WIRE COLOR
1	+5V	ORANGE
1	+12V	RED
2	+5V	ORANGE
2	-5V	GREEN
3	-5V	BLACK
3	GND	BLACK
4	-5V	BLACK
4	-12V	YELLOW
5	N/U	N/U
6	AC INPUT	WHITE
7	AC INPUT	WHITE/BLACK

Sierracin Power Supply Terminal Block
Table 14

4 Remove four screws (36), lock washers (38) and nuts (39) securing Sierracin Power Supply (35) attaching Bracket (37) or IFR Universal Power Supply (28) to side frame (31).

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5 Lift Power Supply (28) and Bracket (37) while allowing leads (43) to pass between them (IFR Universal Power Supply (28) will be free to remove).

CAUTION: DO NOT PLACE UNNECESSARY STRAIN ON MOTHER BOARD CONNECTOR J-18 WHILE REMOVING DC POWER SUPPLY.

(b) IFR Systems, Inc., Power Supply Disassembly (Refer to 2-2-5, Figure 74)

1 Remove four screws (1) securing cover (3) to housing (12).

2 Remove hex nut (5) and washer (6) securing PC Board (9) to shell nut (10).

3 Remove six screws (13) securing rails (7) to housing (12).

NOTE: It is not necessary to remove screw (14) at this time.

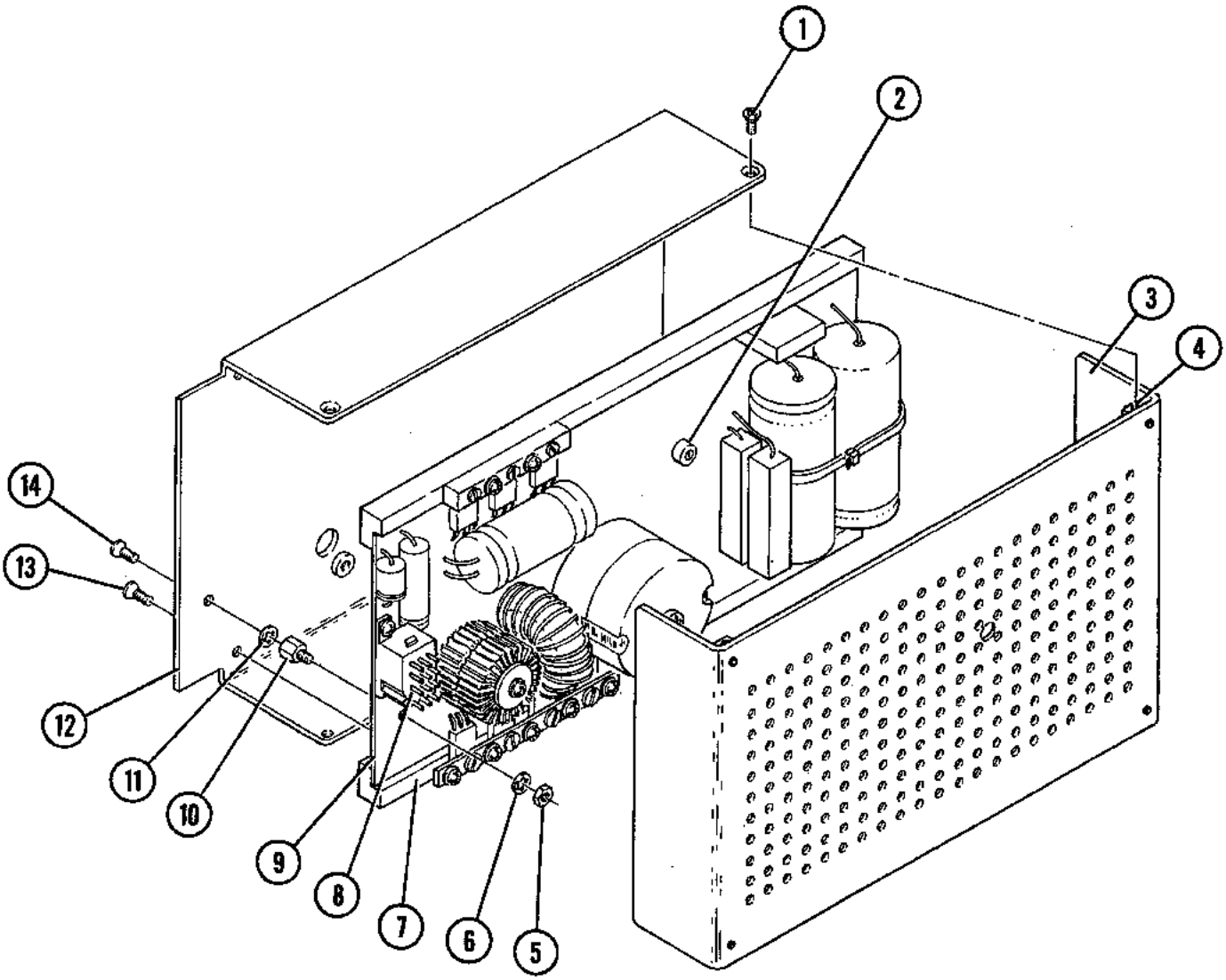
4 Lift PC Board Assembly (9) until it clears shell nut (10) then slide PC Board Assembly (9) out of housing (12) at either end.

5 Remove screw (14) attaching shell nut (10) and lock washer (11) to housing (12).

NOTE: Attach shell nut (10) and lock washer (11) to housing (12) before attaching PC Board (9).

NOTE: It is not necessary to remove Power Supply Cover (3) for access to Adjustment Point R9932 (2).

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IFR Universal Power Supply Assembly
Figure 74

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6. Module Testing

A. General

This section contains an overall testing procedure intended to aid the technician in determining whether a given PC board, suspected as being defective, is serviceable or requires replacement. To individually test each PC board within the card cage, the aid of all other card cage PC boards is required. Otherwise, the use of highly sophisticated and expensive accessory test equipment (such as: Logic Analyzer, Bus Simulator, Z-80 Emulator, etc.) would be necessary. It is advisable that the technician carefully evaluate the repair requirements, as well as his or her abilities and experience, before attempting corrective action. While the recommended corrective action is to replace the defective module or PC board, once it has been isolated and identified, the technician may elect to repair obvious defects such as broken, chipped, cracked or burned components. Under these conditions, the determination of whether to repair or replace a module, is left at the technician's discretion.

2-2-1 of this manual contains a detailed theory of operation for each module within the STD-7000. The technician should find each theory extremely helpful in the repair process. Occasionally, the technician will find it necessary to refer to selected circuit schematics, PC board layout drawings, mechanical drawings, etc. These drawings are located in the following sections of this manual:

Front and Rear Panel Illustrations	1-2-2
Mechanical Assembly Drawings	2-2-5
Circuit Schematics	2-2-7
PC Board Layout Drawings	2-2-8

(1) Safety Precautions

As with any piece of electronic equipment, extreme caution should be taken when working with live circuits. Even though the circuits and/or components within the STD-7000 Bus Controller containing a lethal voltage is isolated to the Power Supply Module, also keep in mind that the circuits and/or components within certain accessory test equipment contain extremely high voltage potentials. All of which are capable of causing serious bodily injury or death. When performing the tests in this section, be sure to observe the precautions listed in the accessory test equipment's service manuals, as well as the following:

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WARNING: DO NOT REMOVE POWER SUPPLY NOR POWER SUPPLY COVER FROM STD-7000 WITH EXTERNAL AC POWER CONNECTED. AFTER EXTERNAL AC POWER IS REMOVED, WAIT A MINIMUM OF 5 MINUTES BEFORE HANDLING, TO ALLOW HIGH VOLTAGE CONTROL CIRCUIT TO DISSIPATE.

WARNING: THE STD-7000 REAR PANEL CORCOM CONNECTOR, CRT POWER RECEPTACLE AND ASSOCIATED WIRING CARRY EITHER 120 OR 240 VAC AS LONG AS EXTERNAL POWER CORD IS CONNECTED TO STD-7000 AND EXTERNAL POWER SOURCE. DO NOT CONTACT THESE OR OTHER ASSOCIATED COMPONENTS DURING TESTING.

WARNING: REMOVE ALL JEWELRY OR OTHER COSMETIC APPAREL BEFORE PERFORMING ANY TESTS INVOLVING LIVE CIRCUITS.

WARNING: HEED ALL WARNINGS AND CAUTIONS PRIOR TO AND IMMEDIATELY FOLLOWING A PARTICULAR STEP BEFORE CONTINUING.

CAUTION: REMOVE AC POWER FROM POWER SUPPLY BEFORE REMOVING OR REPLACING ANY PLUG-IN PC BOARD OR COMPONENT. TO DO THIS, SIMPLY DEPRESS AC POWER SWITCH TO OFF. SERIOUS DAMAGE COULD OCCUR IF THIS CAUTION IS NOT ADHERED TO.

(2) Test Equipment Requirements

Appendix B, at the rear of this manual, contains a comprehensive list of test equipment suitable for performing any test procedure in this manual. Any other test equipment meeting the specifications listed in Appendix B may be substituted in place of recommended models.

(3) Disassembly/Reassembly Requirements

To perform the tests in this section, the top dust cover must be removed from the STD-7000. Refer to 2-2-5, for cover removals, module removals or mechanical assembly drawings.

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B. STD-7000 Module Tests

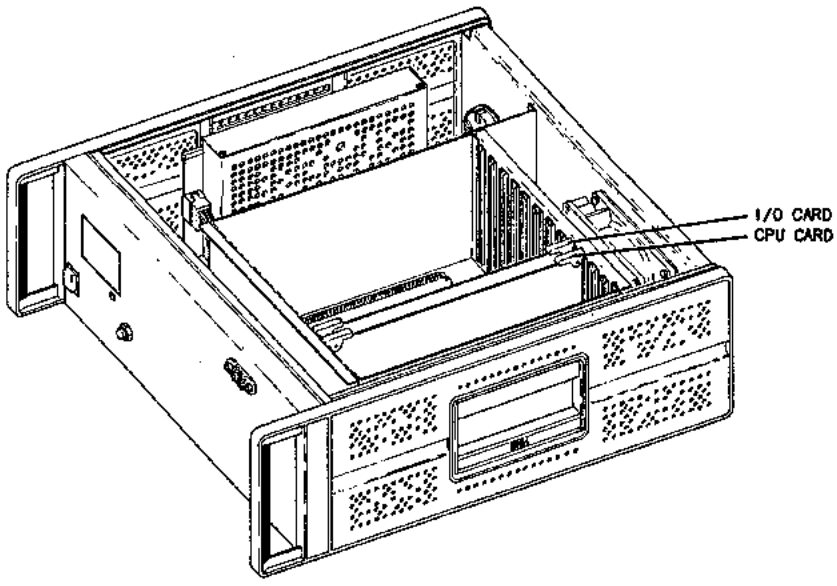
(1) Card Cage

SPECIAL ACCESSORY
EQUIPMENT REQ'D: None

NOTE: Interface the STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad in accordance with instructions located in 1-2-1.

NOTE: Steps 1 thru 12 verify operation of the Tape Cassette and Transport, RS232C and CRT Display, and Processor Bus.

STEP	PROCEDURE
1.	Remove top dust cover (if not previously removed).
2.	Remove all plug-in PC boards from card cage, except CPU (yellow) and I/O (blue), as shown in 2-2-6, Figure 75.



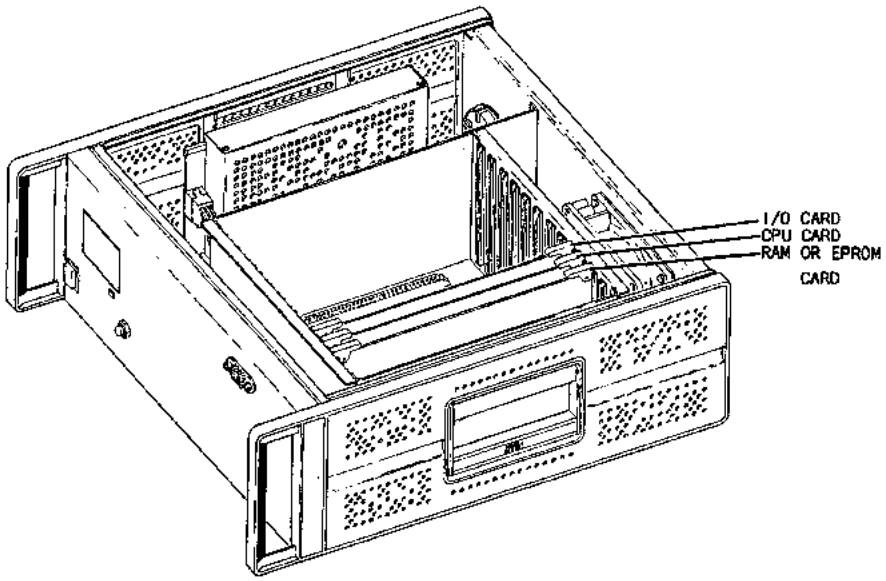
CPU and I/O Test Set-Up
Figure 75

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STEP	PROCEDURE
3.	Connect STD-7000 line cord to an approved external power receptacle (rated at 115 VAC/60 Hz).
4.	Position STD-7000 Rear Panel IEEE-488 Address Switch Segments 7 and 8 to OFF.
5.	Power-up system by depressing AC Power Switch (5), on STD-7000 Front Panel.
6.	Momentarily depress STD-7000 RESET Switch (3) and verify Diagnostic Menu appears on CRT Display screen.
7.	Using Numeric Keypad, enter 9 (9 = TEST RAM) and observe a minimum of five or more asterisks (*****) appear in succession on CRT Display screen.
	NOTE: Disregard arbitrary memory printout on CRT Display screen prior to initiation of asterisks.
8.	Momentarily depress RESET Switch (3) to discontinue RAM TEST and remove asterisks from CRT Display Screen.
9.	Insert a valid mini-cassette personality tape in the Tape Transport.
10.	Using Numeric Keypad, enter 1 (1 = LOAD TAPE). Observe *MEM*4ØØØ ØØ C3 (indicates RAM Memory Card removed).
	NOTE: Steps 11 thru 17 verify operation of RAM, EPROM, and/or CPU Card memory locations.
11.	Remove AC power from Power Supply by depressing AC Power Switch (5) to OFF position.
12.	Install RAM or EPROM Memory Card (orange) in Card Cage memory slot next to CPU Card as shown in 2-2-6, Figure 76.
	NOTE: If both Memory Cards are being used, place RAM Card in slot next to CPU.

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STEP PROCEDURE



Memory Test Set-Up
Figure 76

13. Return AC power to Power Supply by depressing AC Power Switch (5) to ON position.

14. Momentarily depress RESET Switch (3) and verify Diagnostic Menu appears on CRT Display.

15. Using Numeric Keypad, enter 9 (9 = TEST RAM) and observe a minimum of five consecutive asterisks (*****) with no memory errors.

    NOTE: Disregard abitrary memory printout on CRT Display screen, prior to initiation of asterisks.

16. Momentarily depress RESET Switch (3) to discontinue RAM Test and remove asterisks from CRT Display.

17. Using Numeric Keypad, enter 1 (1 = LOAD TAPE) and observe no synchronization (SYNC), check sum (CS), or Memory (MEM) errors exist prior to the appearance of a small L to the right of KEYIN, on CRT Display.

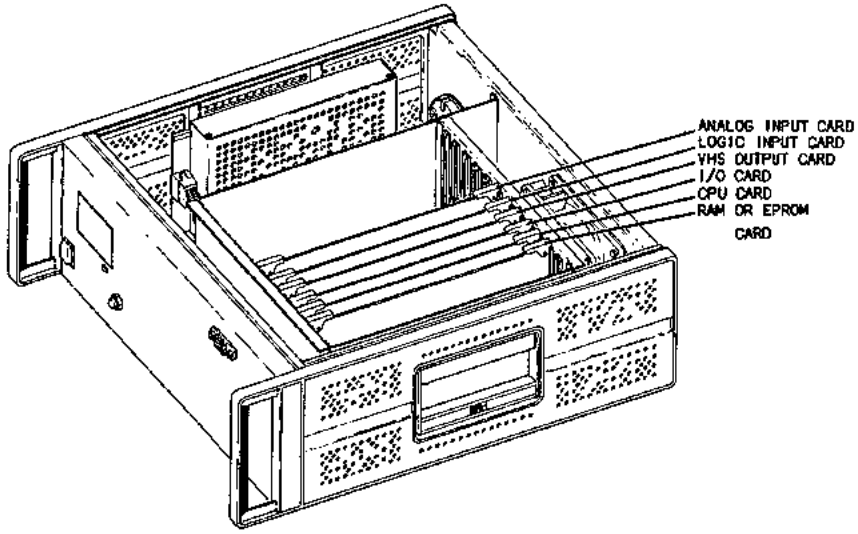
    NOTE: Steps 18 through 23 verify operation of VHS Output Card.

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STEP PROCEDURE

18. Remove AC power from Power Supply by depressing AC Power Switch (5) to OFF position.

19. Install VHS OUTPUT Card (violet) in J405 position (slot next to I/O Card), LOGIC INPUT Card (red) in J406 position and ANALOG INPUT Card (green) in J407 position as shown in 2-2-6, Figure 77.



VHS Output Test Set-Up
Figure 77

20. Apply AC power to Power Supply by depressing AC Power Switch (5) to ON position.

21. Momentarily depress RESET Switch (3) and verify Diagnostic Menu appears on CRT Display.

22. Using Numeric Keypad, enter 5 (5 = EXECUTE TAPE) and observe Master Menu, after rewinding/loading sequence.

23. Proceed to and comply with instructions in 2-2-2B(3).

NOTE: After successful completion of Data Bus Performance Evaluation, return to Step 24 of this test.

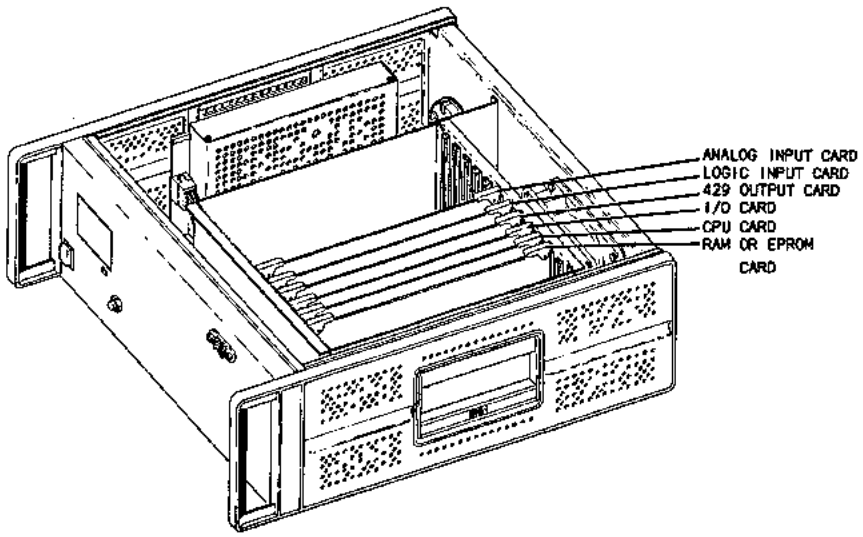
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STEP PROCEDURE

24. Momentarily depress RESET Switch (3).

25. Remove AC power from Power Supply by depressing AC Power Switch (5) to OFF position.

NOTE: Steps 26 through 35 verify operation of 429 OUTPUT Cards. Each card may be tested individually (2-2-5, Figure 78) or as a group (2-2-5, Figure 79) as long as no two 429 OUTPUT Cards have the same jumper locations and no card slots remain empty between CPU Card and last card (ANALOG INPUT Card).



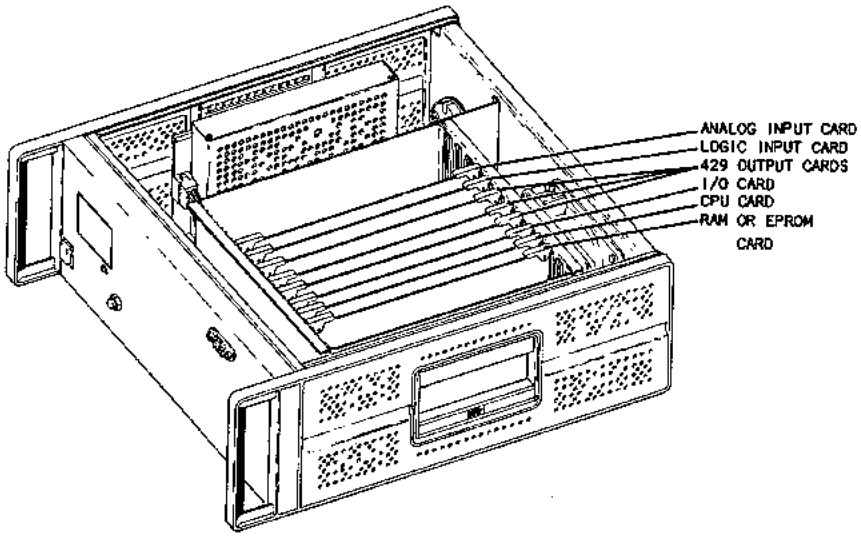
Test Set-Up for One 429 Output Card
Figure 78

26. Remove LOGIC INPUT (red) and ANALOG INPUT Cards (green) and install 429 OUTPUT Card(s) (brown) in slots shown in either 2-2-5, Figure 78 or 2-2-5, Figure 79.

NOTE: If desire is to test 429 OUTPUT only, remove VHS OUTPUT Card (violet) and install first 429 OUTPUT Card (brown) in the slot immediately following the I/O Card (blue). Either install remaining 429 OUTPUT Cards consecutively and/or place LOGIC INPUT (red) and ANALOG INPUT (green) Cards so that no empty slots are between CPU Card (yellow) and ANALOG INPUT Card (green).

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STEP PROCEDURE



Test Set-Up for All 429 Output Cards
Figure 79

27. Install LOGIC INPUT Card (red) in next open slot following last 429 OUTPUT Card (brown).

28. Install ANALOG INPUT Card (green) in next open slot following LOGIC INPUT Card (red).

29. Apply AC power to Power Supply by depressing AC Power Switch (5) to ON position.

30. Proceed to and comply with instructions in 2-2-2B(1) and 2-2-2B(2).

NOTE: Instructions in Step 30 applies to 429 OUTPUT Cards with jumpered locations as follows:

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STEP PROCEDURE

429 OUTPUT CARD	JUMPER LOCATION	BUS
1	ØB-ØA 1B-1A	CONTROL "
2	2B-2A 3B-3A	CONTROL "
3	4B-4A 5B-5A	ATTITUDE "

429 Output Card Jumper Location
Table 15

NOTE: After successful completion of Control and Attitude Bus Performance Evaluations, return to Step 31 of this test.

31. Momentarily depress RESET Switch (3).

32. Depress AC Power Switch (5) to remove AC power from Power Supply.

33. Check configuration of cards within card cage and place each card in its assigned slot if necessary (refer to 2-2-1, Figure 2 for best operational location of each card).

34. Install top dust cover.

35. Remove mini-cassette personality tape.

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(2) Power Supply

SPECIAL ACCESSORY
EQUIPMENT REQ'D: 1 Digital Multimeter - 100 KΩ/V

NOTE: Power Supply Module should be tested under normal operating conditions. Any adjustments made under other than normal operating loads will be inaccurate.

STEP	PROCEDURE
1.	Remove Top (2) and Bottom (25) (2-2-5, Figure 69) dust covers per instructions in 2-2-5.
2.	Interface the STD-7000 Bus Controller, ESP 6515 CRT Display Terminal, CRT Interface and KP-72480 Numeric Keypad in accordance with instructions located in 1-2-1.
3.	Connect STD-7000 line cord to an approved external power receptacle (rated at 115 VAC/60 Hz).
4.	Depress AC Power Switch (5) to ON position.
5.	Set Digital Multimeter to measure and indicate positive DC voltage.
	NOTE: Choice of STD-7000 connector(s) for checking voltages in Steps 6 thru 11 is left to the discretion of the technician, however J405 thru J412 are recommended.
6.	Connect Digital Multimeter ground lead to pin 3 or 4 of either Motherboard connectors J405 thru J412 (accessible on bottom of Motherboard).
7.	Connect Digital Multimeter positive lead to either pin 1 or 2 of J405 thru J412 and verify +5VDC (± 0.2V) is indicated.
8.	Connect Digital Multimeter positive lead to either pin 99 or 100 of J405 thru J412 and observe +12VDC (±0.2V) is indicated.
9.	Set Digital Multimeter to indicate negative DC voltage.
10.	Connect Digital Multimeter positive lead to either pin 5 or 6 of J405 thru J412 and verify -5VDC (±0.2V) is indicated.

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STEP	PROCEDURE
11.	Connect Digital Multimeter positive lead to either pin 95 or 96 of J405 thru J412 and verify -12 VDC (±0.2V) is indicated.
NOTE:	If any of the above values are not obtained, refer to 2-2-3 and check calibration of +5V circuit. If +5V circuit cannot be calibrated, go to appropriate troubleshooting flowchart in 2-2-4.

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7. Schematics

A. General

This section contains interconnect diagrams and circuit schematics for the STD-7000. These drawings are sequenced in the same order they are discussed in 2-2-1.

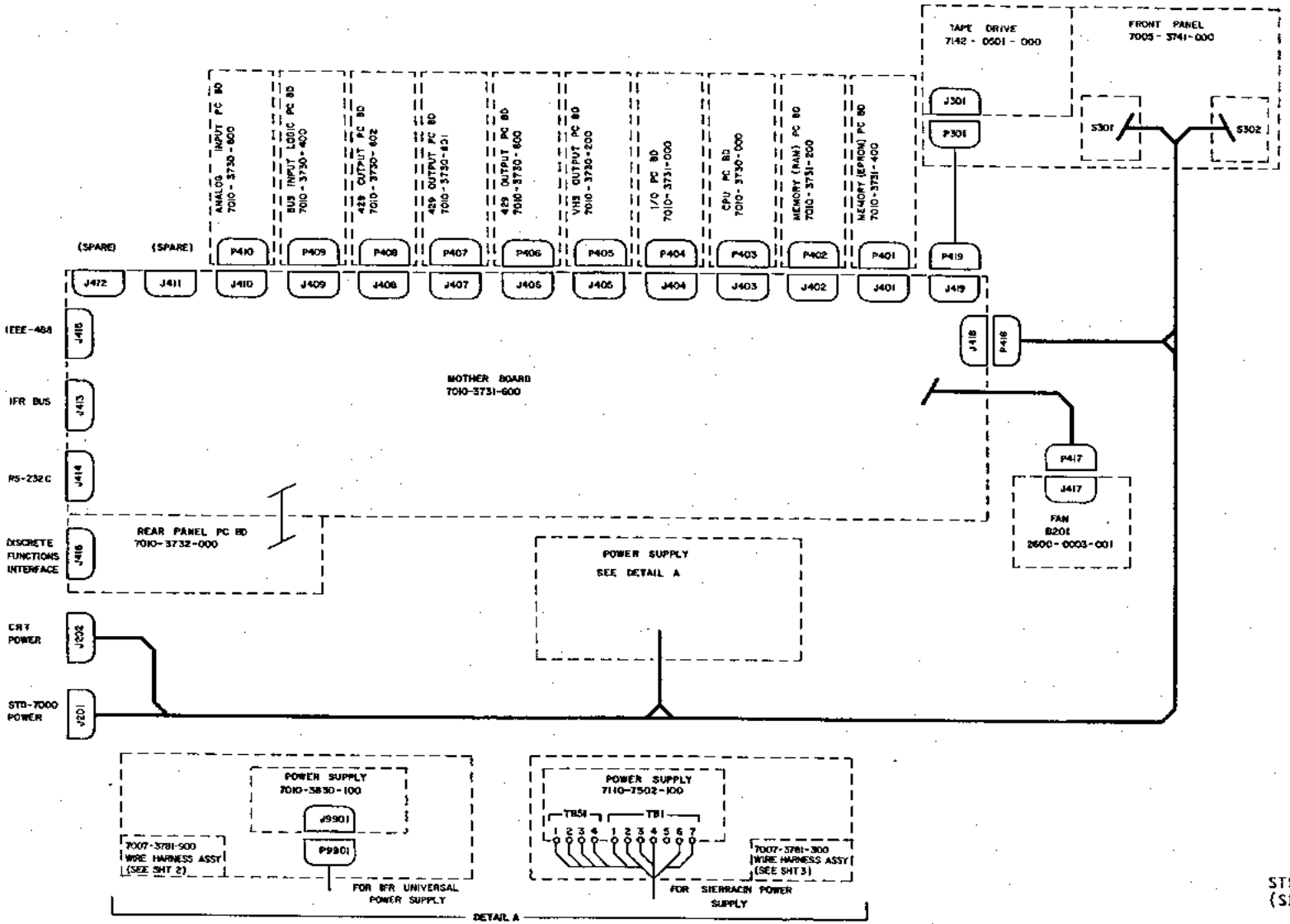
B. Interconnect Diagrams and Circuit Schematics

Figure	Title	Page
80	STD-7000 Interconnect Diagram	3
81	CRT Interface Interconnect Diagram	6
82	STD-7000 Motherboard Circuit Schematic	7
83	STD-7000 Keypad Circuit Schematic	8
84	Rear Panel Circuit Schematic	9
85	32K PROM PC Board Circuit Schematic	10
86	16K RAM PC Board Circuit Schematic	12
87	CPU PC Board Circuit Schematic	14
88	I/O PC Board Circuit Schematic	16
89	VHS Output PC Board Circuit Schematic	19
90	429 Bus Output PC Board Circuit Schematic	21
91	Bus Input Logic PC Board Circuit Schematic ...	26
92	Bus Input Analog PC Board Circuit Schematic ..	28
93	Universal Power Supply, Voltage Regulator Circuit Schematic	30
94	CRT Interface Circuit Schematic	32

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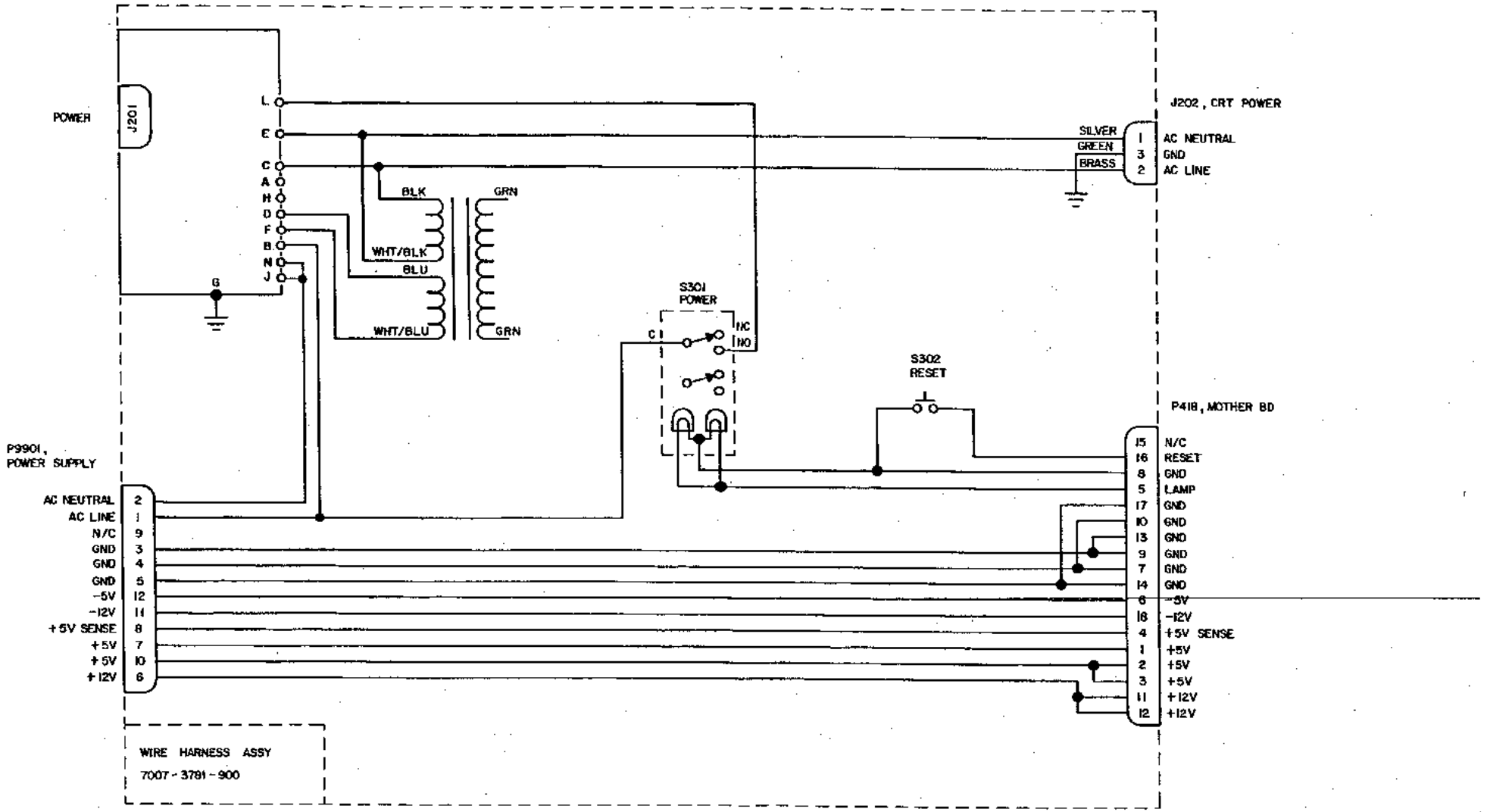
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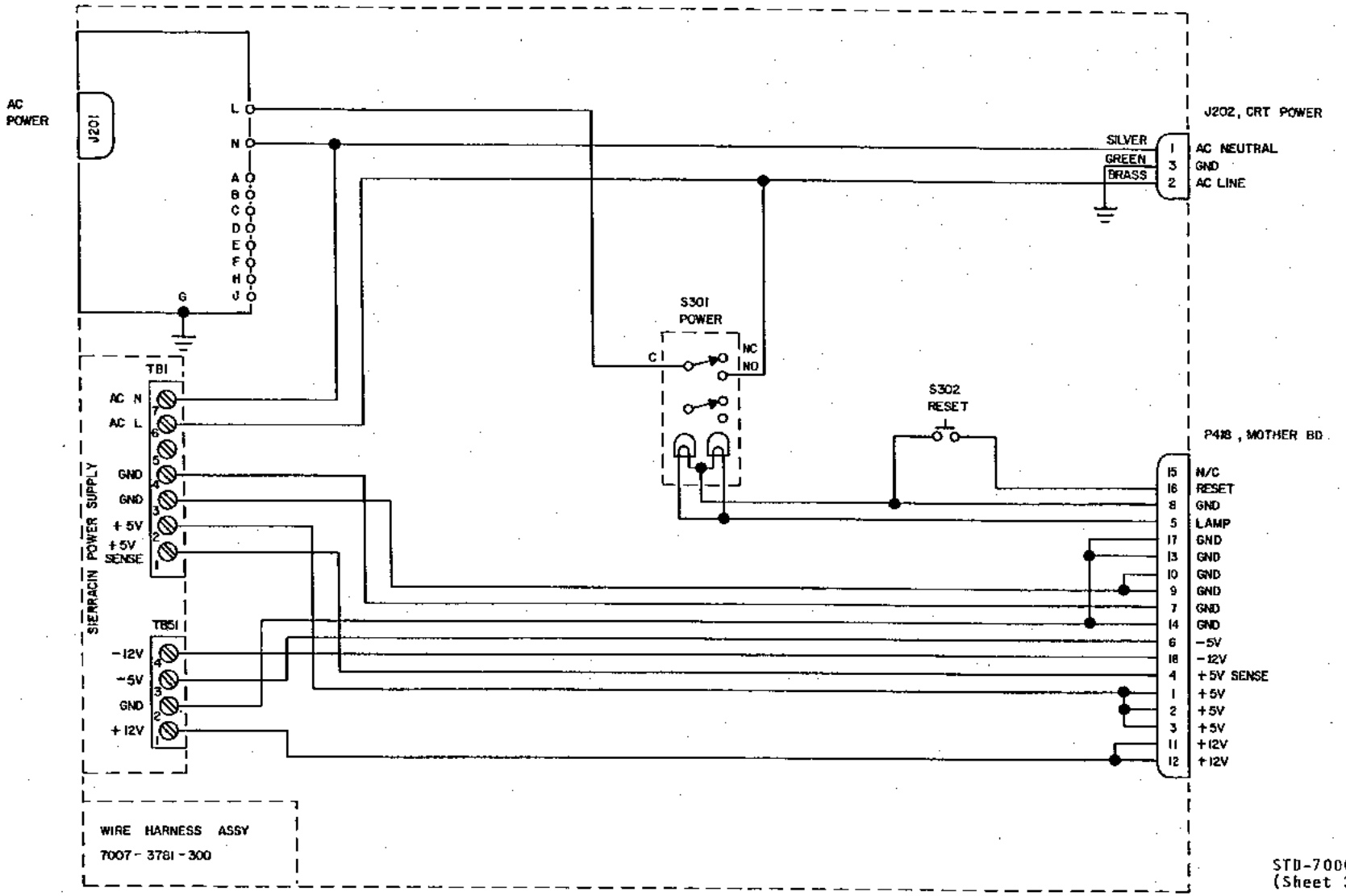
STD-7000 Interconnect Diagram
(Sheet 1 of 3)
Figure 80

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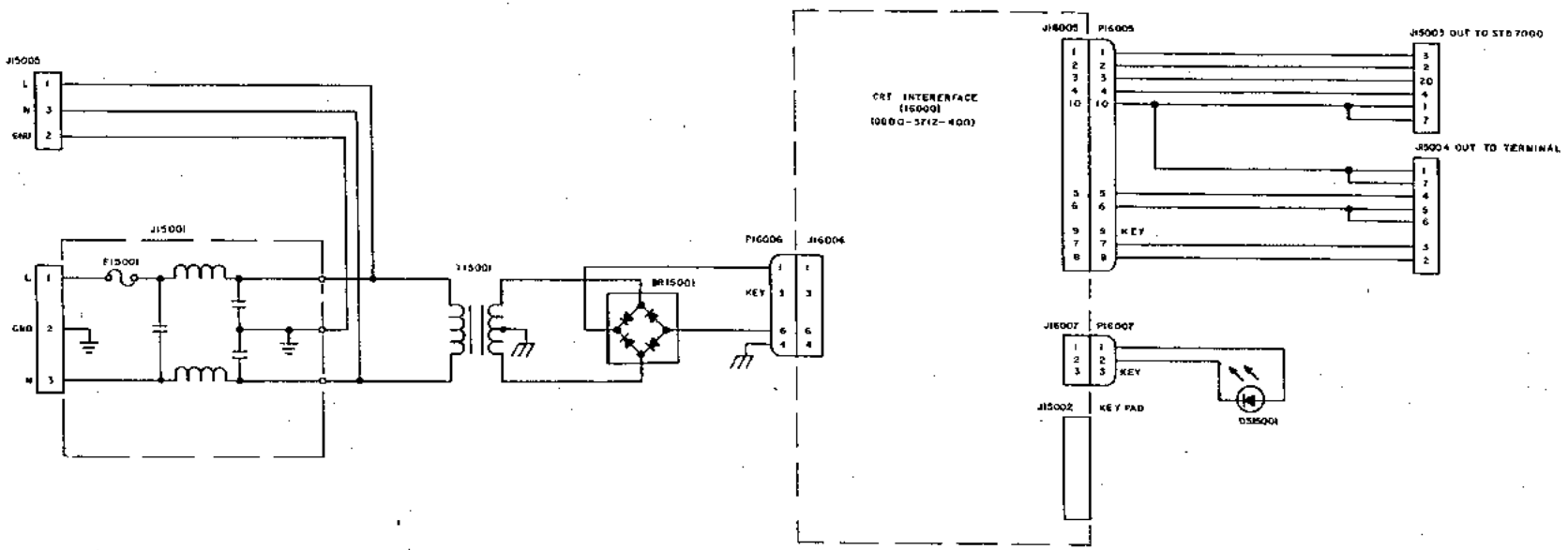
STD-7000 Interconnect Diagram (Sheet 2 of 3)
Figure 80

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STD-7000 Interconnect Diagram
(Sheet 3 of 3)
Figure 80

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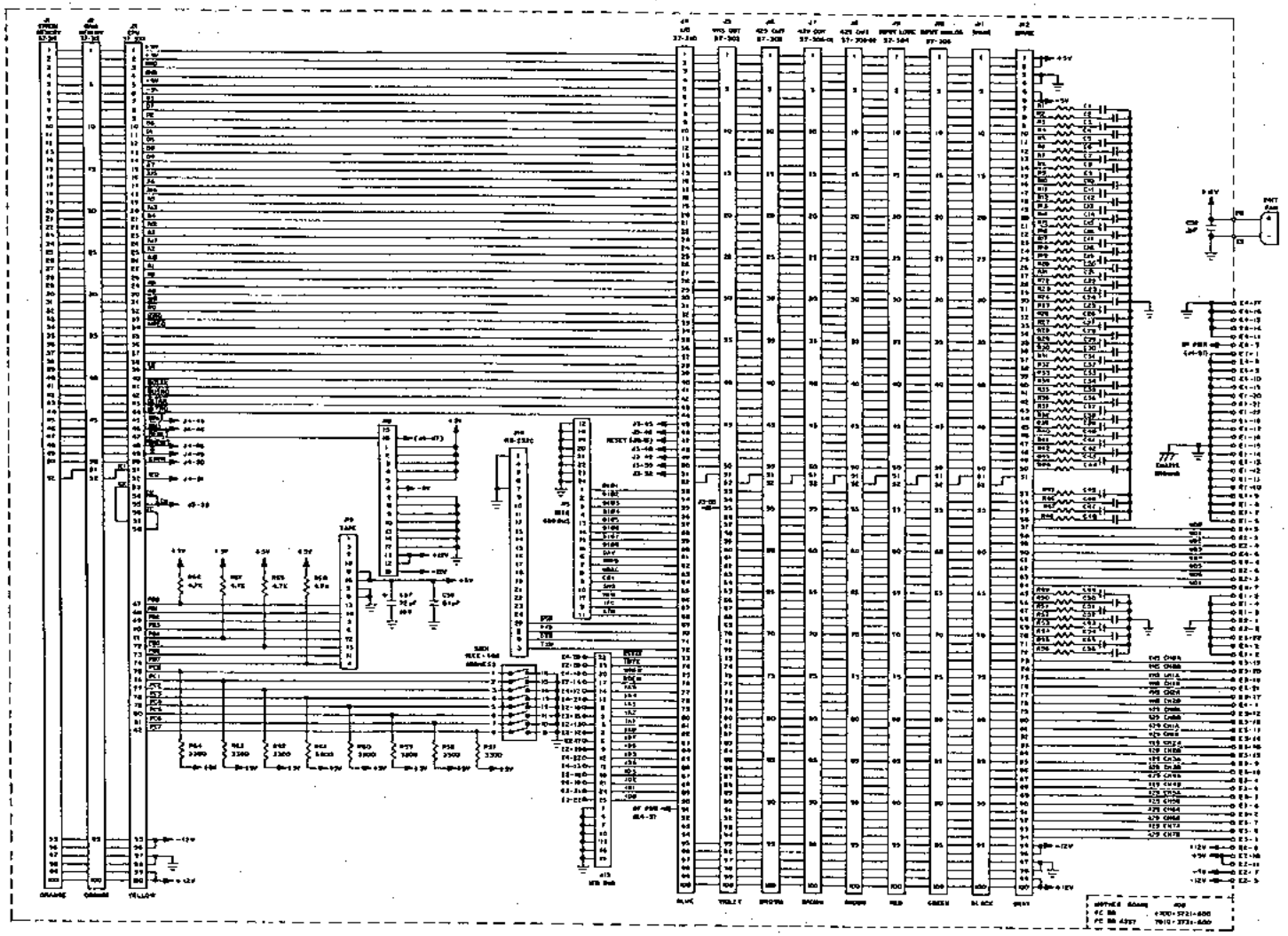


NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 15000 AND 16000 (E.G, F1 IS F15001).
2. ALL AC POWER (PRIMARY) WIRING IS #22 AWG; ALL OTHER WIRING IS #26 AWG.

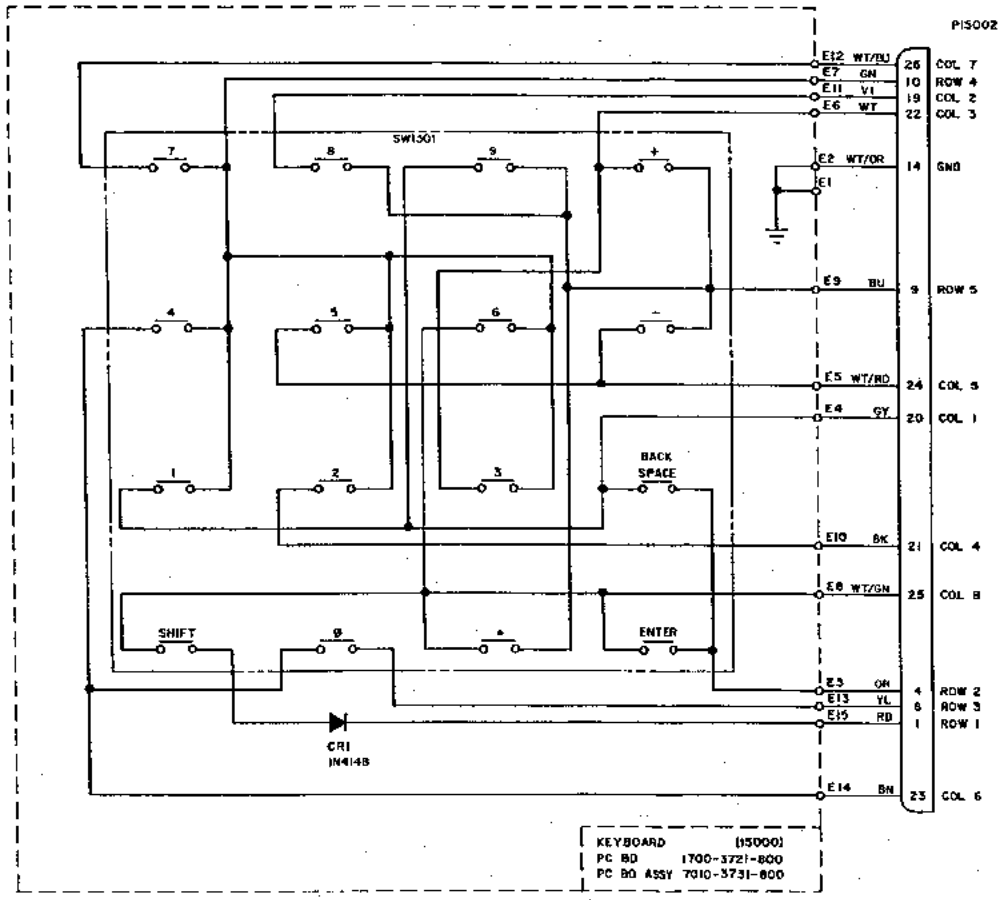
CRT Interface Interconnect Diagram
Figure 81

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Motherboard Circuit Schematic
Figure 82

Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com

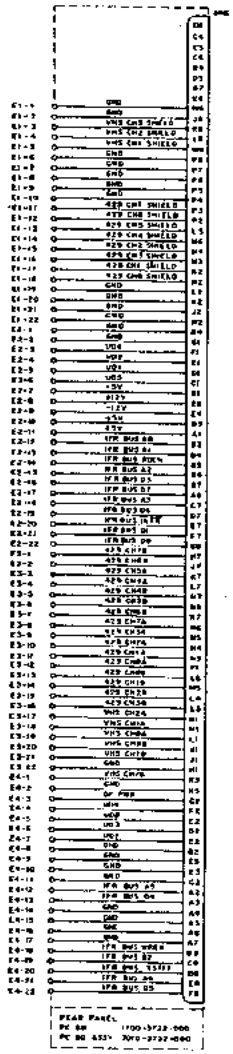


NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 15000 (E.G., CR1 IS CR15001).

STD-7000 Keypad Circuit Schematic
Figure 83

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Rear Panel Circuit Schematic
Figure 84

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NOTES:

1. UNUSED IC GATES:

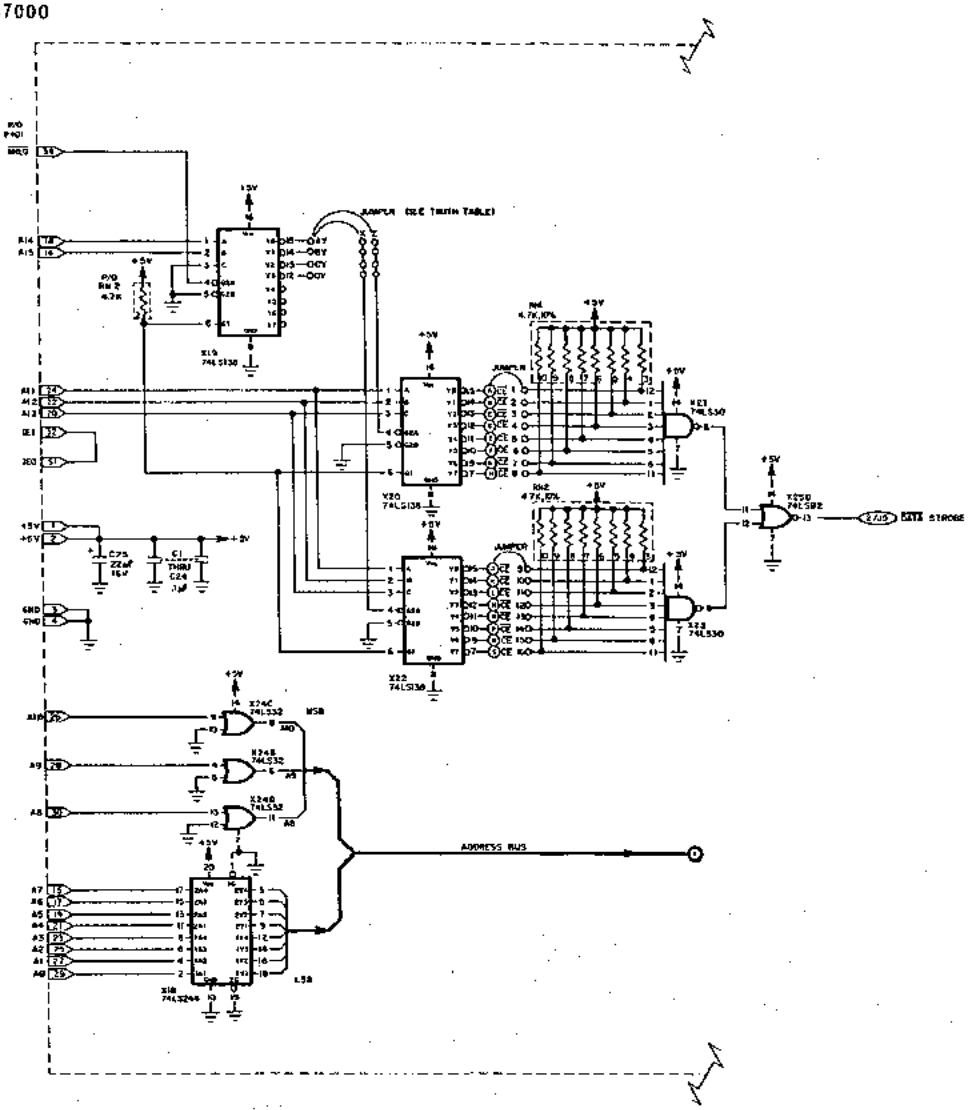
   X25A, B AND C

2. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 1200 (I.E. R1 IS R1201).

PC 60 ADDRESS
TRUTH TABLE

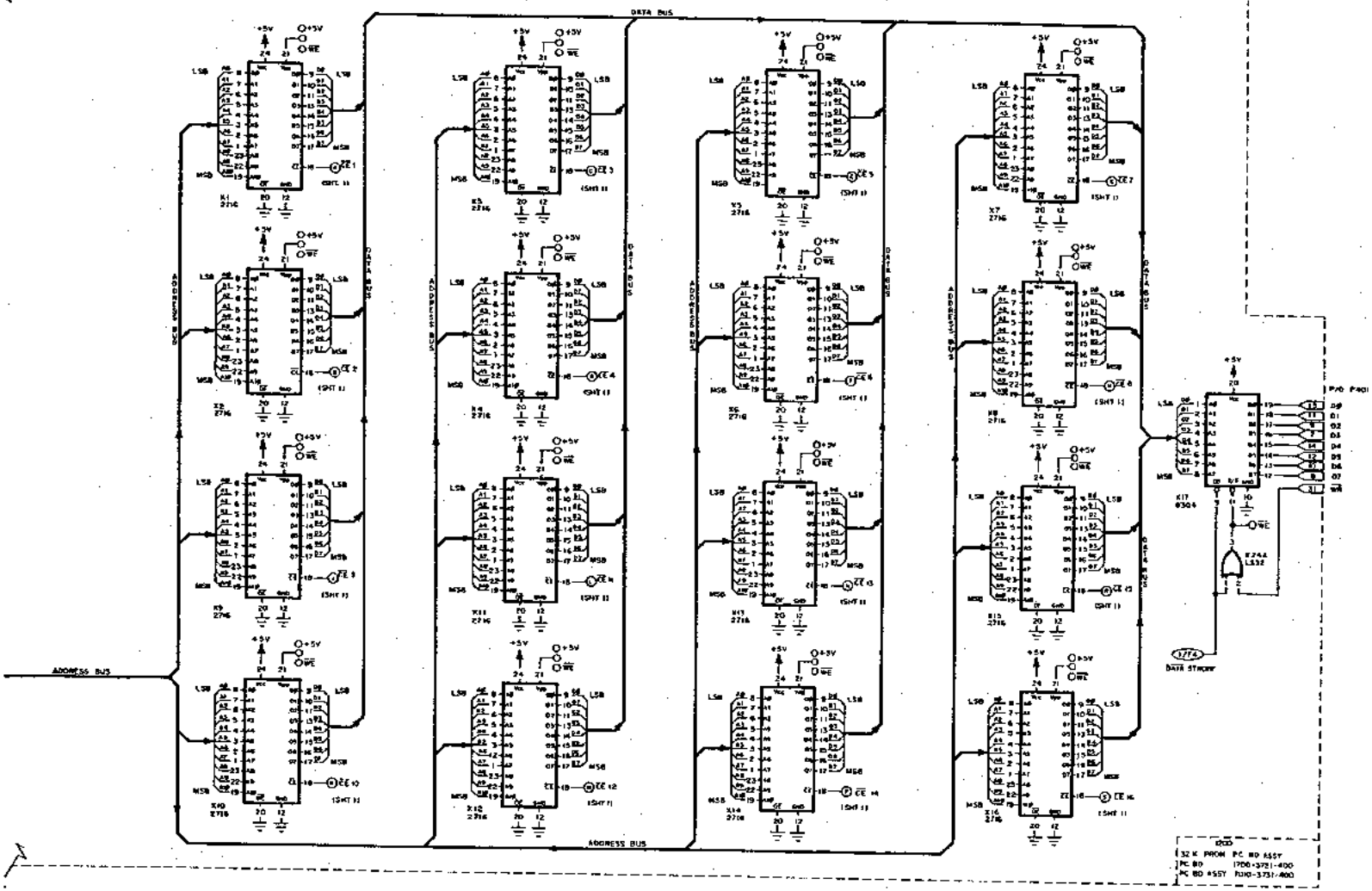
JUMPER LOCATION	ADDRESS	
	X1201-X1208	X1209-X1216
AY-Z	0000-3FFF	N/A
AY-X	N/A	0000-3FFF
BY-Z	4000-7FFF	N/A
BY-X	N/A	4000-7FFF
CY-Z	8000-BFFF	N/A
CY-X	N/A	8000-BFFF
DY-Z	C000-FFFF	N/A

N/A=NOT APPLICABLE



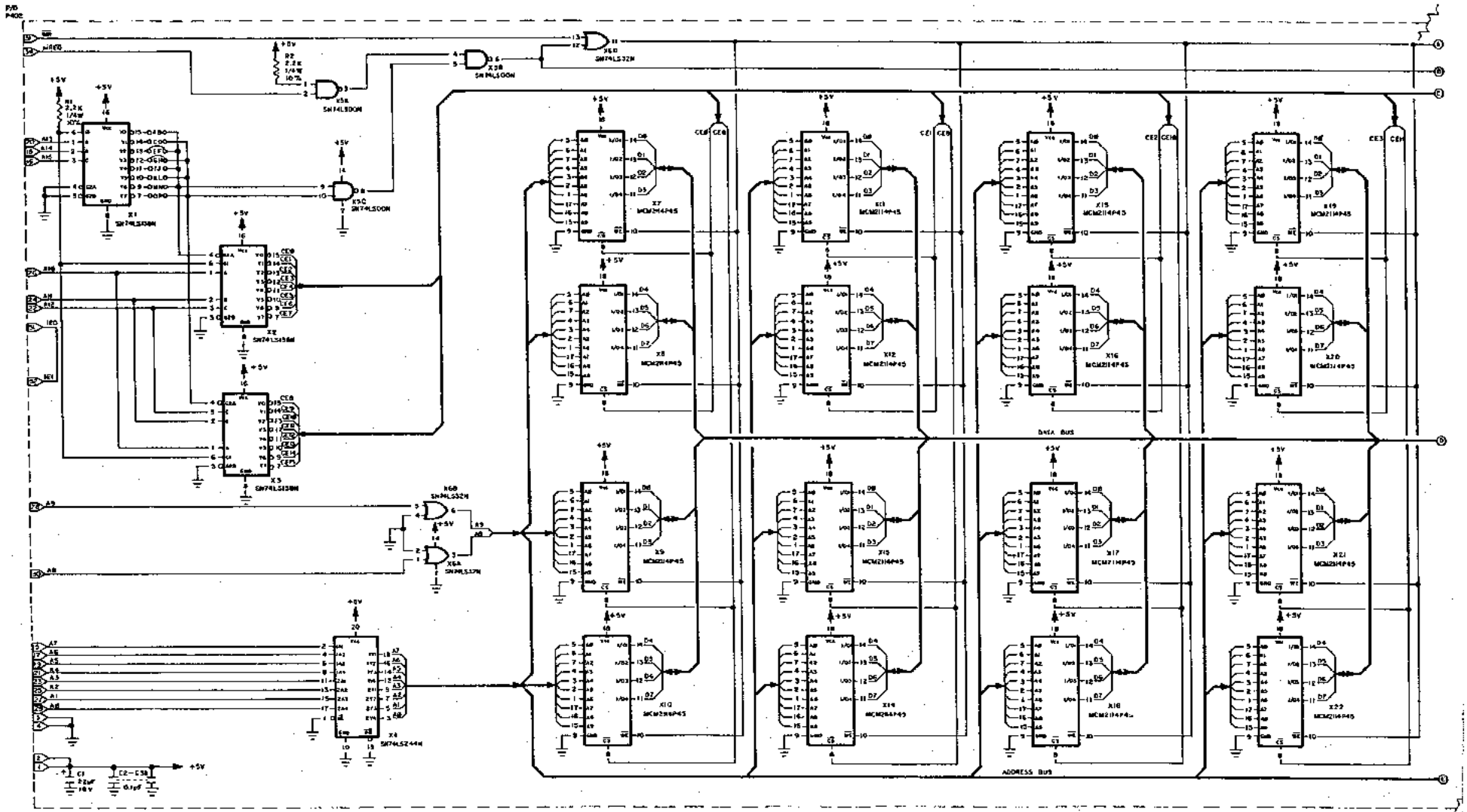
32K PROM Circuit Schematic (Sheet 1 of 2)
Figure 85

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32K PROM Circuit Schematic
(Sheet 2 of 2)
Figure 85

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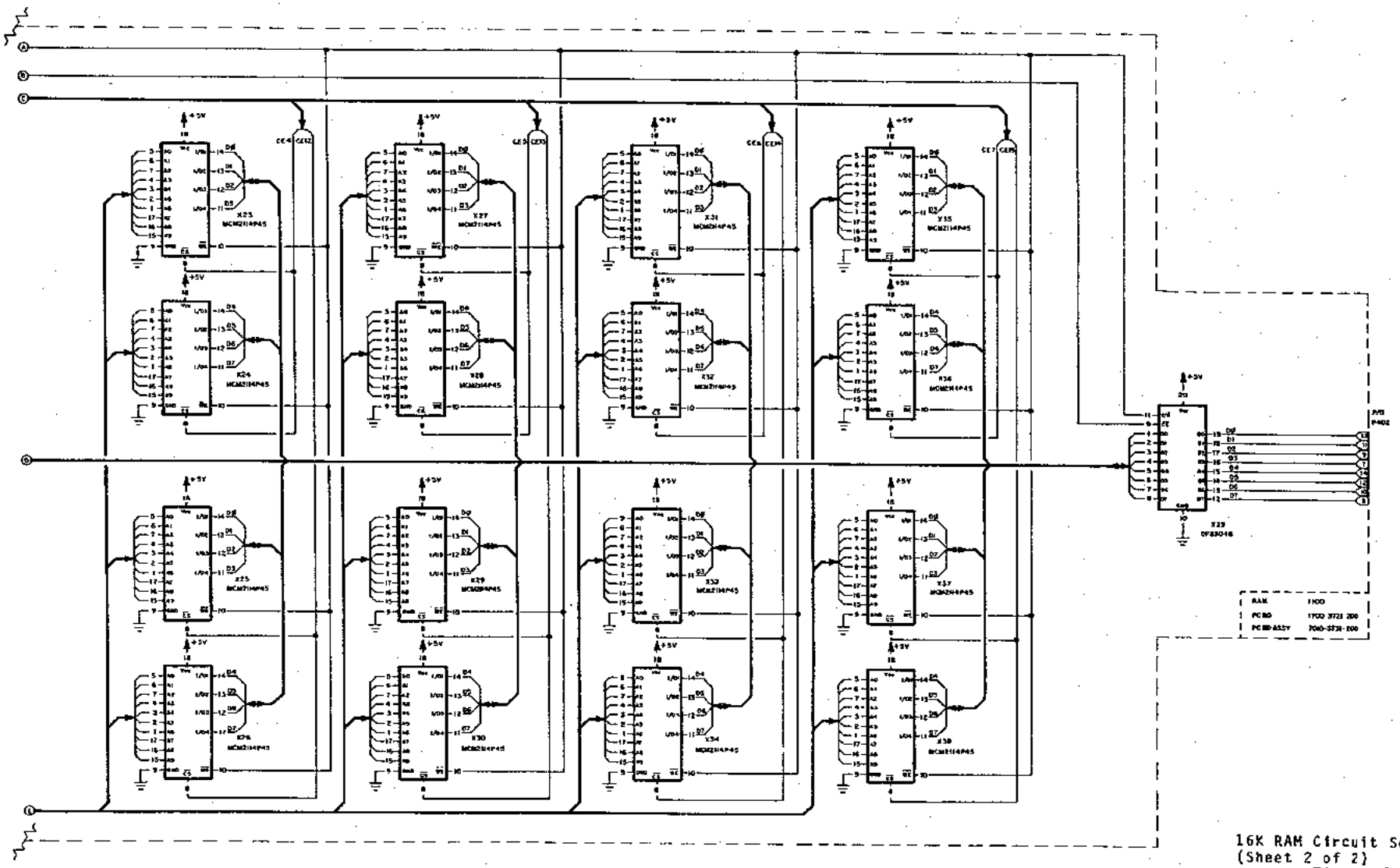


NOTES:

1. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 1100 (I.E. R1 IS R1101).
2. UNUSED IC GATES:
   X5D AND X6C

16K RAM Circuit Schematic (Sheet 1 of 2)
Figure 86

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16K RAM Circuit Schematic
(Sheet 2 of 2)
Figure 86

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NOTES:

1. REFERENCE DESIGNATORS NOT USED:

   R8 AND R9

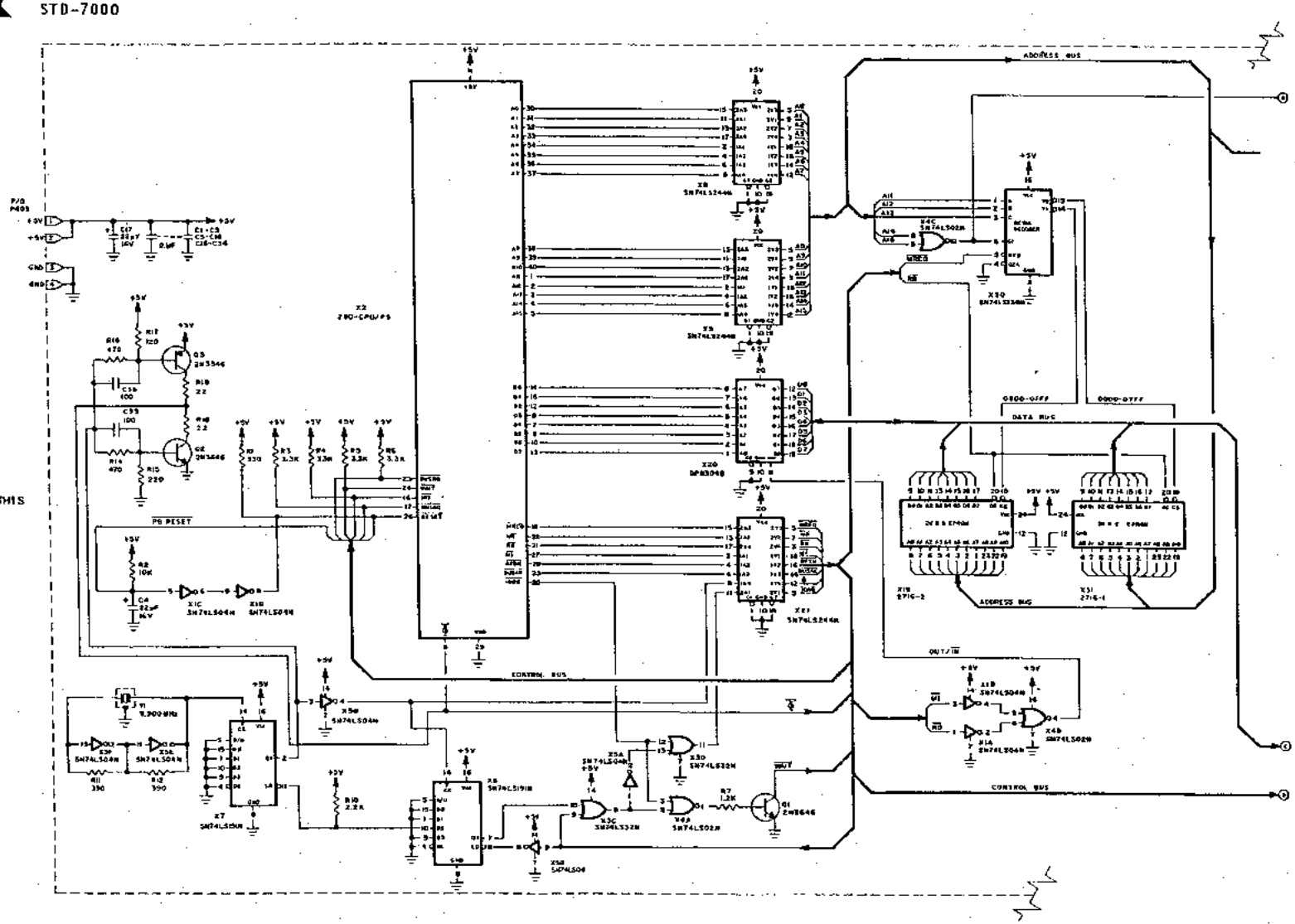
2. ALL RESISTORS ARE 1/4 W, 10%.

3. ALL RESISTANCE IS EXPRESSED IN OHMS.

4. UNUSED IC GATES:

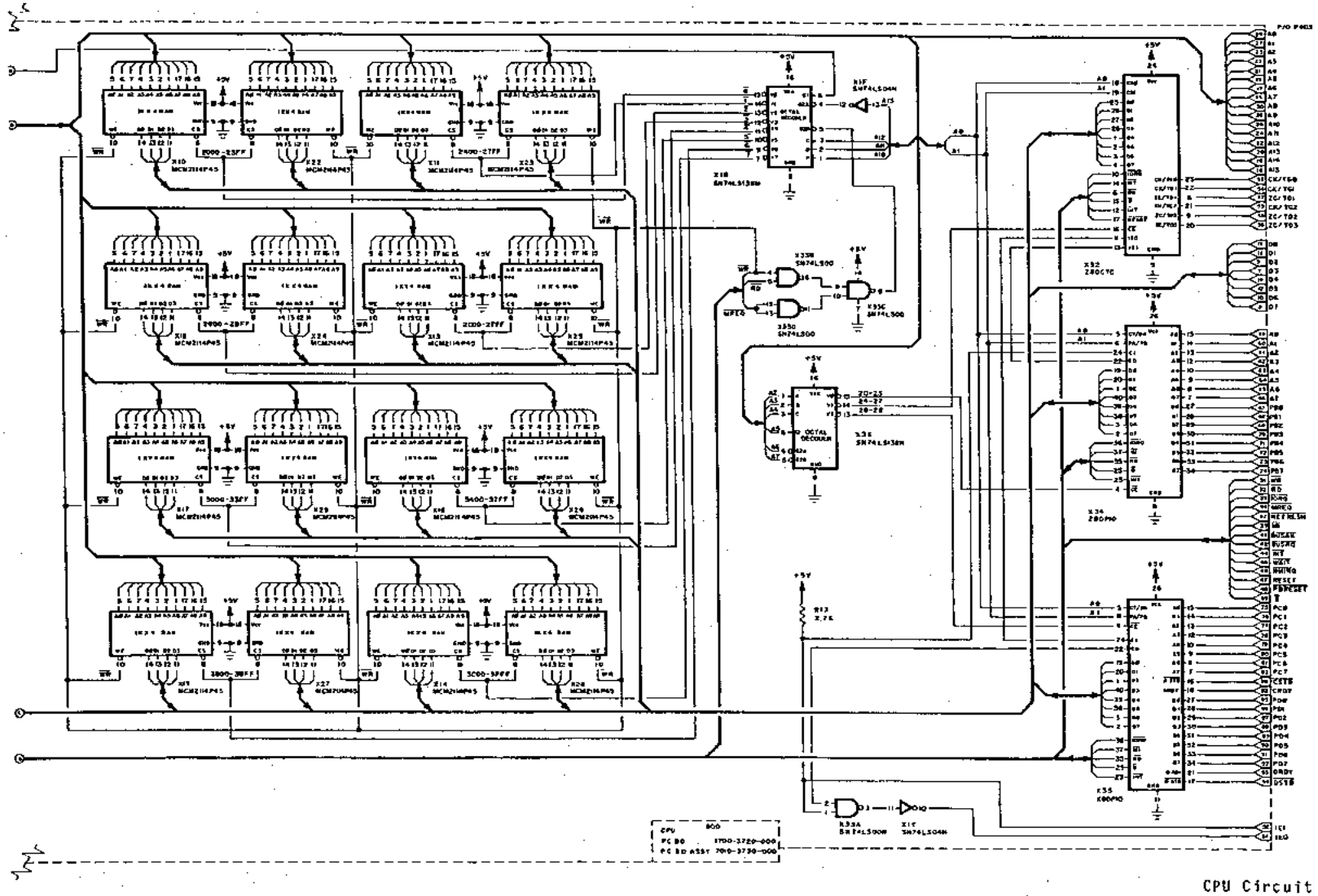
   X3A AND B
   X4D
   X5C

5. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 800 (I.E. R1 IS R801).



CPU Circuit Schematic (Sheet 1 of 2)
Figure 87

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CPU Circuit Schematic (Sheet 2 of 2)
Figure 87

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NOTES:

1. REFERENCE DESIGNATORS NOT USED:

   R2

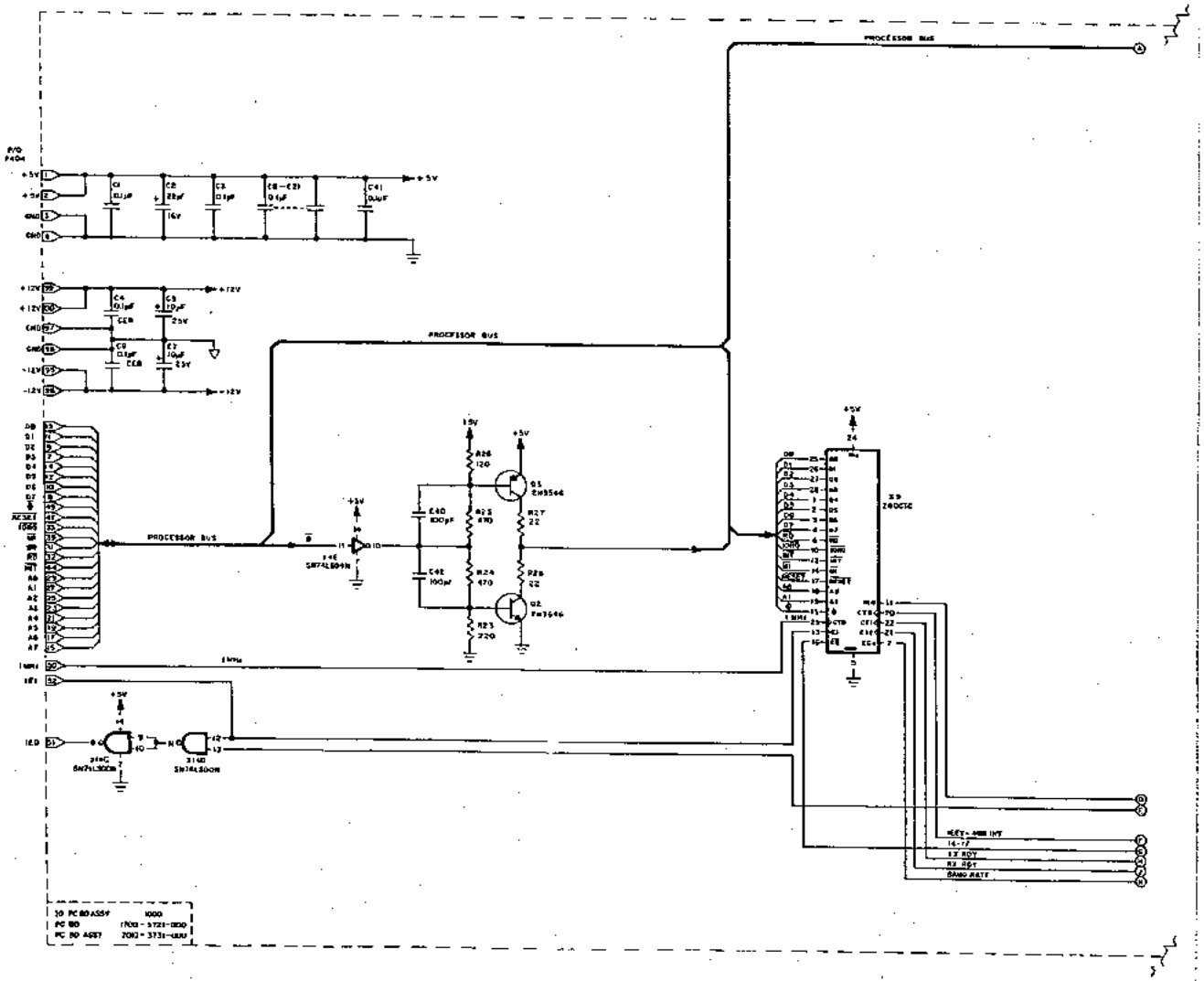
2. ALL RESISTORS ARE 1/4 W, 10%.

3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

4. UNUSED IC GATES:

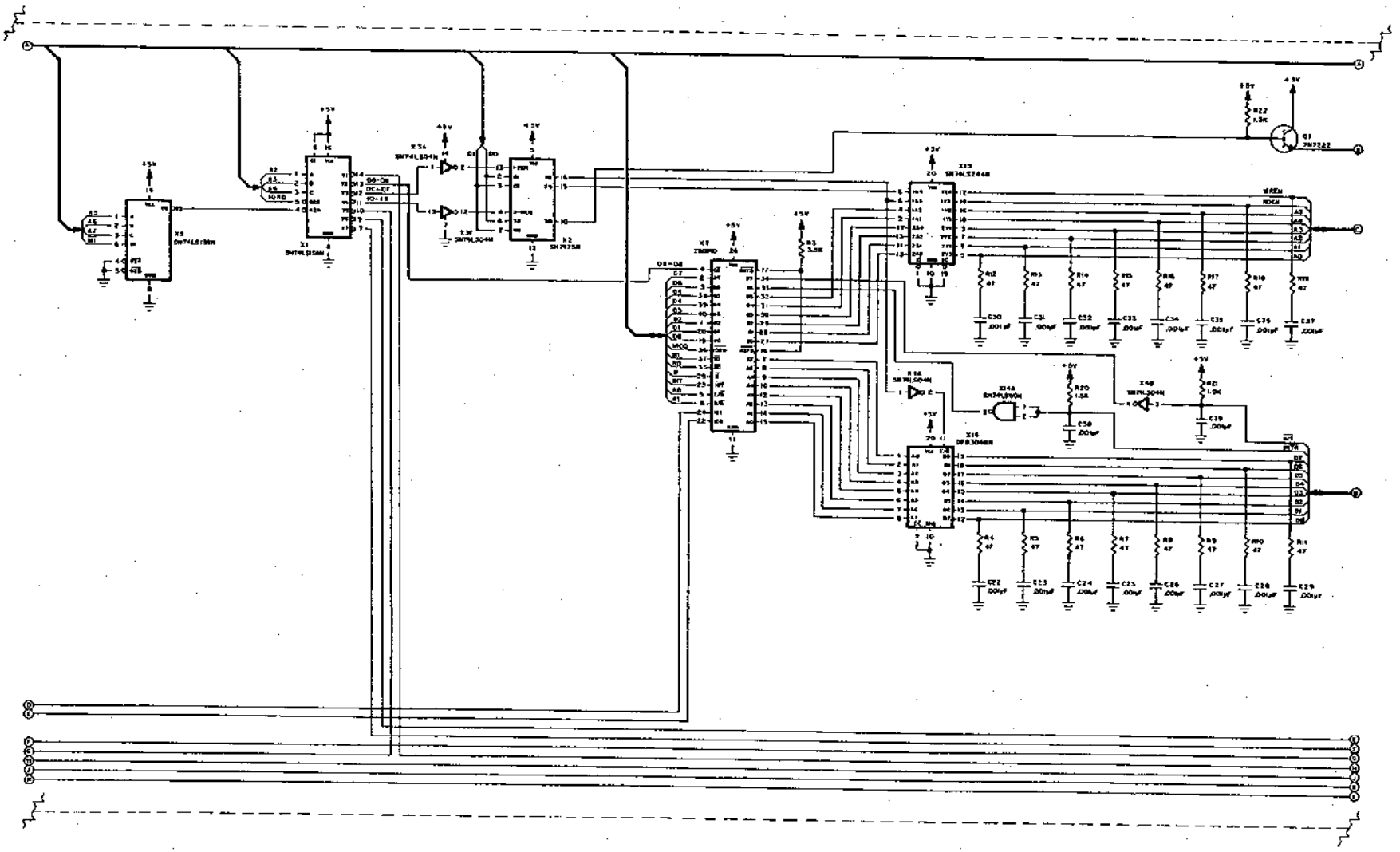
   X38D AND E

5. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 1000 (I.E. R1 IS R1001).



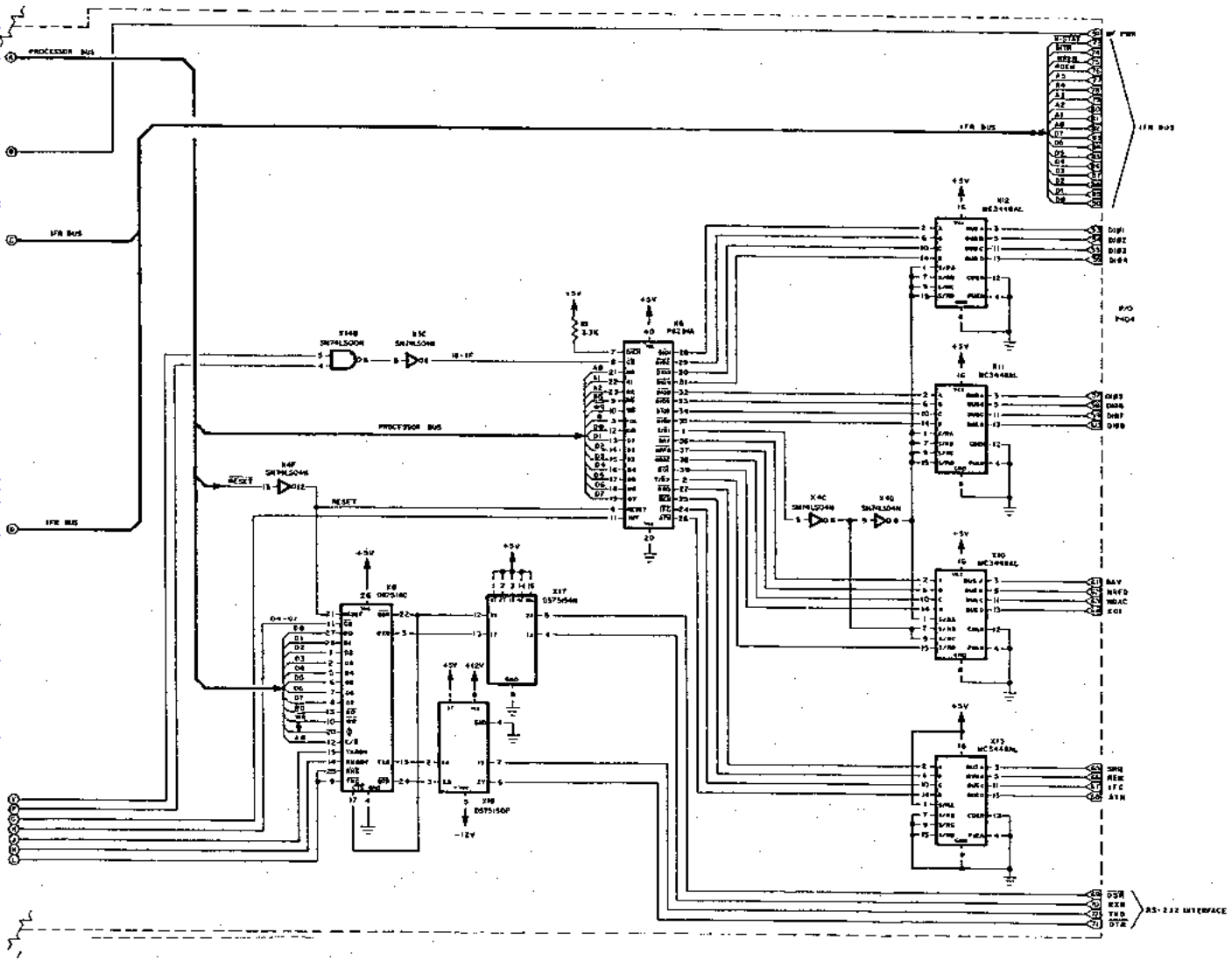
I/O Circuit Schematic (Sheet 1 of 3)
Figure 88

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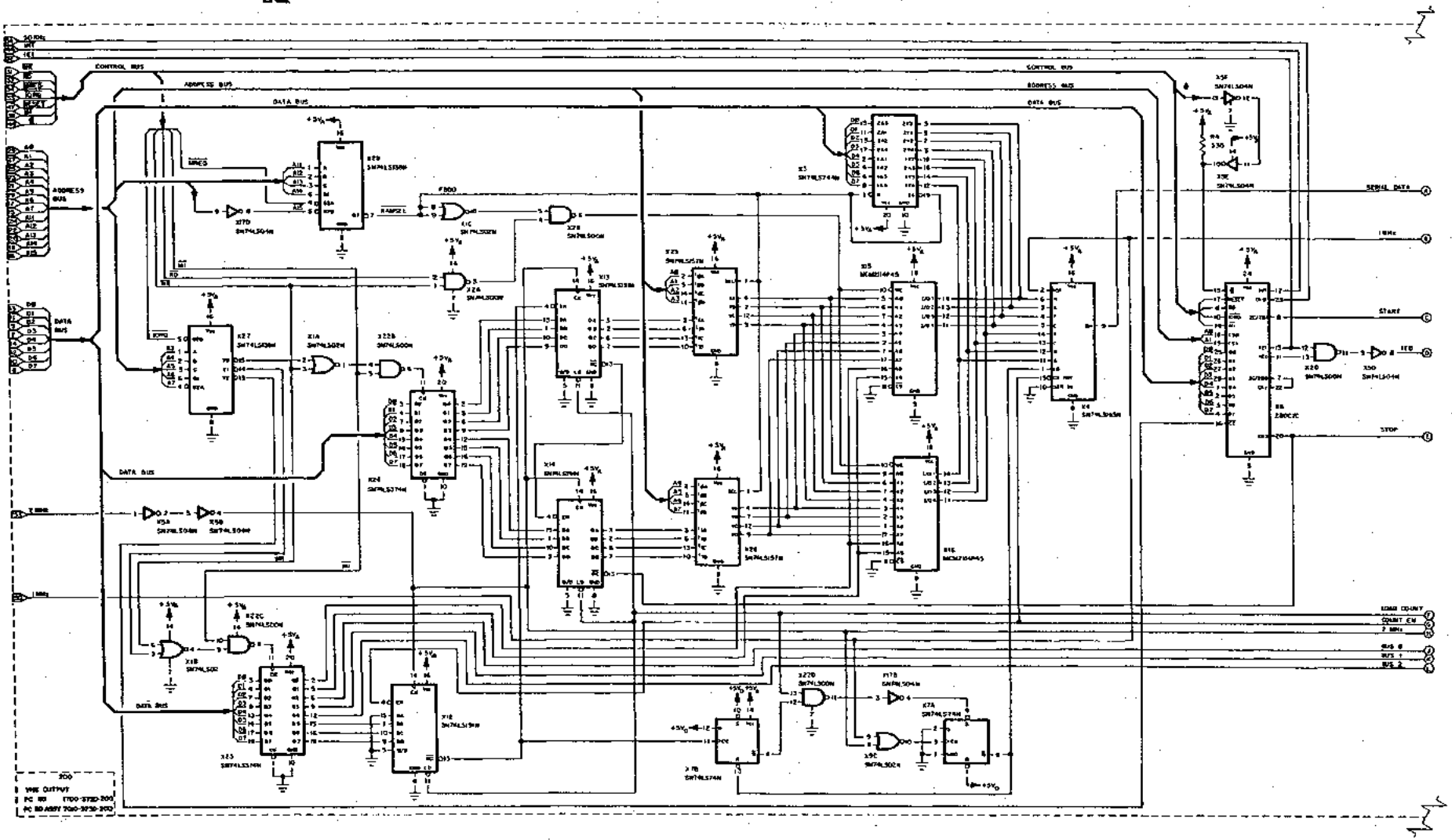
I/O Circuit Schematic (Sheet 2 of 3
Figure 88

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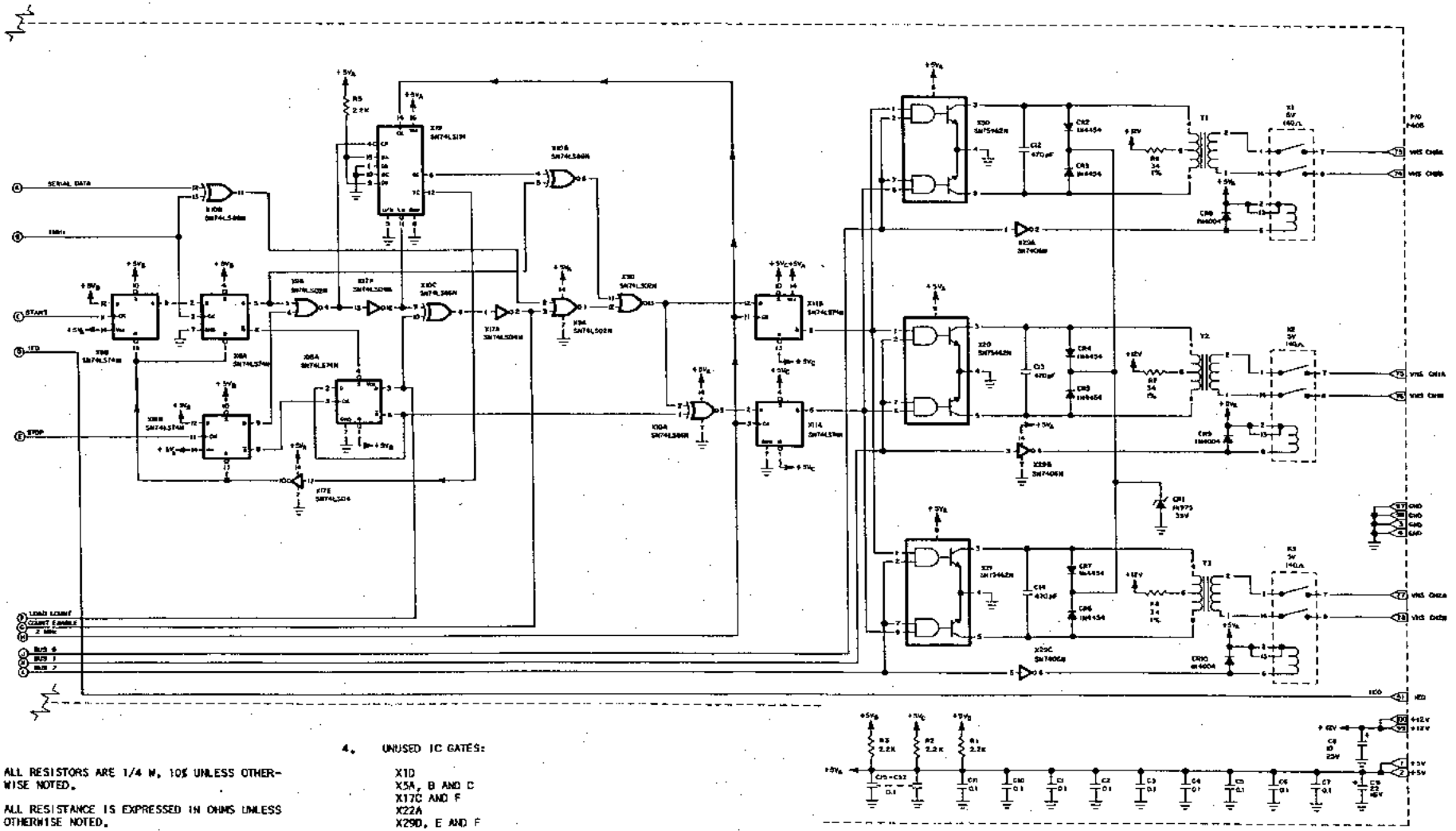
I/O Circuit Schematic (Sheet 3 of 3)
Figure 88

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VHS Output Circuit Schematic
(Sheet 1 of 2)
Figure 89

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NOTES:

1. ALL RESISTORS ARE 1/4 W, 10% UNLESS OTHERWISE NOTED.
2. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
3. ALL CAPACITANCE IS EXPRESSED IN MF UNLESS OTHERWISE NOTED.
4. UNUSED IC GATES:

   X1D
   X5A, B AND C
   X17C AND F
   X22A
   X29D, E AND F

5. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 700 (I.E. R1 IS R701).

VHS Output Circuit Schematic (Sheet 2 of 2)
Figure 89

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NOTES:

1. REFERENCE DESIGNATORS NOT USED:

   C40 R1
   C41 R3
   C48
   C49

2. ALL RESISTORS ARE 1/4 W, 10% UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

4. ALL CAPACITANCE IS EXPRESSED IN MF UNLESS OTHERWISE NOTED.

5. SOLID STATE SWITCH X33 IS SHOWN WITH ALL INPUTS AT LOGIC "0".

6. UNUSED IC GATES:

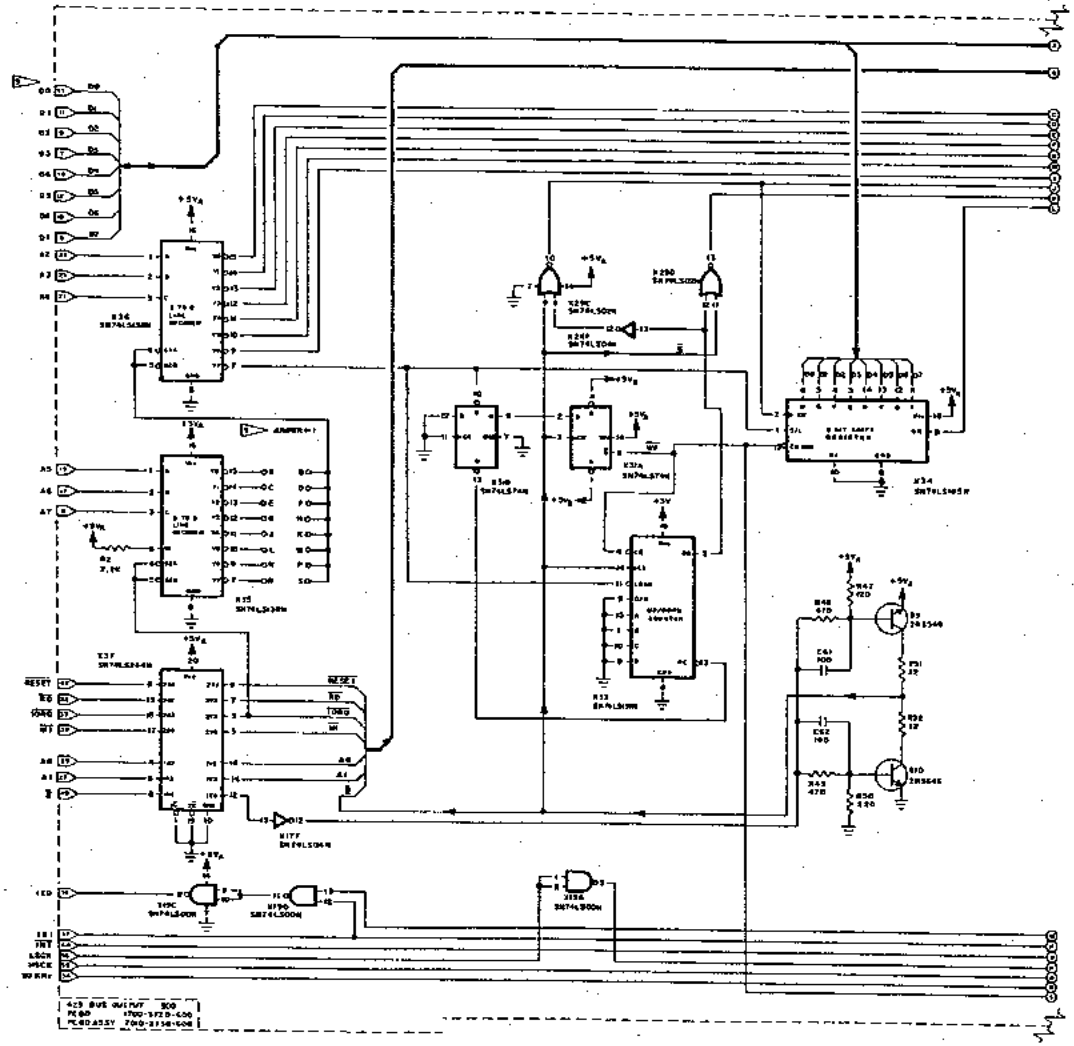
   X17F
   X19B
   X26B AND C

7. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 900 (I.E. R1 IS R901).

8. ⏚ DENOTES ANALOG GROUND.

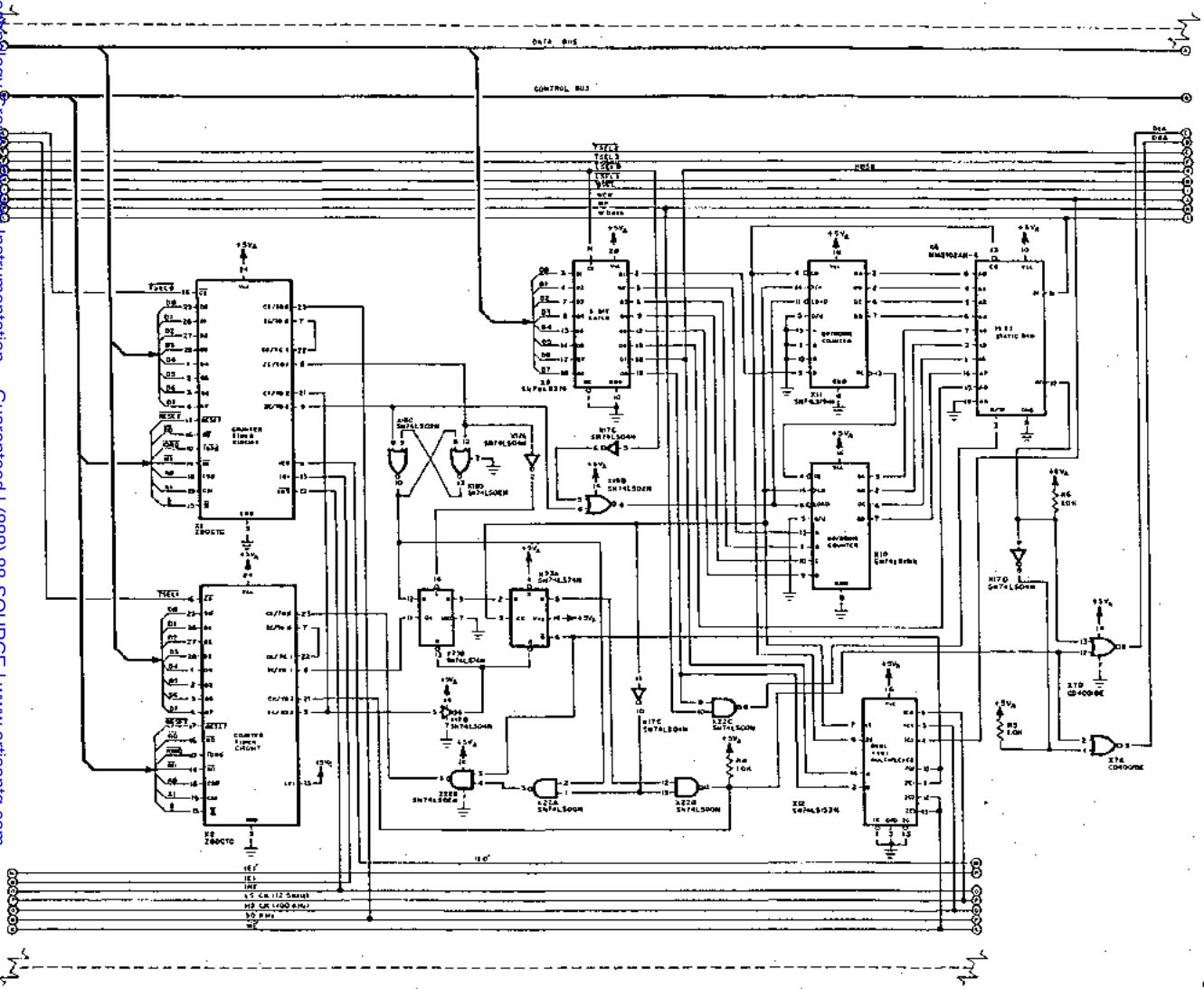
9.

DASH NO.	BOARD	CARD EDGE REF. DES.	JUMPER #1	JUMPER #2	JUMPER #3	JUMPER #4	JUMPER #5
00	A	P406	J TO K	8A	8B	1A	1B
01	B	P407	L TO M	2A	2B	3A	3B
02	C	P408	N TO P	4A	4B	5A	5B



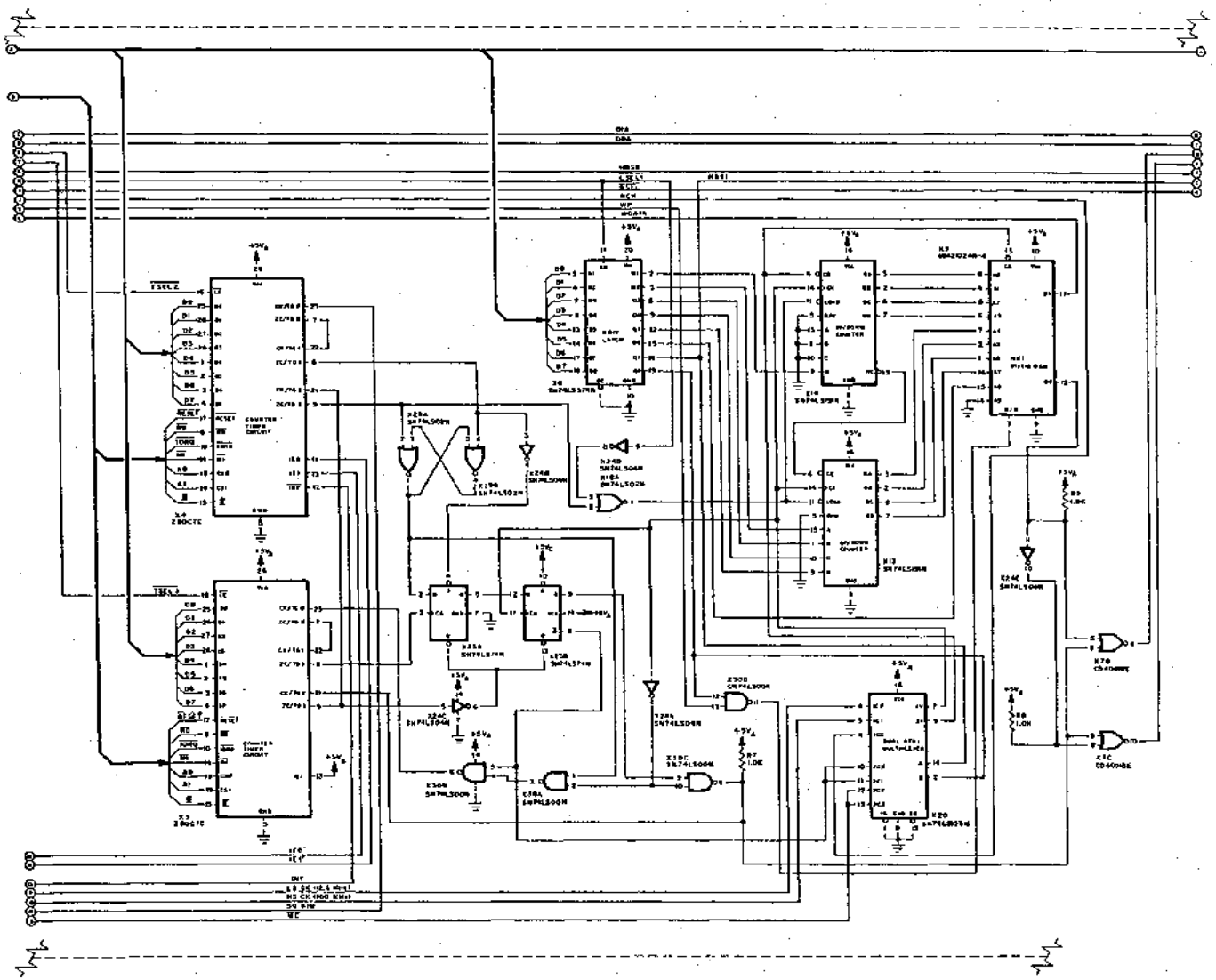
429 Bus Output Circuit Schematic
(Sheet 1 of 5)
Figure 90

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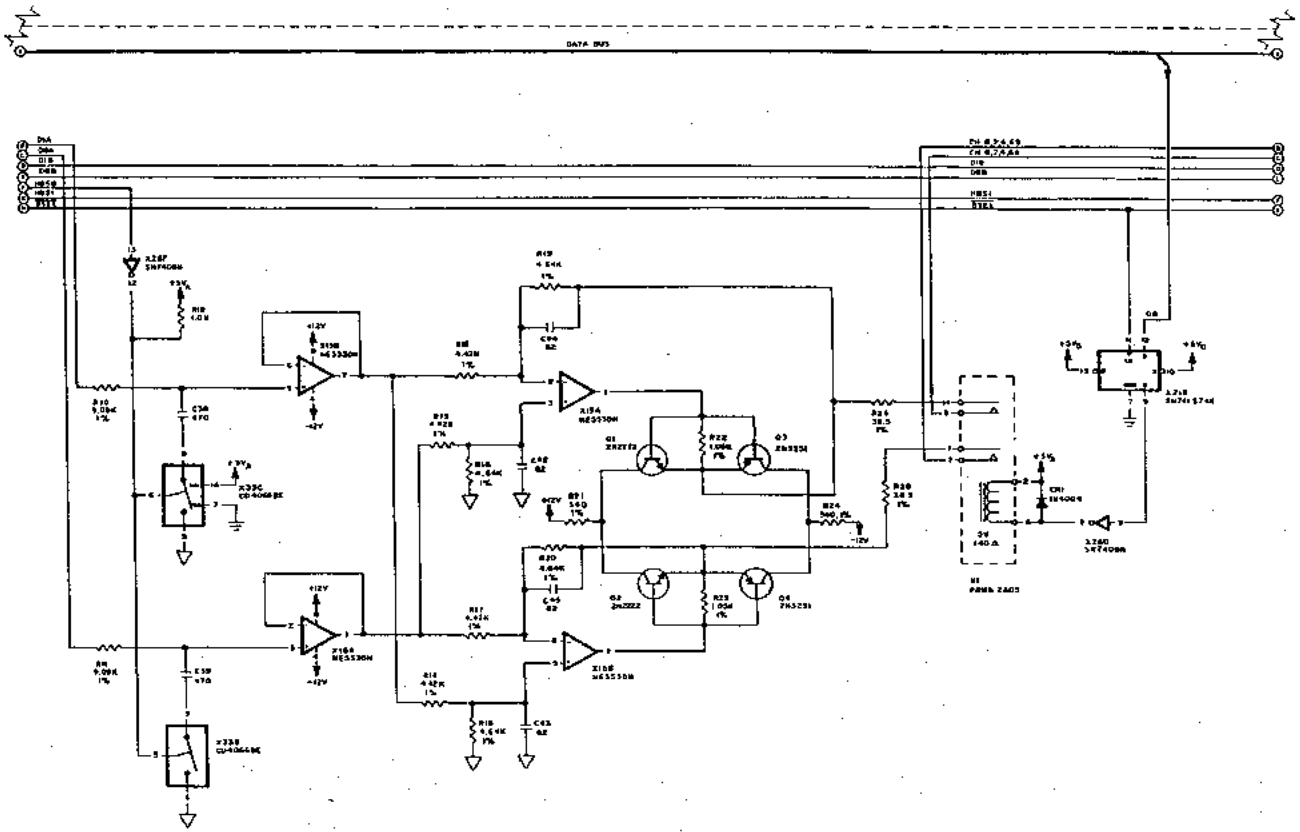
429 Bus Output Circuit Schematic (Sheet 2 of 5)
Figure 90

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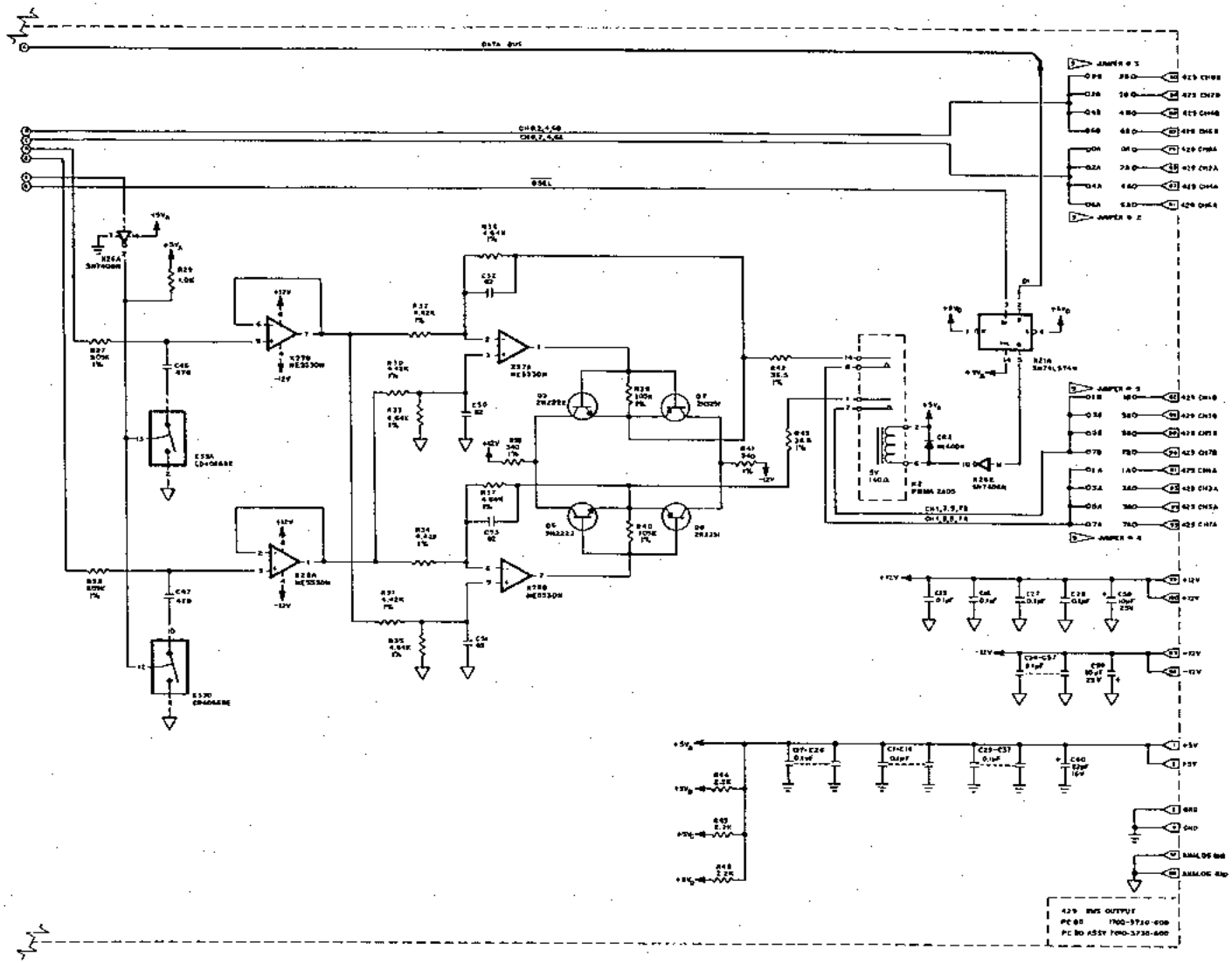
429 Bus Output Circuit Schematic
(Sheet 3 of 5)
Figure 90

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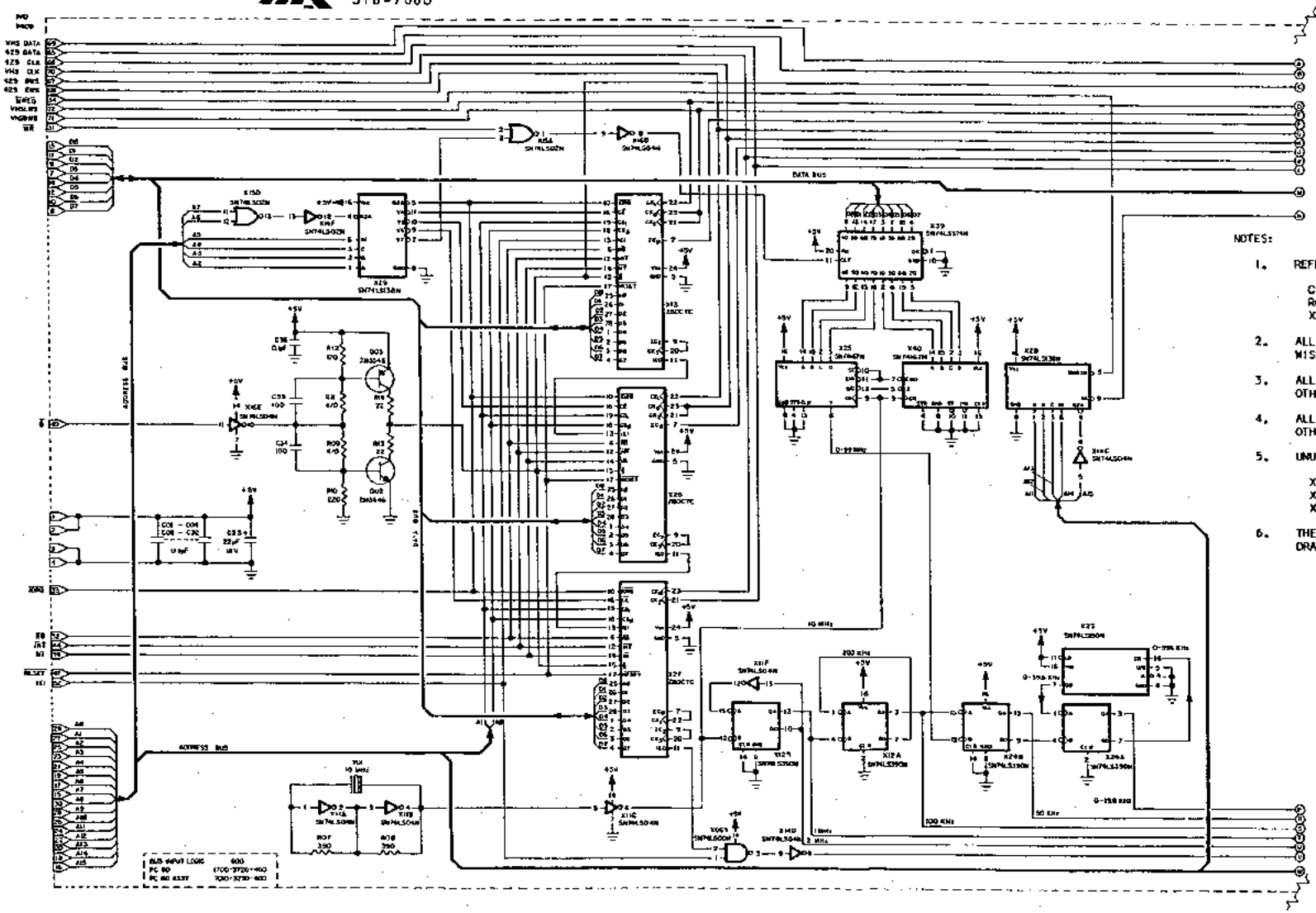
429 Bus Output Circuit Schematic (Sheet 4 of 5)
Figure 90

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429 Bus Output Circuit Schematic
(Sheet 5 of 5)
Figure 90

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NOTES:

1. REFERENCE DESIGNATORS NOT USED:

   C7
   R6
   X22

2. ALL RESISTORS ARE 1/4 W, 10% UNLESS OTHERWISE NOTED.

3. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.

4. ALL CAPACITANCE IS EXPRESSED IN pF UNLESS OTHERWISE NOTED.

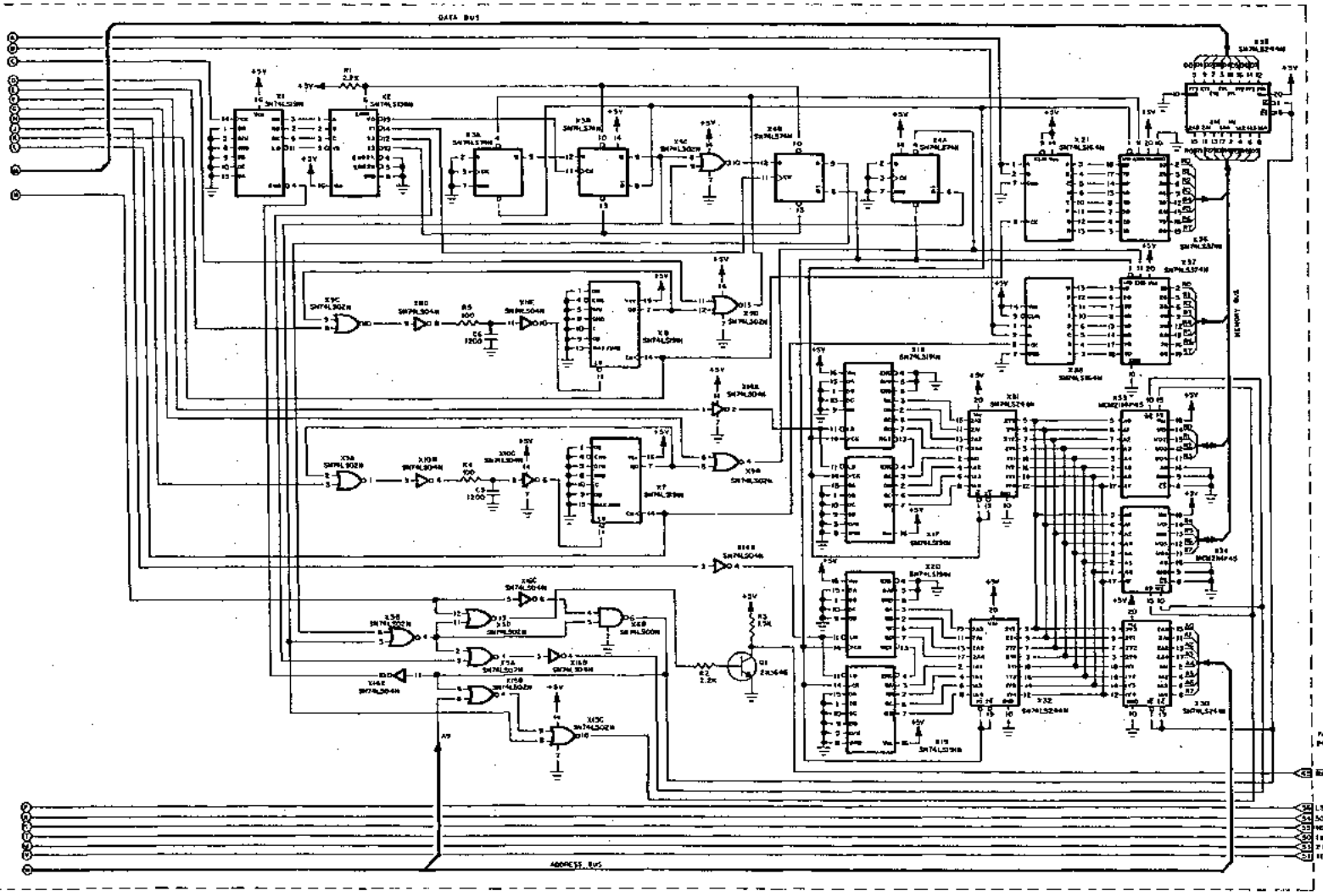
5. UNUSED IC GATES:

   X6C AND D
   X10A, D, E AND F
   X16A AND F

6. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 600 (I.E. R1 IS R601).

Bus Input Logic Circuit Schematic (Sheet 1 of 2)
Figure 91

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Bus Input Logic Circuit Schematic
(Sheet 2 of 2)
Figure 91

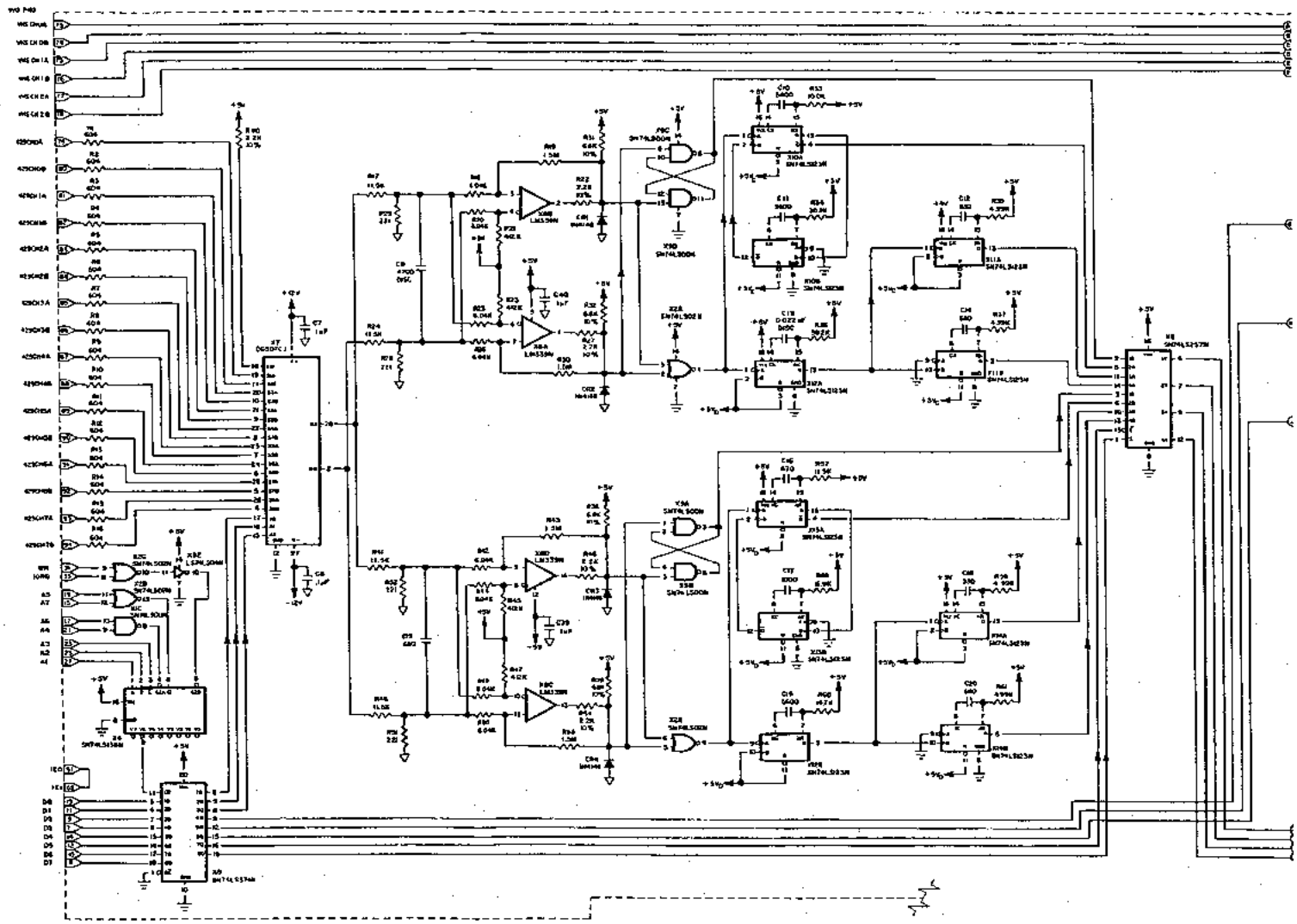
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NOTES:

1. ALL RESISTORS ARE 1/4 W, 10% UNLESS OTHERWISE NOTED.
2. ALL RESISTANCE IS EXPRESSED IN OHMS.
3. ALL CAPACITANCE IS EXPRESSED IN pF.
4. ⏚ DENOTES ANALOG GROUND.
5. UNUSED IC GATES:

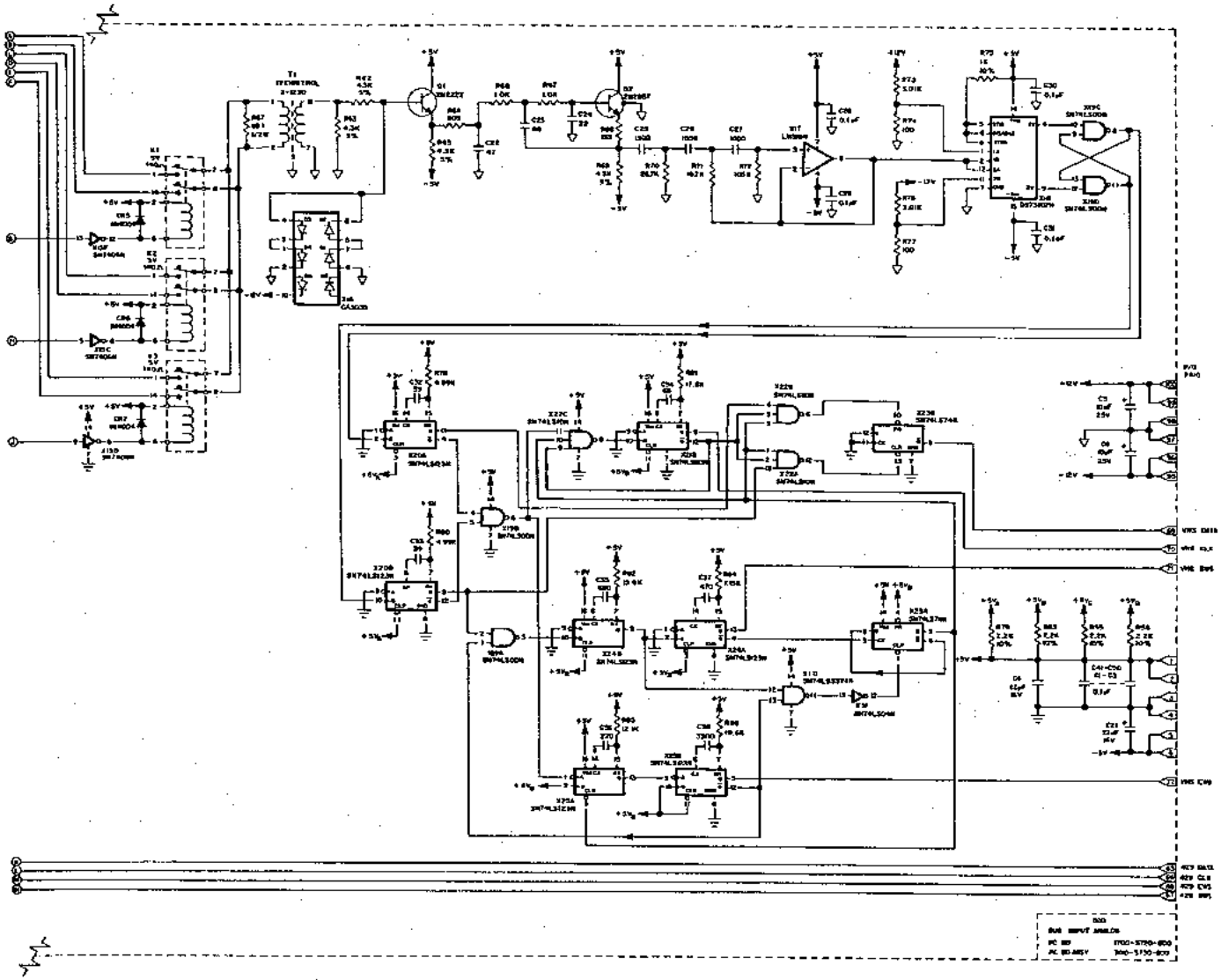
   X1A AND B
   X3A, B, C AND D
   X15A, B AND E
   X21A

6. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 500 (I.E. R1 IS R501).



Bus Input Analog Circuit Schematic (Sheet 1 of 2
Figure 92

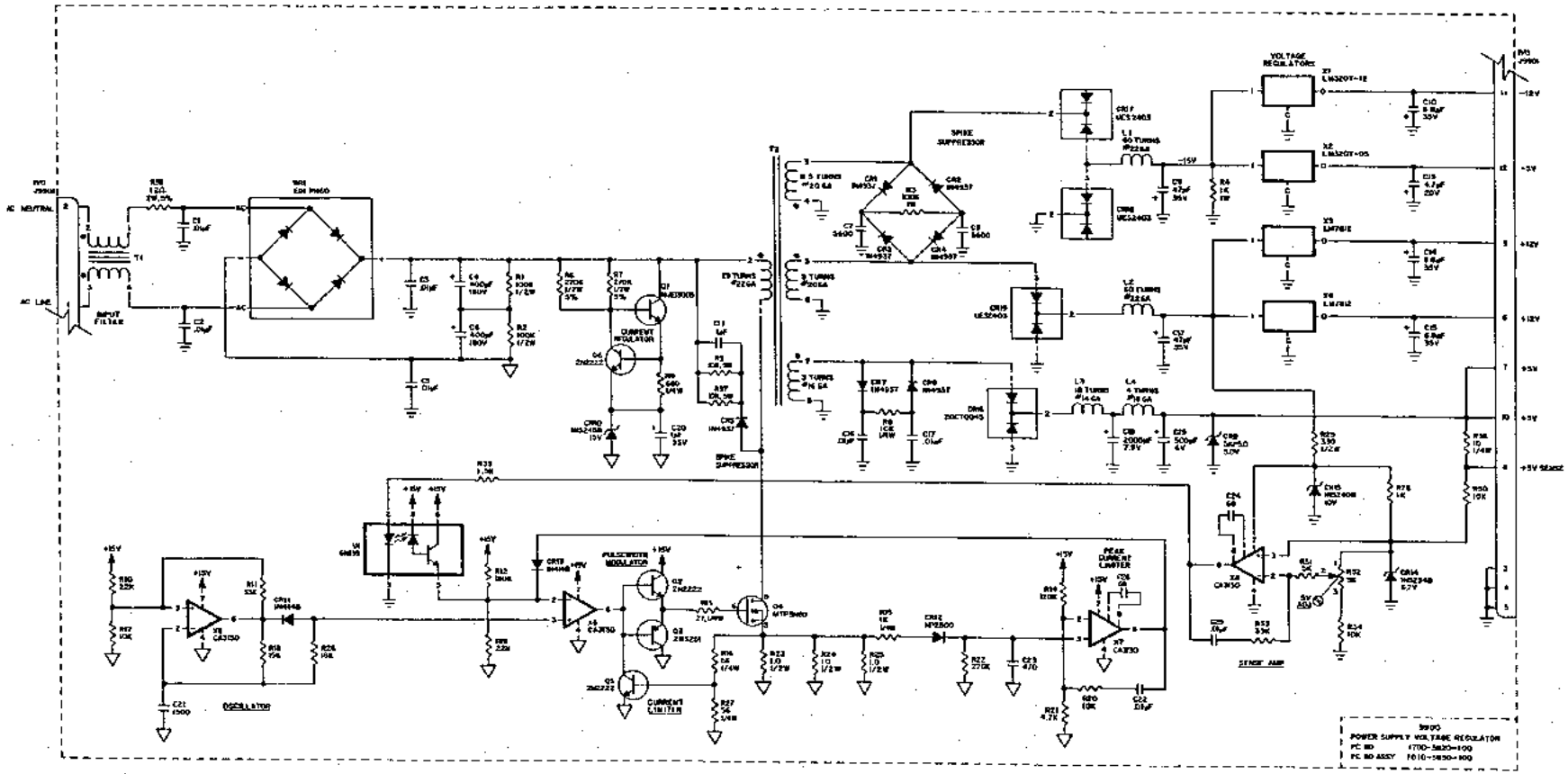
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Bus Input Analog Circuit Schematic
(Sheet 2 of 2)

Figure 92

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NOTES:

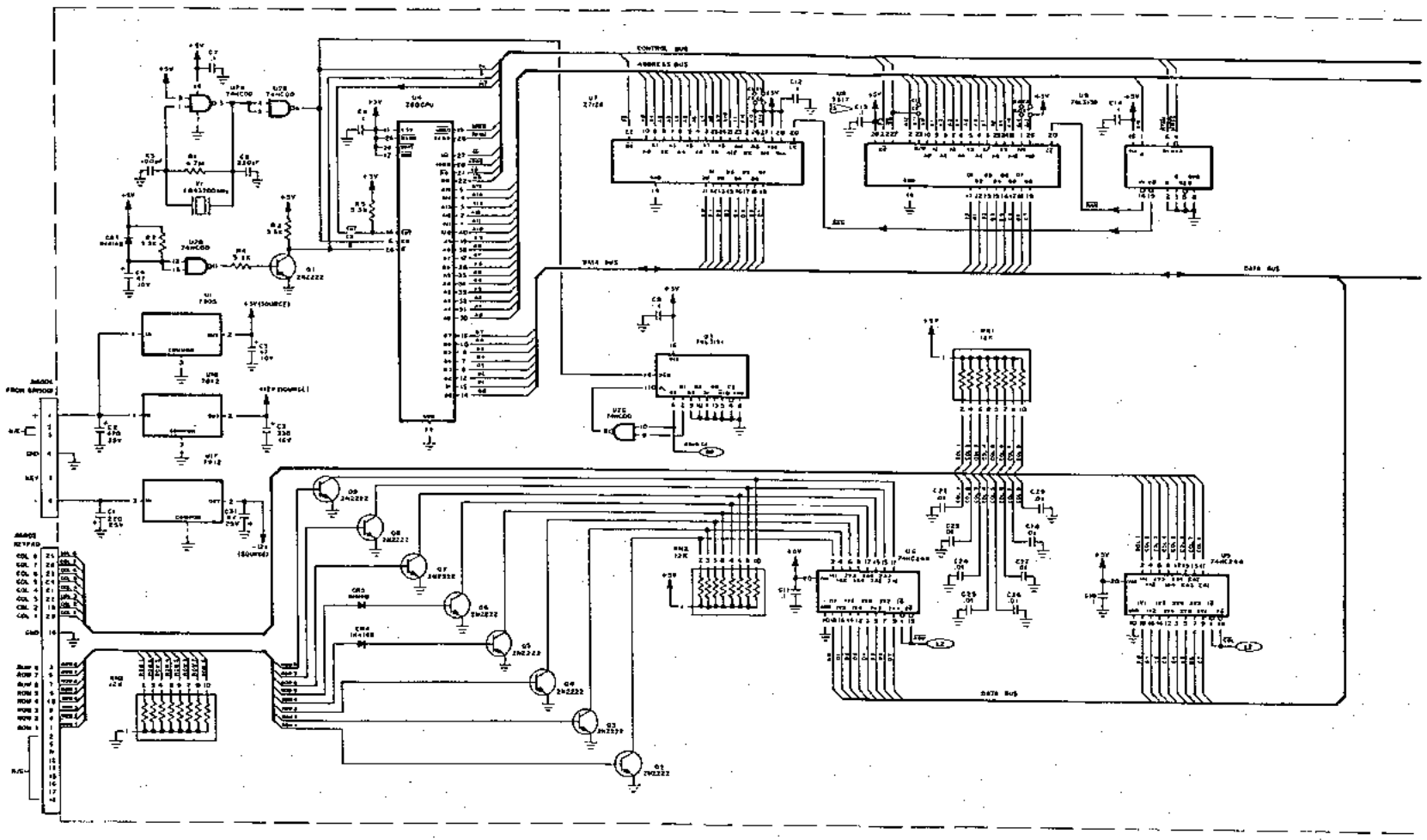
1. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
2. ALL CAPACITANCE IS EXPRESSED IN pF UNLESS OTHERWISE NOTED.
3. ALL RESISTORS ARE 1/8 W, 10% UNLESS OTHERWISE NOTED.
4. THE REFERENCE DESIGNATOR SERIES FOR THIS DRAWING IS 9900 (I.E. R1 IS R9901).
5. ⏚ DENOTES FLOATING GROUND.

Universal Power Supply Circuit Schematic
Figure 93

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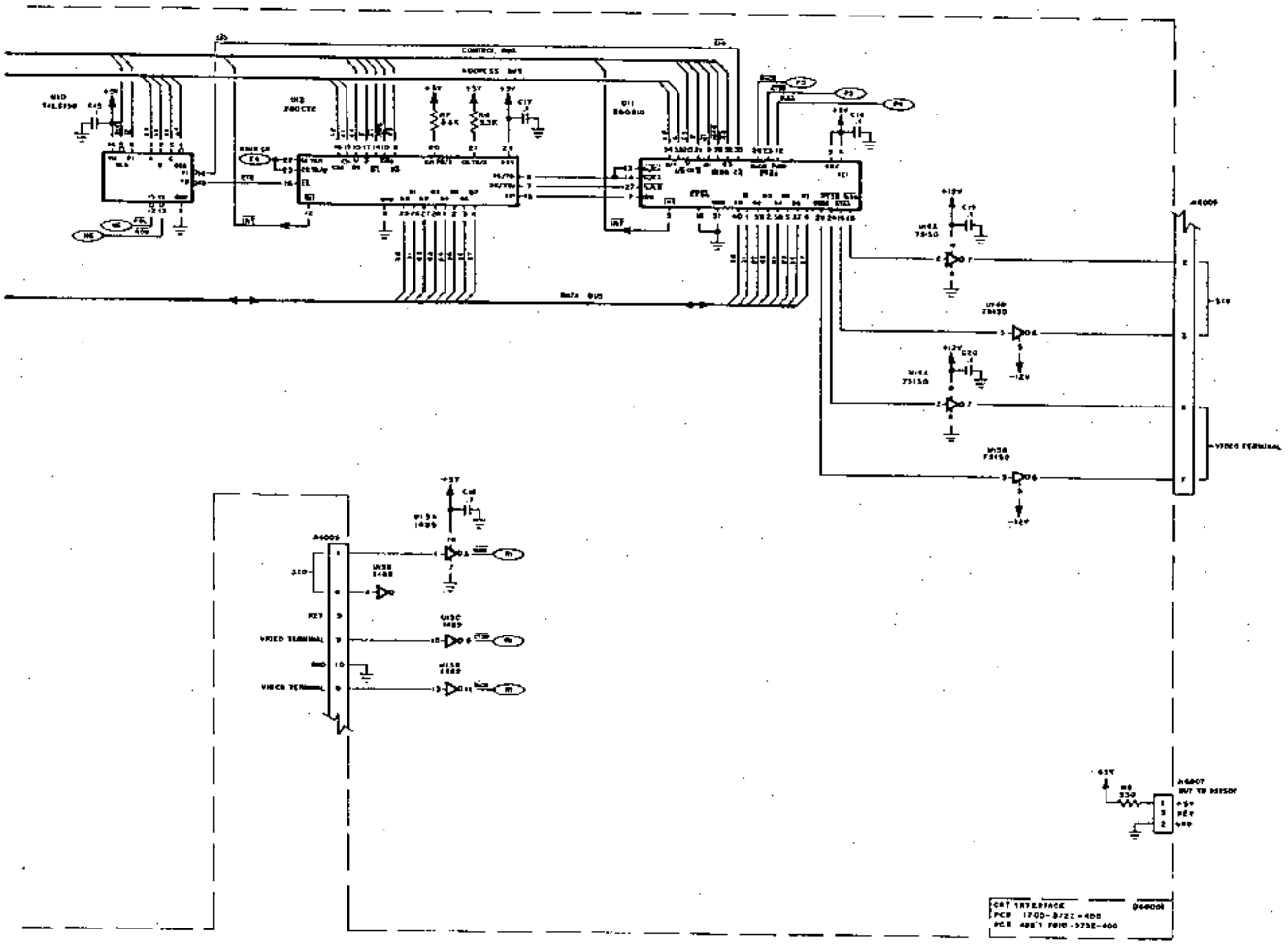
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CRT Interface Circuit Schematic (Sheet 1 of 2
Figure 94

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NOTES:

1. ALL REFERENCE NUMBERS CARRY AN ASSIGNED DESIGNATOR SERIES. THIS SCHEMATIC CARRIES SERIES 15000 (E.G., R) IS R15001).
2. ALL RESISTORS ARE 1/4 W, 10% TOLERANCE UNLESS OTHERWISE NOTED.
3. U8 IS A 24-PIN I.C. INSTALLED IN A 28-PIN SOCKET. THE PIN NUMBERS INDICATED ARE RELATIVE TO THE SOCKET AND NOT THE I.C. THEREFORE, PIN 3 IS PIN 1 OF THE I.C.
4. ALL RESISTANCE IS EXPRESSED IN OHMS UNLESS OTHERWISE NOTED.
5. ALL CAPACITANCE IS EXPRESSED IN MICRO-FARADS UNLESS OTHERWISE NOTED.
6. ALL INDUCTANCE IS EXPRESSED IN MICRO-HENRYS UNLESS OTHERWISE NOTED.

CRT Interface Circuit Schematic
(Sheet 2 of 2)
Figure 94

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8. PC Board Assemblies

A. General

This section contains component layout drawings for all PC boards contained within the STD-7000. These drawings are provided for purposes of locating and identifying discrete components, connectors, test points, etc., which are referenced in other sections of this manual. These drawings are sequenced in the same order they are discussed in 2-2-1.

NOTE: Each figure title for each PC board is followed by a number enclosed within parentheses. This number represents the referenced designator series number assigned to the PC board shown in that figure (e.g., if a PC board carries a designator series number 1200, the component R1 is R1201, X5 is X1205, CR36 is CR1236, etc.).

NOTE: If a PC board has components located on both sides of the board, both a top and bottom view of the PC board will be provided in the Figure. If, however, a PC board has components only on one side, then only the component side will be shown.

NOTE: The drawings in this section are not intended for use in ordering spare or replacement parts. For parts ordering information, see STD-7000 Illustrated Parts Catalog.

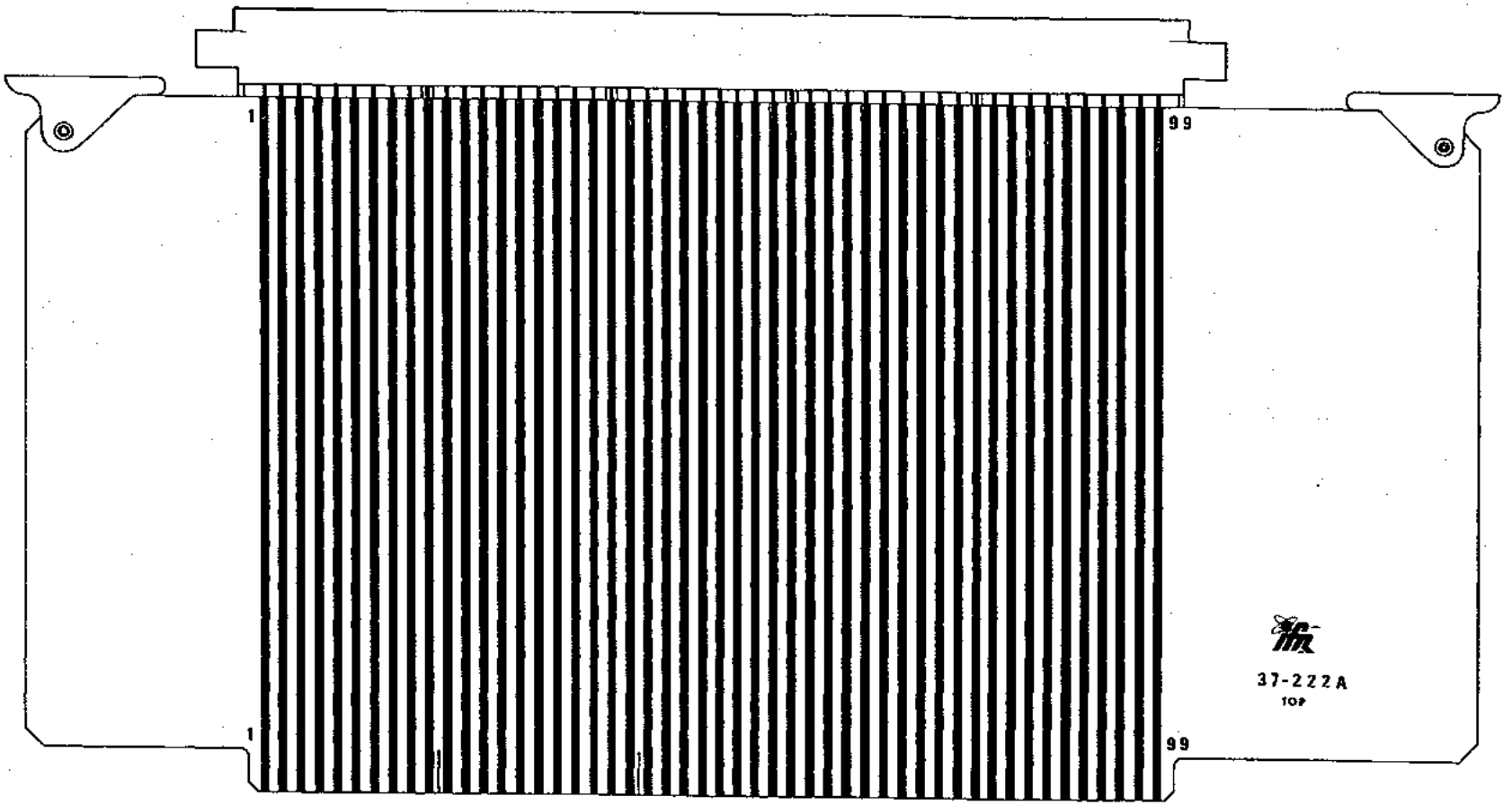
B. PC Board Assemblies

Figure	Title	Page
95	Extender PC Board PC Board	3
96	Motherboard	4
97	Rear Panel PC Board	5
98	32K PROM PC Board (Orange)	6
99	16K RAM PC Board (Orange)	7
100	CPU PC Board (Yellow)	8
101	I/O PC Board (Blue)	9
102	VHS Output PC Board (Violet)	10
103	429 Bus Output PC Board (Brown)	11
104	Bus Input Logic PC Board (Red)	12
105	Bus Input Analog PC Board (Green)	13
106	Universal Power Supply, Voltage Regulator PC Board	14
107	CRT Interface PC Board	16

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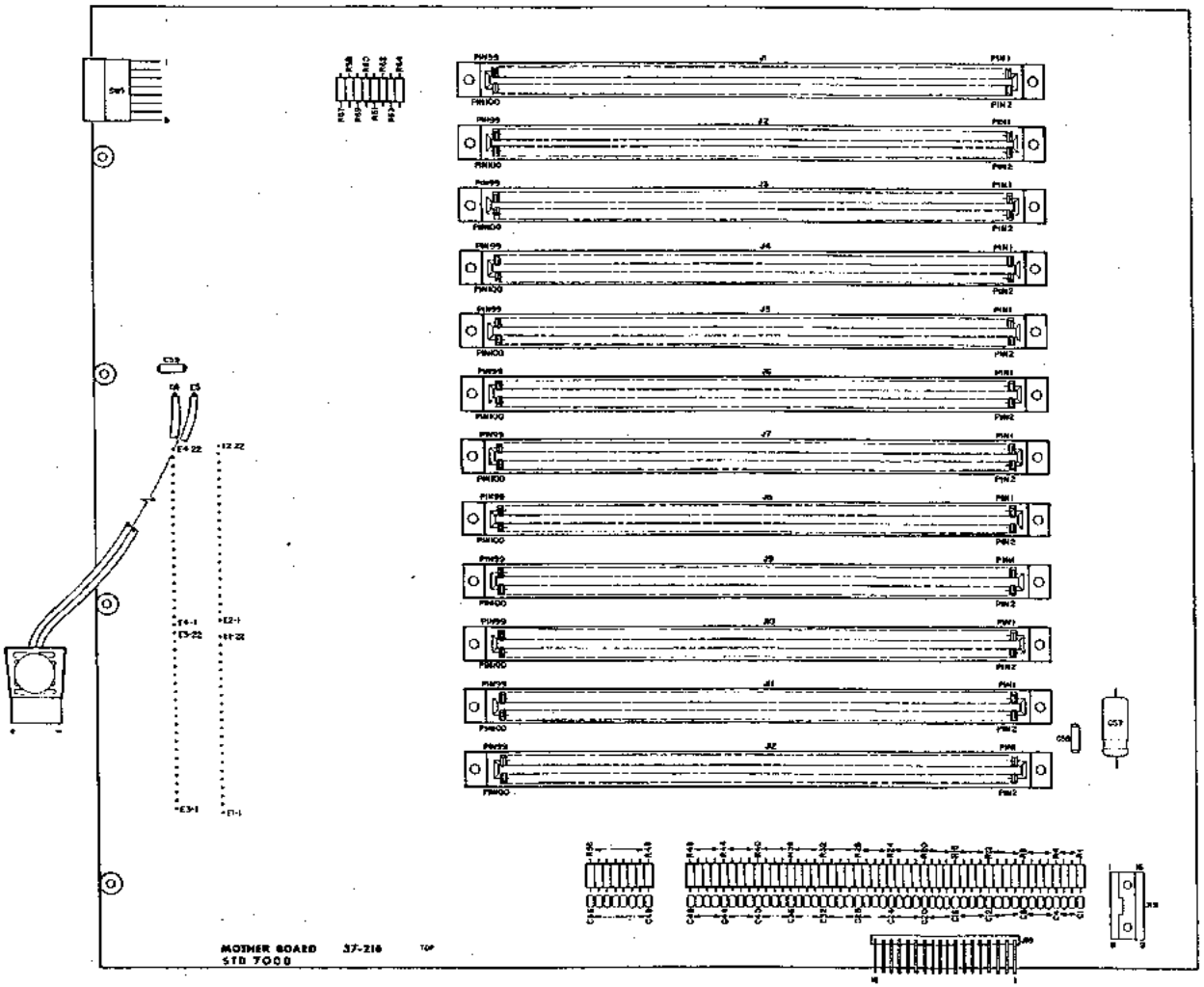
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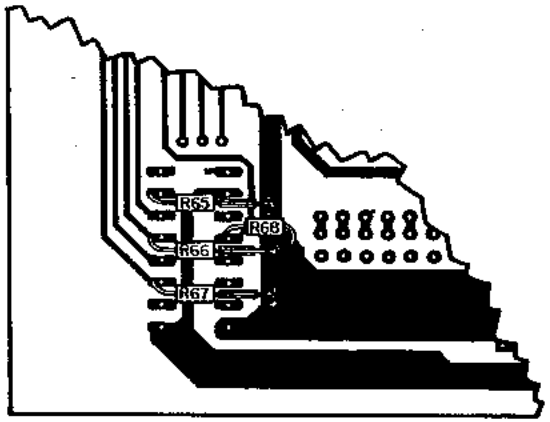
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Extender PC Board
Figure 95

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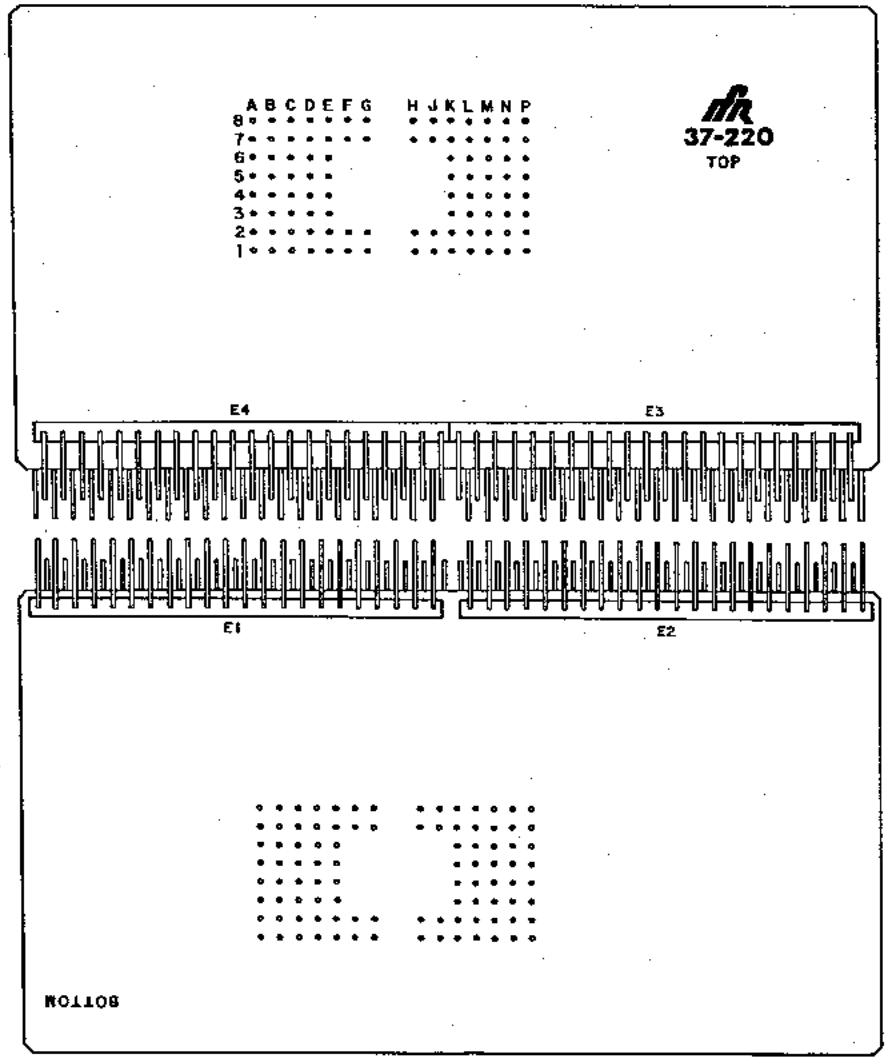




BOTTOM VIEW

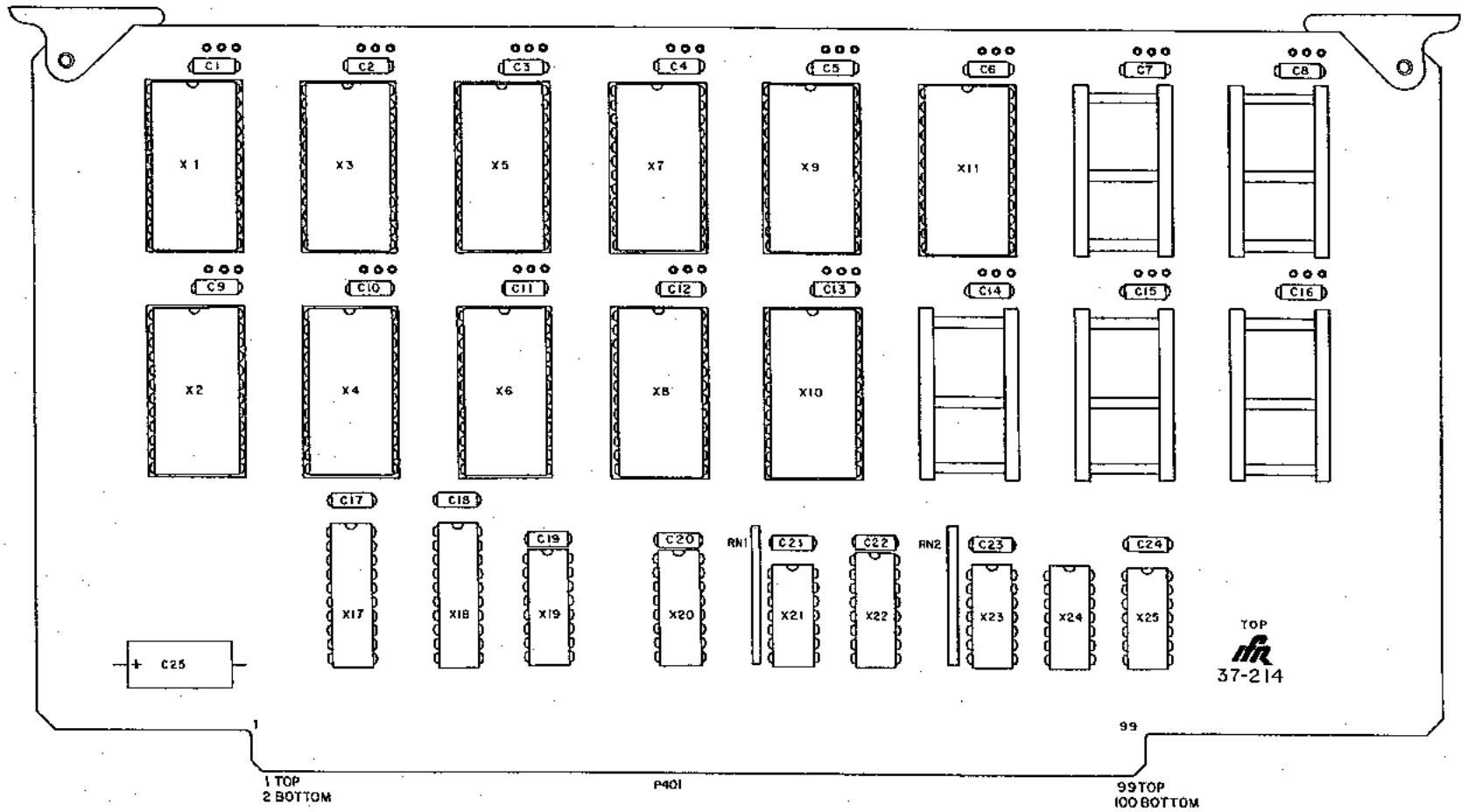
Motherboard PC Board (400)
Figure 96

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Rear Panel PC Board (200)
Figure 97

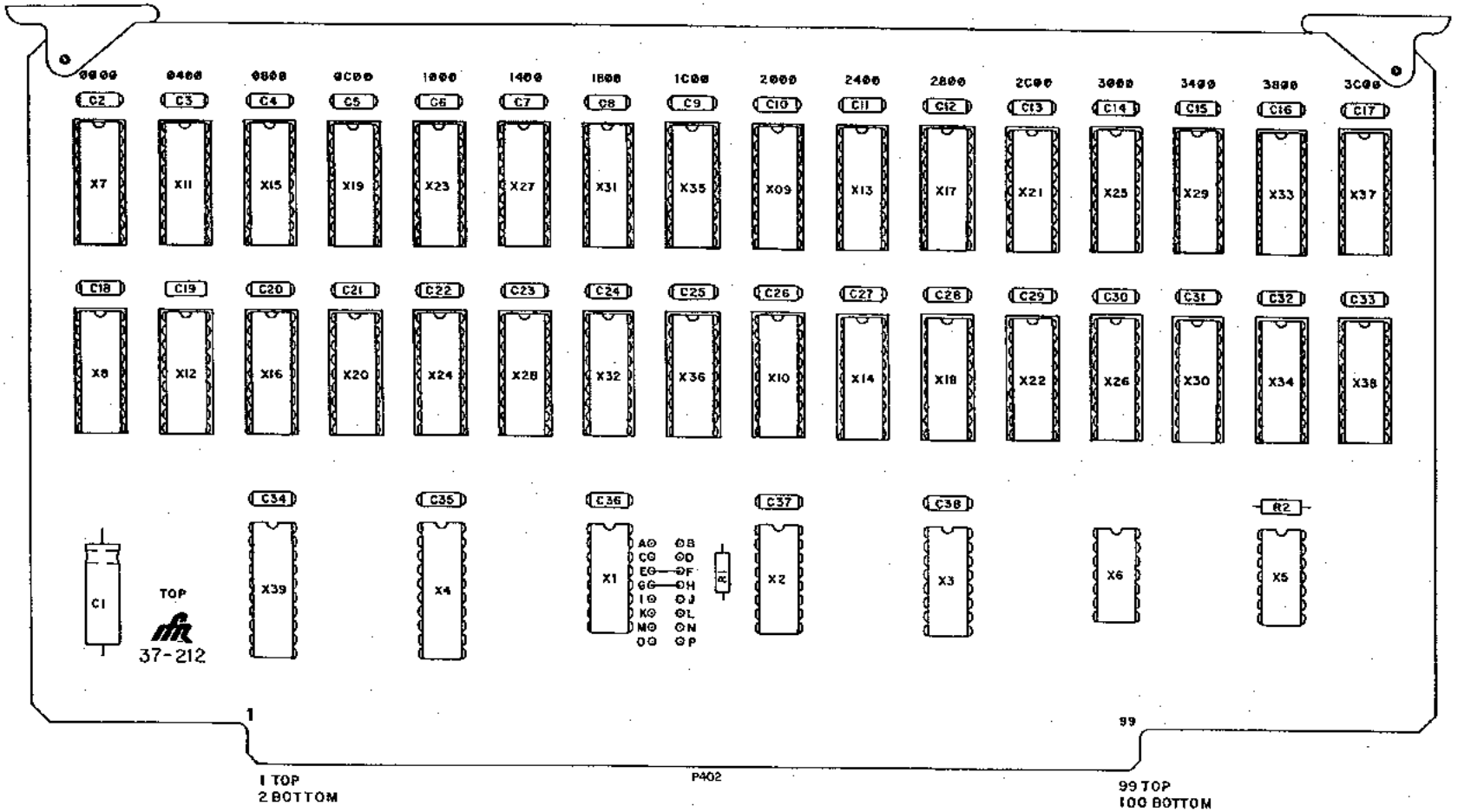
Artisan Technology Group - Quality Instrumentation ... Guaranteed | (888) 88-SOURCE | www.artisantg.com



JUMPER LOCATION	ADDRESS	
	XI201-XI208	XI209 - XI216
AY-Z	0000-3FFF	N/A
AY-X	N/A	0000 -3FFF
BY-Z	4000-7FFF	N/A
BY-X	N/A	4000 -7FFF
CY-Z	8000 - BFFF	N/A
CY-X	N/A	8000 - BFFF
DY-Z	C000 - FFFF	N/A

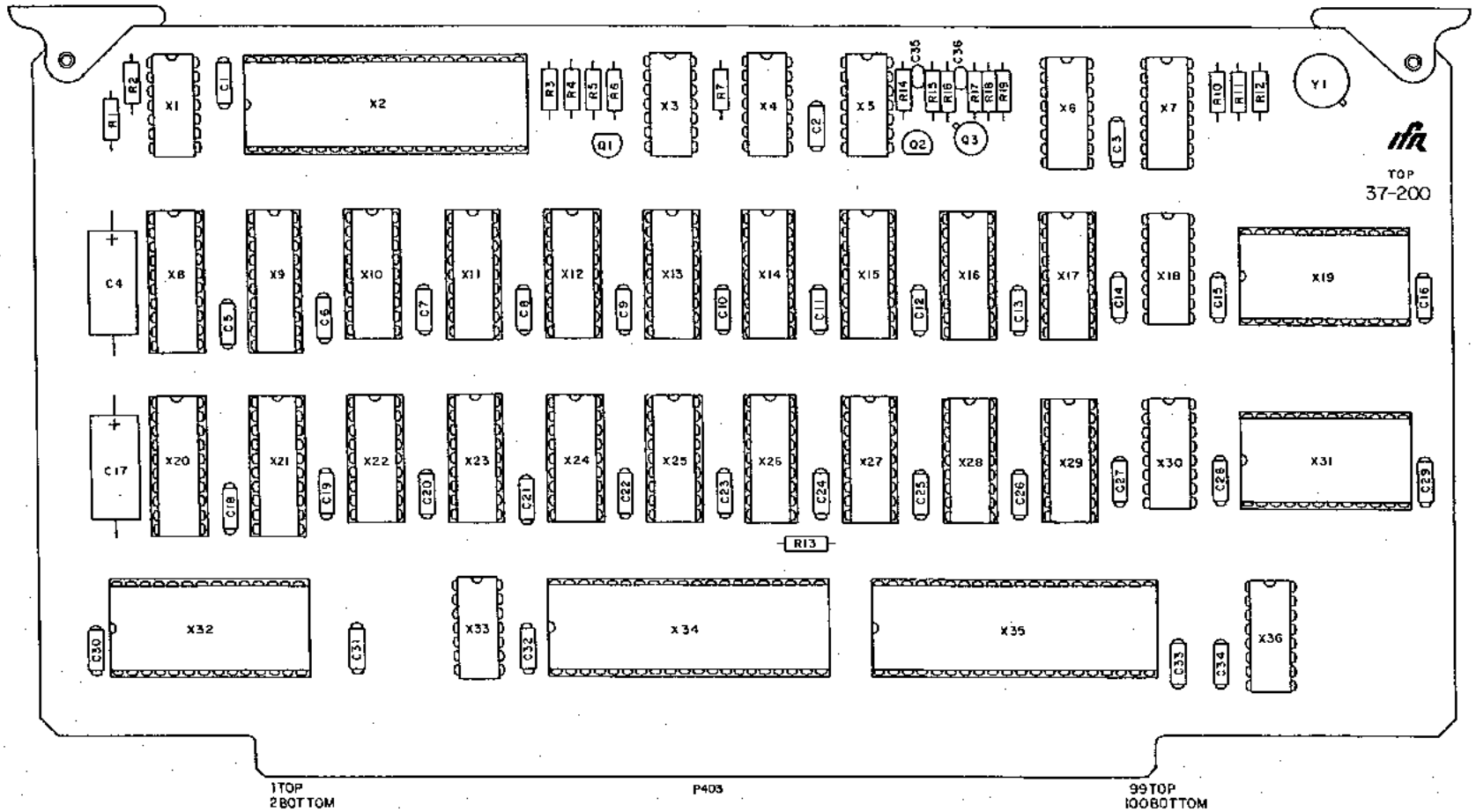
32K PROM PC Board (1200)
Figure 98

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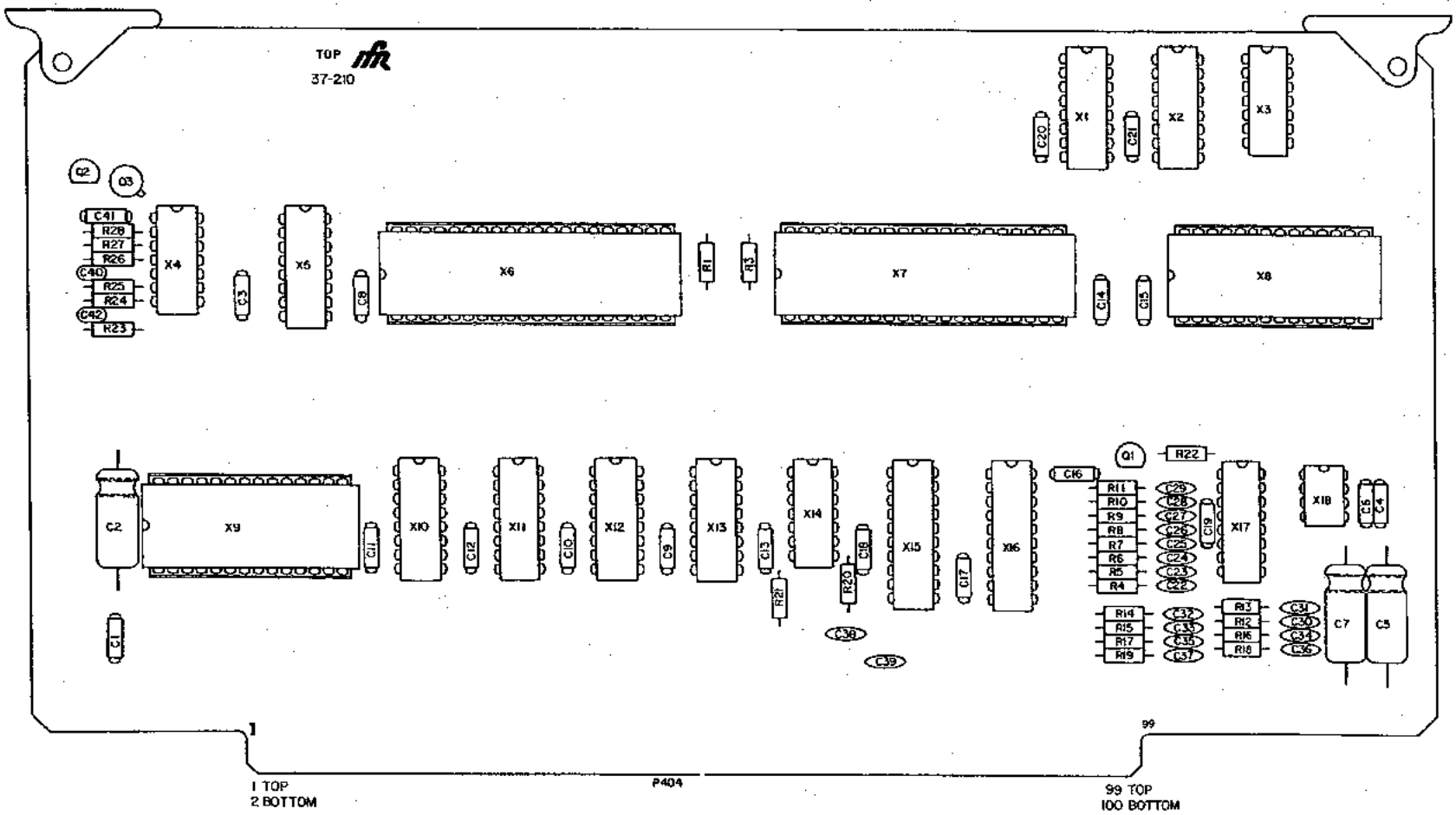
16K RAM PC Board (1100)
Figure 99

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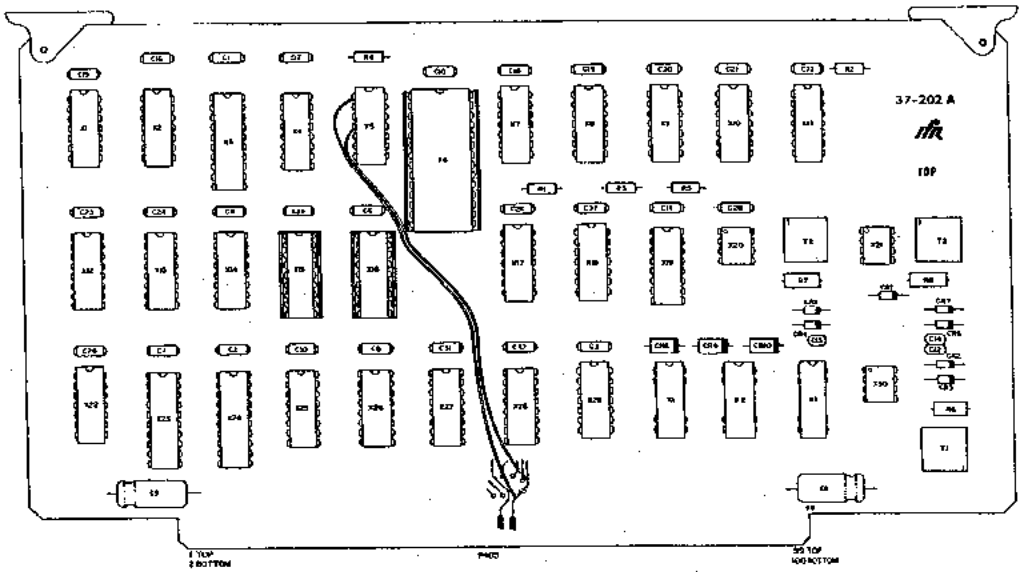
CPU PC Board (800)
Figure 100

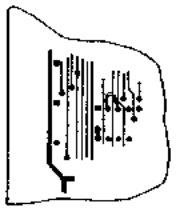
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I/O PC Board (1000)
Figure 101

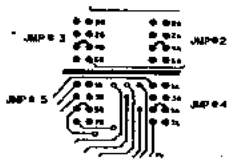
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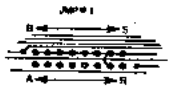




VHS Output PC Board (700)
Figure 102

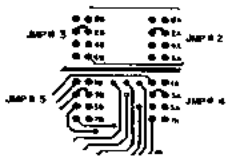
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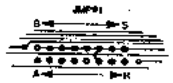


7010-3730-601 ("B" BOARD)



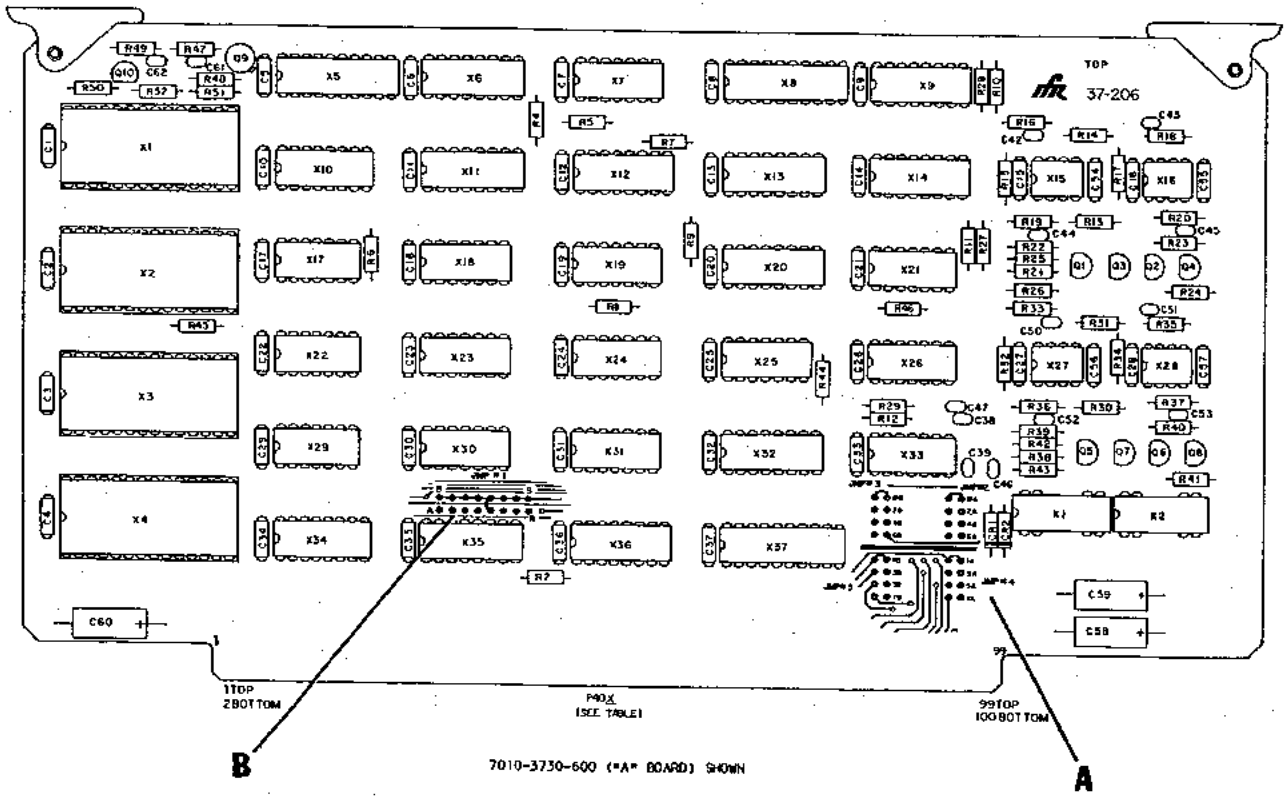
7010-3730-601 ("B" BOARD)



7010-3730-602 ("C" BOARD)



7010-3730-602 ("C" BOARD)

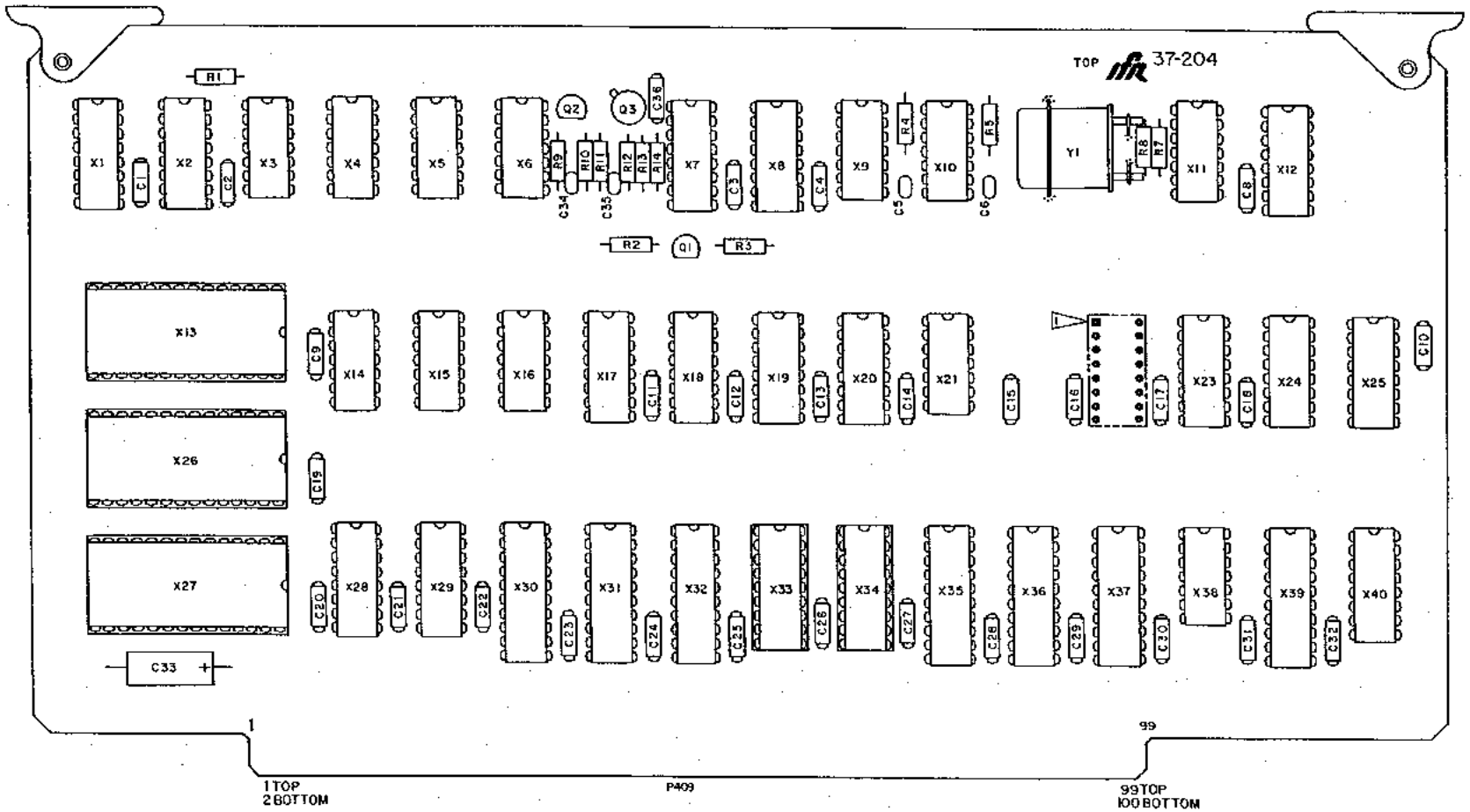


7010-3730-600 ("A" BOARD) SHOWN

DASH NO.	BD NO	CARD EDGE REF DES	JUMPER #1	JUMPER #2	JUMPER #3	JUMPER #4	JUMPER #5
-00	A	P406	J to K	8A	8B	1A	1B
-01	B	P407	L to M	2A	2B	3A	3B
02	C	P408	N to P	4A	4B	5A	5B

429 Bus Output PC Board (900)
Figure 103

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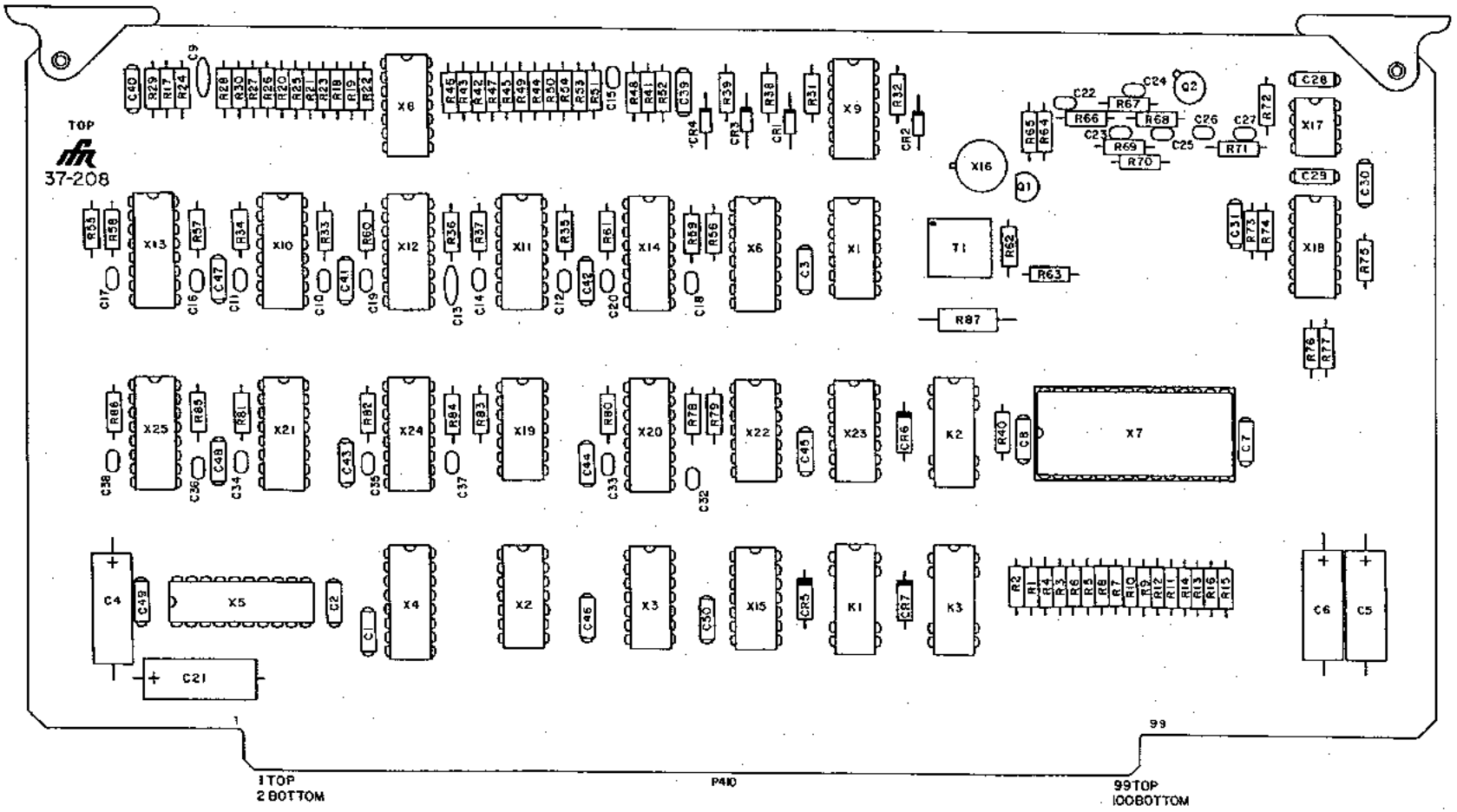


NOTE:

1. LEAVE THIS AREA CLEAR OF SOLDER.

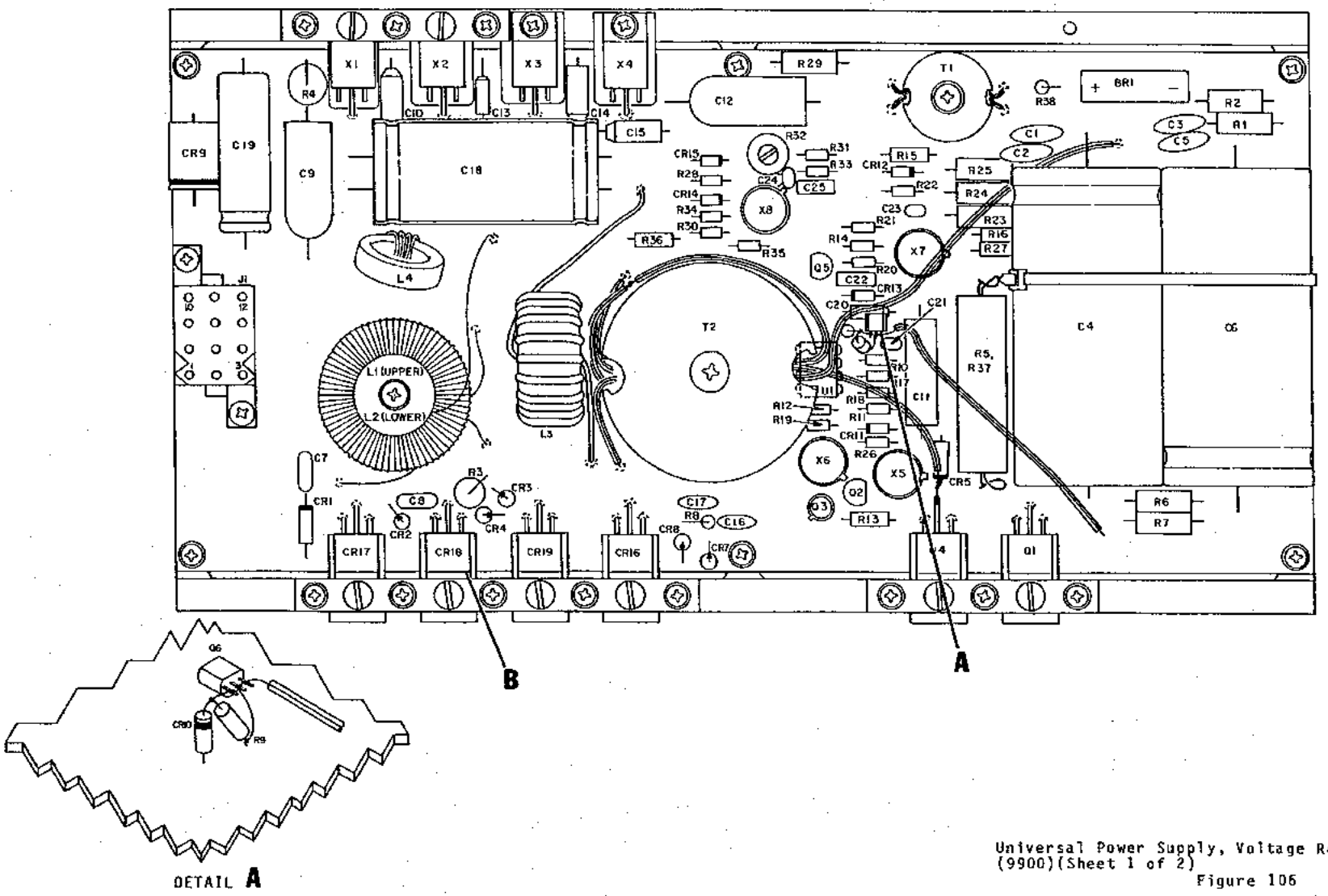
Bus Input Logic PC Board
Figure 104

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Bus Input Analog PC Board (500)
Figure 105

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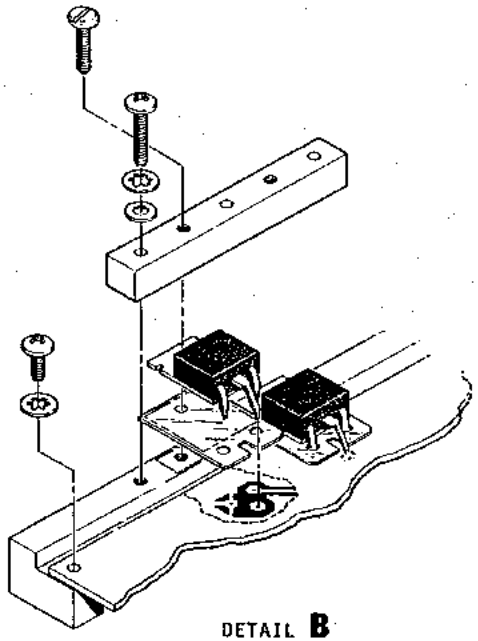


DETAIL **A**

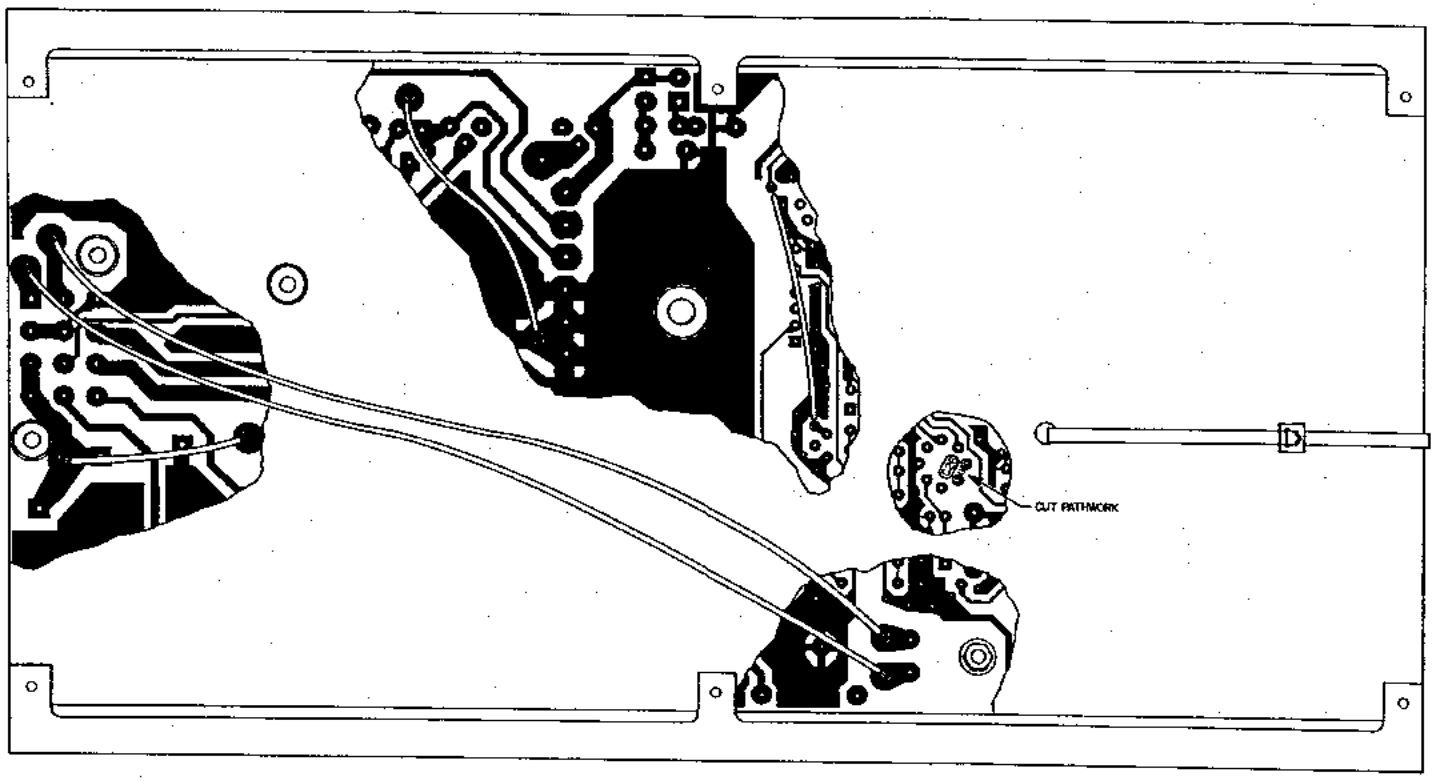
Universal Power Supply, Voltage Regulator PC Board (9900)(Sheet 1 of 2)

Figure 105

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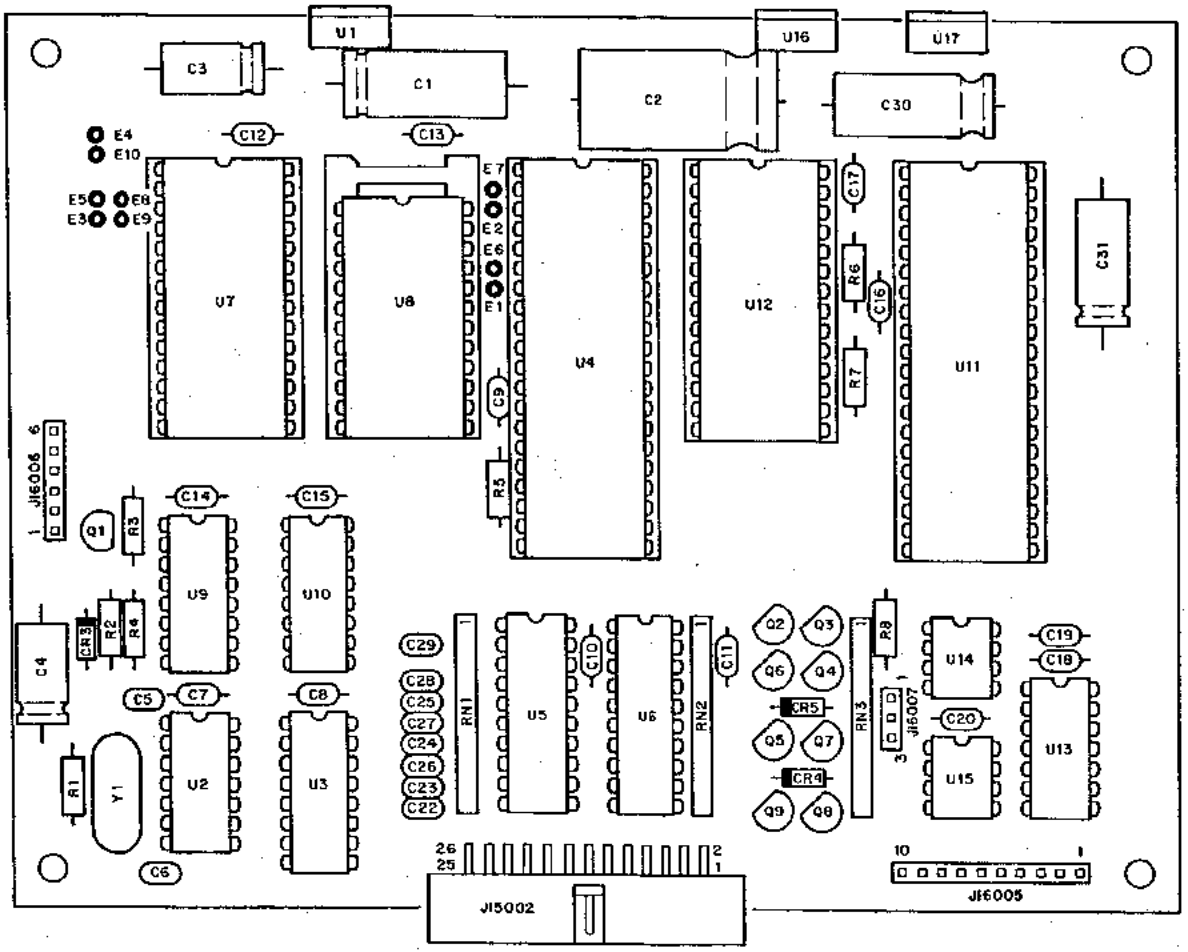
DETAIL B



BOTTOM VIEW

Universal Power Supply, Voltage Regulator PC Board (9900)
(Sheet 2 of 2)
Figure 106

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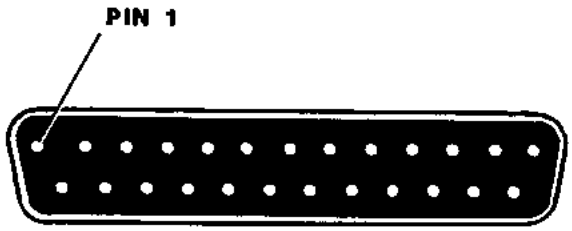
CRT Interface PC Board
Figure 107

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APPENDIX A: PIN OUT TABLES

1. Pin Out Tables

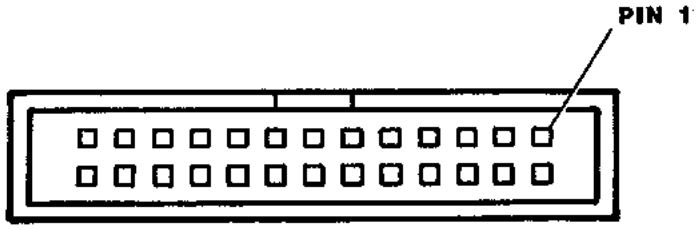
Connector J413		Connector J414		Connector J415	
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	GROUND	1	GROUND	1	DIO1
2	IAØ	2	RXD	2	DIO2
3	IA1	3	TXD	3	DIO3
4	GROUND	4	NOT USED	4	DIO4
5	IA2	5	NOT USED	5	EOI
6	IO7	6	NOT USED	6	DAV
7	GROUND	7	GROUND	7	NRFD
8	IA3	8	DTR	8	NDAC
9	ID6	9	NOT USED	9	IFC
10	GROUND	10	NOT USED	10	SRQ
11	IA4	11	NOT USED	11	ATN
12	ID5	12	NOT USED	12	GROUND
13	GROUND	13	NOT USED	13	DIO5
14	IA5	14	NOT USED	14	DIO6
15	ID4	15	NOT USED	15	DIO7
16	GROUND	16	NOT USED	16	DIO8
17	RDEN	17	NOT USED	17	GROUND
18	ID3	18	NOT USED	18	GROUND
19	GROUND	19	NOT USED	19	GROUND
20	WREN	20	NOT USED	20	GROUND
21	ID2	21	NOT USED	21	GROUND
22	XSTAT	22	DSR	22	GROUND
23	INTR	23	NOT USED	23	GROUND
24	ID1	24	NOT USED	24	GROUND
25	IDØ	25	NOT USED	25	GROUND



25-Pin Connector
Figure 1

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Connector J15002		Connector J15003		Connector J15004	
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
1	ROW 1	1	GND	1	GND
2	N/C	2	TXD	2	RXC
3	ROW 3	3	RXD	3	TXD
4	ROW 2	4	N/U	4	CTS
5	N/U	5	N/U	5	RTS
6	N/C	6	N/U	6	RTS
7	N/U	7	GND	7	GND
8	N/U	8	N/U	8	N/C
9	ROW 5	9	N/U	9	N/C
10	ROW 4	10	N/U	10	N/C
11	N/C	11	N/U	11	N/C
12	N/C	12	N/U	12	N/C
13	N/C	13	N/U	13	N/C
14	GND	14	N/U	14	N/C
15	N/C	15	N/U	15	N/C
16	N/C	16	N/U	16	N/C
17	N/C	17	N/U	17	N/C
18	N/C	18	N/U	18	N/C
19	COL 2	19	N/U	19	N/C
20	COL 1	20	DTR	20	N/C
21	COL 4	21	N/U	21	N/C
22	COL 3	22	N/U	22	N/C
23	COL 6	23	N/U	23	N/C
24	COL 5	24	N/U	24	N/C
25	COL 8	25	N/U	25	N/C
26	COL 7				

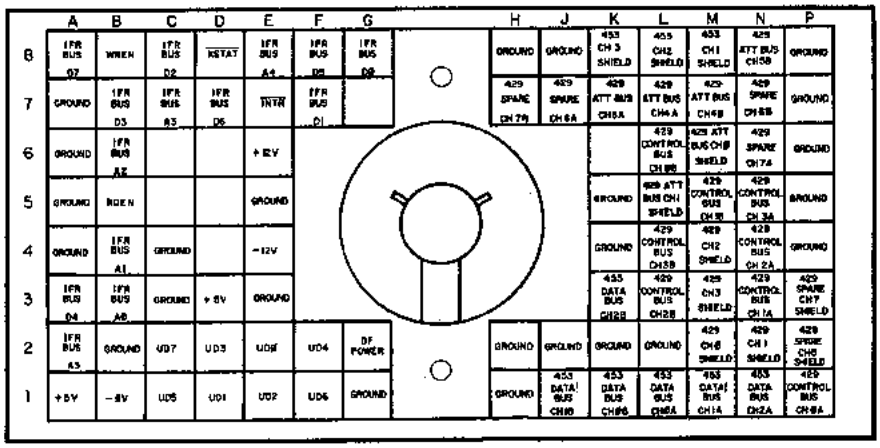


26 Pin Connector
Figure 2

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Connector J416

Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
A-1	+5 V	E-1	UD2	L-1	VHS DB CH1A
A-2	IFR BUS A5	E-2	UDØ/	L-2	GROUND
A-3	IFR BUS D4	E-3	GROUND	L-3	429 CB CH3B
A-4	GROUND	E-4	-12 V	L-4	429 CB CH2B
A-5	GROUND	E-5	GROUND	L-5	429 ATT 1 SH
A-6	GROUND	E-6	+12 V	L-6	429 CB CHØB
A-7	GROUND	E-7	INTR	L-7	429 AT CHØA
A-8	IFR BUS D7	E-8	IFR BUS A4	L-8	VHS CH2 SH
B-1	5 V	F-1	UD6	M-1	VHS DB CH2A
B-2	GROUND	F-2	UD4	M-2	429 CHØ SH
B-3	IFR BUS AØ	F-7	IFR BUS D1	M-3	429 CH2 SH
B-4	IFR BUS A1	F-8	IFR BUS D5	M-4	429 CH3 SH
B-5	RDEN	G-1	GROUND	M-5	429 CB CH1B
B-6	IFR BUS A2	G-2	DF PWR	M-6	429 ATTØ SH
B-7	IFR BUS D3	G-7	N/C	M-7	429 AT CHØB
B-8	WREN	G-8	IFR BUS DØ	M-8	VHS CH1 SH
C-1	UD5	H-1	GROUND	N-1	VHS DB CH3A
C-2	UD7	H-2	GROUND	N-2	429 CH1 SH
C-3	GROUND	H-7	429 SP CH7A	N-3	429 CB CH1A
C-4	N/C	H-8	GROUND	N-4	429 CB CH2A
C-5	N/C	J-1	VHS DB CH2B	N-5	429 CB CH3A
C-6	N/C	J-2	GROUND	N-6	429 SP CH7B
C-7	IFR BUS A3	J-7	429 SP CH6A	N-7	429 SP CH6B
C-8	IFR BUS D2	J-8	GROUND	N-8	429 AT CH1B
D-1	UD1	K-1	VHS DB CH1B	P-1	429 CB CHØA
D-2	UD3	K-2	GROUND	P-2	429 SP6 SH
D-3	+5 V	K-3	VHS DB CH3B	P-3	429 SP7 SH
D-4	N/C	K-4	GROUND	P-4	GROUND
D-5	N/C	K-5	GROUND	P-5	GROUND
D-6	N/C	K-6	N/C	P-6	GROUND
D-7	IFR BUS D6	K-7	429 ATT CH1A	P-7	GROUND
D-8	XSTAT	K-8	VHS CH3 SH	P-8	GROUND



Connector J416
Figure 3

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APPENDIX B - TEST EQUIPMENT REQUIREMENTS

1. General

This appendix contains a list of test equipment suitable for performing all of the maintenance procedures contained in this manual. Any other equipment meeting the specifications listed in this appendix may be substituted in place of recommended models. It should be noted that the equipment listed in this appendix may exceed the minimum required specifications for some of the procedures contained in this manual.

2. Recommended Test Equipment

TYPE	MANUFACTURER AND MODEL	
Oscilloscope	Tektronix 465 B	DC to 100 MHz 5 mV/Div vertical trace 2 nS/Div sweep rate Dual Trace
Oscilloscope	Hewlett-Packard Model 1743A	Dual Trace with Delta Time
Digital Multimeter	Fluke Model 8010A	3½ Digit, ±0.1% basic DC accuracy.

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APPENDIX C - WRX/WRC-7708 GPIB COMMAND TABLES

COMMAND	FUNCTION
1. Pn. or P(n).	Selects page "n" for display and control. The value of "n" may be 1 thru 8, as defined by the Master Menu.
2. P?	Returns number of the page currently active.
3. Fn_1n_2. or $F(n_1n_2)$.	Simulates keyboard selection of field "n_1n_2". If this is a binary field, this command will cause the data to toggle.
4. $Fn_1n_2 = d_1d_2d_3$ or $F(n_1n_2) = d_1d_2d_3$	Causes data of field "n_1n_2" to become "$d_1d_2d_3$". Format of data must be as defined by the WRX/WRC-7708 Systems Operation Manual.
5. Fn_1n_2? or $F(n_1n_2)$?	Causes value of data field "n_1n_2" to be returned to the GPIB controller. Multiple fields may be requested, in which case the response of each field is separated by a ":" delimiter. NOTE: Some fields return more than one response (e.g. Page 6, Field 15). In this case a ";" is used as a delimiter.
6. DOFF.	Cause the STD-7000 display to not be updated.
7. DON.	Causes the STD-7000 display to be updated as in manual operation.
8. DSP?	Returns status of DON/DOFF.

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COMMAND	FUNCTION
9. /	This character causes an Enter key to be simulated wherever it is found in a string. It is intended for use in following two special cases: a. It should be used after each data character in a command to Field 2 on Page 2 (e.g. F2 = 1/2/.). b. It should be used as a delimiter in fields 3 and 4 of page 8 to separate the value and mode fields (e.g. F3 = +20/3).
10. SRQ = $b_6 b_5 b_4 b_3 b_2 b_1$	Sets one to six SRQ interrupt mask bits for servicing errors (see Table 1).
11. SRQ?	Returns the status ($b_6 b_5 b_4 b_3 b_2 b_1$) of the SRQ mask.
12. :	Command separator or terminator.

WRX/WRC-7708 GPIB Command Table
Table 1

SRQ Maskable interrupt conditions set by the command
SRQ = $b_6 \ldots b_1$

b_6	b_5	b_4	b_3	b_2	b_1		Mask condition
Ø	Ø	Ø	Ø	Ø	1	or just 1	WRX-7708 Timeout error implying that the data word has not been received in the required amount of time.
Ø	Ø	Ø	Ø	1	Ø	or just 1Ø	A command entry or syntax error has occurred.

NOTE: Bits three to six are undefined at this time.

SRQ Maskable Interrupt Conditions
Table 2

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APPENDIX D: STD-7000 I/O MAP

ADDRESS	DEVICE
0 0	NOT USED
0 1	NOT USED
0 2	NOT USED
0 3	NOT USED
0 4	RS232C DATA
0 5	RS232C STATUS
0 6	NOT USED
0 7	NOT USED
0 8	IFR BUS DATA
0 9	IFR BUS CONTROL (DATA)
0 A	IFR BUS ADDRESS
0 B	IFR BUS CONTROL (ADDRESS)
0 C	IFR BUS STROBES
0 D	IFR BUS STROBES
0 E	IFR BUS STROBES
0 F	IFR BUS STROBES
1 0	DF POWER CONTROL
1 1	DF POWER CONTROL
1 2	DF POWER CONTROL
1 3	DF POWER CONTROL
1 4	CPU CTC BAUD RATE
1 5	CPU CTC TX READY
1 6	CPU CTC RX READY
1 7	CPU CTC IEEE INTER
1 8	IEEE-488-1978 REGISTERS
1 9	IEEE-488-1978 REGISTERS
1 A	IEEE-488-1978 REGISTERS
1 B	IEEE-488-1978 REGISTERS
1 C	IEEE-488-1978 REGISTERS
1 D	IEEE-488-1978 REGISTERS
1 E	IEEE-488-1978 REGISTERS
1 F	IEEE-488-1978 REGISTERS
2 0	PIO DATA
2 1	PIO CONTROL
2 2	PIO (TAPE) DATA
2 3	PIOT (TAPE) CONTROL
2 4	CPU CTC
2 5	CPU CTC
2 6	CPU CTC
2 7	CPU CTC
2 8	IEEE-488 ADDRESS (DATA)
2 9	IEEE-488 ADDRESS (CONTROL)
2 A	PIO (DATA)
2 B	PIO (CONTROL)
2 C	NOT USED
2 D	NOT USED
2 E	NOT USED
2 F	NOT USED

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ADDRESS	DEVICE
3 0	VHS INPUT (WPM)
3 1	VHS INPUT (EOW)
3 2	VHS INPUT (REP RATE)
3 3	VHS INPUT (REP RATE)
3 4	429 INPUT (WPM)
3 5	429 INPUT (EOW)
3 6	429 INPUT (REP RATE)
3 7	429 INPUT (REP RATE)
3 8	VHS INPUT (BITS PER WORD)
3 9	VHS INPUT (BITS PER WORD)
3 A	429 INPUT (BITS PER WORD)
3 B	429 INPUT (BITS PER WORD)
3 C	LOW SPEED CLOCK FREQUENCY SELECT
3 D	LOW SPEED CLOCK FREQUENCY SELECT
3 E	LOW SPEED CLOCK FREQUNECY SELECT
3 F	LOW SPEED CLOCK FREQUENCY SELECT
4 0	VHS ADDRESS PRESET
4 1	VHS ADDRESS PRESET
4 2	VHS ADDRESS PRESET
4 3	VHS ADDRESS PRESET
4 4	VHS ADDRESS PRESET
4 5	VHS ADDRESS PRESET
4 6	VHS ADDRESS PRESET
4 7	VHS ADDRESS PRESET
4 8	VHS PAGE AND BUS SELECT
4 9	VHS PAGE AND BUS SELECT
4 A	VHS PAGE AND BUS SELECT
4 B	VHS PAGE AND BUS SELECT
4 C	VHS PAGE AND BUS SELECT
4 D	VHS PAGE AND BUS SELECT
4 E	VHS PAGE AND BUS SELECT
4 F	VHS PAGE AND BUS SELECT
5 0	VHS CTC (REP RATE) HI
5 1	VHS CTC (REP RATE) LO
5 2	NOT USED
5 3	VHS CTC (EOW)
5 4	NOT USED
5 5	NOT USED
5 6	NOT USED
5 7	NOT USED
5 8	NOT USED
5 9	NOT USED
5 A	NOT USED
5 B	NOT USED
5 C	NOT USED
5 D	NOT USED
5 E	INPUT BUS SELECT
5 F	INPUT BUS SELECT

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ADDRESS	DEVICE
6 0	NOT USED
6 1	NOT USED
6 2	NOT USED
6 3	NOT USED
6 4	NOT USED
6 5	NOT USED
6 6	NOT USED
6 7	NOT USED
6 8	NOT USED
6 9	NOT USED
6 A	NOT USED
6 B	NOT USED
6 C	NOT USED
6 D	NOT USED
6 E	NOT USED
6 F	NOT USED
7 0	NOT USED
7 1	NOT USED
7 2	NOT USED
7 3	NOT USED
7 4	NOT USED
7 5	NOT USED
7 6	NOT USED
7 7	NOT USED
7 8	NOT USED
7 9	NOT USED
7 A	NOT USED
7 B	NOT USED
7 C	NOT USED
7 D	NOT USED
7 E	NOT USED
7 F	NOT USED
8 0	429 BUS CHANNEL Ø (REP RATE)
8 1	429 BUS CHANNEL Ø (REP RATE)
8 2	429 BUS CHANNEL Ø (WPM)
8 3	NOT USED
8 4	429 BUS CHANNEL Ø (INNER WORD GAP)
8 5	429 BUS CHANNEL Ø (INNER WORD GAP)
8 6	429 BUS CHANNEL Ø (BITS PER WORD)
8 7	NOT USED
8 8	429 BUS CHANNEL 1 (REP RATE)
8 9	429 BUS CHANNEL 1 (REP RATE)
8 A	429 BUS CHANNEL 1 (WPM)
8 B	NOT USED
8 C	429 BUS CHANNEL 1 (INNER WORD GAP)
8 D	429 BUS CHANNEL 1 (INNER WORD GAP)
8 E	429 BUS CHANNEL 1 (BITS PER WORD)
8 F	NOT USED

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ADDRESS	DEVICE
9 0	CHANNEL Ø ADDRESS PRESET
9 1	CHANNEL Ø ADDRESS PRESET
9 2	CHANNEL Ø ADDRESS PRESET
9 3	CHANNEL Ø ADDRESS PRESET
9 4	429 BUS CHANNEL 1 ADDRESS PRESET
9 5	429 BUS CHANNEL 1 ADDRESS PRESET
9 6	429 BUS CHANNEL 1 ADDRESS PRESET
9 7	429 BUS CHANNEL 1 ADDRESS PRESET
9 8	429 BUS CHANNELS Ø AND 1 BUS ENABLE
9 9	429 BUS CHANNELS Ø AND 1 BUS ENABLE
9 A	429 BUS CHANNELS Ø AND 1 BUS ENABLE
9 B	429 BUS CHANNELS Ø AND 1 BUS ENABLE
9 C	429 BUS CHANNELS Ø AND 1 P/S LOAD
9 D	429 BUS CHANNELS Ø AND 1 P/S LOAD
9 E	429 BUS CHANNELS Ø AND 1 P/S LOAD
9 F	429 BUS CHANNELS Ø AND 1 P/S LOAD
A 0	429 BUS CHANNEL 2 (REP RATE)
A 1	429 BUS CHANNEL 2 (REP RATE)
A 2	429 BUS CHANNEL 2 (WPM)
A 3	NOT USED
A 4	429 BUS CHANNEL 2 (INNER WORD GAP)
A 5	429 BUS CHANNEL 2 (INNER WORD GAP)
A 6	429 BUS CHANNEL 2 (BITS PER WORD)
A 7	NOT USED
A 8	429 BUS CHANNEL 3 (REP RATE)
A 9	429 BUS CHANNEL 3 (REP RATE)
A A	429 BUS CHANNEL 3 (WPM)
A B	NOT USED
A C	429 BUS CHANNEL 3 (INNER WORD GAP)
A D	429 BUS CHANNEL 3 (INNER WORD GAP)
A E	429 BUS CHANNEL 3 (BITS PER WORD)
A F	NOT USED
B 0	429 BUS CHANNEL 2 ADDRESS PRESET
B 1	429 BUS CHANNEL 2 ADDRESS PRESET
B 2	429 BUS CHANNEL 2 ADDRESS PRESET
B 3	429 BUS CHANNEL 2 ADDRESS PRESET
B 4	429 BUS CHANNEL 2 ADDRESS PRESET
B 5	429 BUS CHANNEL 2 ADDRESS PRESET
B 6	429 BUS CHANNEL 2 ADDRESS PRESET
B 7	429 BUS CHANNEL 2 ADDRESS PRESET
B 8	429 BUS CHANNELS 2 AND 3 BUS ENABLE
B 9	429 BUS CHANNELS 2 AND 3 BUS ENABLE
B A	429 BUS CHANNELS 2 AND 3 BUS ENABLE
B B	429 BUS CHANNELS 2 AND 3 BUS ENABLE
B C	429 BUS CHANNELS 2 AND 3 P/S LOAD
B D	429 BUS CHANNELS 2 AND 3 P/S LOAD
B E	429 BUS CHANNELS 2 AND 3 P/S LOAD
B F	429 BUS CHANNELS 2 AND 3 P/S LOAD

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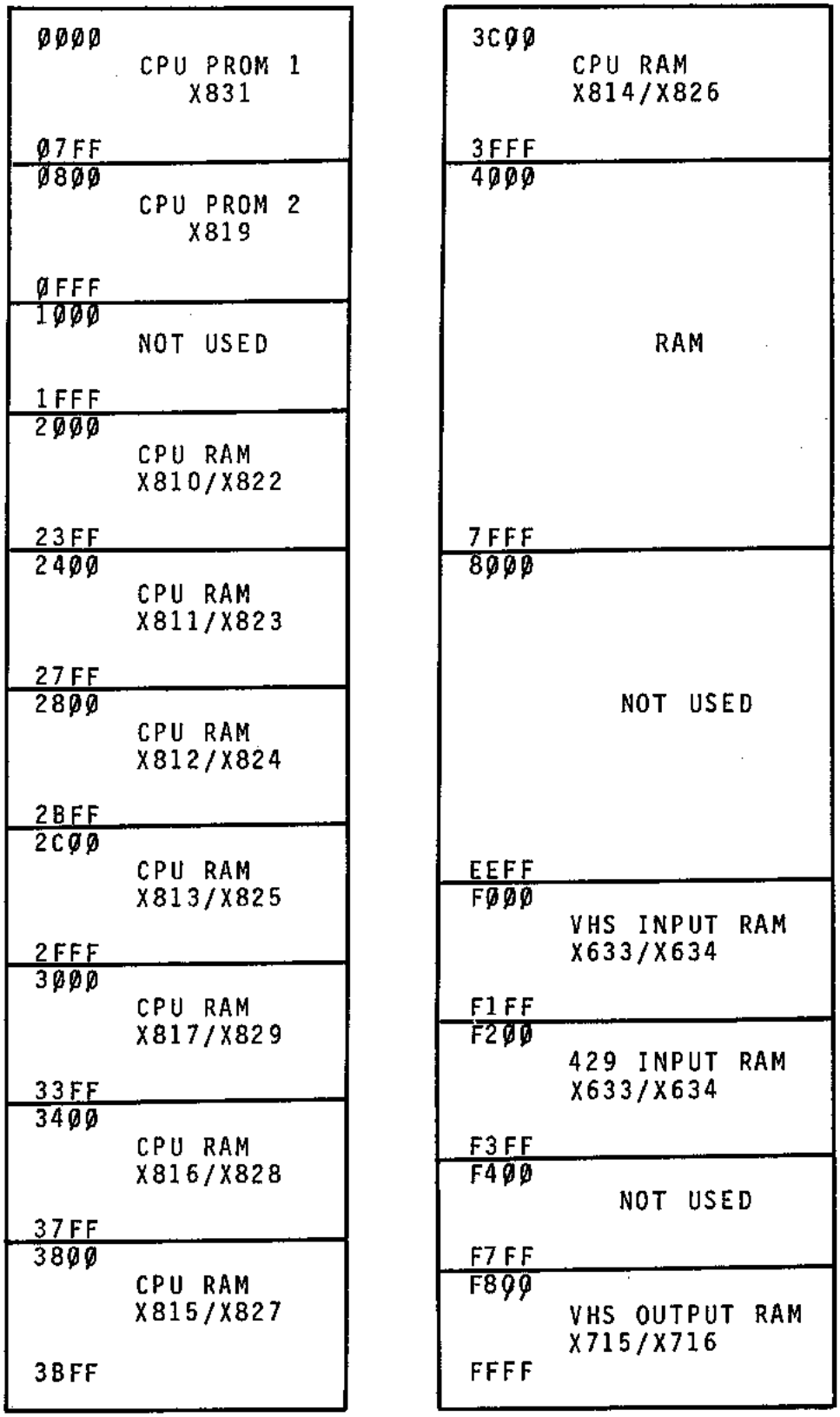
ADDRESS	DEVICE
C 0	429 ATTITUDE BUS CHANNEL Ø (CH 4 REP RATE)
C 1	429 ATTITUDE BUS CHANNEL Ø (CH 4 REP RATE)
C 2	429 ATTITUDE BUS CHANNEL Ø (CH 4 REP RATE)
C 3	NOT USED
C 4	429 ATTITUDE BUS CHANNEL Ø (CH 4 INNER WORD GAP)
C 5	429 ATTITUDE BUS CHANNEL Ø (CH 4 INNER WORD GAP)
C 6	429 ATTITUDE BUS CHANNEL Ø (CH 4 BITS PER WORD)
C 7	NOT USED
C 8	429 ATTITUDE BUS CHANNEL 1 (CH 5 REP RATE)
C 9	429 ATTITUDE BUS CHANNEL 1 (CH 5 REP RATE)
C A	429 ATTITUDE BUS CHANNEL 1 (CH 5 WPM)
C B	NOT USED
C C	429 ATTITUDE BUS CHANNEL 1 (CH 5 INNER WORD GAP)
C D	429 ATTITUDE BUS CHANNEL 1 (CH 5 INNER WORD GAP)
C E	429 ATTITUDE BUS CHANNEL 1 (CH 5 BITS PER WORD)
C E	429 ATTITUDE BUS CHANNEL 1 (CH 5 BITS PER WORD)
C F	NOT USED
D 0	429 ATTITUDE BUS CHANNEL Ø (CH 4 ADDRESS PRESET)
D 2	429 ATTITUDE BUS CHANNEL Ø (CH 4 ADDRESS PRESET)
D 3	429 ATTITUDE BUS CHANNEL Ø (CH 4 ADDRESS PRESET)
D 4	429 ATTITUDE BUS CHANNEL 1 (CH 5 ADDRESS PRESET)
D 5	429 ATTITUDE BUS CHANNEL 1 (CH 5 ADDRESS PRESET)
D 6	429 ATTITUDE BUS CHANNEL 1 (CH 5 ADDRESS PRESET)
D 7	429 ATTITUDE BUS CHANNEL 1 (CH 5 ADDRESS PRESET)
D 8	429 ATTITUDE BUS CHANNELS Ø AND 1 BUS ENABLE
D 9	429 ATTITUDE BUS CHANNELS Ø AND 1 BUS ENABLE
D A	429 ATTITUDE BUS CHANNELS Ø AND 1 BUS ENABLE
D B	429 ATTITUDE BUS CHANNELS Ø AND 1 BUS ENABLE
D C	429 ATTITUDE BUS CHANNELS Ø AND 1 P/S LOAD
D D	429 ATTITUDE BUS CHANNELS Ø AND 1 P/S LOAD
D E	429 ATTITUDE BUS CHANNELS Ø AND 1 P/S LOAD
D F	429 ATTITUDE BUS CHANNELS Ø AND 1 P/S LOAD
E 0	429 SPARE BUS (CH 6 REP RATE)
E 1	429 SPARE BUS (CH 6 REP RATE)
E 2	429 SPARE BUS (CH 6 WPM)
E 3	NOT USED
E 4	429 SPARE BUS (CH 6 INNER WORD GAP)
E 5	429 SPARE BUS (CH 6 INNER WORD GAP)
E 6	429 SPARE BUS (CH 6 BITS PER WORD)
E 7	NOT USED
E 8	429 SPARE BUS (CH 7 REP RATE)
E 9	429 SPARE BUS (CH 7 REP RATE)
E A	429 SPARE BUS (CH 7 WPM)
E B	NOT USED
E C	429 SPARE BUS (CH 7 INNER WORD GAP)
E D	429 SPARE BUS (CH 7 INNER WORD GAP)
E E	429 SPARE BUS (CH 7 BITS PER WORD)
E F	NOT USED

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ADDRESS	DEVICE
F 0	429 SPARE BUS (CH 6 ADDRESS PRESET)
F 1	429 SPARE BUS (CH 6 ADDRESS PRESET)
F 2	429 SPARE BUS (CH 6 ADDRESS PRESET)
F 3	429 SPARE BUS (CH 6 ADDRESS PRESET)
F 4	429 SPARE BUS (CH 7 ADDRESS PRESET)
F 5	429 SPARE BUS (CH 7 ADDRESS PRESET)
F 6	429 SPARE BUS (CH 7 ADDRESS PRESET)
F 7	429 SPARE BUS (CH 7 ADDRESS PRESET)
F 8	429 SPARE BUS CHANNELS 6 AND 7 BUS ENABLE
F 9	429 SPARE BUS CHANNELS 6 AND 7 BUS ENABLE

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APPENDIX E: STD-7000 MEMORY MAP



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APPENDIX F - ABBREVIATIONS

1. General Abbreviations

Defined below are various abbreviations and symbols which are commonly used throughout the STD-7000 Bus Controller Maintenance Manual text:

A	Address
AB	Address Bus
AC	Alternating Current
adj.	adjustment
AM	Amplitude Modulation
ARDY	Register A Ready
ARINC	Aeronautical Radio Inc.
ASCII	American National Standard Code for Information Interchange
Assy	Assembly
ASTB	A Strobe
AT	Attitude Bus
ATE	Automatic Test Equipment
ATN	Attention
Aux	Auxiliary
BCD	Binary-coded Data
BRDY	Register B Ready
BSTB	B Strobe
BUSAK	Bus Acknowledge
BUSRQ	Bus Request
BWS	Beginning Word Sync
CB	Control Bus
ccw	counter clockwise
CH	Channel
CK or CLK	Clock
CLK/TRG	External Clock/Timer Trigger
cm	Centimeter
CRT	Cathode Ray Tube
CS	Chip Select
CW	Continuous Wave
cw	clockwise
D	Data
DAV	Data Available
DB	Data Bus
dB	decibel
dBm	decibel relative to one milliwatt
DC	Direct Current
DF	Discrete Functions
DIP	Dual In-Line Package
DMM	Digital Multimeter
DSR	Data Set Ready

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DTR	Data Terminal Ready
DVM	Digital Voltmeter
EIA	Electronics Industries Association
EOI	Enable In/Out
EPROM	Electrically Programmable Read Only Memory
EWS	End Word Sync
FM	Frequency Modulation
FREQ	Frequency
GEN	Generator
Gd or GND	Ground
GPIB	General Purpose Interface Bus
HS	High Speed
Hz	Hertz
IAW	In Accordance With
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronic Engineers
IEI	Interrupt Enable In
IEO	Interrupt Enable Out
IFC	Interface Clear
INTAK	Interrupt Acknowledge
INTR	Interrupt
INTRQ	Interrupt Request
I/O	Input/Output
IORQ	Input/Output Request
ips	Inches per Second
K	1000
Kg	Kilogram
kHz	Kilohertz
LED	Light Emitting Diode
LS	Low Speed
LSB	Least Significant Bit
MDS	Minimum Discrenible Signal
MHz	Megahertz
MREQ	Memory Request
MSB	Most Significant Bit
mSec or ms	Millisecond
M1	Machine Cycle One
NDAC	No Data Accepted
nm	Nautical Mile
NMI	Non Maskable Interrupt
NRFD	Not Ready for Data
P	Plug
PA	Processor Address
para	paragraph
PB	Processor Bus
PC	Printed Circuit
p-p	peak to peak
pps	pulse per second
PRF	Pulse Repetition Frequency
PROM	Programmable Read Only Memory
PSI	Pounds Per Square Inch
RAM	Random Access Memory

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RD	Read
REF	Reference
REN	Read Enable
RF	Radio Frequency
ROM	Read Only Memory
RXD	Received Data
SDIS	Standard Digital Interface System
SP	Spare
SRQ	Service Request
STD	Standard Digital Interface
sw	switch
Sync	Synchronization/ed
TD	Terminal Board
TCASS	Tape Cassette
TDIN	Tape Direction In
TDOUT	Tape Direction Out
TLDR	Tape Leader
TP	Test Point
T/R	Transmitter/Receiver
TRWD	Tape Rewind
TSLW	Tape Slew
TSTP	Tape Stop
TTL	Transistor - Transistor Logic
TTY	Teletypewriter
TWRT	Tape Write
TXD	Transmit Data
UD	User Data
µSec	Microsecond
UUT	Unit Under Test
V	Volt
VAC	Volts Alternating Current
VCO	Voltage Controlled Oscillator
VDC	Volts Direct Current
VHF	Very High Frequncy
VHS	Very High Speed
Vp-p	Voltage peak to peak
VS&F	Voltage Selecting and Fused
VSWR	Voltage Standing Wave Ratio
W	Watt
WR	Write
XSTAT	External Status
ZC/TO	Zero Count/Time Out
%	Percent
Ω	Ohm
Φ	Clock

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