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COMMTECH

FASTCOM™ ADAPTERS



FASTCOM™: ESCC-PCI-335

High Speed Dual Channel Sync/Async Interface for Universal PCI Bus
Hardware Reference Manual

CERTIFIED

Commtech, Inc.

COMMTECH

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REVISION NOTES

REVISION	PAGE NUMBER	CHANGES MADE
1.0	All	Created manual

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Information Technology Equipment

The Company COMMTECH, INC. declares under its own and full responsibility that the product

" Fastcom: ESCC-PCI-335 - Revision 3.0 "

on which is attached this Certificate is compliant to the "89/336/EEC" Directive, amended by 92/31/EEC and 93/88/EEC.

[ ] The product identified above complies with the requirements of the above EU Directive by meeting the following standards:

- EN 50081-1 (1992) EMC Generic Emission Standard - Part 1, Residential, Commercial and Light Industry
  - EN 55022 (1995), CISPR 22 (1993) Limits and Methods of Measurement of Radio Disturbance Characteristics of Information Technology Equipment, 30 MHz - 1 GHz, Class B Limits

- EN 50082-1 (1992) EMC Generic Immunity Standard - Part 1, Residential, Commercial and Light Industry
  - IEC 801-2 (1984), Method of Evaluating Susceptibility to Electrostatic Discharge, Level 4
  - IEC 801-3 (1984), Radiated Electromagnetic field Requirements, Level 3
  - IEC 801-4 (1988), Electrical Fast Transient/Burst Requirements, Level 2

Products listed on this declaration are exempt from the requirements of the 73/23/EEC directive due to the input voltage specification as stated in Article 1 of the directive.

The technical documentation required to demonstrate that this product meets the requirements of the EMC Directive has been compiled by the signatory below and is available for inspection by the relevant enforcement authorities.

In WICHITA, KS on October 31st of 2003

COMMTECH™
COMMUNICATION • TECHNOLOGIES

Glen R. Alvis

Mr. Glen R. Alvis
Chief Engineer

CE

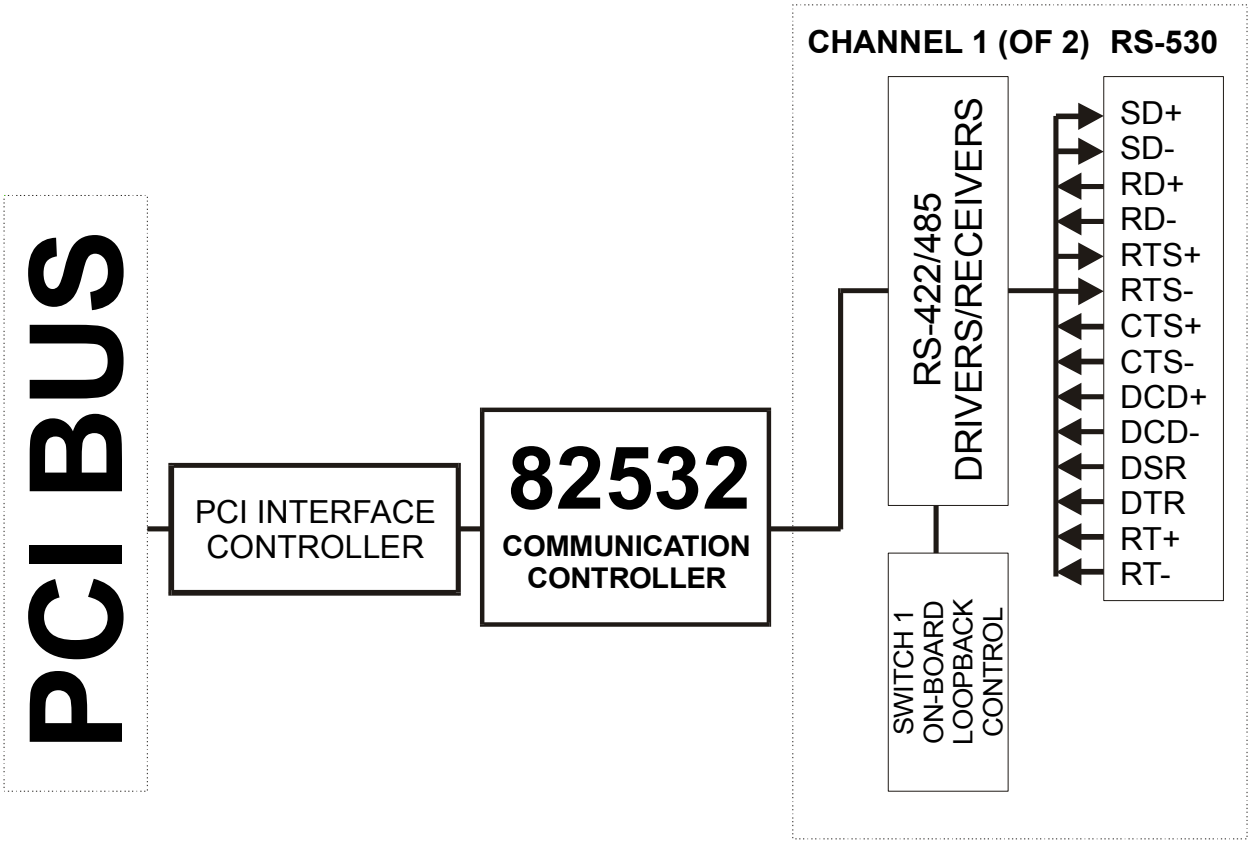
INTRODUCTION

Designed to comply with the latest PCI specifications, the FASTCOM: ESCC-PCI-335 Universal PCI adapter will operate in both 5V and 3.3V PCI slots. This means the card will work in the high speed PCI-X slots commonly found in most new servers, as well as the standard PCI slots in desktop PC's. This flexibility allows for a single serial interface board to be used across a wide range of different types of computers, including both current and future computing systems.

The new FASTCOM: ESCC-PCI-335 is a very high speed, dual channel, synchronous/asynchronous serial communications adapter based upon the Siemens 82532 Enhanced Serial Communication Controller (ESCC), and is designed for use in the PCI bus. It is designed to support data rates up to 10 Mbits/second (maximum data rates are affected by many factors, including computer performance, cable quality, and software overhead), and to reduce the hardware and software overhead needed for serial communications. Each sync/async channel on the FASTCOM: ESCC-PCI-335 has its own DPLL encoder/decoder and programmable protocol support. In addition, a built-in 64 byte FIFO provides the FASTCOM: ESCC-PCI-335 with a very high throughput as well as requiring less system CPU time than any other HDLC adapter. The FASTCOM: ESCC-PCI-335 directly supports HDLC, X.25 LAP B, ISDN LAP D, SDLC, ASYNC, and BISYNC protocols, and features a high speed RS-422/RS-485 interface conforming to ANSI/EIA/TIA-530-A-1992 configuration (RS-530). HDLC features include choice of CRC polynomial (CRC-CCITT or CRC-32), expanded line encoding methods (FM and Manchester), and preamble transmission.

Many engineers have avoided using synchronous communication adapters because of their programming complexity. The FASTCOM: ESCC-PCI-335 provides high-speed data communications to designers and engineers, while *greatly reducing development time* and system complexity.

The following diagram illustrates the basic structure of the FASTCOM: ESCC-PCI-335:



SPECIFICATIONS:

COMMUNICATION CONTROLLER:	SIEMENS 82532
DRIVERS/RECEIVERS:	RS-422/RS-485
CONNECTOR CONFIGURATION:	ANSI/EIA/TIA-530-A-1992
POWER REQUIREMENTS:	+5V @ 800mA (typical)
BUS INTERFACE:	PCI version 2.3
ENVIRONMENT:	
Operating Temperature Range:	0 to 70 C
Humidity:	0 to 90% (non-condensing)

FEATURES:

High speed, up to 10Mbits/s
Much easier to program and use than other HDLC adapters
Supports HDLC, SDLC, ISDN LAP D, and X.25 LAP B, ASYNC, BISYNC

Drivers: RS-422/RS-485 multi-drop

Excellent noise rejection, cable lengths up to 4000 feet
Use low cost "twisted pair" cable
RS-485 mode
Up to 32 FASTCOM: ESCC-PCI-335 adapters can share the same "twisted pair"
Driver control is automatic (via the RTS line)

Serial Interface:

Internal or External Clock Source
Asynchronous, Monosync/Bisync, and HDLC/SDLC data formatting.
1X (isosynchronous) or 16X oversampling for Asynchronous format
Different modes of data encoding (NRZ,NRZI,FM0,FM1,Manchester)
CRC-CCITT or CRC-32 (for HDLC/SDLC modes)
CRC-CCITT or CRC-16 (for BISYNC mode)
Modem control lines (RTS, CTS, DTR, DCD, DSR)
Collision resolution
Programmable bit inversion
Transparent RD/SD of data bytes without HDLC framing

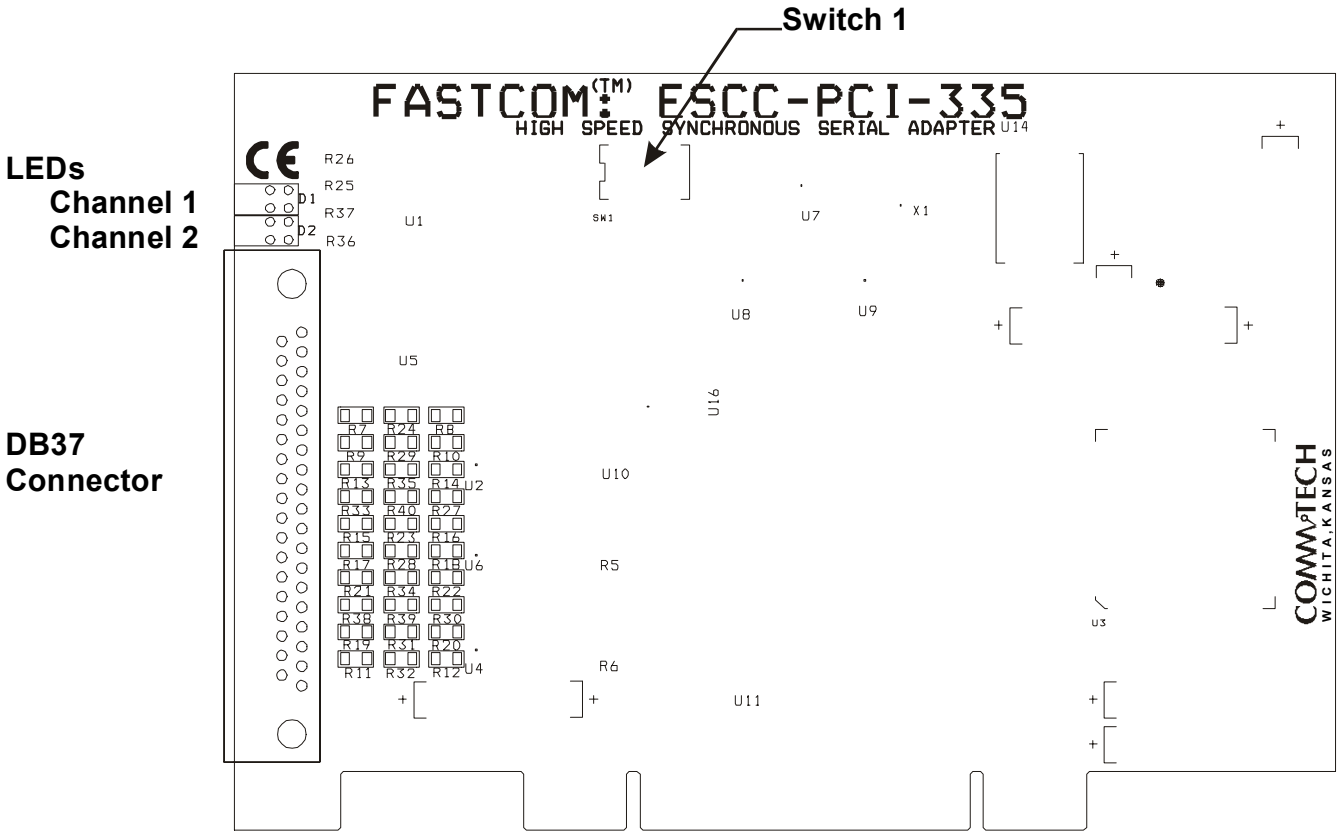
Protocol Support (HDLC/SDLC):

Types of protocol support - Automatic, Manual, Transparent
Handling of bit-oriented functions in all modes
Handling of I and S frames in Auto mode
Modulo 8 and 128 operation

64 byte FIFOs per direction
Storage of up to 17 short received frames

FASTCOM: ESCC-PCI-335

BOARD LAYOUT



TERMINATION REFERENCE:

	SIGNAL	REF	PULLUP	PULLDOWN
CHANNEL 1:	RD	R24	R8	R7
	CTS	R29	R10	R9
	ST	R35	R14	R13
	DCD	R40	R27	R33
	RT	R32	R12	R11
CHANNEL 2:	RD	R23	R16	R15
	CTS	R28	R18	R17
	ST	R34	R22	R21
	DCD	R39	R30	R38
	RT	R31	R20	R19

LED INDICATORS:

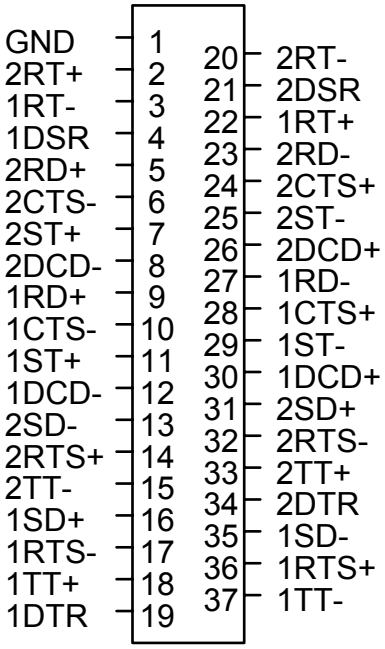
RED	TRANSMIT ACTIVE
GREEN	RECEIVE ACTIVE

PACKING LIST:

FASTCOM: ESCC-PCI-335 CARD
CABLE ASSEMBLY
FASTCOM CD

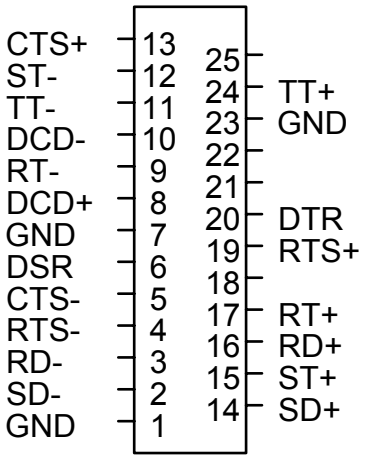
If an omission has been made, please call technical support for a replacement.

FASTCOM: ESCC-PCI-335
DB37 FEMALE CONNECTOR PIN DESCRIPTION



The cable provided splits each channel from this DB37 to individual RS-530 pin out DB25 male connectors. The DB25 pin outs are shown on the next page.

FASTCOM: ESCC-PCI-335
DB25 CABLE CONNECTOR
DESCRIPTION (RS-530 pin out)



PIN DESCRIPTIONS

PIN#	DESCRIPTION	422 TYPE	CONNECTED TO	530 CIRCUIT
1	SHIELD/GROUND		GND	
7	SIGNAL/GROUND		GND	AB
2	TRANSMIT DATA	A	SD-	BA
14	TRANSMIT DATA	B	SD+	BA
3	RECEIVE DATA	A	RD-	BB
16	RECEIVE DATA	B	RD+	BB
4	REQUEST TO SEND	A	RTS-	CA
19	REQUEST TO SEND	B	RTS+	CA
5	CLEAR TO SEND	A	CTS-	CB
13	CLEAR TO SEND	B	CTS+	CB

The RS-422 "A" side is 0 volts when a "1" is on the line (A side is the negative terminal of the 422 driver).

6	DATA SET READY	DSR	INPUT	
20	DATA TERMINAL READY	DTR	OUTPUT	

CLOCK SIGNALS

PIN#	DESCRIPTION	422 TYPE	CONNECTED TO	530 CIRCUIT
8	DATA CARRIER DETECT	A	DCD+	CF
10	DATA CARRIER DETECT	B	DCD-	CF
24	TRANSMIT CLOCK OUT	A	TT+	DA
11	TRANSMIT CLOCK OUT	B	TT-	DA
17	RECEIVE CLOCK IN	A	RT+	DD
9	RECEIVE CLOCK IN	B	RT-	DD
15	TRANSMIT CLOCK IN	A	ST+	DB
12	TRANSMIT CLOCK IN	B	ST-	DB

These are *opposite* of RS-422 in order to invert the signals going to the FASTCOM: ESCC-PCI-335. The 530 specification states that data is valid on the rising edge of the clock (0->1 transition), whereas the FASTCOM: ESCC-PCI-335 clocks on the falling edge (1->0 transition). DCD is inverted because a "1" at DCD means active to the FASTCOM: ESCC-PCI-335, but the 530 specification requires DCD to be "0" to be active.

On the same note, if you are using Clock Mode 1 and you are not using DCD, it must be strapped Active to allow data reception.

NOTE: The DTR and DSR signals are single ended (unbalanced) as required by ANSI/EIA/TIA-530 specifications.

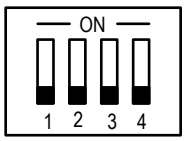
INSTALLATION

Important: Observe Electrostatic Discharge (ESD) precautions when handling the FASTCOM: ESCC-PCI-335 board.

1. Unpack the FASTCOM: ESCC-PCI-335. Keep the box and static bag for warranty repair returns.
2. Check the switches to be sure that they are set as illustrated below (Factory Switch Settings).
3. Select an open PCI slot in your PC.
4. After removing the blank bracket from your PC, install the FASTCOM: ESCC-PCI-335 in the PC by pressing it firmly into the slot. Install the bracket screw to hold it firmly in place.
5. Re-install the cover on your PC.

FACTORY SWITCH SETTINGS

ON-BOARD LOOPBACK CONTROL (SW1) NO LOOPBACK

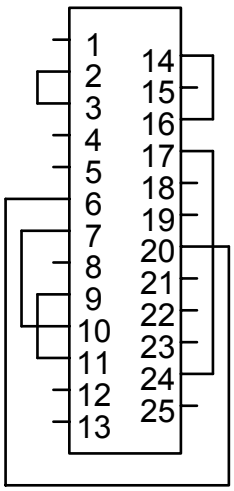


SOFTWARE INSTALLATION

Select the link above to open the Installation Manual. Under FASTCOM: ESCC-PCI-335, select your operating system and follow the instructions. When you are finished, select FASTCOM: ESCC-PCI-335 from the list at the end of the FASTCOM: ESCC-PCI-335 section to return to this manual.

TESTING THE INSTALLATION

To fully test the installation of your FASTCOM: ESCC-PCI-335, you will need to build a "loop back plug". Materials needed are a DB25 female receptacle (solder-cup style) and a few short pieces of 20 or 24 AWG stranded wire. Jumper the pins together on the DB25 as illustrated:

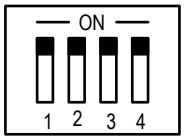


SIGNALS

2	SD-
3	RD-
6	DSR
7	GND
9	RT-
10	DCD-
11	TT-
14	SD+
16	RD+
17	RT+
20	DTR
24	TT+

NOTE: You can also create a "loop back" condition on the FASTCOM: ESCC-PCI-335 without building an adapter plug by setting the On-Board Loopback Control Switch (SW1) as follows:

485 CONTROL



Both ESCC-PCI channels are looped back

However, we recommend that you make the "loop back" plug for two reasons: one, the clock circuit can be tested and, two, you will not have to change switch settings from the factory defaults. In addition, our technical support engineers can better service your technical questions if you have made the "loop back" plug. **If you have made the loop back plug, do not change the setting of the Mode switch.**

FASTCOM: ESCC-PCI-335 WINDOWS 2000/XP TEST

1. Attach a loopback plug to the cable #1 (ESCC0, port 0)
2. From the Start button menu, select Run
3. Enter:
   D:\fastcom_disks\esccp\nt\escctest\esccptest 0 h
   Click the OK button
4. You should see:

   Created esccdrv--ESCC0
   ESCC 82532 version status:82
   # receive buffers ready:0
   resetting
   HDLC settings
   SETTINGS SUCCESSFUL:184
   DTR not SET
   DSR not SET
   DTR SET
   DSR SET[1]
   waiting for a key
   read thread started
   status thread started

   [1] The DSR SET could be a DSR not SET if you do not have a DTR -> DSR loopback wired

5. Press the letter "U" on the keyboard. You should see:

   WRITEFILE esccdrv1024
   TX returned TRUE

waiting for a key
STATUS, Receive Frame Start
STATUS, All Sent
received 1025 bytes:
UUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUUU

Enter: D:\fastcom_disks\esccp\nt\esccpmfc\esccpmfc
Click OK

2. From the main menu select Options -> Port
   Enter 0, click OK
   (this selects port 0, make sure you have your loopback on cable #1)

3. From the main menu select Options -> Settings
   (the settings dialog will open)
   Click OK
   (the TXD status indicator should turn green)

4. Type a short message on the keyboard, press enter to send it.

The message you typed should appear in the lower window, and the RXD, RFS, and ALLS status indicators should turn green (if it was a short message (<32 bytes or so); a long message will likely only get an RXD status indicator).

If when running any of these tests you do not get the expected result, check your loopback plug. Next, check to make sure that the driver loaded and is running. Watch the BIOS startup screen to verify that the system recognized that the card is present (installed PCI devices are displayed on some startup sequences). The FASTCOM: ESCC-PCI-335 will be listed as a "Simple Communication Controller". Verify that it is listed, and that the BIOS assigned an IRQ to the device.

Troubleshooting tips:

1. Incorrect loopback, faulty wiring
2. Board not inserted fully
3. Driver not running/installed

SWITCH DESCRIPTIONS

There is one dip switch on the FASTCOM: ESCC-PCI-335, labeled SW1 (See Board Layout Illustration for location).

SWITCH 1, ON-BOARD LOOPBACK CONTROL

POSITION	DESCRIPTION
1	TXD+ to RXD+ loopback for RS-485 channel 0
2	TXD- to RXD- loopback for RS-485 channel 0
3	TXD+ to RXD+ loopback for RS-485 channel 1
4	TXD- to RXD- loopback for RS-485 channel 1

PROGRAMMING

Refer to the enclosed FASTCOM CD for example programs, product updates, and software for testing your installation. Refer to the Siemens SAB 82532 User's Manual for register information.

NOTES

Always set the SAB 82532 port configuration register (PCR) to E0H.
Always set the SAB 82532 interrupt port configuration (IPC) to 03H.
Always set the SAB 82532 CCR1 ODS bit to 1.

SAB 82532 PVR Register

The 82532 has an 8 bit I/O port (PVR) that has the following functions on the FASTCOM: ESCC-PCI-335.

Bit:: 0 - Clock generator data
1 - Clock generator clock
2 - Clock generator strobe
3 - DTR channel 1 (output)
4 - DTR channel 2 (output)
5 - DSR channel 1 (input)
6 - DSR channel 2 (input)
7 - N/C

RS-422 / RS-485

Most engineers have worked with RS-232 devices at least once in their career. If you have never worked with RS-422 or RS-485 devices, you will be pleased to know that working with the FASTCOM: ESCC-PCI-335 is not much different from working with an RS-232 device.

The RS-422 standard was developed to correct some of the deficiencies of RS-232. In commercial and industrial applications, RS-232 has some significant problems. First, the cable length between RS-232 devices must be short (usually less than 50 feet at 9600 Baud). Second, many RS-232 errors are the result of cables picking up normal industrial electrical noises such as fluorescent lights, motors, transformers, and other EMF sources. Third, RS-232 data rates are functionally limited to 19.2K Baud. On the other hand, the newer RS-422 standard makes cable lengths up to 5000 feet possible and is highly immune to most industrial noises. Data rates are also improved -- the FASTCOM: ESCC-PCI-335 features data rates up to 10 Mega Baud. These improvements were made possible by differentially driving and receiving the data as opposed to the single ended method employed by the RS-232 standard. With the RS-422 standard, the transmit signal (TX in RS-232) is a differential signal consisting of SD+ and SD-; the receive signal (RX in RS-232) consists of RD+ and RD-.

Another draw back of RS-232 is that more than two devices cannot share a single cable. This is also true of RS-422, and that's why the RS-485 standard was developed. RS-485 offers all of the benefits of RS-422 and also allows multiple units (up to 32) to share the same twisted pair. RS-485 is often referred to as a "multi-drop" or "two-wire, half duplex" network because the drivers (transmitters) and receivers share the same two lines. In fact, up to 32 stations can share the same "twisted pair". In order for an RS-485 system to work, only one driver (transmitter) can occupy the network at a time. This means that each station on the network must control the enabling/disabling of their drivers in order to avoid network conflicts. If two drivers engage the network at the same time, data from both will be corrupted. In RS-485 mode, the receivers are always enabled.

For a more detailed description of RS-422 and RS-485, we recommend the following references:

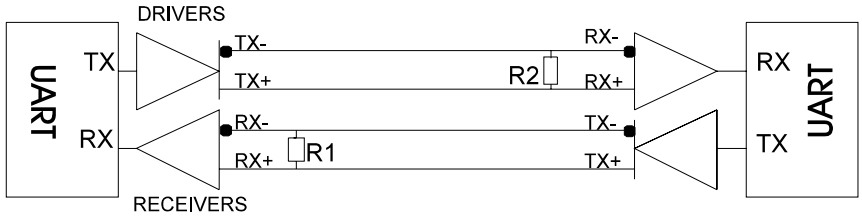
> LINEAR AND INTERFACE CIRCUITS APPLICATIONS, Volume 2: Line Circuits, Display Drivers. By D.E. Pippenger and E. J. Tobaben. Published 1985 by Texas Instruments. ISBN-0-89512-185-9
>
> Note: This book may be difficult to find in a bookstore. The best place to get it is directly from Texas Instruments or from one their component dealers. Publication # SLYA002.
>
> "Driver/Receiver Family Extends Data-Link Performance", ELECTRONIC PRODUCTS, January 15, 1985. By Dale Pippenger and Joe Miller

TERMINATION RESISTANCE

In both the RS-422 and the RS-485 mode, the receiver end of the cable between two stations must be terminated with a resistor equal to the characteristic impedance of the wire. This is to prevent signal reflections in the wire and to improve noise rejection. However, **you do not need to add a terminator resistor to your cables when you use the FASTCOM: ESCC-PCI-335. The termination resistance is built in.** We have installed a terminator resistor for each receiver: between each RD+ and RD- and between CTS+ and CTS- for each channel.

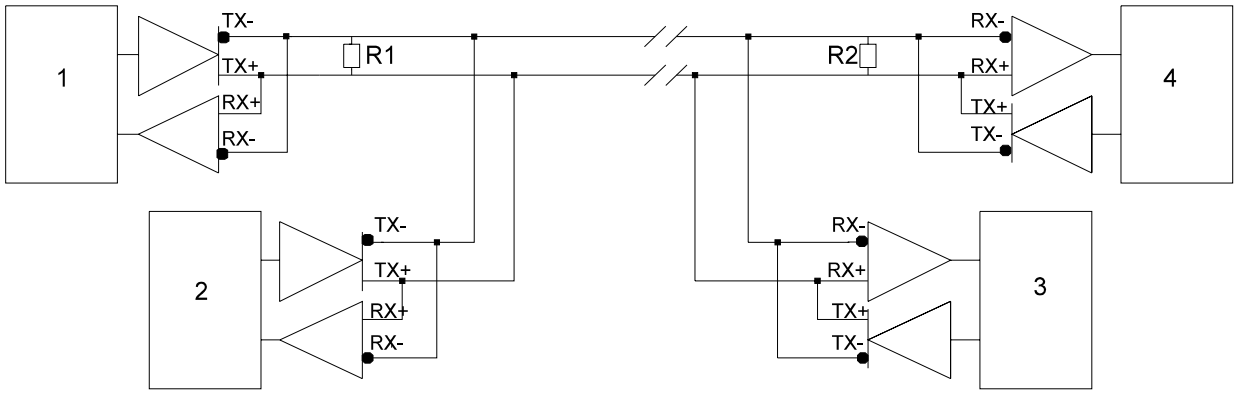
If you are using the FASTCOM: ESCC-PCI-335 in a multi-drop network, the termination resistor should be removed from all units except the first and last (see the RS-485 illustration below). Call for technical support if you need to modify the resistor. You may also order the FASTCOM: ESCC-PCI-335 without the termination resistor installed (it is easier to add the resistor than to remove it). Observe the resistors in the following drawings and remember that they are built into the FASTCOM: ESCC-PCI-335:

Typical RS-422



R1 & R2 -- Line Termination (100 Ohms)

Typical RS-485



PROGRAMMABLE CLOCK GENERATOR

The FASTCOM: ESCC-PCI-335 features a programmable clock generator, which offers a fully user-programmable phase-locked loop in a single 16-pin package. The output may be changed "on the fly" to any desired frequency value between 6-200 MHz (the FASTCOM: ESCC-PCI-335 maximum is 33 MHz). The ability to dynamically change the output frequency adds a whole new degree of freedom for the designer.

FEATURES

- Clock outputs ranging from 6 to 200 MHz (the FASTCOM: ESCC-PCI-335 maximum is 33 MHz)
- Phase-Locked Loop oscillator input derived from external reference clock (18.432 MHz on the FASTCOM: ESCC-PCI-335)
- Three-State output control disables output for test purposes
- Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters
- Low power consumption makes device ideal for power- and space-critical applications
- Programmable using the FASTCOM: ESCC-PCI-335 PVR register, bits 0 and 1 (see page 17)
- 5V operation
- High-speed CMOS technology

PROGRAMMING NOTE

Revision 3.2A of the Siemens 82532 utilizes both standard and enhanced modes of the Baud Rate Generator Register (BGR). In standard mode, the following formula is used to calculate the divisor for baud rate generation:

k = (N+1) * 2

The following hexadecimal values of N are equivalent to N equaling zero:

0x000	0x100	0x200	0x300
0x040	0x140	0x240	0x340
0x080	0x180	0x280	0x380
0x0C0	0x1C0	0x2C0	0x3C0

This is a known bug of the 82532.

DETERMINING AND SELECTING BAUD RATES

Selecting the bit rate can either be very easy or quite complicated, depending on a number of factors. The best place to start is to determine the big picture (broad perspective) and narrow down the options using the various constraints that the hardware imposes.

There are four basic things that make up what the actual bitrate will be. They are:

1. Register settings of the 82532 chip. These include:
   A. Operating mode (HDLC, Bisync, Async)
      1. If async is used is it truly async (oversampled BCR=1), or
      2. isosynchronous (async format with no oversampling).
   B. Clock mode (internal or external clocks)
      1. If internal clocks, does it use clock recovery (DPLL)
      2. If BGR is used is the BDF bit 1 or 0.
2. The setting of the clock generator that feeds the OSC input to the 82532 (only a factor if an internal clock mode is used, i.e., BGR or DPLL is involved).
3. The revision of the ESCC 82532 chip (silicon)
   A. The rev 3.2 silicon incorporates an enhanced baud rate mode.

We will start with the simplest case. If you are using the Asynchronous data mode, then the most likely clock mode that you should use is 7b. It is possible to use the other clock modes; however, mode 7b is the most straightforward to work with. The bitrate will be determined by the output of the baud rate generator. The baud rate generator is clocked by the OSC input (which is set by the programmable clock generator). So you have:

If you are not using oversampling (BCR = 0) the formula is:

bitrate = (input clock / BGR)

If you are using oversampling (BCR = 1 (the normal case for async)) the formula is:

bitrate = (input clock / BGR)/16

If BDF = 0	then BGR = 1
If BDF = 1	then BGR = (N+1)*2
If BDF = 1 and EBRG = 1	then BGR = (n+1)*2^m

The BCR bit is in CCR1 (bit 3)
The BDF bit is in CCR2 (bit 5)
The EGRG bit is in CCR4 (bit 6)
N = (CCR2&0xC0)<<2) + BGR, or if you prefer

	Most significant bit..... Least significant bit
n =	BGR bit 5, BGR bit 4, BGR bit 3, BGR bit 2, BGR bit 1, BGR bit 0
m =	CCR2 8, CCR2 7, BGR 7, BGR 6
N =	CCR2 8, CCR2 7, BGR 7, BGR 6, BGR 5, BGR 4, BGR 3, BGR 2, BGR 1, BGR 0

Some things to keep in mind:

The range on the programmable clock generator output is 6 to 200MHz.
The usable range if the master clock enable bit is clear (not using master clock) is 6 to 33Mhz. If the master clock is set, then the range is from 6 to 10MHz.
Using master clock mode also places a restriction on the ratio of receive/transmit clock to the master clock frequency (as per note 2 on page 84 of the 82532 data sheet).
Fmaster/Ftransmit >= 2.5
Freceive/Fmaster <3 or 1.5 (if CCR3 bit 4 (RADD) is set and an address recognition mode is used in HDLC).

To use Master clock mode or not to use Master clock mode; that is the question.

The 82532 operating in standard (non-master clock) mode uses the transmit clock source (refer to table 5 page 84 of the data sheet) to run the internal timing of the chip. If your transmit clock source is running very slow or it is not running continuously (if external clock is supplied), then it is a good idea to switch to master clock mode. Each command issued to the 82532 (any write to the CMDR register) can take up to 2.5 clocks to complete. If the clock is very slow or stops from time to time, this can be a significant amount of time and allows for the possibility of a command being lost (written but not executed, because a previous command is not complete). If your baud rate is slow (<1MHz) or you are using a gated external clock, you should use master clock mode to allow the PC interface to the 82532 to continue to execute quickly. If this mode is used, then the OSC input must be less than 10MHz (the speed rating of the internals of the 82532). If you have a 82532 rev 3.x (silicon), then you can cause the master clock to be OSC/4 by setting CCR4 bit 7 (MCK4), thus allowing the 10MHz restriction to be lifted.

If you are using a clock mode that uses external clocks, you should respect the restriction on the ratio of receive to transmit clock frequency given in note 2 of table 5 (Freceive/Ftransmit <3 or 1.5).

If you are running in not extended baud rate mode, do not set BGR bits 5-0 to all = 0, or the chip will assume that all of the BGR bits are 0. This is a glitch in the 82532 rev 3.2 and makes the following values for N identical:

0x000,0x040,0x080,0x0C0
0x100,0x140,0x180,0x1C0
0x200,0x240,0x280,0x2C0
0x300,0x340,0x380,0x3C0

Setting the baud rate generator to any of these values will produce the same affect as setting it to 0x000.

If you use the Enhanced baud rate generator and set m = 0, the clock output will be asymmetric (non 50/50 duty cycle).

An important fact about the clock generator

There is only one programmable clock generator, and only 1 OSC input to the 82532 chip. The clock generator can be programmed from either channel (ESCC0 or ESCC1), but it programs the same part. The result is that while the baud rate generators are unique on a per channel basis, the OSC input is not (i.e., the baud rate generators are independent, but the clock that feeds them is the same). If you change the clock generator output you will change the input clock to both channels. The practical thing to note about this is that if you have multiple baud rates that must be generated on multiple channels, you should select the input clock such that all baud rates can be derived from one clock value. *Changing the clock generator output will affect the baud rates of both channels (ESCC0, ESCC1)!!!!*

If you are using HDLC or Bisync as a data format, there is not a BCR setting (no oversampling). However, if you select a clock mode that uses the DPLL as a source, it will effectively add a divide by 16 to your function.

Selecting the appropriate clock mode is a matter of identifying what clock signals are available external to the Fastcom card, and what clock signals are required by the external device. The simplest mode is using external clocks only (mode 0a); in this mode both the receive and transmit timing are taken from the connector (RT for receive, ST for transmit). The rest of the modes are a mix of external signals and internally generated clocks/clock recovery. The DPLL modes only operate up to 2 MHz. If the bitrate is above that, you should use a non-DPLL mode.

The bitrate functions are similar to the async case:

If you are not using a clock mode that uses the DPLL, the formula is:

bitrate = (input clock / BGR)

If you are using the DPLL, the formula is:

bitrate = (input clock / BGR)/16

The input clock will depend on the clock mode. It is usually either the OSC input or the RXCLK (RT+/-) input (see table 5 page 84 of the 82532 data sheet).

If BDF = 1	BGR = 1
If BDF = 0	BGR = (N+1)*2
If BDF = 0 and EBRG = 1	BGR = (n+1)*2^m (V 3.x of the 82532 silicon only)

The BDF bit is in CCR2 (bit 5)
N = (CCR2&0xC0)<<2) + BGR, or if you prefer

	Most significant ..... Least significant bit
m =	CCR2 bit 8,CCR2 bit 7, BGR bit 7, BGR bit 6
n =	BGR 5, BGR 4, BGR 3, BGR 2, BGR 1, BGR 0
N =	CCR2 8,CCR2 7, BGR 7, BGR 6, BGR 5, BGR 4, BGR 3, BGR 2, BGR 1, BGR 0

If you are using the DPLL, you should try to set its input clock to be as close to the actual bit frequency as possible. This will allow for optimal clock recovery. Also, clock recovery relies on edges in the data stream; if you transmit long segments of 0s or 1s using an encoding method that produces no edges, the results will be non-optimal. The ideal encoding for clock recovery is Manchester or a non '1' idle pattern (i.e., constant flag sequences on idle if HDLC is used, etc.).

Let's start with something easy

Let's say that you want to set up an ESCC channel to run in HDLC mode at 19200 bps, that the device in question supplies a clock with its data (receive clock), and that we need to generate (transmit) a clock that matches our transmitted data. To achieve this we should set the 82532 to clock mode 0b. Set the mode switch position 5 (or 7) to on, enabling the txclk output driver (selecting txclk as an output on TT+/-). The baudrate function bitrate = input clock / (N+1)*2 will be used. If there are no other constraints other than operating one channel at 19200 bps, then we can select both the input clock and N arbitrarily, so long as we do not violate any of the notes.

So, by selecting a value for input clock that is less than 10 MHz (since the bit rate is slow we will want to use master clock mode, which will require a 10 MHz or less clock), we can then calculate the value needed for N to get a 19200 bps output. I will pick 7.372800 MHz for the input clock. To set this frequency, run:

```
setclock.exe 0 7372800
```

Calling the IOCTL_ESCCDRV_SET_CLOCK_FREQ ioctl function with 7372800 as the desired frequency will also get us an input clock of 7.3728 MHz (referred to as OSC in table 5).

Then solving for N we get:

```
19200 = 7.3728E6/((N+1)*2)
N = 191 = 0x0BF
```

Checking the notes to make sure we did not violate anything:

Fm/Fx = 7.3728E6/19200 = 384 > 2.5 (we are OK on this one)

Fr/Fm = rxclk input / 7.3728E6 < 3 (assuming a 19200 clock input) 19200/7.3728E6 = .0026 < 3 (we are OK on this one)

(0x0BF & 0x3f) <= 0 (checking the value of n to make sure it isn't forced to zero due to the glitch in the 82532)

Important Register Settings

MODE = 0x88

This sets the 82532 in transparent HDLC mode 0. This will use a frame structure as:
0x7E | data | CRC | CRC | 0x7E
No address recognition is used
The timer is in external mode
RTS is handled by the 82532 (active while transmitting)
Timer resolution is 32768 clocks

CCR0 = 0xC0

This sets the 82532 in power up mode
Master clock mode is enabled
NRZ is the encoding type
HDLC mode is selected

CCR1 = 0x10

This selects clock mode 0(b)
The tx pin is using a push-pull output (required)
Time fill is all '1's (idle pattern = 0xff)

CCR2 = 0x38

This selects the BGR = (N+1)*2 divisor
Selects txclk to be an output
Selects clock mode 0b (the B part)
Enables the CRC-CCITT polynomial

CCR3 = 0x00

No preamble output
CRC reset level = 0xffff
CRC is in use (both transmit and receive), not including CRC in received Data (not returned to the user)
Not using extended window for DPLL

CCR4 = 0x00

Not using master clock/4
Not using enhanced baud rate generator
FIFO threshold is 32 bytes (mandatory for NT driver in HDLC mode)

BGR = 0xBF

This sets the output clock rate to 19200 (given that the input clock was previously set to 7.3728 MHz, and the above registers are set as shown)

CCR0, CCR1, CCR4 and BGR are the most critical registers that effect the bitrate, the rest are shown for completeness, and, depending on the system, you can easily change some parameters without affecting the bitrate (i.e., line encoding, address recognition, crc type, etc.).

And now for something a bit more difficult:

Let's say that you want to run one channel asynchronously at 38400 bps, and the second channel synchronously using HDLC at 2 Mbps. How would you go about it?

Start with the fastest bit rate and determine if there is an external clock that is received with that data or if the clock must be recovered (DPLL mode). Let's say that you want to recover the clock from the data (there are no clock lines in the system), and that the data is Manchester encoded. To get a 2 Mbps clock rate using a DPLL we will need to use the bitrate = (input clock/1)/16 function. This will require a 32 MHz input clock. To get this input

clock run:

setclock.exe 0 32000000

using the following register settings:

MODE = 0x88
CCR0 = 0x98
CCR1 = 0x16
CCR2 = 0x18
CCR3 = 0x00
CCR4 = 0x00

The receive source will be recovered from the data stream. The transmit source will be the BGR/16 output.

Now for the async channel. We are locked into the 32 MHz input clock, so we will try to find a value for N that gets our desired 38400 bps:
38400 = (32E6/16)/((N+1)*2)
N = 25.04 (we cannot attain non-integer values for N).

If we use N = 25 we would get:
bitrate = (32E6/16)/(25+1)*2 = 38462 bps

If we use N = 26 we would get:
bitrate = (32E6/16)/(26+1)*2 = 37037 bps

Using the closest value and setting the registers to
MODE = 0x08,
CCR0 = 0xC3,
CCR1 = 0x1F,
CCR2 = 0x38,
CCR3 = 0x00,
CCR4 = 0x80, and
BGR = 0x19
will yield an asynchronous data format (with 16X oversampling) at about 38400 bps.

If later you decide that you need to get 115200 bps on the async channel you will find:
115200 = (32E6/16)/((N+1)*2)
N = 7.68

Using N = 7
bitrate = (32E6/16)/((7+1)*2) = 125000 bps

Using N = 8
bitrate = (32E6/16)/((8+1)*2) = 111111 bps

The ideal situation would be to adjust the 32 MHz clock such that the deviation between the desired and actual rates is spread between both channels (with the DPLL recovering the clock, the actual clock that feeds it is not as critical as a clock mode that uses the clock directly).

Clock modes 0b, 3b, 4, and 7b are more sensitive to the selected rate in synchronous modes, as there is no oversampling. The rate you select is the rate you will get, whereas oversampling modes (using the DPLL or ASYNC BCR) are more tolerant to differences between the rate you set and the rate you want.

FASTCOM: ESCC-PCI-335 BOARD-SPECIFIC REGISTER

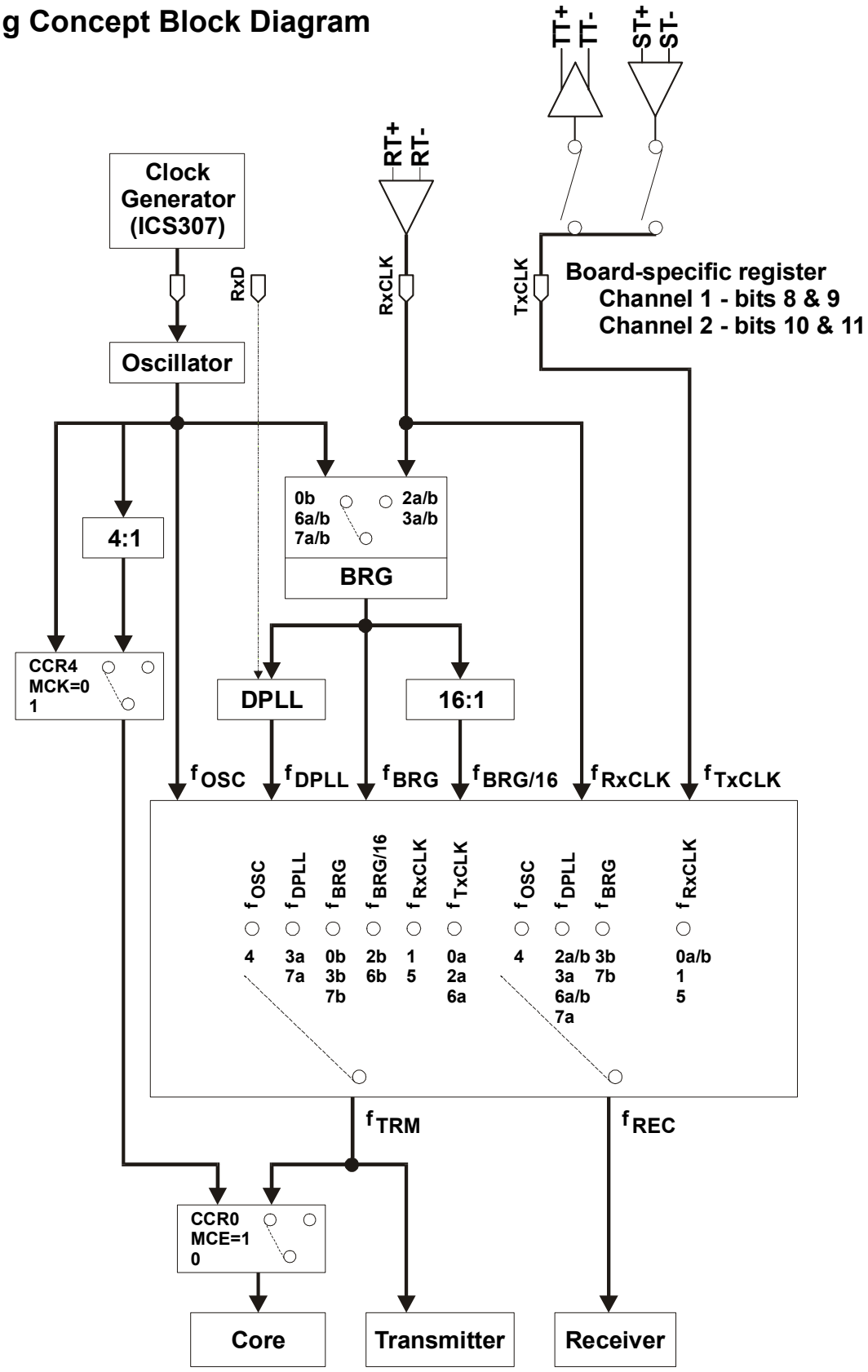
First I/O Range

	BIT NUMBER	SIGNAL	SETTINGS
Channel 1	0	Receive echo control	0 = RTS controls RD 1 = RD always on
	1	SD 485 control	0 = /RTS controls SD 1 = SD always on
	2	TT 485 control	0 = /RTS controls TT 1 = TT always on
	3	CTS disable	0 = CTS always active 1 = CTS from connector
Channel 2	4	Receive echo control	0 = RTS controls RD 1 = RD always on
	5	SD 485 control	0 = /RTS controls SD 1 = SD always on
	6	TT 485 control	0 = /RTS controls TT 1 = TT always on
	7	CTS disable	0 = CTS always active 1 = CTS from connector
Channel 1	8	Txclk = ST	0 = txclk connected to ST input 1 = txclk not connected to ST input
	9	Txclk = TT	0 = txclk connected to TT output 1 = txclk not connected to TT output
Channel 2	10	Txclk = ST	0 = txclk connected to ST input 1 = txclk not connected to ST input
	11	Txclk = TT	0 = txclk connected to TT output 1 = txclk not connected to TT output

Second I/O Range

The second I/O range is the 82532 registers mapped flat.

Clocking Concept Block Diagram



TECHNICAL SUPPORT

All products manufactured by Commtech are warranted against defective materials and workmanship for the lifetime of the product. This warranty is available only to the original purchaser. Any product found to be defective will, at the option of Commtech, be repaired or replaced with no charge for labor or parts not excluded by the warranty. This warranty does not apply to any products that have been subjected to misuse, abuse, or accident or as a result of service or modification by anyone other than Commtech. In no case shall Commtech liability exceed the original product purchase price.

If any Commtech product is damaged such that it cannot be repaired, you can return it to Commtech for replacement under our *Non-Repairable Replacement* policy, regardless of the cause of damage. Commtech will replace the unit at 60% of the then-current list price.

Commtech provides extensive technical support and application suggestions. Most of the problems that occur with the FASTCOM: ESCC-PCI-335 can be corrected by double-checking the switch positions, your cables and your program. We recommend that you build the loop back plug that is described in the Programming section of this manual. With that plug, you can quickly isolate the problem to the board, cables, or software.

If you still have unresolved questions, use the following procedure to get technical support:

Ask for technical support for the FASTCOM: ESCC-PCI-335. Be ready to describe the problem, your computer system, your application, and your software.

If necessary, our staff will give you an RMA number (Return Material Authorization). Use this number on the mailing label and in all references to your board. Put the board back in its static bag and in its box. Ship the board back to us as directed.

APPENDIX A

SAB 82532

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