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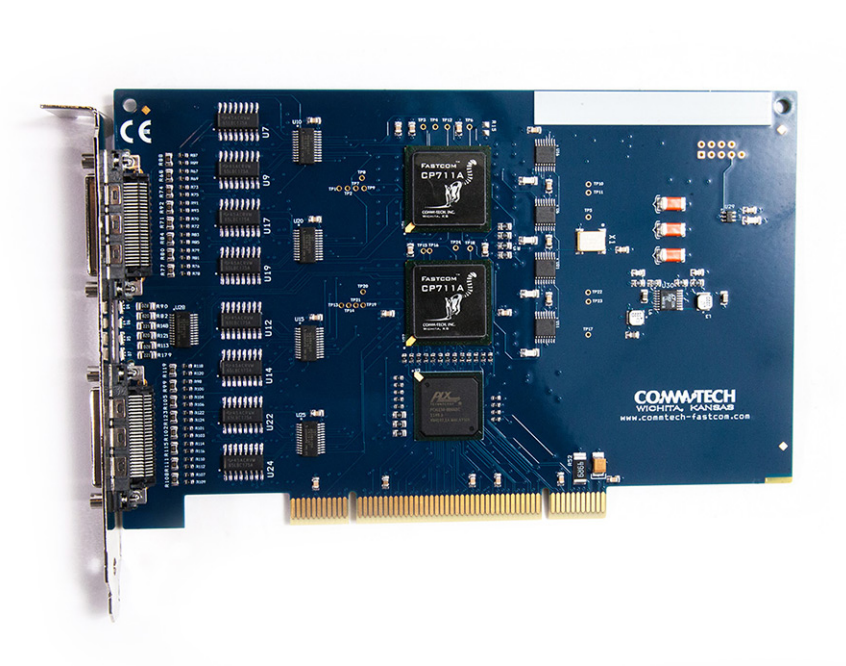
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Fastcom: FSCC/4

P/N: 140I2000



DETAILS +

Designed to comply with the latest PCI specifications, the Fastcom: FSCC/4 Universal PCI (PCI version 2.3) adapter This means the card will work in the high speed PCI-X slots commonly found in most new servers, as well as the star flexibility allows for a single serial interface board to be used across a wide range of different types of computers in systems. The Fastcom: FSCC/4 adapter is the one of the most advanced synchronous communications adapters in t supports data rates up to 20 Mbit/s[1]. The Fastcom: FSCC/4 is a four channel adapter, with each one being individual ASYNC (using FC950 UARTS), or protocols. Although similar to the ESCC and SuperFastcom families of adapters, t adapters. The most notable expansion is the longevity of the components of the board. Faced with the inevitability put an end to the lifespan problems that plague most computing customers. We designed a serial communications mind, and built a card around it. Wholly designed and owned by Commtech, Inc, this FPGA based SCC has most of t a quality Fastcom product. It also includes a few new features that come directly from customer requests. If the exis discontinued by the chip manufacturer, the design can simply be re-targeted to the next generation of FPGA chip w

Difference Between Fastcom: FSCC/4 and Fastcom: SuperFSCC/4

The SuperFSCC/4 card features bus-mastering DMA; therefore, it greatly decreases the amount of interrupts that m freeing it up for other activities. By utilizing this DMA, the SuperFSCC/4 is able to stream gapless, full duplex data a card is only able to perform the same task at around 20 Mbit/s. The standard card is capable of operating at rates u sustain higher rates without generating gaps in the data (e.g. idle between frames).

[1]This is possible as long as the operating parameters are within reason. For instance, you cannot expect to perform Mbit/s with 2 byte frames. This will require reasonable sized frames with a minimum size of around 1024 bytes. If yo card can meet your needs, please contact Technical Support.

SPECIFICATIONS -

- **COMM. CONTROLLER:** Fastcom F-Core
- **INTERFACE:** RS422 / RS485
- **CONNECTOR CONFIGURATION:** Cable assembly (2 ft.) — Two CHAMP 50 VHDCI connectors to four DB25 plugs

- **BUS INTERFACE:** PCI Version 2.3
- **BAUD RANGE:** Using the user independent programmable clock generator in conjunction with the baud rate register, virtually any baud rate from 1 bps to 20 Mbit/s can be attained.
    - Maximum data rates are estimates. They are greatly affected by a number of different factors. See the data rates section of the for more details. This is possible as long as the operating parameters are within reason. If you have any question about whether the card can meet your needs, please contact .
- **POWER REQUIREMENTS:** +5V @ 650mA (typical)
- **ENVIRONMENT:**
    - Operating Temperature Range: 0 to 70 C
    - Humidity: 0 to 90% (non-condensing)
- **DIMENSIONS:**
    - Half-length full-height
    - Height: 4.2" (107 mm)
    - Length: 6.9" (175.26 mm)
    - Weight: .2380 lbs (107.955 g)

FEATURES +

- **Never Obsolete**
- **Customizable Firmware:** The firmware for our FSCC and SuperFSCC product lines is fully-customizable. If you listed, please contact us about modifying our firmware to meet your specific needs.
- **High speed:** Up to 20 Mbit/s
- **Drivers:** RS422 / RS485 multi-drop
- True-Async mode. Each port can be set to use the on-board FC950 UARTs and can be used as a standard seria
- Automatic RS-485 handling
- Transmit and Receive status LED's for each port.
- On board RS-485 termination network for each receive signal pair
- **Four independent full duplex serial channels**
    - Data clocking mechanism independently selectable per channel per direction
        - Externally generated Rx and Tx clocks
        - Internally generated Rx and Tx clocks
        - On chip DPLL clock recovery
        - Independent baud rate generators
- **FIFOs**
    - RxFIFO = 8KB per port (non-uart modes)
    - TxFIFO = 4KB per port (non-uart modes)
    - Programmable interrupt trigger levels (watermark)
- **Data protocols**
    - **HDLC/SDLC**
        - The FSCC and SuperFSCC families of cards fully supports the HDLC framing convention. It does no SDLC control fields. If control bytes are present in received frames they will be passed to the user a control bytes are required to be transmitted they will have to be generated by the user and written
        - Automatic flag detection and transmission
        - General frame format: 0x7e,info,CRC,CRC,[CRC,CRC,]0x7e
        - Frame format with maskable address enabled: 0x7e,address,[address,]info,CRC,CRC,[CRC,CRC,]0x
        - Zero insertion/deletion
        - One insertion/deletion
        - Shared flag mode: opening flag and closing flag of back-to-back frames can use the same flag.
        - Error detection (abort, overrun, underrun, CRC error, too long/short frame)
        - Can use CRC8, CRC-CCITT, or CRC32
    -
        - Any begin/end frame sync sequence of up to 4 bytes
        - Frame format: SYN1,[SYN2,SYN3,SYN4,]info,[CRC,CRC, CRC,CRC,][TCR1,TCR2,TCR3,TCR4]
        - Maskable: can select all or parts of the sync sequence to be a sync match
        - Termination sequence detection up to 4 bytes (maskable)
        - Shared flag mode: opening flag and closing flag of back-to-back frames can use the same flag.
        - Error detection
        - Can use any of the available CRC methods
    - **Transparent Mode**
        - Fully bit transparent (no framing or bit manipulation)
        - Can synchronize using selectable frame sync signals
- **Data encoding schemes:**

    - NRZ, NRZI, FM0/FM1, Manchester, Differential Manchester
- **Selectable frame sync signals**
    - Pulse width of one clock at first bit of data
    - Pulse width of one clock at last bit of data
    - Pulse width of the entire frame
    - Optionally insert a variable number of clock cycles between data and FSS
    - Selectable polarity
- Optional data flow control using modem control lines (RTS, CTS)
- Programmable 8-bit preamble and postamble with selectable repetition rate (1 to 255 repetitions)
- Data can be oriented as selectable MSB first or LSB first
- Interframe time fill: idle as repetitive 1's, flags, or sync sequences
- **CRC Support**
    - Automatic handling in the transmit/receive direction
    - CRC-CCITT (also known as CRC16-ITU) (HDLC), CRC32 (HDLC), CRC16, CRC8 (HDLC)
    - Transparent CRC option
    - Reset as 0's / 1's
- Continuous transmission of 1 to 4096 bytes
- **Selectable data rates**
    - Synchronous (internally clocked) data rates up to 20 Mbit/s
    - Synchronous (externally clocked) data rates up to 20 Mbit/s
    - Asynchronous (DPLL clock recovery) data rates up to 12.5 Mbit/s
    - These maximum data rates are estimates. They are greatly affected by a number of different factors. See more details.
- Data and clock inversion
- Interruptible hardware timer
- Transmit a single frame on the expiration of the hardware timer
- Transmit a single frame on the detection of external signal
- Cable, documentation, and software drivers included
- **Designed and manufactured by COMMTECH, INC. Wichita, Kansas, USA**

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