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TECHNOLOGY GROUP

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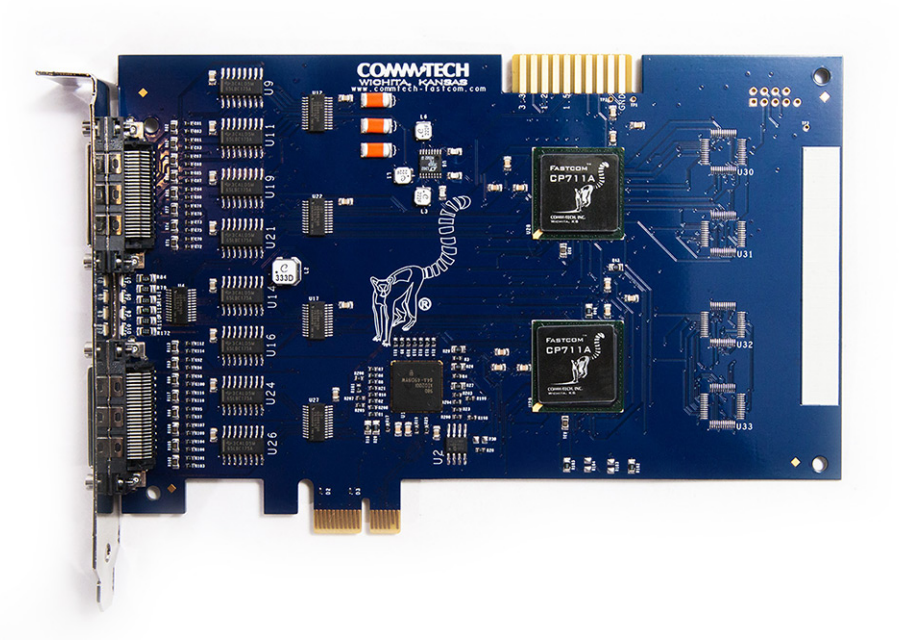
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Visit our website - *Click HERE*

Fastcom: SuperFSCC/4-PCIe

P/N: 24022000

$1,169.00



NEVER OBSOLETE

FULLY PROGRAMABLE DATA RATE

LEGENDARY TECHNICAL SUPPORT

LIMITED LIFETIME WARRANTY

DETAILS +

The Fastcom: SuperFSCC/4-PCIe adapter is the one of the most advanced synchronous communications adapters ir PCIe supports data rates up to 50 Mbit/s[1]. The Fastcom: SuperFSCC/4-PCIe is a four channel adapter, with each one HDLC/SDLC, ASYNC (using FC950 UARTS), or Fastcom®: X-Sync protocols. Although similar to the SuperFastcom ai SuperFSCC/4-PCIe expands on our previous adapters. The most notable expansion is the longevity of the componei inevitability of obsolescence, Commtech decided to put an end to the lifespan problems that plague most computin

communications controller with our customers' needs in mind, and built a card around it. Wholly designed and owne SCC has most of the features that you are used to seeing in a quality Fastcom product. It also includes a few new fe requests. If the existing FPGA technology is ever discontinued by the chip manufacturer, the design can simply be re chip with no impact on compatibility.

[1]This is possible as long as the operating parameters are within reason. For instance, you cannot expect to perform c Mbit/s with 2 byte frames. This will require reasonable sized frames with a minimum size of around 1024 bytes. If you card can meet your needs, please contact Technical Support.

SPECIFICATIONS +

- **COMM. CONTROLLER:** Fastcom F-Core
- **INTERFACE:** RS422 / RS485
- **CONNECTOR CONFIGURATION:** Cable assembly (2 ft.) — Two CHAMP 50 VHDCI connectors to four DB25 plu
- **BUS INTERFACE:** PCIe x1 Gen 2.0
- **BAUD RANGE:** Using the user independent programmable clock generator in conjunction with the baud rate re bps to 50 Mbit/s can be attained.
    - Maximum data rates are estimates. They are greatly affected by a number of different factors. See the da details. This is possible as long as the operating parameters are within reason. If you have any question a needs, please contact Technical Support.
- **POWER REQUIREMENTS:** +3.3V 200mA (typical), and +12V 350mA (typical)
- **ENVIRONMENT:**
    - Operating Temperature Range: 0 to 70 C
    - Humidity: 0 to 90% (non-condensing)
- **DIMENSIONS:**
    - Half-length full-height
    - Height: 4.2″ (107 mm)
    - Length: 6.9″ (175.26 mm)
    - Weight: .2455 lbs (111.357 g)

FEATURES +

- **Never Obsolete**
- **Customizable Firmware:** The firmware for our FSCC and SuperFSCC product lines is fully-customizable. If you listed, please contact us about modifying our firmware to meet your specific needs.
- A drop in replacement for your FSCC and SuperFSCC PCI cards!
- **High speed:** Up to 50 Mbit/s
- **Drivers:** RS422 / RS485 multi-drop
- True-Async mode. Each port can be set to use the on-board FC950 UARTs and can be used as a standard seria
- Automatic RS-485 handling
- Transmit and Receive status LED's for each port.
- On board RS-485 termination network for each receive signal pair
- **Four independent full duplex serial channels**
    - Data clocking mechanism independently selectable per channel per direction
        - Externally generated Rx and Tx clocks
        - Internally generated Rx and Tx clocks
        - On chip DPLL clock recovery
        - Independent baud rate generators
- **FIFOs**
    - RxFIFO = 8KB per port (non-uart modes)
    - TxFIFO = 4KB per port (non-uart modes)
    - Programmable interrupt trigger levels (watermark)
- **Data protocols**
    - **HDLC/SDLC**
        - The FSCC and SuperFSCC families of cards fully supports the HDLC framing convention. It does no SDLC control fields. If control bytes are present in received frames they will be passed to the user a control bytes are required to be transmitted they will have to be generated by the user and written
        - Automatic flag detection and transmission
        - General frame format: 0x7e,info,CRC,CRC,[CRC,CRC,]0x7e
        - Frame format with maskable address enabled: 0x7e,address,[address,]info,CRC,CRC,[CRC,CRC,]0x
        - Zero insertion/deletion

        - One insertion/deletion
        - Shared flag mode: opening flag and closing flag of back-to-back frames can use the same flag.
        - Error detection (abort, overrun, underrun, CRC error, too long/short frame)
        - Can use CRC8, CRC-CCITT, or CRC32
    - **Arbitrary Sync Sequence (Fastcom®: X-Sync)**
        - Any begin/end frame sync sequence of up to 4 bytes
        - Frame format: SYN1,[SYN2,SYN3,SYN4,]info,[CRC,CRC, CRC,CRC,][TCR1,TCR2,TCR3,TCR4]
        - Maskable: can select all or parts of the sync sequence to be a sync match
        - Termination sequence detection up to 4 bytes (maskable)
        - Shared flag mode: opening flag and closing flag of back-to-back frames can use the same flag.
        - Error detection
        - Can use any of the available CRC methods
    - **Transparent Mode**
        - Fully bit transparent (no framing or bit manipulation)
        - Can synchronize using selectable frame sync signals
- **Data encoding schemes:**
    - NRZ, NRZI, FM0/FM1, Manchester, Differential Manchester
- **Selectable frame sync signals**
    - Pulse width of one clock at first bit of data
    - Pulse width of one clock at last bit of data
    - Pulse width of the entire frame
    - Optionally insert a variable number of clock cycles between data and FSS
    - Selectable polarity
- Optional data flow control using modem control lines (RTS, CTS)
- Programmable 8-bit preamble and postamble with selectable repetition rate (1 to 255 repetitions)
- Data can be oriented as selectable MSB first or LSB first
- Interframe time fill: idle as repetitive 1's, flags, or sync sequences
- **CRC Support**
    - Automatic handling in the transmit/receive direction
    - CRC-CCITT (also known as CRC16-ITU) (HDLC), CRC32 (HDLC), CRC16, CRC8 (HDLC)
    - Transparent CRC option
    - Reset as 0's / 1's
- Continuous transmission of 1 to 4096 bytes
- **Selectable data rates**
    - Synchronous (internally clocked) data rates up to 50 Mbit/s
    - Synchronous (externally clocked) data rates up to 30 Mbit/s
    - Asynchronous (DPLL clock recovery) data rates up to 12.5 Mbit/s
    - These maximum data rates are estimates. They are greatly affected by a number of different factors. See more details.
- Data and clock inversion
- Interruptible hardware timer
- Transmit a single frame on the expiration of the hardware timer
- Transmit a single frame on the detection of external signal
- **Included Libraries:**
    - C
    - C++
    - .NET
    - Python
    - Network Analyzer
    - Wireshark
- Cable, documentation, and software drivers included
- **Designed and manufactured by COMMTECH, INC. Wichita, Kansas, USA**

MANUAL & SOFTWARE -

- Drivers are available for:
    - Windows XP through Windows 10, 32 and 64 bit
    - Linux 2.6.16-3.X
- Included Libraries:
    - C
    - C++

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