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"FASTCOM® is the solution to all of your industrial/commercial serial communication needs"

SuperFastcom-cPCI

Four Port High Speed Synchronous Serial Adapter RS422/485 Interface (3U Height)

(Please call for pricing and availability)

SuperFastcom-cPCI Synchronous RS422 & RS485 Compact PCI Bus Serial Communications Interface Adapter

The SuperFastcom-cPCI (3U Height) Compact PCI adapter is a very high speed, four channel, synchronous serial communications adapter designed for use in Windows and Linux based industrial/commercial systems. Its outstanding features include data rates up to 40 Mbits/s[1] and the ability to buffer up to 4 Gigabytes of data (Windows 2000) in system memory.

The SuperFastcom-cPCI supports all standard synchronous protocols (HDLC, SDLC) and their variations as well as all standard asynchronous data formats at data rates up to 40 Mbits/s[1]. The external on-board clock generator provides a high-speed clock source for your system and eliminates the need for an external clock. The board also features high-speed RS422 / RS485 drivers/receivers with on board line termination.

SuperFastcom-cPCI Cable

SuperFastcom-cPCI Synchronous RS422 & RS485 Compact PCI Bus Serial Communications Interface Adapter Cable

DB78 plug to four DB25 plugs (Included)

Programming is simplified with the inclusion of drivers, example programs, and comprehensive documentation supplied on the Fastcom CD. Software drivers are included for Windows 2000, XP, 2003, and Linux kernels 2.4 and 2.6. The SuperFastcom-cPCI provides high speed and high reliability while greatly reducing development time and system complexity.

The following diagram illustrates the basic structure of the SuperFastcom-cPCI:

Basic Structure Diagram for the SuperFastcom-cPCI

The SuperFASTCOM family of adapters also includes RS422/485 and RS232 PCI, PC/104+, and cPCI Rear I/O Bus Styles.

SPECIFICATIONS:

- **COMM. CONTROLLER:**

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	◦ INFINEON PEB20534 (Data Sheet) • **DRIVERS/RECEIVERS:** High-speed RS422 / RS485 • **SIGNALS:** ◦ SD, RD, RTS, CTS, DCD, TT, RT, ST • **BUS INTERFACE:** 32 bit Compact PCI • **FORM FACTOR:** 3U • **MAXIMUM DATA RATE:** 40 Mbits/s[1] per channel
POWER REQUIREMENTS:	• +5V @ 450mA (typical)
ENVIRONMENT:	• Operating Temperature Range: 0 to 70 C • Humidity: 0 to 90% (non-condensing)
FEATURES:	• High speed, up to 40Mbits/s[1] • Drivers: RS422 / RS485 multi-drop • **Serial Communication Controllers (SCCs)** ◦ Four independent channels ◦ Full duplex data rates on each channel of up to 10Mbits/s sync - 2Mbit/s with DPLL, 2 Mbits/s async ◦ 17 DWORDs deep receive FIFO per SCC (+ 128 DWORDs central receive FIFO) ◦ 8 DWORDs deep transmit FIFO per SCC (+128 DWORDs central transmit FIFO) • **Serial Interface** ◦ On-chip clock generation or external clock sources ◦ On-chip DPLLs for clock recovery[2] ◦ Baud rate generator ◦ Clock gating signals ◦ Clock gapping capability ◦ Programmable time-slot capability for connection to TDM interfaces ◦ Encoding Schemes: NRZ (Non-Return-To-Zero), NRZI (Non-Return-To-Zero-Inverted), FM0 (Bi-Phase Space), FM1 (Bi-Phase Mark), Manchester (Bi-Phase) ◦ Optional data flow control using modem control lines (/RTS, /CTS, CD) ◦ **HDLC/SDLC Protocol Modes** ▪ Automatic flag detection and transmission ▪ Shared opening and closing flag ▪ Generation of interframe-time fill '1's or flags ▪ Detection of receive line status ▪ Zero bit insertion and deletion ▪ CRC generation and checking (CRC-CCITT or CRC-32) ▪ Transparent CRC option per channel and/or per frame ▪ Programmable Preamble (8bit) with selectable repetition rate ▪ Error detection (abort, long frame, CRC error, short frame) ◦ **Bit Synchronous PPP Mode** ▪ Bit oriented transmission of HDLC frame (flag, data, CRC, flag) ▪ Zero bit insertion/deletion ▪ 15 consecutive '1' bits abort sequence ◦ **Asynchronous (ASYNC) Protocol Mode** ▪ Selectable character length (5 to 8 bits) ▪ Even, odd, forced or no parity generation/checking ▪ 1 or 2 stop bits ▪ Break detection/generation ▪ In-banc flow control by XON/XOFF ▪ Immediate character insertion ▪ Termination character detection for end of block identification ▪ Time out detection ▪ Error detection (parity error, framing error) ◦ **BISYNC Protocol Mode** ▪ Programmable 6/8 bit SYN pattern (MONOSYNC) ▪ Programmable 12/16 bit SYN pattern (BISYNC)

        - Selectable character length (5 to 8 bits)
        - Even, Odd, forced or no parity generation/checking
        - Generation of interframe-time fill '1's or SYN characters
        - CRC generation (CRC-16 or CRC-CCITT)
        - Transparent CRC option per channel and/or per frame
        - Programmable Preamble (8bit) with selectable repetition rate
        - Termination character detection for end of block identification
        - Error detection (parity error, framing error)
    - **Extended Transparent Mode**
        - Fully bit transparent (no framing, no bit manipulation)
        - Octet-aligned transmission and reception
    - **Protocol and Mode Independent**
        - Data bit inversion
        - Data overflow and underrun detection
        - Timer
- **Protocol Support**
    - **Address Recognition Modes**
        - No address recognition (Address Mode 0)
        - 8-bit (high byte) address recognition (Address Mode 1)
        - 8-bit (low byte) or 16-bit (high and low byte address recognition (Non Auto Mode)
- On-chip Rx and Tx data buffer; 128 32-bit words each
- Programmable buffer size in transmit direction per channel; buffer allocation in receive direction on request
- Internal test loop capability
- Programmable watermark for receive channels to control transfer of receive data to host memory
- Two programmable watermarks for each transmit channel. One controlling data loading from host memory and one controlling transfer of transmit data to the corresponding Serial Communication Controller (SCC)
- Status LEDs for system development/debugging
- Two programmable on-board clock generators (one internal, one external).
- Cable, documentation, and software drivers included
- **Designed and manufactured by COMMTECH, INC. Wichita, Kansas, USA**
- For a more complete and detailed list of features available on this card, please see the documentation for the PEB20534 serial communication controller

[1]The aggregate data rate for all channels is 108 Mbits/s per direction. Data rates are limited by factors such as cable length, cable quality, and the type of linear drivers and receivers used.
[2] According to section 3.1.3 of the PEB20534 Errata Sheet (DS7 2003-07-31): DPLL clock recovery is non-functioning when recovering from an FM0 (Bi-Phase Space), FM1 (Bi-Phase Mark) or Manchester (Bi-Phase) encoded receive data stream. If using NRZ (Non-Return-To-Zero) or NRZI (Non-Return-To-Zero-Inverted) line encoding, DPLL clock recovery will function properly.

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