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Technical Reference Manual for VP 34x/02x VME Intel® Pentium® M Processor Single Board Computer

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CONVENTIONS

Throughout this manual the following conventions will apply:

- # or * after a name represents an active low signal. e.g. INIT* or INIT#
- h denotes a hexadecimal number. e.g. FF45h
- byte represents 8-bits
- word represents 16-bits
- dword represents 32-bits

NOTATIONAL CONVENTIONS

NOTE:	Notes provide general additional information.

WARNING:	Warnings provide indication of board malfunction if they are not observed.

CAUTION:	Cautions provide indications of board or system damage if they are not observed

BIST	Built In Self Test
CPU	Central Processing Unit
DDR	Double Data Rate
DMA	Direct Memory Access
ECC	Error Checking and Correcting
EPROM	Electrically Programmable Read Only Memory
FWH	Firmware Hub
GMCH	Graphics and Memory Controller Hub
ICH	I/O Controller Hub
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
IRQ	Interrupt Request
LPC	Low Pin Count
LED	Light Emitting Diode
LFM	Linear Feet per Minute
NVRAM	Non-Volatile RAM
PCI	Peripheral Component Interconnect
PMC	PCI Mezzanine Card
POST	Power-on Self Test
RAM	Random Access Memory
RoHS	Restriction of Hazardous Substances
RST	Reset
SDRAM	Synchronous Dynamic RAM
SIO	Serial Input/Output
SO-DIMM	Small Outline Dual Inline Memory Module
SCSI	Small Computer Systems Interface
UMA	Unified Memory Architecture
USB	Universal Serial Bus
VME	Versa Module Europe

Revision	Summary of Changes	Date
01	First Release	May 2005
02	Removed AD VP2/003-20; updated LDT Status and Control Register	May 2005
03	Updated for Rev B board: added SCSI interface details and new breakout modules	August 2005
04	Updated for Rev C board: changed SCSI controller; added 1.0 GHz Celeron processor	June 2006
05	Changed SW2-1 to reflect factory default settings. Correction to COM1/COM2 connectors in figures.	November 2008

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1 INTRODUCTION

1.1 General

This manual is a guide and reference handbook for engineers and system integrators who wish to use the Concurrent Technologies' VP 34x/02x ultra high-performance Intel® Pentium® M processor single board computer. The board has been designed for high-speed multiprocessing applications using a PC-AT™ architecture operating in a VME Bus environment.

The VP 34x/02x board is available in several different variants which differ by the CPU speed, the amount of fitted DDR SDRAM and the rear I/O connector configuration. Currently the board is available with a 1.0 GHz Ultra Low Voltage Intel® Celeron® M processor 373, a 1.6 GHz Intel® Pentium® M processor, a 1.4GHz Intel Pentium M processor Low Voltage 738 or 1.8 GHz Intel Pentium M processor 745. These models are designated VP 345/021, VP 345/022, VP 347/020 and VP 347/021 respectively. The other configuration options are specified by a two-digit suffix to the board name; refer to the product datasheet for further details. Further details of other board options are given in Section 1.3. References to the board in this document will use the name VP 34x/02x unless they apply only to a specific variant, in which case the full name will be used.

The information contained in this manual has been written to provide users with all the information necessary to configure, install and use the VP 34x/02x as part of a system. It assumes that the user is familiar with the VME bus and PC-AT bus architectures and features.

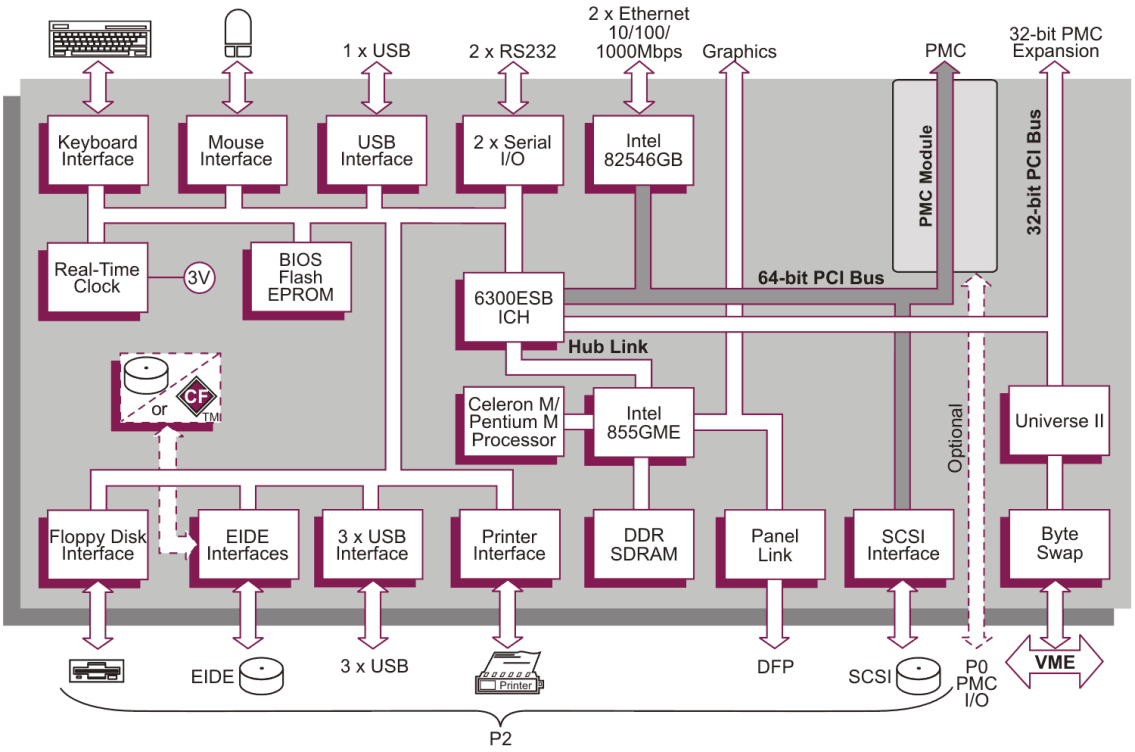


Figure 1-1 Overview

1.2 The VP 34x/02x - Main Features

The VP 34x/02x is a member of the Concurrent Technologies range of single board computers for the VME bus architecture. It has been designed as a powerful single board computer based upon the Intel Pentium M or Celeron M processor, an 82546GB dual channel Gigabit Ethernet controller, PCI to VME bus bridge chip and the 6300ESB I/O hub. It also provides one IEEE 1386.1 PMC interface, PMC expansion carrier interface, optional on-board mass storage, digital flat panel video and interfaces for standard PC-AT based peripherals.

1.2.1 Central Processor

The central processor used on this board is an ultra high performance Intel Pentium M processor operating internally at 1.4 GHz, 1.6 GHz or 1.8 GHz. Alternatively the board may be fitted with a low power Intel Celeron M processor operating at 1.0 GHz. These 32-bit processors support the Dual Independent Bus (DIB) architecture with the backside bus connected to the on die Level 2 cache and the 64-bit frontside bus connected to the memory controller at 400 MHz to provide a maximum theoretical transfer bandwidth of 3.2 Gbytes/s. The processor is capable of addressing 4 Gbytes of physical memory, all of which is cacheable, and 64 Terabytes of virtual memory.

The processor is upwardly code-compatible with the other members of the x86 family of microprocessors. The processor has an in-built floating point coprocessor for compatibility with 486 and 386/387 designs.

1.2.2 Cache Memories

The Level 1 and Level 2 caches are both implemented on the processor die for maximum performance. The Level 1 cache stores 32 Kbytes of instructions and 32 Kbytes of data. The Level 2 cache on the 1.0 GHz processor stores 512 Kbytes of instructions and data. The Level 2 cache on the 1.6 GHz processor stores 1 Mbyte of instructions and data. The Level 2 cache on the 1.4GHz and 1.8 GHz processors stores 2 Mbytes of instructions and data.

The Level 2 cache operates at the core frequency and is based on Intel's Advanced Transfer Cache architecture.

1.2.3 Chipset

The VP 34x/02x uses the Intel 855GME + 6300ESB chipset. This is comprised of the 855GME Graphics and Memory Controller Hub (GMCH) and the 6300ESB I/O Controller Hub (ICH).

The 855GME interfaces to the CPU's host bus. It provides a DDR SDRAM memory controller, graphics interface and high speed Bus which connect to the other chipset devices. It supports concurrent Hub Link and CPU bus operations.

The 6300ESB provides two PCI busses for supporting high performance PCI devices. The 6300ESB connects to the 855GME via a Hub Link 1.5 interface which supports a maximum transfer bandwidth of 266 Mbyte/s.

The 6300ESB also provides a variety of peripheral functions including EIDE controllers, USB controller, LPC (Low Pin Count) Bus bridge, IOAPIC interrupt controller and other legacy PC-AT architectural functions.

The LPC Bus is used to connect to the on-board Firmware Hub (FWH) and PC87417 Super I/O Controller. The PC87417 Super I/O Controller implements the keyboard and mouse controller, floppy disk, parallel port and the X-Bus interface to the Status & Control registers. The FWH contains the BIOS and VSA firmware.

1.2.4 SDRAM

The 855GME GMCH SDRAM controller provides a single DDR333 memory channel to provide a maximum transfer bandwidth of 2.66 Gbytes/s and features ECC data protection. Up to 1 Gbyte of on-board memory plus up to 1 Gbyte of SODIMM memory is supported.

1.2.5 PCI Busses

There are two on-board PCI busses provided by the 6300ESB ICH:

1) The primary bus is 64 bits wide, operates at 33 or 66 MHz, and connects to the 10/100/1000Mbits/s Ethernet interfaces (82546GB), SCSI controller and the PMC site.
2) The secondary bus is 32 bits wide, operates at 33 MHz, and connects to the VME bus bridge and PMC expansion carrier interface.

1.2.6 EPROM

The board contains a 1 Mbyte Firmware Hub Flash EPROM for the BIOS code, fixed data and VSA firmware. The Firmware Hub is connected to the LPC bus provided by the 6300ESB ICH.

1.2.7 VME Interface

The VP 34x/02x VME interface is provided by a Tundra® Universe II™ VME to PCI bridge. The VME interface supports transfers up to 64-bits wide. Hardware Endian swapping is configurable under software control. The board can act as system controller when in the first VME Bus slot.

1.2.8 EIDE Controllers

The VP 34x/02x has two EIDE/Ultra ATA100 interfaces. One EIDE interface is available via the P2 connector, the other via an on-board connector for use by the optional CompactFlash carrier or on-board disk drive.

1.2.9 Serial ATA Controller

Two Serial ATA150 interfaces are supported via the P0 connector. This interface is not accessible in all board configurations.

1.2.10 USB

Four USB 2.0 channels are provided by the board. These are available via the P2 connector and a front panel connector.

1.2.11 PMC Site

A PMC site which supports single width 64 or 32-bit PMC modules complying with the IEEE 1361.1 standard is provided. The PMC site supports 3.3V PCI signaling for 66MHz modules and both 5V and 3.3V PCI signaling for 33 MHz modules. The PMC site will also accept dual function PMC modules and Processor PMC modules. The latter will operate only in non-Monarch mode. Rear I/O connections are provided on variants fitted with P0.

1.2.12 PMC Carrier Interface

The VP 34x/02x may be fitted with a PMC expansion carrier board such as the AD CR2/PMC. This carrier board supports two single width 32-bit PMC modules complying with the IEEE 1361.1 standard. Both 5V and 3.3V PCI signaling environments are supported.

1.2.13 SCSI Interface

An LSI Logic™ 53C1020 SCSI controller provides a Single Ended Wide SCSI interface. This interface is available via the P2 connector.

1.2.14 Ethernet Controllers

A single 82546GB Gigabit Ethernet controller is used to provide two high performance PCI to Ethernet interfaces. Both support 10, 100 and 1000Mbits/s operation via front panel RJ45 connectors.

1.2.15 Graphics Controller

The 855GME GMCH is used to provide a high performance graphics accelerator with up to 64 Mbytes of UMA memory. An analog CRT interface is provided via a 15-way high density D-Type connector on the front panel. A digital flat panel interface is provided via P2.

1.2.16 Serial Communications

The VP 34x/02x provides two RS232 serial data communication channels. These are implemented by the 6300ESB ICH and are available via front panel RJ45 connectors. The baud rate clock is generated internally by the device's I/O Controller.

1.2.17 Keyboard and Mouse

PS/2™ type keyboard and mouse interfaces are provided by the Super I/O Controller. They are available via a 6-way Mini-DIN front panel connector. A splitter cable is required to access the mouse interface.

1.2.18 Real Time Clock (RTC)

A battery backed RTC device provides PC-AT clock, calendar and configuration RAM functions.

The RTC and BIOS are year 2000 compliant. The clock and configuration RAM functions can be maintained from an external supply for battery free operation if required.

1.2.19 Other Interfaces

The VP 34x/02x has 2 TTL compatible I/O pins accessible via P2 which are available for user defined I/O.

1.3 Additional Board Options

The VP 34x/02x board may be ordered in one of a few hard-wired configurations to support different combinations of rear I/O. Each board is typically supplied with an appropriate breakout (paddle) board to provide connections behind the backplane, and the standard options are described in Appendix B. Table 1-1 indicates the interfaces provided by each of these breakout boards.

Breakout	VME P2 Connector pins	Floppy Disk	Narrow SCSI	Wide SCSI	EIDE (ATA)	Flat Panel Interface (DFP)	USB	PMC Rear I/O	External Reset	General Purpose I/O	Parallel Port
AD VP2/001-10	96	✔	✔						✔		✔
AD VP2/001-20	96	✔			✔				✔		✔
AD VP2/002-10	160	✔	✔		✔		✔ x1		✔	✔	✔
AD VP2/003-10	160	✔	✔	✔	✔	✔	✔ x1		✔	✔	
AD VP2/007-40	160	✔	✔	✔	✔	✔	✔ x3	✔		✔	

Table 1-1 VME Breakout Interfaces

Note that some breakout boards are fitted with 160-way P2 connectors as many of the I/O interfaces are connected via rows D and Z of the VP 34x/02x P2 connector. Some configurations of the VP 34x/02x board also use the P0 connector to provide some of the I/O interfaces. In these cases, the appropriate backplane (typically for VME64x) will be required to connect the breakout boards.

Additional mass storage option kits are available for the VP 34x/02x:

- The AD CP1/DR1 provides a 2.5 inch EIDE hard disk drive of at least 40 Gbytes capacity
- The AD 200/001 provides two CompactFlash sites which also support the Hitachi GST MicroDrive™ hard disks

NOTE: It is possible to fit both the mass storage option kit and a PMC module to the board.

Refer to the VP 34x/02x Datasheet for ordering information for all these options.

1.4 Extended Temperature Options

All variants of the board are qualified for the standard operating and storage temperature ranges indicated in section A.2.1. Some variants of the board are available which offer a wider range of operating and storage temperatures, but certain board features are no longer available with these variants. In particular the option for on-board mass storage using a 2.5 inch hard disk drive is not supported for the extended temperature specifications.

Consult your distributor or Concurrent Technologies directly for details of the extended temperature options.

1.5 Compliance to RoHS 2002/95/EC



This product is offered in a form which complies with the RoHS 2002/95/EC directive. The European Union RoHS 2002/95/EC directive restricts the use of six materials in electronic components and assemblies. Specifically, these materials are Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr VI), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE). Concurrent Technologies is committed to compliance to the RoHS directive.

The product may also be available in an alternative form which includes components which do not comply with the RoHS directive. Consult your supplier to determine order codes for RoHS compliant and non-compliant products.

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2 INSTALLATION

2.1 General

This chapter contains general information on unpacking and inspecting the VP 34x/02x after shipment, and information on how to configure board options and install the board into a VME chassis.

CAUTION: It is strongly advised that, when handling the VP 34x/02x and its associated components, the user should at all times wear an earthing strap to prevent damage to the board as a result of electrostatic discharge.

The list below outlines the steps necessary to configure and install the board. Each entry in the list refers to a section in this chapter which will provide more details of that stage of the procedure.

Unpack the board - see Section 2.2.

1) Check the board jumper and switch settings match the required operating mode - see Section 2.3.
2) Locate the board's indicators and switches - see Section 2.4.
3) Fit the battery if required - see Section 2.5.
4) Fit any optional mass storage modules - see Section 2.6.
5) Fit a PMC module if required - see Section 2.7.
6) Install the board - see Section 2.8.

CAUTION: It is strongly recommended that the user reads all the sections in this chapter before installing the board in a VME backplane, or before fitting a PMC module. In particular, additional cautionary notes will highlight areas needing special consideration.

2.2 Unpacking and Inspection

Immediately after the board is delivered to the user's premises the user should carry out a thorough inspection of the package for any damage caused by negligent handling in transit.

CAUTION: If the packaging is badly damaged or water-stained the user must insist on the carrier's agent being present when the board is unpacked.

Once unpacked, the board should be inspected carefully for physical damage, loose components etc. In the event of the board arriving at the customer's premises in an obviously damaged condition Concurrent Technologies or its authorized agent should be notified immediately.

2.3 Default Jumper and Switch Settings

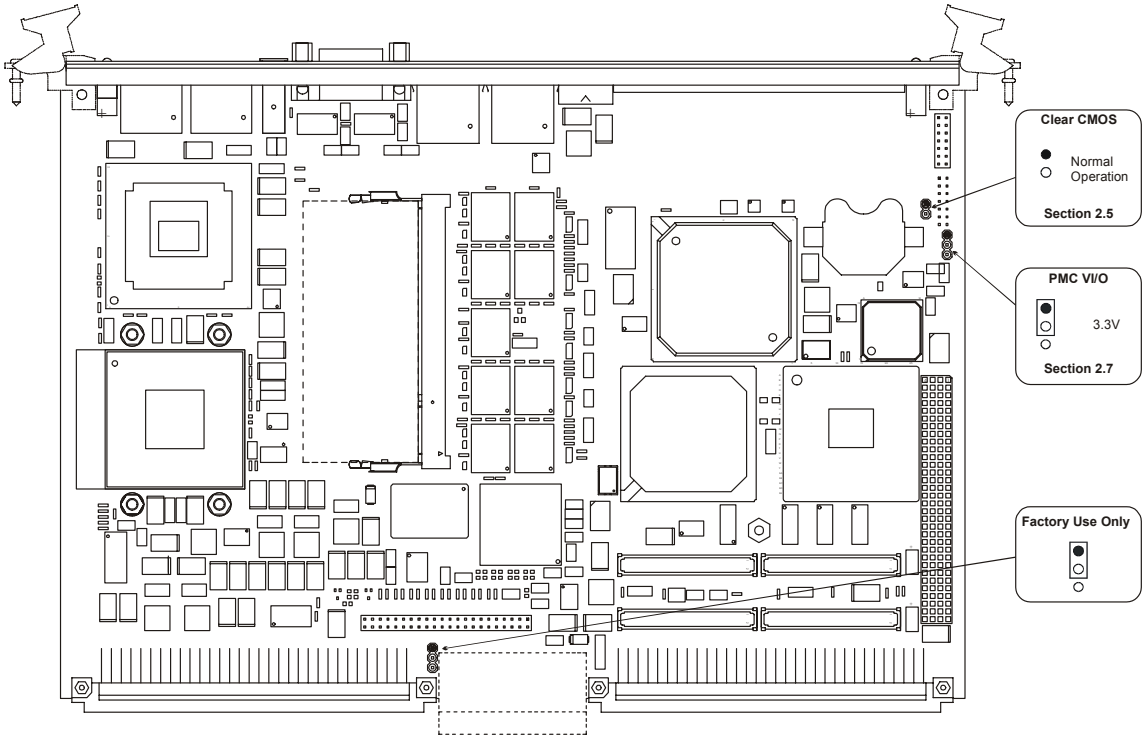


Figure 2-1 Default Jumper Settings (Component Side)

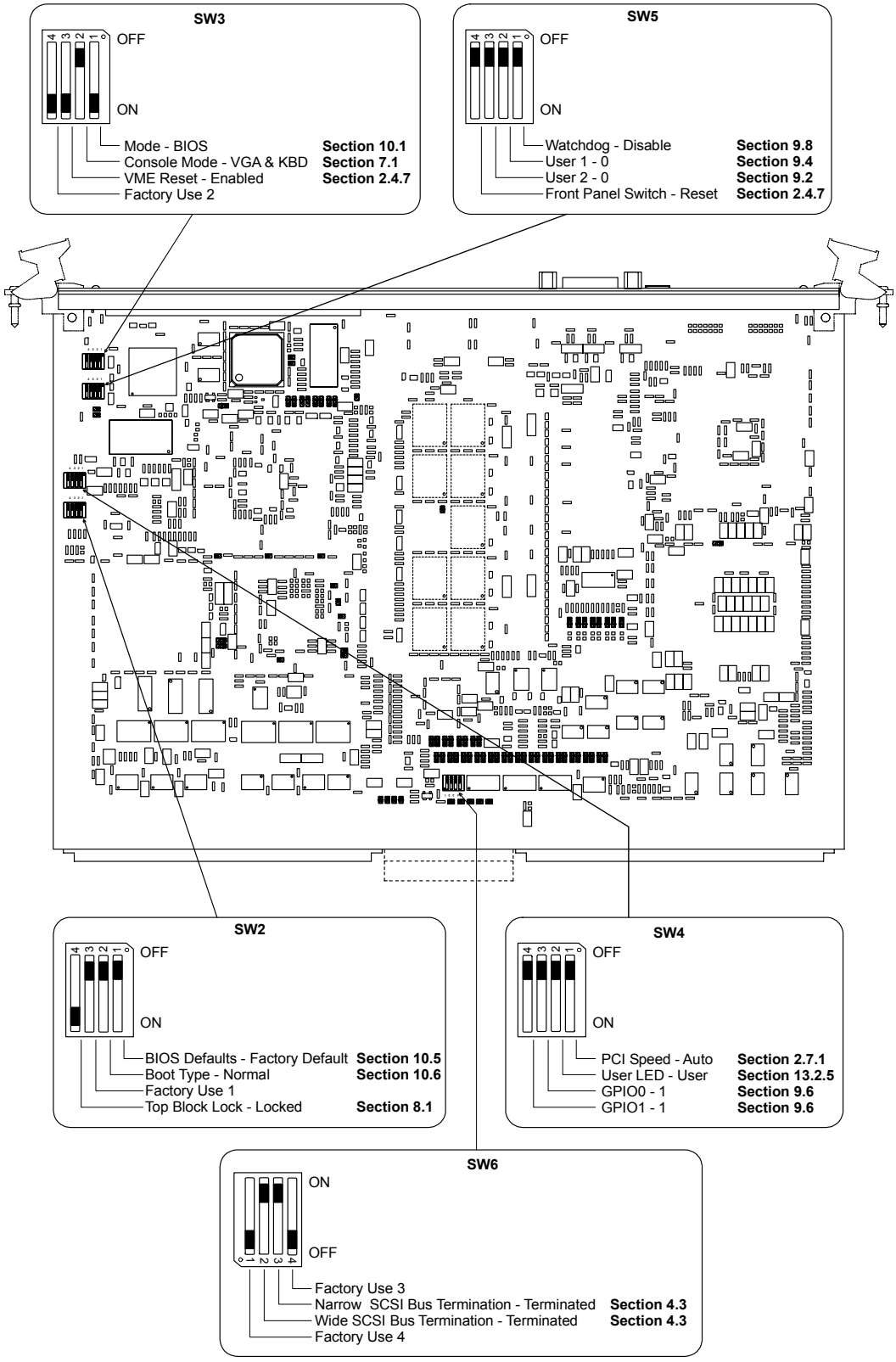


Figure 2-2 Default Switch Settings (Solder Side)

2.4 Front Panel Indicators and Controls

When installing or removing the board for the first time, or when checking it's operation, it can be very useful to note the behavior of the LEDs on the front panel. Figure 2-3 shows the location of the LEDs, and their purpose is outlined below. A recessed pushbutton switch is also accessed through the front panel and this is described below.

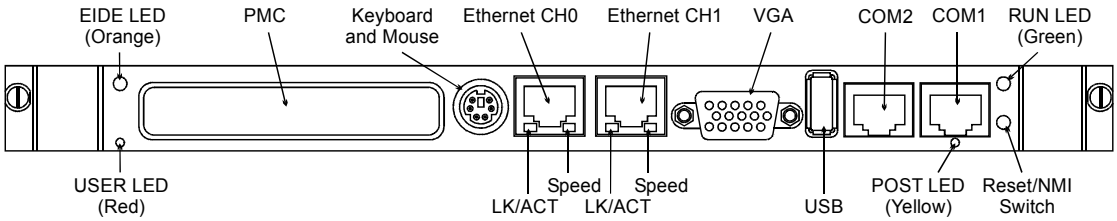


Figure 2-3 Front Panel Indicators and Controls

2.4.1 Run LED (Green)

The run LED indicates that activity is occurring on the internal PCI bus. This allows the user to quickly assess how active the PCI busses are.

2.4.2 POST LED (Yellow)

The POST LED is used to indicate that a power on self test has failed. This LED will also flash when outputting sound on the speaker.

2.4.3 Ethernet Speed LEDs (Yellow)

These LEDs indicates the operating speed of the Ethernet interfaces, as follows:

- Off = 10Mbits/s
- Steady On = 100Mbits/s
- Flashing = 1000Mbits/s

2.4.4 Ethernet LK/ACT LEDs (Green)

These LEDs light when connection has been made on the Ethernet interfaces. They will flash to indicate link activity, and during periods of high Ethernet activity the LED may switch off for several seconds.

2.4.5 EIDE LED (Orange)

This LED lights when there is activity on the on board EIDE interface.

2.4.6 USER LED (Red)

The default use for this LED is user definable. It is controlled by a bit in Status and Control register 4 (see Section 9.6). This LED can be reconfigured to light when the processor die reaches the critical temperature at which thermal management activates (see Section 13.2.5 for further details). When in this mode, if this LED lights during normal operation then it indicates that the chassis cooling system may have failed or is incapable of cooling the board.

The User LED mode is set by the User LED Mode option switch. Figure 2-2 shows the location of this switch.

2.4.7 Reset Pushbutton

This pushbutton can be configured via the FP Switch Function switch to perform one of two functions:

a) a board and/or system reset
b) a local Non-Maskable Interrupt (NMI)

Figure 2-4 shows the location and settings of the FP Switch Function switch.

When the FP Switch Function switch is in the "NMI" position, operating the pushbutton causes an NMI to the local CPU.

When the FP Switch Function switch is in the “Reset” position, operating the pushbutton causes a reset locally on the board. If the board is the System Controller, this reset may also be propagated to the VME backplane via the SYSRESET# signal, depending on the setting of the VME Reset switch (see below). If the board is not the System Controller, only the board itself will be reset.

The VME Reset switch prevents or disables both the reset action of the front panel pushbutton and the Watchdog Timer expiry event (see Section 9.8) from activating the VME bus reset signal SYSRESET#. When this switch is in the "Disabled" position, the pushbutton reset and Watchdog Timer expiry reset will only act locally on this board. When this switch is in the "Enabled" position, both the pushbutton reset and Watchdog Timer expiry reset will cause a VME bus reset via the SYSRESET# signal. Regardless of the setting of the VME Reset switch, the board will always generate a VME bus reset both from power up (when acting as System Controller) and when the Universe II chip has been programmed to do this.

Figure 2-4 shows the location and settings of the VME Reset switch.

The board's response to SYSRESET# being activated by another board is also configurable. Status and Control register 3 (see Section 9.5) contains a bit which can be programmed to allow or prevent the backplane SYSRESET# signal causing a reset to the board.

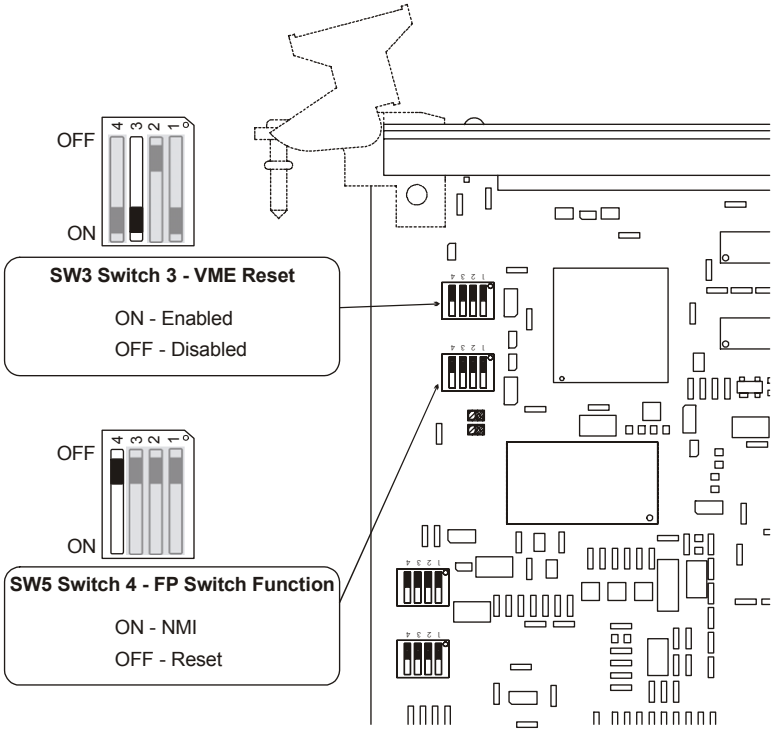


Figure 2-4 Reset Configuration Switches

2.5 Battery Installation/Replacement

The on-board Real-Time Clock and CMOS memory used by the PC BIOS firmware are powered by a 3V Lithium battery when the board is powered off. It is advisable, though not essential, for the battery to be fitted prior to using the board. Figure 2-5 shows how to do this. One battery is supplied with the board, but it is not normally fitted when the board is shipped.

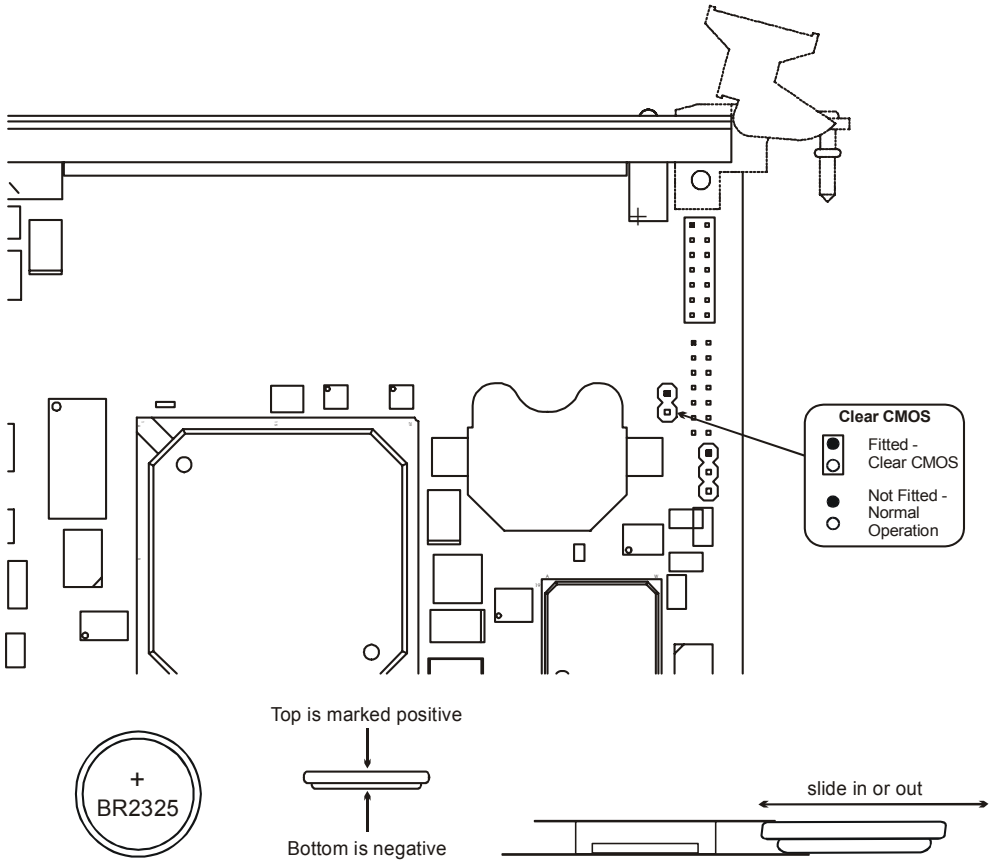


Figure 2-5 Battery Fitting and CMOS Clear Jumper

The battery should be replaced when the voltage falls below 2.5V. Depending on the way in which the board is operated and stored, battery life should be in excess of 5 years. The life expectancy will fall if the battery is subjected to long periods at temperatures of 45°C or above.

It will also fall if the battery is fitted to a board that is stored in its conductive bag even at room temperature. Operation without a battery is possible by connecting the VME Bus VCC_STANDBY supply to an external 5V source. The contents of the CMOS memory will be maintained and the Real-Time Clock will continue to function as long as the VCC_STANDBY supply is maintained to the board.

NOTE: When replacing the board it is not necessary to remove power from the VCC_STANDBY supply.

CAUTION: When replacing the battery, proper anti-static precautions must be observed.

WARNING: Dispose of battery properly. DO NOT BURN. The date and time settings will need to be initialized if the battery is disconnected.

If the BIOS setup screens have been used to set up the board for an invalid configuration, or in other fault conditions, it may be useful to be able to reset the contents of the CMOS RAM and Real-Time Clock. In this case, the CMOS Clear jumper can be used.

To clear the CMOS RAM to a known state, fit the CMOS jumper and apply power. When the board is next powered down remove the Clear jumper, otherwise CMOS RAM will again be reset. After the BIOS settings have been re-configured, they can be saved to Flash EPROM as user default values. See Section 10.5 for more details of this capability, which is very useful when the board is running without a battery or power through VCC_STANDBY.

2.6 Installation of On-Board Mass Storage

The VP 34x/02x supports two on-board mass storage options, namely a 2.5” EIDE hard disk drive or a CompactFlash carrier. Both mass storage options connect to the EIDE header that is located in front of the P2 connector. This is shown in Figure 2-6 below. The following sections detail the installation procedures for the mass storage options.

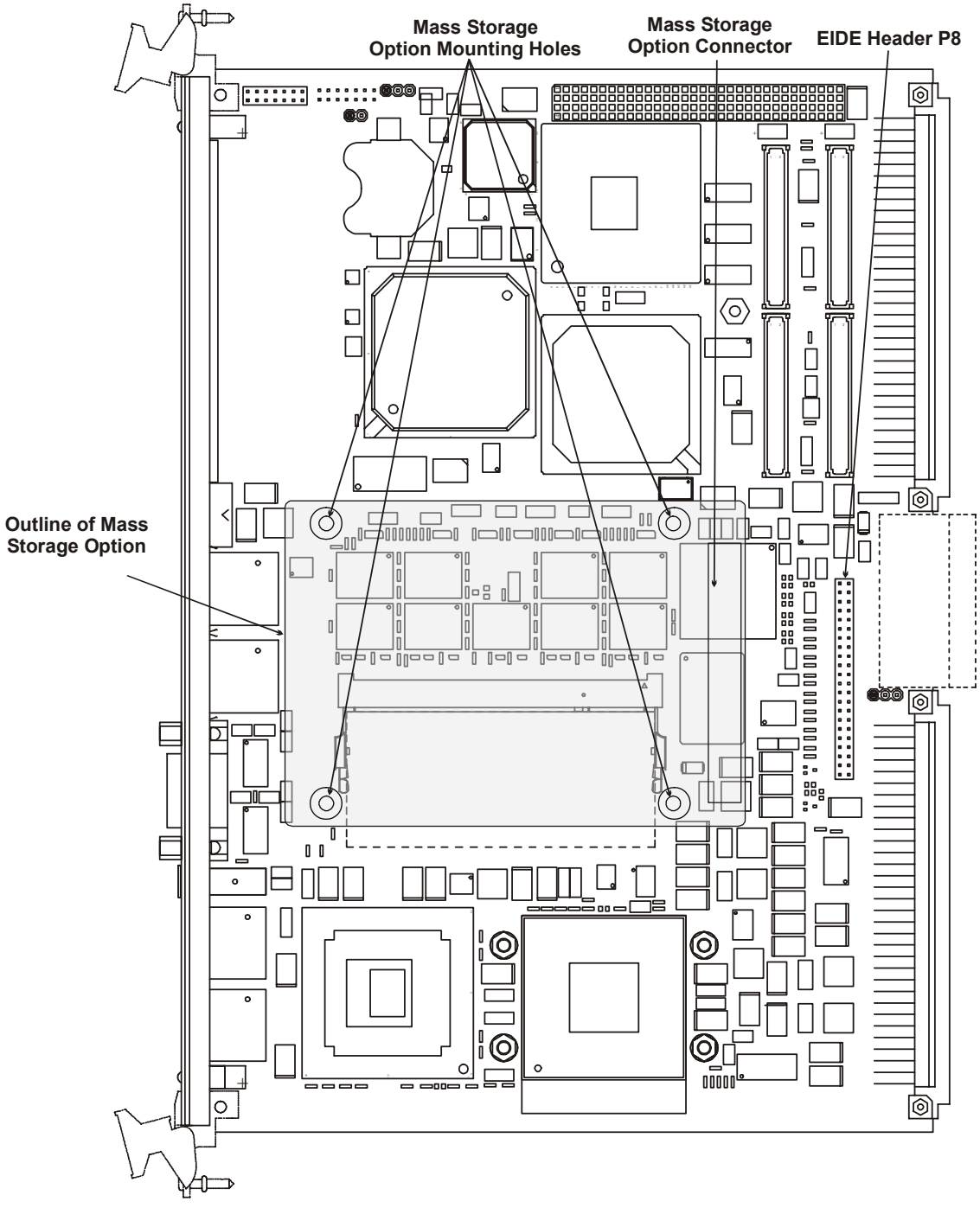


Figure 2-6 Mass Storage Connector and Fixing Screws

2.6.1 Hard Disk Storage Kit (AD CP1/DR1)

The option kit comprises:

- A 2.5 inch EIDE disk drive (dependent upon variant ordered)
- A ribbon cable assembly
- Four M3 x 4mm screws
- Four M3 x 5mm pillars

The ribbon cable assembly has a 50-way connector at one end and a 44-way connector at the other end. The 50-way connector plugs into the disk drive and the 44-way plugs into the EIDE connector on the host board.

a) Screw the four pillars into the bottom of the disk drive until the pillar and the disk drive meet, i.e. there should be no gap between them. Do not over tighten the pillars.
b) Plug the 50-way connector into the disk drive as shown in Figure 1 below, note the orientation.

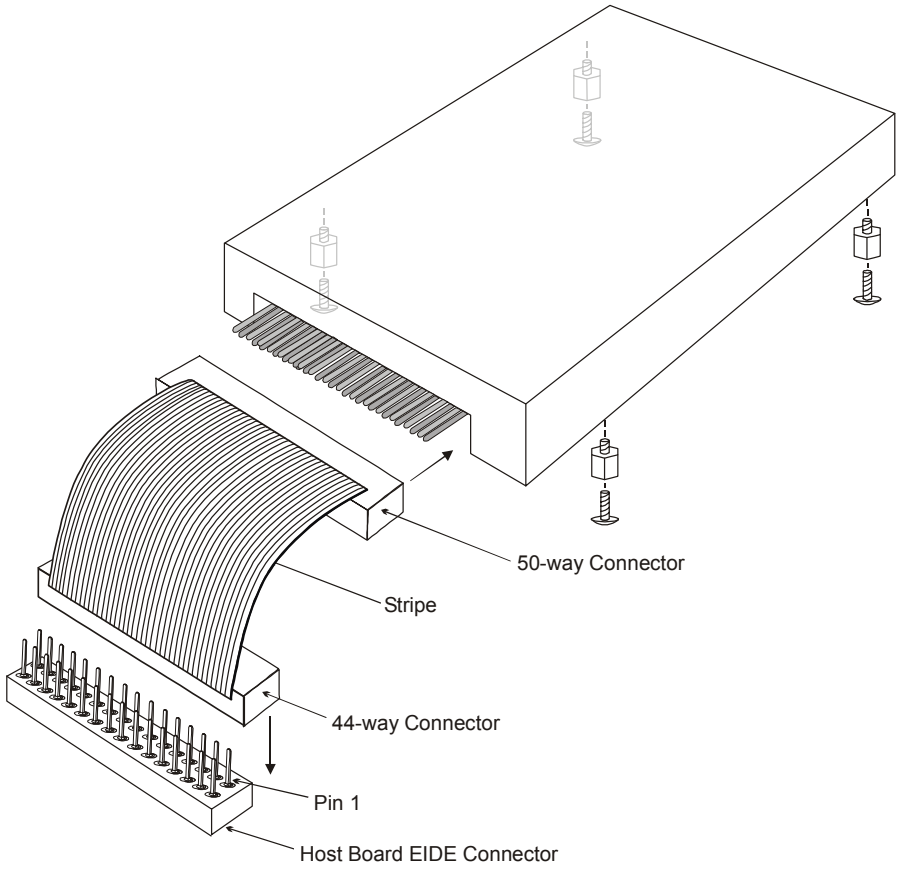


Figure 2-7 Disk Drive Cable Installation

c) Plug the 44-way connector into the host board's EIDE connector, note the orientation.
d) Fix the disk drive into position, placing the four screws provided through the appropriate holes in the host board and screwing them into the bottom of the pillars. Do not over tighten the screws.

NOTE: If the board is likely to be subjected to mechanical vibration a suitable thread lock compound applied to the screws should be considered.

2.6.2 CompactFlash Storage Kit (AD 200/001)

The option kit comprises:

- A CompactFlash carrier module
- Four M3 panhead screws

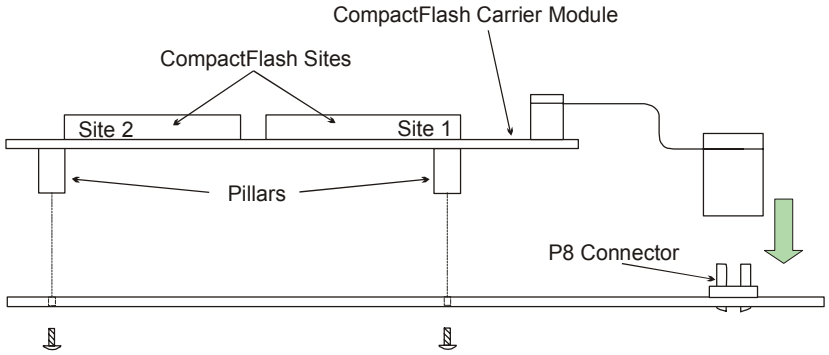


Figure 2-8 CompactFlash Storage Kit Installation

To install the CompactFlash Storage Kit use the following procedure:

1) The M3 panhead screws may be loosely screwed into the end of the pillars, if so unscrew them.

NOTE: Do not unscrew the countersunk screws attaching the pillars to the circuit board.

2) Plug the carrier module in to the 44way connector as shown above. Check that the module is aligned correctly and that the pillars are aligned with the mounting holes in the board.
3) Fix the module into position using the four panhead screws referred to earlier. Do not over tighten the screws.

NOTE: If the board is likely to be subjected to mechanical vibration a suitable thread lock compound applied to the screws should be considered.

The CompactFlash sites are labeled CompactFlash 1 and CompactFlash 2. If a single CompactFlash card is fitted, it should always be installed into site 1. Site 2 should be used only when two CompactFlash cards are fitted.

The CompactFlash card(s) may be retained in position by fitting short M3 screws and spacers into the holes near the long edge of the carrier. This will protect against accidental removal due to vibration or deliberate but unauthorized removal.

NOTE: If more than one CompactFlash module is fitted, the module in the CompactFlash 2 site must support operation as a Slave device.

The DIL switch on the AD 200/001 should be set as shown in Figure 2-9.

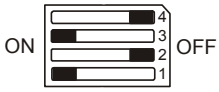


Figure 2-9 AD 200/001 DIL Switch Settings

2.7 Installing or Removing a PMC Module

Before installing a PMC module, check that the VP 34x/02x board PMC V(I/O) voltage is configured to match the requirements of the PMC module.

CAUTION: If the VP 34x/02x is not correctly configured to match the PMC module V(I/O) requirements, it may result in damage to the module or the VP 34x/02x.

Setting the correct PMC V(I/O) voltage on the VP 34x/02x requires the positioning of a detachable polarizing key, and the setting of a board jumper. Figure 2-10 shows the location of the key for 3.3V V(I/O) or 5V V(I/O) configurations, and how to fit the PMC module to the VP 34x/02x board. Figure 2-11 shows the location and settings for the PMC V(I/O) jumper.

NOTE: The position of the polarizing key must correspond with the setting of the PMC V(I/O) jumper.

NOTE: The VP 34x/02x board is supplied with a PMC blanking plate which must be removed before a new module can be fitted.

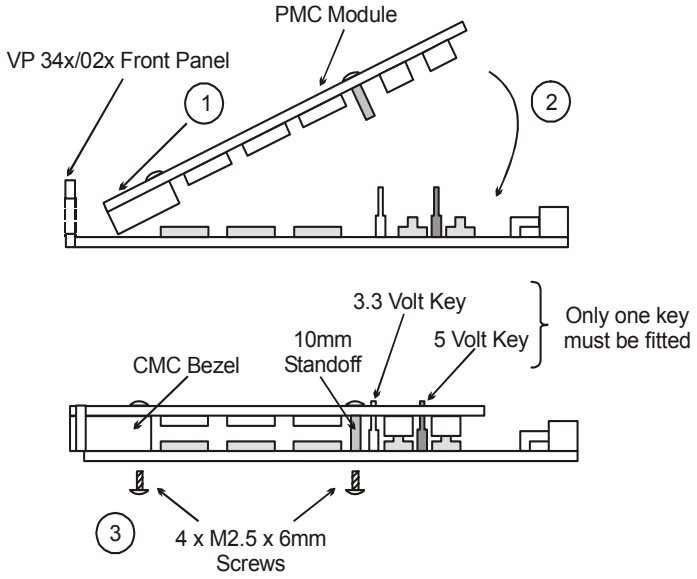


Figure 2-10 PMC Installation Diagram

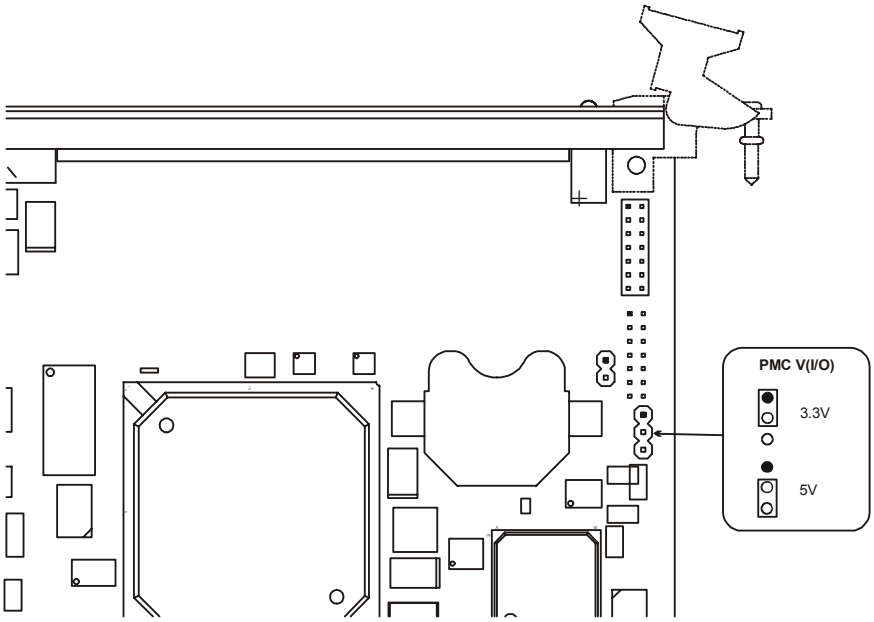


Figure 2-11 PMC V(I/O) Jumper

2.7.1 PMC Bus Speed Selection

When debugging a new PMC module or driver software, or to reduce the CPU load when the PMC module is operating at 66 MHz, it can sometimes be an advantage to reduce the PCI bus clock speed. A switch is provided to force the PCI bus connecting the PMC site, SCSI controller and the dual Ethernet controller to operate at 33 MHz. The location and settings of the PCI Speed Select switch are shown in Figure 2-12.

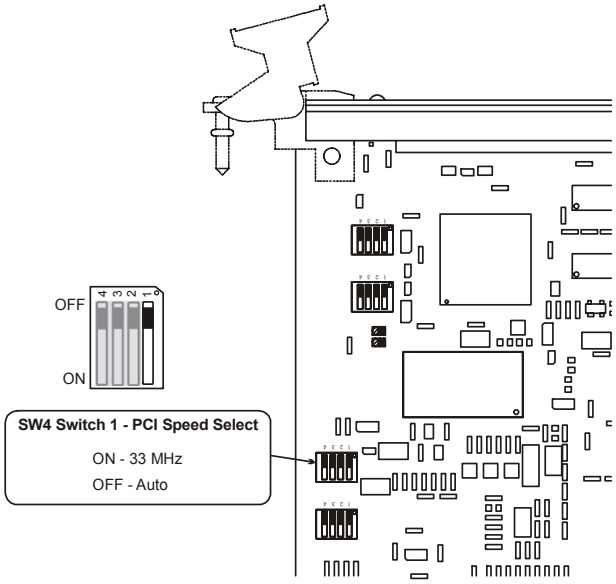


Figure 2-12 PCI Speed Select Switch

2.8 Installing the Board in a VME Backplane

Before the board is installed in a VME chassis, check the following points:

- When installing a variant of the board which is fitted with a P0 connector into a backplane which does not have the corresponding socket, check to see that no strengthening bars or other tall objects are present on the backplane before inserting the board. If bars or other objects are present then verify that the P0 connector and/or the backplane will not be damaged when the board is fully seated in the slot.
- The Power Supply Unit current capabilities. The board draws current primarily from the +5V rail, and the details are provided in Section A.4.
- The board can be installed in any standard VME slot. When installed in the first occupied slot the board will become the system controller.

2.8.1 Installing the Board

The board is installed and powered up as follows:

1) Make sure that system power is turned OFF (VCC_STANDBY may be left ON if used).
2) Slide the board into the designated slot, making sure that the board fits neatly into the runners.
3) Push the board into the card-cage until the P0, P1 and P2 connectors are firmly located. Use the ejector handles for the final push.
4) Screw the ejector handle retaining bolts into the holes in the chassis.
5) Connect the I/O cables to the connectors on the board's front panel and fix in place with the connectors' retaining screws.
6) If using a Breakout Module, install it at the rear of the backplane and connect the I/O cables.
7) Power-up the system. The following sequence of events should then occur:
8) The green "RUN" LED and the yellow "POST" LED on the front panel will light
9) The yellow "POST" LED will switch OFF

If power-up does not follow the sequence described above this will indicate that the board is not operational.

NOTE: This sequence of events assumes the VP 34x/02x has Concurrent Technologies standard BIOS firmware and that the board is configured to the factory settings described in Section 2.3.

2.8.2 Removing the Board

To remove the board, shut down the application and operating system software before powering down the system, unscrewing the ejector handle retaining bolts, opening the ejector handles and extracting the board.

CAUTION: The VP 34x/02x is not hot swappable. The main system power must be off before attempting to install or remove the board.

3 SOFTWARE INSTALLATION

In most cases, installing operating system software on the VP 34x/02x board follows the same sequence as installing on a PC. However, there are some additional points to note. The sections below summarize the special actions required for a few common operating systems.

3.1 Starting up for the First Time

Many operating systems running on the board will want to use the standard Real-Time Clock hardware. To maintain the date and time settings, and several other settings recorded by the PC BIOS, the battery must be fitted (or VCC_STANDBY connected). When the board is first powered up, or at the first power-up after changing the battery, carry out the following steps to set up the board.

1) Fit a battery as shown in Section 2.5 (if required).
2) Make sure that the Console Mode switch is set to the correct state for the console device which will be used (VGA monitor and keyboard, or serial terminal). Most operating systems which install on the target hardware will require a monitor and keyboard during installation, even if they can subsequently be re-configured to use only a serial terminal. See Section 7.1 for details of how to configure the board for this option.
3) Connect any additional modules and peripherals especially any mass storage devices.
4) Connect the console device and power up the board. Wait for the PC BIOS to sign on and run its memory test.
5) When the test finishes, the BIOS may report a setup or date/time setting error. If this occurs, press the <F2> key as soon as possible after the error is reported, and carry out the following:
6) Set the time and date by using the cursor keys to move around the screen and reading the help information in the right-hand screen panel.
7) When the time and date have been set, move the cursor to any other field on the same screen, then press the <F4> key to exit.
8) Press the ‘y’ key to accept the changes and restart.
9) The BIOS will then completely restart and re-run its memory test. This time it should complete and begin bootloading. To proceed with software installation, check that all necessary mass storage devices are connected before continuing with one of the sequences below.

3.2 Bootloading from CD-ROM or Floppy Disk

Operating systems which install on the target hardware will generally install from CD-ROM, or may require both a CD-ROM and floppy disk. Both Legacy and USB floppy drives are supported.

To use a USB floppy disk drive the USB interface must first be enabled in the BIOS. When the board boots and is running the memory test press <F2> to enter the BIOS setup.

Use the following procedure:

1) Disable Legacy Diskette A (Main Screen)
2) Disable Legacy Diskette B (Main Screen)
3) Enable the USB interface (Advanced | Advanced Chipset Control | ICH Control Sub-Menu)
4) Enable Legacy USB Support (Advanced Screen)

Press the <F4> key to exit and press the ‘y’ key to accept the changes and restart.

To bootload from CD-ROM, use the following procedure:

1) While the BIOS is running its memory test, press the <ESC> key.
2) Wait for the pop-up boot device menu to be displayed.
3) Select the CD-ROM drive using the cursor keys, then press the <Enter> key.

3.3 Installing Microsoft® Windows® Operating Systems

Installing these operating systems on the VP 34x/02x is generally very similar to installing them on a desktop PC. However, Concurrent Technologies also offers a Board Support Package on CD-ROM (part number CD WIN/VM1-L0) which provides installation and configuration information, including appropriate drivers. Please refer to your supplier for further details or to obtain this package.

3.4 Installing RedHat® Linux®

To install RedHat Linux from CD-ROM, set up the board initially using the steps outlined in Sections 3.1 and 3.2 above, ensuring that all the necessary drives are connected.

The standard distribution of RedHat Linux 8.0 does not currently handle the Intel Pentium M processor, so Concurrent Technologies can provide instructions and additional software to overcome this. In most respects, the installation process is the same as for a standard PC.

4 MASS STORAGE INTERFACES

The VP 34x/02x board has four interfaces which can be used to attach mass storage devices:

- A Primary EIDE (ATA100) interface is accessible via the VME P2 connector.
- A Secondary EIDE (ATA100) interface supporting the on-board Mass Storage option kits.
- A Serial ATA (SATA150) interface accessible in selected configurations only via the VME P0 connector.
- A single ended wide/narrow SCSI interface accessible via the VME P2 Connector.

The order in which the PC BIOS firmware tries to bootload from these drives can be changed via the BIOS Setup screen for **Boot**.

4.1 EIDE Interfaces

The board supports two EIDE (ATA100) interfaces.

The Primary EIDE interface connects via the VME P2 connector of the VP 34x/02x board, or through the Transition Module. Up to two EIDE peripherals may be connected to this interface. The BIOS Setup screens, for **Main | Primary Master** and **Main | Primary Slave** allow the user to see what is connected to this interface, and to select some characteristics of the drives manually. Normally the PC BIOS firmware will automatically determine the drive characteristics from the drives themselves.

The Secondary EIDE interface connects to the on-board 44-pin header for use by the optional Hard Disk or CompactFlash Mass Storage Kits. Up to two EIDE peripherals may be connected to this interface. The Hard Disk kit will appear as the Secondary Master device. The CompactFlash modules on the CompactFlash kit will appear as the Secondary Master and Secondary Slave devices.

Note that when using faster EIDE drives the overall cable length from the VP 34x/02x board to the drive furthest from the board must be kept as low as possible, and in any case no more than 18 inches or 450 mm. If this is not practical, it may be necessary to reduce the interface performance using the **UltraDMA Mode** and **Transfer Mode** fields of the BIOS Setup screens indicated above.

To achieve the faster speeds (above ATA33) via the Primary EIDE Interface it will also be necessary to use the correct (80-way) type of EIDE cable. Also, the **User** configuration and **UDMA 4** or **UDMA 5** speeds for the drive will need to be set by using the BIOS Setup screens for **Main | Primary Master** and **Main | Primary Slave** as appropriate. If one of the Concurrent Technologies P2/P0 breakout boards (see Appendix B) is being used, it will also be necessary to select the 80-way cable type using a jumper on the breakout board. Selection of the fastest speed for the Secondary (on-board) EIDE interface is automatic.

Either or both of the EIDE interfaces may be enabled using the BIOS Setup options for **Advanced | Parallel ATA**.

4.2 Serial ATA Interface

Two Serial ATA (SATA150) interfaces are supported, and are accessed via the P0 connector in selected board configurations.

The Serial ATA interface may be enabled or disabled via the BIOS Setup options for **Advanced | Serial ATA.**

4.3 SCSI Interface

An LSI Logic 53C1020 Ultra320 Wide SCSI controller is supported, though in this application its speed is limited due to the restricted number of pins available to connect the SCSI bus. This controller was selected for long-term supply reasons. The interface may be configured for wide (16 bits) or Narrow (8 bits) Single-Ended operation with transfer rates up to 40 Mbytes/s. The interface is accessible via the P2 connector in selected board configurations.

Active terminations are provided which may be set via DIL switches to provide appropriate termination for the system configuration. These are shown in Figure 4-1.

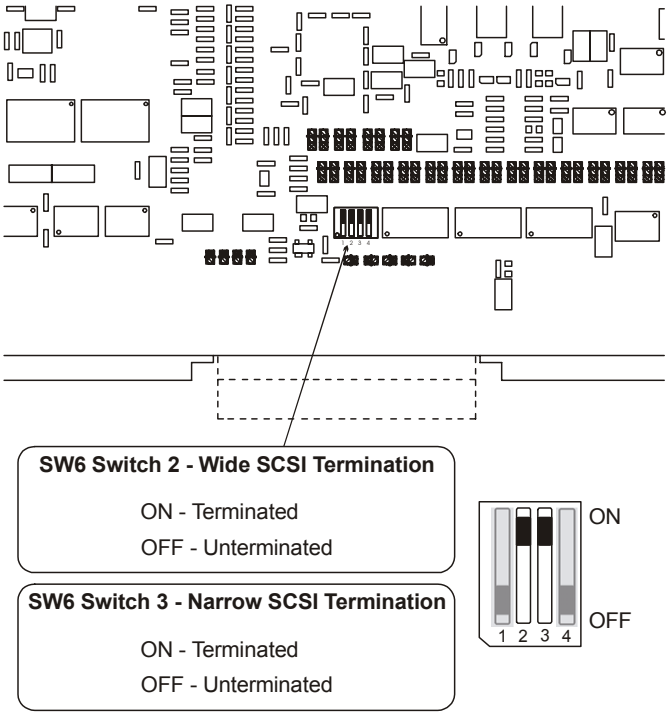


Figure 4-1 SCSI Interface Termination Options

Termination power is always supplied by this board.

The Termination is selectable for narrow and wide bus connections. Each termination should be set to terminate if the card is at the end of the appropriate SCSI bus. Otherwise it should be set to the unterminated position. The wide termination should also be enabled if a narrow cable is being used.

The narrow termination terminates the lower data bus bits 7 to 0 & Parity along with all control signals. The wide termination terminates the upper data bus and parity only.

The SCSI interface is capable of transferring 20 Mbytes/s in narrow mode or 40 Mbytes/s in wide mode.

NOTE: This interface is only available for boards configured for SCSI. This is a build time option and must be specified when the board is ordered. Refer to the VP34x/02x Datasheet for ordering details.

NOTE: The default setting for the PC BIOS disable the execution of an additional SCSI BIOS extension at startup. If the SCSI interface is to be used in any mode, the SCSI BIOS extension should be enabled via the BIOS setup option for
`Main | Boot Options | SCSI BIOS Firmware`

5 ETHERNET INTERFACES

The VP 34x/02x board is fitted with two independent Ethernet interfaces, implemented with a single Intel 82546GB controller.

It is possible to bootload the board through the Ethernet interfaces by setting appropriate BIOS configuration options. See Section 10.3 for more details.

5.1 Ethernet Channel 0

Ethernet Channel 0 is wired to a front panel RJ45 Ethernet connector. Speeds of 10, 100 and 1000 Mbits/s are supported.

5.2 Ethernet Channel 1

Ethernet channel 1 is wired to a front panel RJ45 Ethernet connector. Speeds of 10, 100, and 1000 Mbits/s are supported.

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6 VME INTERFACE

The VP 34x/02x board is fitted with a Tundra Universe II PCI-to-VME bus bridge device together with additional support logic. This hardware implements a flexible interface to and from the VME bus with the following key characteristics.

6.1 VME Bus Interface Features

The VP 34x/02x can be programmed as a VME master supporting off-board VME memory addressing accessible by any PCI bus master. The VP 34x/02x can also be programmed as a VME slave allowing other VME masters to access any PCI bus slave. This access is achieved by programming the appropriate Universe II device register. “PCI slave” registers are used for VP 34x/02x master accesses and “VME slave” registers for VME accesses to the VP 34x/02x.

The VME interface supports A32/A24/A16/MBLT64 addressing modes and D64/D32/D16/D08 (EO) data widths in both user and supervisor address space.

The VME interface performs auto-syscon detect at power up to provide system controller functionality, if the board is located in the first occupied VME slot. As system controller the Universe II will arbitrate VME mastership of the bus using DEMAND request mode.

The VP 34x/02x can act as an interrupt controller for any combination of VME interrupts and can be an interrupter generating either a software interrupt or any of the Universe’s internal interrupt sources on any IRQ level. All VME interrupts are directly mapped between the Universe II registers and the VME bus backplane. Of the PCI LINT lines only LINT0 is mapped into the PCI interrupt and LINT1 is mapped to NMI.

The Universe II device uses the linear incrementing mode when being accessed by a PCI master. The Universe II supports VME mailbox interrupts. See the Universe II data sheet for further details.

WARNING: VME bus access is allowed to the full VP 34x/02x memory map. Care must be taken to ensure that no accesses are made to areas that will corrupt the system memory or the configuration of any of the interfaces.

The PC BIOS firmware fitted to this board includes several setup screens which allow up to 4 PCI Slave and VME Slave access windows to be configured. The configuration is retained in Flash EPROM and is programmed automatically into the Universe II chip when the board starts up. This allows basic access to or from the VME bus to be established without the need to write any operating software for the board, or for the Universe II chip. For further details, refer to the BIOS setup screens for the **`Universe`**, **`Universe|PCI Slave`** and **`Universe|VME Slave`** options.

The VP 34x/02x board will assert the VME SYSFAIL signal after a power-on or system reset. In some cases it may be desirable to deactivate this signal early in the boot process, while in others it can be left to the operating software to do this at a later stage. The SYSFAIL signal is controlled by the Universe II chip. The PC BIOS provides a user setup option to allow this signal to be deactivated by the BIOS itself during its initialization sequence, or to simply leave it unchanged after the restart. In the latter case, SYSFAIL will remain asserted until the operating software deactivates it. The setup option is provided on the menu for **`Universe`**.

6.2 VME Byte Swapping

The VP 34x/02x provides hardware that performs fast byte swapping for aligned D16, D32 and D64 VME transfers. Byte swapping can be enabled separately for master and slave transfers under software control, using Status & Control Register 0 (see Section 9.2 for further details). Swapping is performed as follows:-

D16 (Double Byte 2 - 3):

D[31...24]	< - >	D[23...16]
D[23...16]	< - >	D[31...24]

D16 (Double Byte 0 - 1):

D[15....8]	< - >	D[7.....0]
D[7.....0]	< - >	D[15....8]

D32 (Quad Byte 0 - 3):

D[31...24]	< - >	D[7....0]
D[23...16]	< - >	D[15....8]
D[15....8]	< - >	D[23...16]
D[7.....0]	< - >	D[31...24]

D64 (Octal Byte 0 - 7):

D[63...56]	< - >	D[39...32]
D[55...48]	< - >	D[47...40]
D[47...40]	< - >	D[55...48]
D[39...32]	< - >	D[63...56]
D[31...24]	< - >	D[7…...0]
D[23...16]	< - >	D[15.....8]
D[15....8]	< - >	D[23...16]
D[7.....0]	< - >	D[31...24]

The hardware decodes the VME transfer taking place to see if it is swappable, checks to see if swapping is enabled and then configures a set of multiplexors to perform the required data swap. For master and slave read cycles the byte swap hardware imposes negligible delay on the VME bus cycle since the decode and configuration occur before the data is valid. For write cycles the hardware imposes an approximate delay of 50ns in order to provide the required setup time before the data strobes are asserted. The delay applies to single cycle transfers and the first cycle of block transfers.

NOTE: The delay can be turned off under software control, but only if the user can guarantee that only swappable cycles will be run across the VME interface.

6.3 VME Bus Error Interrupt

The VP 34x/02x contains hardware to detect bus errors for VME bus cycles in which the Universe is the bus master. The hardware is controlled by Status and Control register 1 (see Section 9.3). The bus error interrupt is connected to the Universe LINT0 interrupt, so software to deal with the VME bus error interrupt can be added to the normal Universe interrupt handler.

6.3.1 VME Bus Error Detection Example Code

The following code fragments show how the system software can, by using the on-board hardware, detect and handle bus errors occurring in coupled bus cycles on the VME bus when the Universe peripheral is the VME bus master. A VME bus error is generated when the slave device fails to complete the bus transaction within the nominal bus error timeout period (default value approximately 64ms).

The VME Bus Error Detection control and status flags are in Status and Control register 1 and defined thus:

```
/* Status and Control Register 1's aliases */
#define STATCTL_1                  (0x0212U)
#define SC1_BUS_ERROR                (0x20U)
#define SC1_BUS_ERRINT_ENABLE        (0x10U)
```

The code fragment to poll for VME bus errors is:

```
if ((inbyte (STATCTL_1) & SC1_BUS_ERROR) == SC1_BUS_ERROR)
{
    /*
     * a VME bus error has been detected — simply clear the
     * error condition by resetting the VME bus error flag in
     * Status/Control Register 1, thus:
     */
    outbyte (STATCTL_1, inbyte (STATCTL_1) & ~SC1_BUS_ERROR);
}
```

It may be convenient to generate an interrupt when a VME bus error occurs and the following code fragment shows how the interrupts are enabled.

```
outbyte (STATCTL_1, inbyte (STATCTL_1) | SC1_BUS_ERRINT_ENABLE);
```

The following code fragment shows only the basic interrupt handling function to process the VME bus error interrupt.

```
#pragma interrupt (vInterruptHandler)
static void vInterruptHandler (void)
{
    /*
     * clear the source of the interrupt by resetting the VME
     * bus error flag in Status / Control Register 1, thus:
     */
    outbyte (STATCTL_1, inbyte (STATCTL_1) & ~SC1_BUS_ERROR);
    /*
     * perform relevant actions to acknowledge the interrupt
     * in the PIC, etc ...
     */
```

6.4 VME Address Capture

The VP 34x/02x provides hardware that captures the VME address and upon a VME Bus Error cycle. The captured data consists of the A31-A0, DS1-0, AM5-0, LWord and WR signal states.

A single register at I/O address 0213h controls this function. The register provides access to the captured information via a series of read cycles as shown in Table 6-1. Three control bits are also defined, which permit the capture mode to be enabled, the read sequence to be reset and a capture to be aborted.

The Bus Error event may be detected by means of the Bus Error Interrupt or by polling the VME Address Capture status bit. When using the Bus Error Interrupt with the VME Address Capture, these functions must be enabled together and outside the monitored transfer. This will permit both functions to detect the Bus Error event.

The VME Bus Error Interrupt does not have to be enabled for the VME Address Capture to operate. The VME Address Capture Function must be enabled via bit 0 of the VME Address Capture Control register.

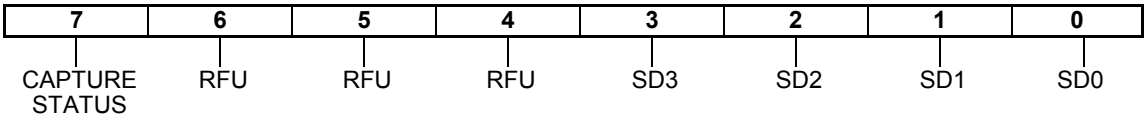
To ensure the VME address information is read from the start following a capture, the read data sequence must be reset back to the start prior to the read activity. The internal read sequence counter is advanced for every read of the VME Address Capture Status register. To reset the read sequence a write of 0x02 is performed to the control register.

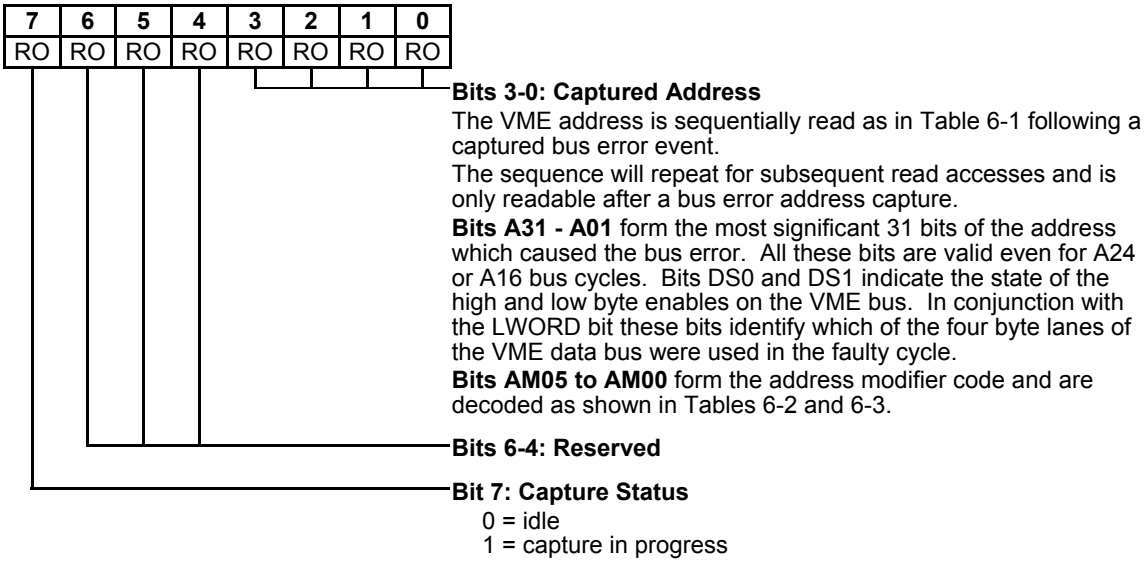
The VME address information is valid when the Capture Status bits indicates Idle following a Bus Error event. A read of the VME address at any other time or following a capture abort is invalid.

See Section 6.4.3 for some example code showing how to enable the VME Address Capture Function and how to retrieve the address information.

6.4.1 VME Address Capture Read Register (Read Only)

This register is at I/O address 213h.





SD3	SD2	SD1	SD0	Read Cycle
A31	A30	A29	A28	1
A27	A26	A25	A24	2
A23	A22	A21	A20	3
A19	A18	A17	A16	4
A15	A14	A13	A12	5
A11	A10	A09	A08	6
A07	A06	A05	A04	7
A03	A02	A01	LWORD	8
DS1	DS0	AM05	AM04	9
AM03	AM02	AM01	AM00	10
WR	XX	XX	XX	11
XX	XX	XX	XX	12
XX	XX	XX	XX	13
XX	XX	XX	XX	14
XX	XX	XX	XX	15
XX	XX	XX	XX	16

Table 6-1 VME Address Capture Read Register

AM05	AM04	AM03	AM02	AM01	AM00	Hex	Access Type
0	0	0	0	0	0	00	A64 64-bit MBLT
0	0	0	0	0	1	01	A64 single transfer
0	0	0	0	1	0	02	RFU
0	0	0	0	1	1	03	A64 BLT
0	0	0	1	0	0	04	A64 lock command (LCK)
0	0	0	1	0	1	05	A32 lock command (LCK)
0	0	0	1	1	0	06	RFU
0	0	0	1	1	1	07	RFU
0	0	1	0	0	0	08	A32 non-privileged 64-bit MBLT
0	0	1	0	0	1	09	A32 non-privileged data
0	0	1	0	1	0	0A	A32 non-privileged program
0	0	1	0	1	1	0B	A32 non-privileged BLT
0	0	1	1	0	0	0C	A32 supervisory 64-bit MBLT
0	0	1	1	0	1	0D	A32 supervisory data
0	0	1	1	1	0	0E	A32 supervisory program
0	0	1	1	1	1	0F	A32 supervisory BLT
0	1	0	0	0	0	10	User-defined
0	1	0	0	0	1	11	User-defined
0	1	0	0	1	0	12	User-defined
0	1	0	0	1	1	13	User-defined
0	1	0	1	0	0	14	User-defined
0	1	0	1	0	1	15	User-defined
0	1	0	1	1	0	16	User-defined
0	1	0	1	1	1	17	User-defined
0	1	1	0	0	0	18	User-defined
0	1	1	0	0	1	19	User-defined
0	1	1	0	1	0	1A	User-defined
0	1	1	0	1	1	1B	User-defined
0	1	1	1	0	0	1C	User-defined
0	1	1	1	0	1	1D	User-defined
0	1	1	1	1	0	1E	User-defined
0	1	1	1	1	1	1F	User-defined

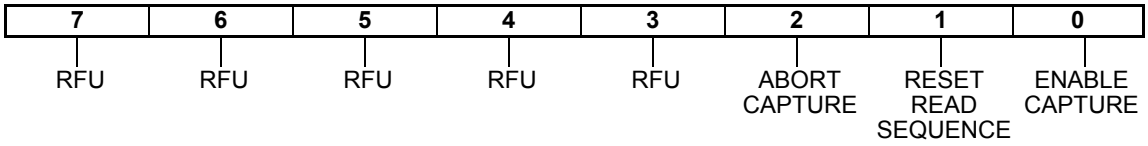
Table 6-2 VME Address Modifier Codes

AM05	AM04	AM03	AM02	AM01	AM00	Hex	Access Type
1	0	0	0	0	0	20	RFU
1	0	0	0	0	1	21	RFU
1	0	0	0	1	0	22	RFU
1	0	0	0	1	1	23	RFU
1	0	0	1	0	0	24	RFU
1	0	0	1	0	1	25	RFU
1	0	0	1	1	0	26	RFU
1	0	0	1	1	1	27	RFU
1	0	1	0	0	0	28	RFU
1	0	1	0	0	1	29	A16 non-privileged
1	0	1	0	0	0	2A	RFU
1	0	1	0	0	1	2B	RFU
1	0	1	1	1	0	2C	A16 lock command (LCK)
1	0	1	1	1	1	2D	A16 supervisory
1	0	1	1	1	0	2E	RFU
1	0	1	1	1	1	2F	Control/Status register
1	1	0	0	0	0	30	RFU
1	1	0	0	0	1	31	RFU
1	1	0	0	1	0	32	A24 lock command (LCK)
1	1	0	0	1	1	33	RFU
1	1	0	1	0	0	34	RFU
1	1	0	1	0	1	35	RFU
1	1	0	1	1	0	36	RFU
1	1	0	1	1	1	37	RFU
1	1	1	0	0	0	38	A24 non-privileged 64-bit MBLT
1	1	1	0	0	1	39	A24 non-privileged data
1	1	1	0	1	0	3A	A24 non-privileged program
1	1	1	0	1	1	3B	A24 non-privileged BLT
1	1	1	1	0	0	3C	A24 supervisory 64-bit MBLT
1	1	1	1	0	1	3D	A24 supervisory data
1	1	1	1	1	0	3E	A24 supervisory program
1	1	1	1	1	1	3F	A24 supervisory BLT

Table 6-3 VME Address Modifier Codes (continued)

6.4.2 VME Address Capture Control Register (Write Only)

This register is at I/O address 213h.



7	6	5	4	3	2	1	0
WO	WO	WO	WO	WO	WO	WO	WO

Bit 0: Enable Capture
0 = no action
1 = enable capture for a subsequent VME bus error

NOTE: It is recommended that the bus error interrupt is used to give notification of the bus error event.

Bit 1: Reset Read Sequence
0 = no action
1 = reset captured address read access sequence to entry 1

Bit 2: Abort Capture
0 = no action
1 = Abort Current Capture (following this action all VME address information is invalid)

Bits 7-3: Reserved

6.4.3 VME Bus Error Address Capture Example Code

The following code extracts demonstrate how the VME Address Capture registers may be used to report the VME address where a bus error occurred.

The VME Address Capture register would normally be read following a bus error interrupt.

Register bit-field defines:

```
#define VME_ADR_CAP_WR     0x0213 /* VME Address Capture Write Register */
#define VME_ADR_CAP_RD     0x0213 /* VME Address Capture Read Register */

#define VME_ABORT_CAPTURE  0x04   /* Abort Capture (Write Register) */
#define VME_RESET_CAPTURE  0x02   /* Reset Read Sequence (Write Register) */
#define VME_ENABLE_CAPTURE 0x01   /* Enable Capture (Write Register) */

#define VME_CAPTURE_STATUS 0x80   /* Capture Status (Read Register) */
#define VME_CAPTURE_DATA   0x0F   /* Data Mask (Read Register) */

#define LEN_ADR_SEQ        16     /* length of address capture sequence */
```

Enable the address capture logic:

```
outbyte (VME_ADR_CAP_WR, VME_ENABLE_CAPTURE);
```

Read the faulting address following a bus error interrupt:

```
UINT32  dCapturedAddress;
UINT16  wTimeout;
UINT8   abCapture [LEN_ADR_SEQ];
UINT8   bIndex;

/* Wait for address capture to complete by polling the Capture
 * Status bit in the read register
*/

wTimeout = 100;

while ( ((inbyte (VME_ADR_CAP_RD) & VME_CAPTURE_STATUS) != 0)
            && --wTimeout > 0)
{
    CFS_delay (1);
}

/* Read the captured address, providing capture completed */

if ((inbyte (VME_ADR_CAP_RD) & VME_CAPTURE_STATUS) == 0)
{
/* Reset the read sequence to ensure the first read returns A31-A28 */

    outbyte (VME_ADR_CAP_WR, VME_RESET_CAPTURE);

    /* Read in the captured address and status nybles */

    for (bIndex = 0; bIndex < LEN_ADR_SEQ; bIndex++)
        abCapture [bIndex] = inbyte (VME_ADR_CAP_RD) & VME_CAPTURE_DATA;

    /* Assemble the error address */

    dCapturedAddress = abCapture[0] * 0x10000000L +    /* A31 - A28 */
                       abCapture[1] * 0x1000000L +     /* A27 - A24 */
                       abCapture[2] * 0x100000L +      /* A23 - A20 */
                       abCapture[3] * 0x10000L +       /* A19 - A16 */
                       abCapture[4] * 0x1000L +        /* A15 - A12 */
                       abCapture[5] * 0x100L +         /* A11 - A8  */
                       abCapture[6] * 0x10L +          /* A7  - A4  */
                      (abCapture[7] & 0xFE);           /* A3  - A1  */
}
```

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7 OTHER INTERFACES

Many additional standard interfaces are provided on the VP 34x/02x board. These interfaces consist primarily of those found in a regular desktop or mobile PC, and are outlined below.

7.1 Serial Ports

Two serial interfaces are provided, and connect via the front panel. The serial ports are implemented in the PC chipset used on the board, using standard 16550-style devices. The serial lines may be configured for speeds up to 115kbaud.

With some operating systems, or in some applications, it is preferable to use a serial terminal as an operator console device for the board. In this case, it will be necessary to configure the board for operation with a Serial Console. When configured in this mode, the PC BIOS firmware will re-direct its output to a COM port, and similarly will take its input from this port, rather than using the VGA screen and PC keyboard. A board DIL switch must be set to select this mode, as shown in Figure 7-1 below.

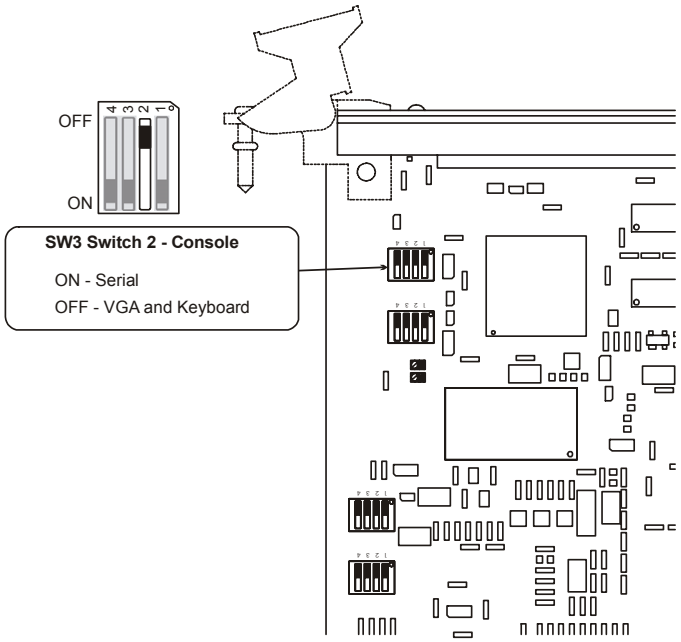


Figure 7-1 Console Mode Switch

The serial line speed used for the Serial Console mode may be selected from the BIOS Setup screen for **`Main | Boot Options`** configuration.

7.2 Keyboard and Mouse Ports

A 6-way Mini-DIN connector on the front panel of the board provides connections for a PC keyboard and a PS/2 mouse. The pin-out of the front panel connector is detailed in Section A.5.8.

A splitter cable is required to access the mouse interface.

Power for the keyboard and mouse interfaces is protected by a self-resetting current limiting circuit. To reset this circuit power the board off, remove and replace the faulty keyboard or mouse device, then power up again.

NOTE: External devices that derive power from the keyboard/mouse interface may be used provided that the total current taken by all devices is less than 500mA.

7.3 Graphics (VGA) Controller

A graphics controller is integrated into the 855GME GMCH. It uses up to 64 Mbytes of UMA RAM, and supports many different modes of operation, including VGA and SVGA, with resolutions up to 2048 x 1536 and color depths up to 24-bits (16 million colors). The analog CRT interface is available on a 15-way High Density D-Type front panel connector.

See also Section 7.1 for information about how to switch the PC BIOS console device between VGA screen and keyboard, and a serial port.

The VGA interface is also available as a digital flat panel interface via P2. This interface can be used to display the same screen as the VGA interface or it can display another independant screen. Operation in dual screen mode is dependant on the drivers for the operating system supporting this function.

7.4 Real-Time Clock

A conventional PC Real-Time Clock is included on this board. This is Year 2000 compliant and can be powered by an on-board Lithium battery when main power to the board is removed. See Section 2.5 for more details of how to fit or replace the battery. The Clock device also provides 242 bytes of CMOS RAM, in which the PC BIOS keeps much of its setup screen data and other information. To allow for the case where no battery supply is present, the BIOS Setup data can be saved in Flash EPROM and restored as default values when the BIOS runs again at power-up or after reset. See Section 10.5 for further details.

Alternatively the CMOS settings and Real-Time clock can be maintained in the absence of power by connecting a 5V source to the VMEbus VCC_STANDBY input.

7.5 Universal Serial Bus (USB)

Four USB 2.0 interfaces are provided on this board. One channel is routed to the front panel connector, the other channels connect to the P2 connector. All channels can operate at 1.5Mbits/s, 12Mbits/s or 480Mbits/s. The PC BIOS firmware supports bootloading via any of these ports.

Power for the Front Panel USB interface is protected by a self-resetting current limiting circuit. To reset this circuit power the board off, remove and replace the faulty device, then power up again.

Power for the P2 USB interfaces is protected by a self-resetting current limiting circuit on the Breakout Module. To reset this circuit power the board off, remove and replace the faulty device, then power up again.

NOTE: External devices that derive power from the USB interfaces may be used provided that the total current taken by all devices is less than 500mA per interface.

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8 FLASH EPROM AND DRAM

8.1 Firmware Hub Flash EPROM

The VP 34x/02x is fitted with one Flash EPROM part, namely an Intel 82802AC8 or equivalent Firmware Hub (FWH). This device is not socketed and is programmed at the factory with PC BIOS and factory test firmware. This EPROM will not normally be reprogrammed by the user, but Concurrent Technologies has programming software which allows BIOS updates to be carried out in the field when necessary, perhaps to add new features. Contact Concurrent Technologies for a copy of this software, and for the BIOS reprogramming information, if you believe that such an update is required.

Also programmed into the FWH at the factory is a Recovery BIOS, which allows the board to be restarted in a basic functional mode even if the main BIOS firmware has been corrupted. See Section 10.6 for further details of this feature.

The lower part of the FWH device is used by Concurrent Technologies for storage of factory test firmware. The user may overwrite the factory test firmware if desired, but should be aware that it may be re-instated if the board is ever returned to Concurrent Technologies for repair or upgrading.

A switch is provided to protect the top block of the Firmware Hub Flash device against accidental erasure or programming. It is recommended to leave this switch in the locked position. Refer to Figure 8-1 for the switch settings.

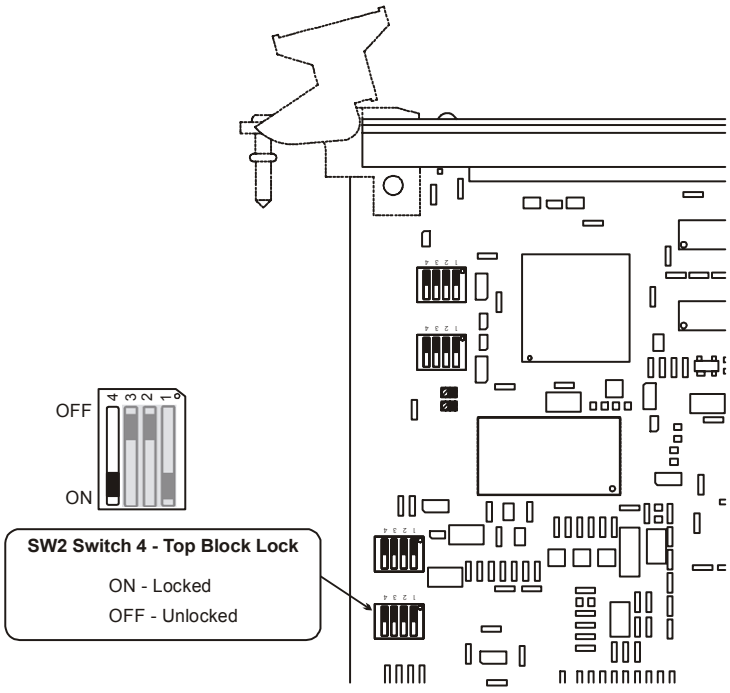


Figure 8-1 Top Block Lock Switch

8.2 DRAM

The VP 34x/02x board supports a large amount of ECC DDR SDRAM. The board comes with 512 Mbytes or 1Gbyte of on-board memory as standard. A further 512 Mbytes or 1Gbytes of SODIMM memory may be fitted giving a maximum size of 2 Gbytes. The DRAM can be accessed from the processor, the local PCI busses and the VME backplane.

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9 ADDITIONAL LOCAL I/O FUNCTIONS

The VP 34x/02x supports a variety of I/O functions whose addresses are summarized in Table 9-1.

I/O Address Range	Description
0000-001Fh	DMA Controller (6300ESB)
0020-002Dh	Interrupt Controller (6300ESB)
002E-002Fh	Configuration Index & Data Registers (Super I/O)
0030-003Dh	Interrupt Controller (6300ESB)
0040-0043h	PIT Timers (6300ESB)
0050-0053h	PIT Timers (6300ESB)
0060h	Keyboard Controller
0061h	NMI Status (6300ESB)
0064h	Keyboard Controller
0070h	NMI Enable/RTC Address (6300ESB)
0071h	RTC Data (6300ESB)
0080h	Port 80 Debug Port
0092h	Port 92 Reset Generator (6300ESB)
00A0-00A1h	Slave Interrupt Controller (6300ESB)
00C0-00DFh	Slave DMA Controller (6300ESB)
00F0h	Maths Coprocessor Error
0210-021Fh	Control & Status Registers, Long Duration Timer (CPLDs)
02F8-02FFh	COM2 Serial (6300ESB)
03BC-03BFh	Parallel Port LPT1 (Super I/O)
03F0-03F7h	Floppy Controller (Super I/O)
03F8-03FFh	COM1 Serial (6300ESB)
04D0-04D1h	Interrupt Control (6300ESB)
0CF8-0CFFh	PCI Configuration Registers (855GME)
0D00-FFFFh	PCI Free I/O Space

Table 9-1 I/O Address Map

Most of the addresses are standard PC-AT compatible values, but at address 0210-021Fh the board provides custom Status & Control registers for the board specific features.

ADDITIONAL LOCAL I/O FUNCTIONS

9.1 Onboard Status & Control Registers

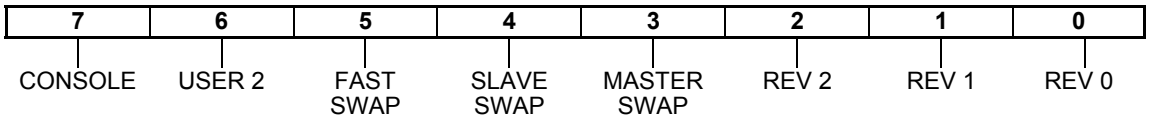
There are 11 byte wide status and control registers. They are accessed at the following I/O addresses:

- 210h for Status & Control Register 0
- 211h for Status & Control Register 2
- 212h for Status & Control Register 1
- 213h for VME Address Capture Registers
- 217h for Status & Control Register 3
- 218h for Long Duration Timer LS byte
- 219h for Long Duration Timer Mid Low byte
- 21Ah for Long Duration Timer Mid High byte
- 21Bh for Long Duration Timer MS byte
- 21Ch for Long Duration Timer Status & Control Register
- 21Dh for Status & Control Register 4

The functions provided by the VME Address Capture Data & Control registers are described in Chapter 6. The functions of the remaining registers are detailed in the following sections.

9.2 Status & Control Register 0

This register is at I/O address 210h.



7	6	5	4	3	2	1	0
RO	RO	R/W	R/W	R/W	RO	RO	RO

Bits 2 - 0: Hardware Revision Strapping

000 = Rev A
001 = Rev B, etc...

Bits 5 - 3: VME Hardware Byte Swapping

Bit 3: VME byte swapping for master (0 = off, 1 = on)
Bit 4: VME byte swapping for slave. (0 = off, 1 = on)
Bit 5: VME fast byte swapping, i.e. partial cycle type decode (0 = off, 1 = on).

Byte swapping is only supported for aligned transfers, 64-bit transfers are treated as dual 32-bit transfers. When swapping is enabled, the hardware will normally decode the VME cycle type as it takes place to determine if swapping is possible. It then configures a set of multiplexors to perform the swap. To meet the VME bus timing specifications for write cycles it is necessary to delay the cycle while the multiplexors are configured. Setting bit 5 of this register turns off the delay, but should only be done if all VME cycles are guaranteed swappable. See Section 6.2 for more details.

Bit 6: User 2 Switch

This bit indicates the setting of the User 2 switch, which is provided for any application-defined purpose.

0 = switch is OFF
1 = switch is ON

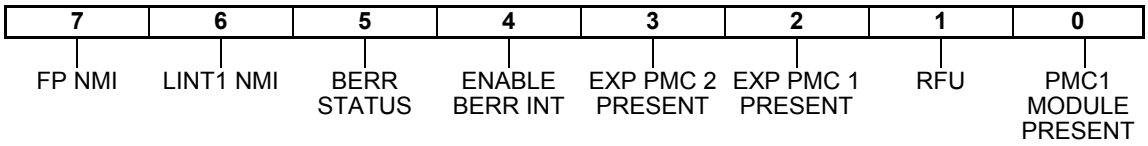
Bit 7: Console Mode Switch

This bit indicates the setting of the Console Mode switch, which is used to define the BIOS default standard input/output mode. See Section 7.1 for more details.

0 = input via keyboard/output via VGA Controller
1 = input/output via selected COM Port

9.3 Status & Control Register 1

This register is at I/O address 212h.



7	6	5	4	3	2	1	0
R/C	RO	R/C	R/W	RO	RO	RO	RO

Bit 0: PMC Module Present

These bits indicate whether or not a PMC module is present on the board.

0 = No PMC module present
1 = PMC module present

Bit 1: Reserved

Bits 3-2: Carrier Expansion PMC Module Present

Bits 2 and 3 indicate whether or not a PMC module is present on sites 1 and 2 of a PMC carrier connected via the 32-bit expansion interface.

0 = No PMC module present
1 = PMC module present

Bit 4: VME Bus Error Interrupt Enable

0 = VME bus error interrupt disabled
1 = VME bus error interrupt enabled

Bit 5: VME Bus Error Flag

This flag is set by a bus error occurring during a cycle in which the Universe is VME bus master. The bit can be cleared by writing to the register with a zero in its bit position. This should be done as part of the VME bus error interrupt routine.

0 = VME bus error has not occurred
1 = VME bus error has occurred

Bit 6: LINT1 from the Universe is the cause of NMI

This bit is set by the Universe and should be cleared by writing to the appropriate Universe register.

0 = LINT1 has not occurred
1 = LINT1 has occurred

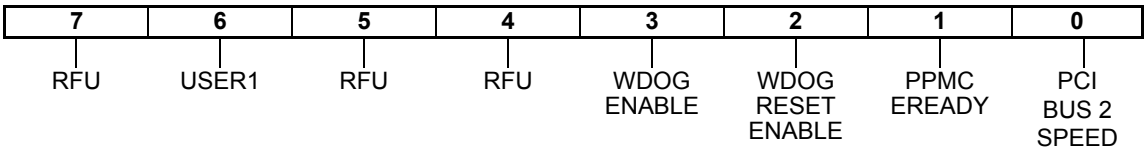
Bit 7: Front Panel Switch is the cause of NMI

0 = event has not occurred
1 = event has occurred

Writing zero to this bit will clear it to zero, writing one will leave it unchanged.

9.4 Status & Control Register 2

This register is at I/O address 211h.



7	6	5	4	3	2	1	0
RO	RO	RO	RO	RO	R/W	RO	RO

Bit 0: PCI Bus 2 Speed
This bit indicates if an on-board PMC module or PCI Speed Select switch has forced the PCI bus (number 2) to 33 MHz operation. By default the bus speed will be 66 MHz.
0 = Bus speed is 33 MHz
1 = Bus Speed is 66 MHz

Bit 1: Processor PMC EREADY
1 = Processor PMC module ready for enumeration.

Bit 2: Watchdog Reset Enable
This bit enables the Watchdog reset of the board. It will override any settings in the 6300ESB ICH.
0 = Watchdog reset disabled
1 = Watchdog reset enabled

Bit 3: Watchdog Enable Switch
This bit reflects the setting of the Watchdog enable switch. User code or the BIOS will use the status of this switch to configure the Watchdog in the 6300ESB ICH.
0 = Disable Watchdog
1 = Enable Watchdog

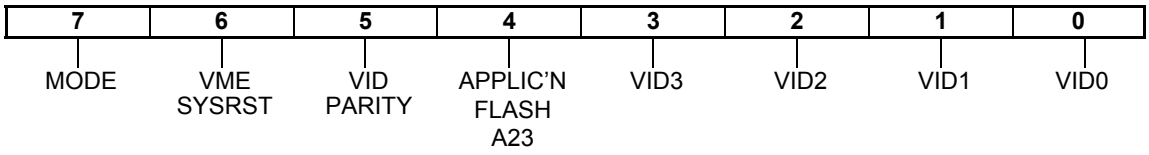
Bits 5-4: Reserved
These bits are reserved for future use. Always read as '0'.

Bit 6: User 1 Switch
This bit indicates the setting of the User 1 switch, which is provided for any application-defined purpose.
0 = switch is OFF
1 = switch is ON

Bit 7: Reserved
This bit is reserved for future use. Always reads as '0'.

9.5 Status & Control Register 3

This register is at I/O address 217h.



7	6	5	4	3	2	1	0
RO	R/W	RO	RO	RO	RO	RO	RO

Bits 4-0: VME Slot ID
The VME slot ID (VME connector P1 pins GA4# to GA0#) can be read via these bits.

Bit 5: VME Slot ID Parity
Parity bit for the VIDn bits (VME connector P1 pin GAP#).

Bit 6: VME System Reset Enable
This bit controls the effect of the SYSRESET# input from the VME Bus.
0 = System Reset is disabled (default)
1 = System Reset is enabled

Bit 7: Mode Switch
This bit indicates the setting of the Mode switch, which is used to define the operating mode following a reset. See Section 10.1 for further details.
0 = VSA operation
1 = BIOS operation

9.6 Status & Control Register 4

This register is at I/O address 21Dh.

7	6	5	4	3	2	1	0
RFU	GPIO2 DIR	GPIO1 DIR	GPIO0 DIR	RFU	GPIO2 DATA	GPIO1 DATA	GPIO0 DATA

Three general purpose I/O (GPIO) signal lines are provided on this board. Two of these (GPIO0 and GPIO1) are connected to pins on the P2 connector. GPIO2 is only connected on-board to the User LED. GPIO1 and GPIO0 are connected to individual on-board switches and pull-up resistors. Each line also has a direction control (bits 6-4 of this register), allowing them to be individually specified as inputs or outputs (GPIO2 must only be configured as an output).

If a GPIO line is configured as an input, it can either report the switch setting or the external signal status. To allow the external signal status to be reported, the appropriate switch (see Figure 2-2) must be set to OFF. To allow the switch status to be reported, the external signal must not be connected. In this case, status bits 1-0 of this register are set as follows:

0 = switch is ON
1 = switch is OFF

NOTE: This is the opposite logic to User Switch 1 and 2

7	6	5	4	3	2	1	0
R/W	R/W	R/W	R/W	RO	R/W	R/W	R/W

Bits 1-0: GPIO1-0 Data
Data written to these bits will be output on the GPIO pins when the direction is set for output. Reads of these bits will read the data present on the GPIO pins.

Bit 2: GPIO2 Data
Data written to this bit will be output to the User LED when the direction is set for output. A logic 0 will light the LED. Reads of this bit will read the data written to this location.

NOTE: When the User LED is configured for Processor Hot indication (see Section 13.3), writes to this bit will have no effect on the User LED. Reads will still reflect the last data written.

Bit 3: Reserved
Reads as a zero.

Bits 6-4: GPIO Direction
These bits set the data direction for GPIO pins 2-0 respectively.
0 = pin is an input
1 = pin is an output

NOTE: GPIO2 Direction is permanently set to a 1 (output) and can not be changed.

Bit 7: Reserved
Should only be written as zero.

9.7 PORT 80

A header has been provided for monitoring data written to I/O Port 80. The PC BIOS writes status bytes to Port 80 that indicate a boot progress status and/or highlight any faults found. Data written to this port can be monitored using a Logic State Analyzer (LSA) or seven segment hexadecimal displays. See Section A.5.13 for details of the connector used for this port.

After boot-up this port can be used to monitor other status bytes written to port 80, which can be useful for debug purposes.

9.8 Watchdog Timer

The VP 34x/02x board includes a hardware Watchdog timer which can be used by the operating software to monitor the normal operation of the system. The timer is enabled by a board switch (see Figure 9-1) and controlled by software. Once enabled it must be restarted at regular intervals. If it is not restarted the timer will expire and cause a Non-Maskable Interrupt or reset to the local processor.

The watchdog timer facility is provided by the 6300ESB I/O Controller Hub. Details of how it is used are provided in the Intel data sheet.

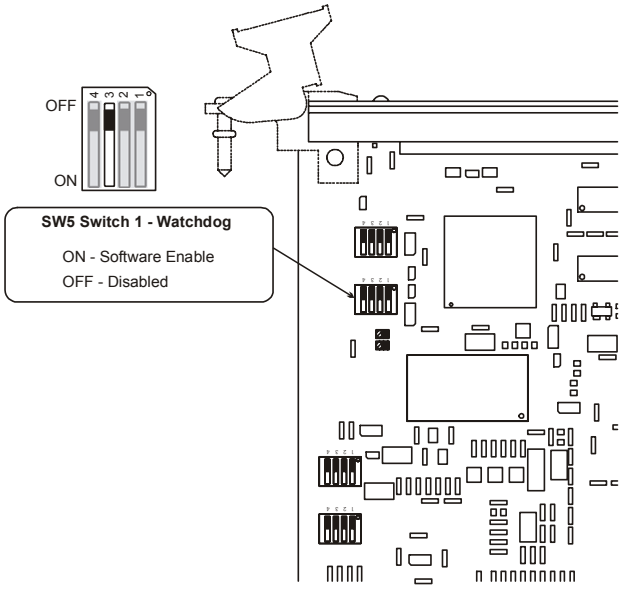


Figure 9-1 Watchdog Configuration Switch

The VP 34x/02x provides an additional gating of the Watchdog Reset output from the 6300ESB. This can be useful for testing purposes or when it is not desirable to generate a reset from a Watchdog timeout. Bits 2 and 3 of Status & Control register 2 provide for enabling a Watchdog reset, and whether or not to enable the Watchdog, respectively. See Section 2.4.7 for additional information regarding the effect of a reset from the Watchdog Timer.

9.9 Long Duration Timer / Periodic Interrupt Timer

The Long Duration Timer (LDT) consists of a 32-bit free running counter with a 32-bit holding register and a status & control register. It may be used by user software to timestamp events to a resolution of 1 microsecond. The counter bytes are laid out in little-endian format to permit multi-byte read/write operations. The status & control register controls the operation of the LDT. A 32-bit holding register is provided to ensure stable count values are read. Read operations return the holding register byte values. A read operation on the low byte of the counter causes the count value to be transferred to the holding register. Hence, the low byte should be read first to ensure a stable count value.

The counter may be preset by writing to the registers. The counter bytes may be written independently. The counter should be stopped before writing to it or the outcome may be indeterminate. The counter registers are cleared at power-on, but not by subsequent reset operations. If necessary, the LDT can be cleared by writing zero to all four counter bytes. An interrupt may be generated when the counter rolls over (from FFFFFFFFh to zero). This occurs approximately every 72 minutes (1 MHz clock).

The LDT doubles as a simple Periodic Interrupt Timer (PIT). It offers 7 fixed interrupt rates, namely: 100, 200, 500, 1,000, 2,000, 5,000 and 10,000Hz (1 MHz clock). The mode / interrupt rate is set by three bits in the LDT status & control register.

NOTE: If the LDT clock frequency is not 1 MHz (i.e. HF Clock = 4 MHz), the above rates should be scaled accordingly.

In PIT mode, the counter counts up to a pre-determined maximum value and then goes back to zero. To ensure a full first interval, the low and mid-low bytes of the counter should be cleared before the counter is started.

9.9.1 Long Duration Timer / Periodic Interrupt Timer Low Byte

This register is at I/O address 218h.

7	6	5	4	3	2	1	0
LDT7	LDT6	LDT5	LDT4	LDT3	LDT2	LDT1	LDT0

Bits 7 - 0: Low byte of LDT / PIT (Read/Write)
Reading this register causes the current value of the LDT to be transferred to a holding register. This allows a stable 4 byte count to be read. The low byte of the holding register is returned by the read.

Writing to this register loads a value into the low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.9.2 Long Duration Timer / Periodic Interrupt Timer Mid-low Byte

This register is at I/O address 219h.

7	6	5	4	3	2	1	0
LDT15	LDT14	LDT13	LDT12	LDT11	LDT10	LDT9	LDT8

Bits 7 - 0: Mid-low Byte of LDT / PIT (Read/Write)
Reading this register returns the mid-low byte of the holding register.

Writing to this register loads a value into the mid-low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.9.3 Long Duration Timer / Periodic Interrupt Timer Mid-high Byte

This register is at I/O address 21Ah.

7	6	5	4	3	2	1	0
LDT23	LDT22	LDT21	LDT20	LDT19	LDT18	LDT17	LDT16

Bits 7 - 0: Mid-high Byte of LDT (Read/Write)
Reading this register returns the mid-high byte of the holding register.

Writing to this register loads a value into the mid-high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.9.4 Long Duration Timer / Periodic Interrupt Timer High Byte

This register is at I/O address 21Bh.

7	6	5	4	3	2	1	0
LDT31	LDT30	LDT29	LDT28	LDT27	LDT26	LDT25	LDT724

Bits 7 - 0: High Byte of LDT (Read/Write)
Reading this register returns the high byte of the holding register.

Writing to this register loads a value into the high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.9.5 LDT / PIT Status & Control Register

This register is at I/O address 21Ch. It controls the operation of the LDT.

The LDT clock signal is obtained from the Super I/O controller HF Clock output. The HF Clock is derived from an internal 48 MHz signal. A programmable divider within the Super I/O controller gives a choice of HF Clock frequencies. The HF Clock frequency is further divided by 4 or 128 before being fed to the LDT clock input. The following clock frequencies are available:

HF Clock / 4: 12 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, 1.5 MHz, 1 MHz, 750kHz.
HF Clock / 128: 375kHz, 187.5kHz, 125kHz, 93.75kHz, 62.5kHz, 46.875kHz, 31.25kHz, 23.4375kHz

NOTE: The BIOS will configure the Super I/O and LDT for a 1 MHz clock frequency.

7	6	5	4	3	2	1	0
RFU	RFU	CLOCK SELECT	INTERRUPT FLAG	MODE 2	MODE 1	MODE 0	RUN

Bit 0: LDT / PIT run (Read/Write)
This bit controls whether the LDT / PIT runs or is stopped.

0 = Stop (default)
1 = Run

Bits 3 - 1: LDT / PIT mode (Read/Write)
These bits set the mode of the timer as follows:

0 0 0 = LDT
0 0 1 = PIT 100Hz
0 1 0 = PIT 200Hz
0 1 1 = PIT 500Hz
1 0 0 = PIT 1,000Hz
1 0 1 = PIT 2,000Hz
1 1 0 = PIT 5,000Hz
1 1 1 = PIT 10,000Hz

NOTE: The above PIT rates require LDT CSR bit 5 = 0 and the HF Clock output from the Super I/O controller to be 4 MHz. This results in an LDT clock frequency of 1 MHz.

Bit 4: LDT / PIT Interrupt Flag (Read/Clear)
The interrupt flag is active whenever the timer is running. It is set if the LDT RUN bit is set AND either the LDT rolls over or the PIT interval expires. It can be cleared by writing to the register with a zero in its bit position. This should be done in the LDT / PIT interrupt service routine.

0 = LDT / PIT interrupt has not occurred
1 = LDT / PIT interrupt has occurred

Bit 5: LDT / PIT Clock Source (Read/Write)
This bit selects the clock source for the LDT / PIT as follows:

0 = Super I/O HF Clock / 4 (1 MHz)
1 = Super I/O HF Clock / 128 (31.25kHz)

Bit 6: Reserved
This bit should be set to '0'.

Bit 7: Reserved
This bit should be set to '0'.

9.9.6 Programming the LDT/PIT

The following code fragments illustrate how the system software, by using the on-board hardware, can create accurate time delays and measure elapsed times, accurate to 1us, irrespective of the CPU's operating frequency.

The LDT and PIT control registers and operational modes are defined thus:

```
#define TIMER_BYTE_0            (0x0218U)
#define TIMER_BYTE_1            (0x0219U)
#define TIMER_BYTE_2            (0x021AU)
#define TIMER_BYTE_3            (0x021BU)
#define CONTROL_STATUS          (0x021CU)

#define INTERRUPT_MASK              (0x10U)
#define INTERRUPT_ENABLE            (0x10U)
#define INTERRUPT_DISABLE           (0x00U)
#define INTERRUPT_SET               (0x10U)
#define INTERRUPT_RESET             (0x00U)

#define TIMER_ROLLOVER              (0x10U)

#define MODE_MASK                   (0x0EU)
#define MODE_PIT_10000Hz            (0x0EU)
#define MODE_PIT_5000Hz             (0x0CU)
#define MODE_PIT_2000Hz             (0x0AU)
#define MODE_PIT_1000Hz             (0x08U)
#define MODE_PIT_500Hz              (0x06U)
#define MODE_PIT_200Hz              (0x04U)
#define MODE_PIT_100Hz              (0x02U)
#define MODE_LDT                    (0x00U)

#define MODE_RUN_MASK               (0x01U)
#define MODE_RUN_GO                 (0x01U)
#define MODE_RUN_STOP               (0x00U)
```

The following code fragment illustrates how a simple delay of 10ms is implemented.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);

/* wait until the PIT rolls over ... */

while (inbyte (CONTROL_STATUS) & TIMER_ROLLOVER) == 0)
    ; /* do nothing ... */

/* reset the PIT "rollover" flag ... */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

It is possible to implement delays of 5ms, 2ms, 1ms, 500µs, 200µs and 100µs by utilizing other PIT modes.

The PIT can generate an interrupt whenever the PIT rolls over. The system programmer must initialize the interrupt vector, enable PIC interrupts, etc. The following code fragment shows the basic interrupt handling function.

```
static volatile signed long int dCounter;

#pragma interrupt (vInterruptHandler)
static void far vInterruptHandler (void)
{
    /*
     * clear the source of the interrupt by resetting the rollover
     * flag, thus:
     */

    outbyte (CONTROL_STATUS, inbyte (CONTROL_STATUS) & ~INTERRUPT_MASK);

    /*
     * perform the relevant actions to acknowledge the interrupt
     * in the PIC, etc ...
     */

    dCounter--;
}
```

The following code fragment used in conjunction with the previous code fragment illustrates another method of implementing a timed delay. The `dCounter` variable is declared to be `volatile` which prevents any C compilers, which conform to the ANSI standard, from optimizing accesses to the `dCounter` variable.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);
dCounter = 500; /* 500 * (1 / 100) == 5 seconds */

/*
 * install the interrupt for the PIT counter, modify the
 * PIC settings, etc. and ensure interrupts are enabled.
 */

while (dCounter > 0)
    ; /* do nothing ... */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

The following code fragment uses the LDT to measure the elapsed time to a resolution of 1ms. In this example, the LDT is zeroed at the start of the test and so there is no need to subtract the LDT's initial value from its final value.

```
static UINT32 dElapsedTime;

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_LDT | MODE_RUN_GO);

/*
 * perform action to be timed ...
 */
outbyte (CONTROL_STATUS, MODE_STOP);
dElapsedTime  =  (UINT32) inbyte (TIMER_BYTE_0);
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_1)) << 8;
```

```
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_2)) << 16;
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_3)) << 24;
printf ("Elapsed time = %u.%06u seconds\n",
         dElapsedTime / 1000000U, dElapsedTime % 1000000U);
```

The `TIMER_BYTE_0`, `TIMER_BYTE_1`, `TIMER_BYTE_2` and `TIMER_BYTE_3` control registers are at successive addresses and form a 32-bit register in "little endian" format. It is possible to read and write the timer's value in a single 32-bit I/O operation. For example, to read the timer's value, the following C statement suffices.

```
dCounterValue = inlong (TIMER_BYTE_0);
```

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10 PC BIOS

The VP 34x/02x board is fitted with PC BIOS firmware that performs many of the functions of a standard desktop PC. It also includes additional features specifically tailored for the VME bus environment. In addition to the core BIOS firmware, the board is fitted with BIOS Extensions for VGA interface, SCSI interface and remote bootload capability via any of the on-board Ethernet channels. To improve the flexibility of the board, some of these features may be selectively enabled or disabled by an operator using BIOS setup menus. Many of the features provided by the PC BIOS are unlikely to be adjusted by the user, but there are several options which many users will find helpful. Some of these are already referenced in other sections of this manual, but the remainder of this chapter will describe some other commonly-used options. More information about each of the options available is provided in the Help box of the BIOS setup menus.

10.1 Entering the PC BIOS

The startup mode of the board may be selected using the Mode switch, but can be either of the following: PC BIOS mode (the factory default setting), which generally follows the behavior of a desktop PC, and VSA mode (a more flexible and comprehensive testing mode), which can be used for system or board testing. Figure 10-1 shows the location of the switch on the board and its settings.

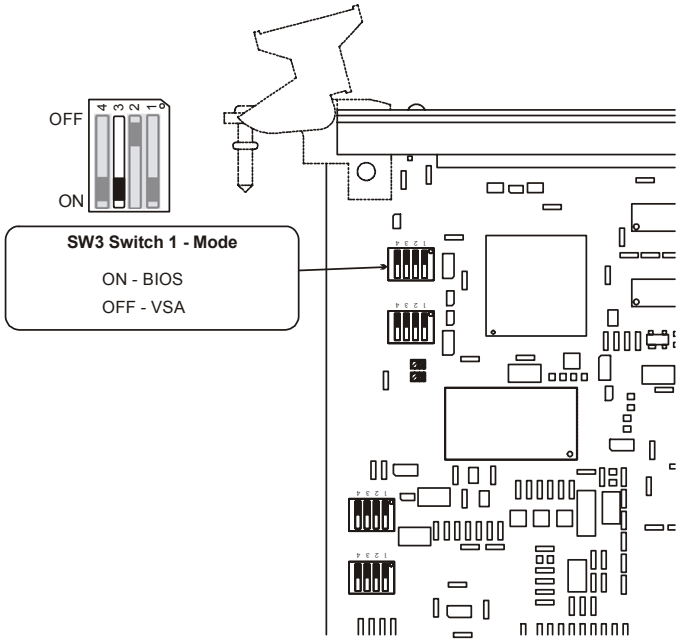


Figure 10-1 Mode Switch

VSA mode may be exited either by operator command, or by allowing the board to proceed through the VSA startup sequence without intervention. In either case, the board will enter PC BIOS mode and continue as if this mode had been selected with the switch. When the board is reset, it will generally restart in the switch-selected operating mode. However, a reset caused by a keyboard <CTRL-ALT-DEL> keystroke combination, or by a programmed reset using one of several different I/O access sequences, will only cause a PC BIOS restart. A complete board or system reset (using the front panel switch) will cause the board to restart in the mode selected by the Mode switch setting.

Operator communication with the PC BIOS is normally through the VGA display and a separate keyboard. This can be reconfigured via an on-board switch to use a serial terminal connected to the COM1 port. Section 7.1 describes the location and settings for this switch. A VT100-compatible serial terminal or emulator program should be used. By default the serial line is programmed to operate at 9600 Baud with 8 data bits, 1 stop bit and no parity (8N1). There is no flow control. For fast terminals, the baud rate can be increased via the Serial Console Baud Rate field of the **`Main | Boot Options`** Setup menu.

10.2 The PC BIOS Startup Sequence

When the board starts up without operator intervention, it will run a basic Power-On Self-Test (POST) sequence, including ECC DRAM initialization and a DRAM test. The full DRAM test will be omitted on subsequent restarts if the BIOS configuration settings have not been changed. Once the DRAM test has completed, the board will try to bootload application software from any attached mass storage medium or through one of the Ethernet interfaces. When the PC BIOS starts after changing the battery, losing battery power or after using the CMOS CLEAR switch, it may report a CMOS Checksum Error or some other problem. This will be followed by a prompt to the operator to press <F1> to continue or <F2> to enter Setup mode. If no key is pressed within approximately five seconds, the PC BIOS will continue with its normal startup sequence. It will also re-calculate the CMOS Checksum to prevent this error occurring again at a subsequent restart.

Pressing the <F2> key at any time during the PC BIOS startup sequence will result in the BIOS Setup menu being entered. The Setup menu is quite extensive, and is provided with context-sensitive help information which is displayed in the right-hand panel on screen.

NOTE: When the F2 key is pressed, a few seconds may elapse before the BIOS Setup menu appears. The PC BIOS will always run BIOS Extensions for the on-board SCSI and for any PMC modules it detects before responding to the keypress.

10.3 Boot device selection

The order in which the PC BIOS searches for a bootable medium is pre-configured but may be altered by the operator using the Boot setup menu. When the order is changed using this menu it will be retained in non-volatile memory so that the order is maintained after a restart. It is also possible to specify a one-time override of the boot device when the board starts, by pressing the <ESC> key. This will result in a pop-up menu appearing. The appropriate boot device may be selected from a list by using the cursor keys and pressing <ENTER>, but this is not retained in non-volatile memory, so the correct device must be re-selected if necessary at a subsequent restart.

NOTE: When the <ESC> key is pressed, a few seconds may elapse before the boot device selection menu appears. The PC BIOS will always run BIOS Extensions for the on-board SCSI and any PMC modules it detects before responding to the keypress.

The SCSI Controller and Ethernet channels require their BIOS Extension firmware to be enabled before they can be used as boot devices. BIOS setup options are provided to control whether or not the board runs these BIOS Extensions which are accessible from the **Main | Boot Options** menu. The **PXE Boot Firmware** field controls the Ethernet boot firmware and **SCSI BIOS Firmware** controls the SCSI boot firmware.

Because of the limited space available for BIOS Extension firmware, it may be necessary to restrict the number of times the Extension ROM is executed (by default the Extension ROM is executed once for each instance of a supported device). The **Main | Boot Options | Option ROM Loading** field controls the number of times Extension ROM Firmware executed.

The Ethernet boot firmware allows remote booting using BOOTP/TFTP or PXE. The method to be used is selected by the **Network Boot Protocol** field of the **Boot Options** sub-menu on the BIOS **Main** setup screen. The BOOTP/TFTP firmware is based on the “Etherboot” software available from http://etherboot.sourceforge.net. Further information on the capabilities of this software is available at this site. The PXE protocols are defined by Intel and further information can be obtained from http://developer.intel.com.

NOTE: The BIOS has limited space available for Extension ROMs. If a PMC module containing extension firmware is fitted to the board, it may be necessary to disable the PXE firmware extension before the PMC firmware can be loaded.

10.4 PCI Bus Resource Management

The local bus structure of the VP 34x/02x is quite complex, and is based around two independent PCI busses. The 855GME GMCH to 6300ESB ICH connection is via a Hub Link V1.5 bus. This connection while not being PCI looks to the processor as a PCI bus. This is the first bus in the system and devices connected to it (internal to the 855GME GMCH and 6300ESB ICH) are configured in the same way as a PCI bus. In some cases the user may need to understand this structure and in particular how the PC BIOS firmware allocates addresses and interrupt signals to the available hardware resources. The following sections outline this allocation process and provide further details of the PCI bus configuration.

There are two on-board PCI busses: a 64-bit bus which connects to the PMC site, the SCSI controller and the 82546GB Gigabit Ethernet controller, a second 32-bit bus which connects to the Universe II VME controller and the PMC expansion carrier interface. Each bus has four dedicated interrupt lines, which must be shared by all devices on that bus.

10.4.1 PCI Resource Allocation

The PC BIOS initializes all devices on the local PCI bus, and allocates appropriate memory address ranges, I/O address ranges, and interrupt routings for all these devices. This process is automatic as part of the BIOS "Plug-and-play" setup. The Intel chipset allows for a flexible allocation of many PCI bus interrupts to the available interrupt inputs on the PC-compatible interrupt controllers provided on the board. The PC BIOS uses this feature to program default settings which it considers appropriate for the combination of on-board devices and any device fitted to the PMC site. In some configurations, depending on the operating system being used and the capability of the relevant device drivers, it may be necessary for the user to modify this default configuration, to minimize the sharing of interrupt lines. The PC BIOS Setup screens for **`Advanced | PCI Device Configuration`** allow this. These screens allow the user to override the PC BIOS default selections for interrupt allocation, but care must be taken when doing this to avoid conflicts which may result in operating system or even BIOS "crashes". To allow maximum flexibility of choice for the user, the PC BIOS performs limited checks on the user's interrupt allocation. In the event that there is a problem, it may be necessary to clear the CMOS memory (see Section 2.5), or even to reset the Extended System Configuration Data via the **`Reset Configuration Data`** field of the BIOS Setup screen for **`Advanced`** configuration settings. The PC BIOS does not allow the user to override the allocation of memory and I/O address ranges.

> **NOTE:** When reallocating interrupts using the BIOS Setup screens, try to avoid allocating the SCSI or PMC interrupts to ones also allocated to other devices. This sharing of interrupts can cause problems with some operating systems where device drivers do not correctly handle shared interrupts.

Table 10-1 lists the configurable interrupts for this board. The actual allocation of PCI bus interrupts to available interrupt controller inputs will depend on both the default "Plug-and-play" settings programmed by the PC BIOS, and the way in which the user has overridden them using the Setup screens. When more than one PCI bus interrupt is routed to the same interrupt controller input, that input will remain active while any of the sources connected to it are active.

32-bit PCI Bus INTA
32-bit PCI Bus INTB
32-bit PCI Bus INTC
32-bit PCI Bus INTD
64-bit PCI Bus INTE
64-bit PCI Bus INTF
64-bit PCI Bus INTG
64-bit PCI Bus INTH

Table 10-1 Configurable PCI Bus Interrupts

10.4.2 PCI Device IDs

Each PCI bus, and each device on an individual PCI bus, has a unique ID. For the VP 34x/02x, the bus and device IDs are listed in Table 10-2. The Intel chipset includes two PCI bus bridges to interface to the 64-bit and 32-bit on-board PCI busses, and these bridges are identified by the same PCI device ID but with different function codes.

Device	Bus	ID	PCI Function Code
855GME	0	0	0
6300ESB – Hub Interface to PCI-X Bridge	0	28	0
6300ESB – USB Controller #1	0	29	0
6300ESB – USB Controller #2	0	29	1
6300ESB – Watchdog Timer	0	29	4
6300ESB – IOxAPIC (Interrupt Controller)	0	29	5
6300ESB – USB 2.0 Controller	0	29	7
6300ESB – Hub Interface to PCI Bridge	0	30	0
6300ESB – PCI to LPC Bridge	0	31	0
6300ESB – IDE Controller	0	31	1
6300ESB – SATA Controller	0	31	2
6300ESB – SMBus Controller	0	31	3
6300ESB – AC'97 Audio Controller (Not Used)	0	31	5
6300ESB – Modem Controller (Not Used)	0	31	6
SCSI 53C1020 Interface	2	0	0
82546GB – Channel 0	2	1	0
82546GB – Channel 1	2	1	1
PMC	2	3	0
PMC Second Function	2	4	0
Universe II PCI to VME Bridge	n+2	1	0
PMC Carrier Expansion PCI to PCI Bridge	n+2	14	0

Table 10-2 PCI Device Numbers

NOTE: The bus number used for the Universe II and PMC Carrier Expansion will depend on the bus structure of any PMC module installed on the VP 34x/02x board. If a simple module without a PCI-PCI bridge is used, the bus number for the Universe and PMC Carrier Expansion will be 3.

10.5 User Selectable NVRAM Defaults

The BIOS provides a facility through which the user can save preferred setup option settings to Flash memory. Then, if the BIOS detects that the contents of NVRAM is corrupt, the user can elect to restore the contents from the saved settings, rather than loading factory configured defaults. This facility also allows the board to operate without fitting the battery, but with NVRAM settings different to the factory defaults.

The **`Save User Defaults`** option in the BIOS setup **`Exit`** menu is used to write the current NVRAM settings to Flash memory. When settings are saved to Flash memory, the current BIOS date and time will also be stored; this allows the board to start operating with an appropriate date and time.

NOTE: Saving settings to Flash memory may take a number of seconds to complete.

The NVRAM restore feature is controlled by the BIOS Defaults switch (see Figure 10-2). When the BIOS detects that the NVRAM contents are corrupt, NVRAM settings will be restored from Flash memory (provided that valid settings have been saved). The switch selects between a user saved setting or the factory-configured defaults. If no user setting has been saved then the factory-configured defaults will be used.

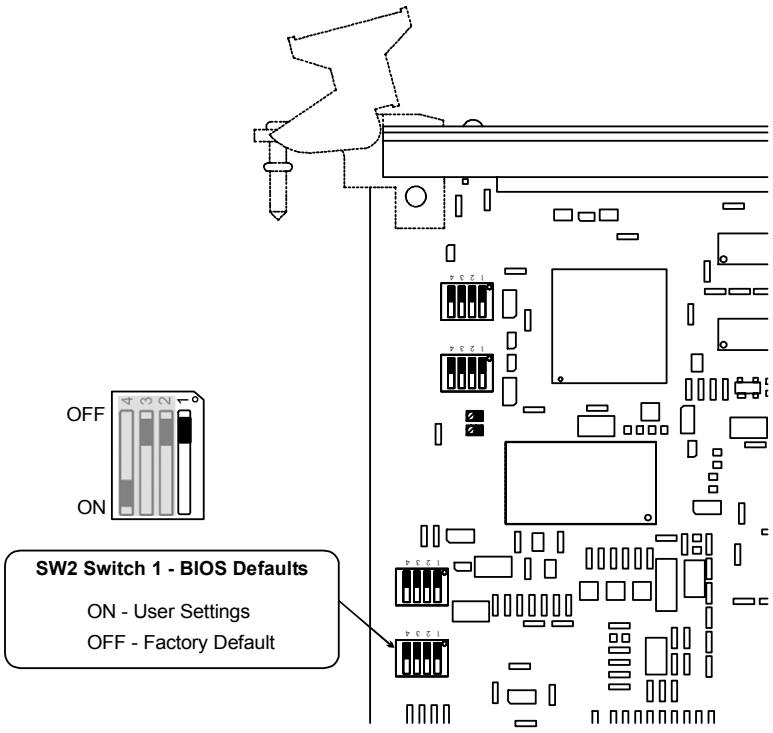


Figure 10-2 BIOS Defaults Switch

To configure and save preferred NVRAM settings:

- Configure the BIOS in the usual manner via the setup menus
- Reboot the board and allow it to proceed through to the bootloader without error
- Reboot the board and enter Setup
- From the **`Exit`** menu; select **`Save User Defaults`**
- Set the BIOS Defaults switch to 'User Setting'

NOTE: It is possible to configure BIOS settings which prevent the board working correctly. In these cases, normal operation can be restored by setting the BIOS Defaults switch to the 'Factory Default' setting, restarting the board and repeating the BIOS setup sequence above with valid settings.

10.6 The Recovery BIOS

In the unlikely event that the board's BIOS ROM contents becomes corrupted and it is not possible to perform the normal BIOS update procedure, the board provides a minimal Recovery BIOS that will allow the board to boot from a specially prepared floppy disk and restore a known-good BIOS image. Contact Concurrent Technologies for further details.

The Recovery BIOS is located in a special sector in the BIOS ROM that is protected from accidental erasure by hardware means. When a BIOS update is performed, the Recovery BIOS does not get updated.

When power is applied to the board, or when the board is reset, the CPU starts to execute the Recovery BIOS. From here a checksum test is performed on the first 64Kbytes of the main BIOS to ensure that it is intact. When the checksum is validated, control passes to the main BIOS and the board boots normally. If the checksum test fails, the BIOS recovery process is invoked automatically.

The BIOS recovery process can also be forced using the Boot Type Switch, see Figure 10-3.

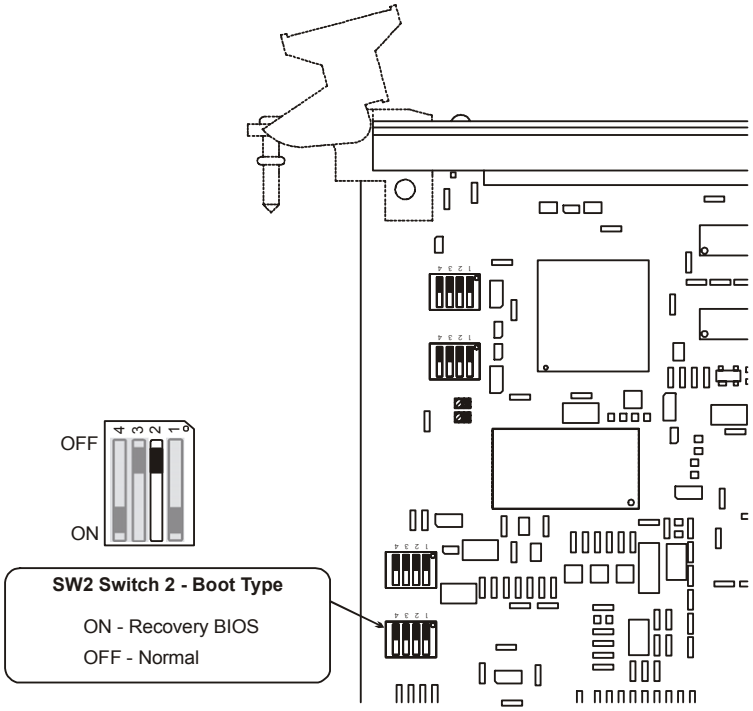


Figure 10-3 Boot Type Switch

The recovery BIOS will indicate its progress via a serial terminal connected to COM1. VGA output is not supported.

The recovery BIOS requires a specially prepared disk image; a suitable recovery disk image can be obtained from Concurrent Technologies, if required.

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11 VME SYSTEM ARCHITECTURE TEST HANDLER

11.1 Introduction

The VME System Architecture (VSA) Test Handler firmware provides an environment where interactive testing may be performed on one or more Concurrent Technologies' VME CPU boards.

The level of testing provided by VSA is more comprehensive than that provided by the BIOS POST, and testing can also be looped to aid diagnosis of intermittent faults. Failing tests provide diagnostic information that can be used to identify the cause of the problem.

VSA mode also provides an interactive command-line interface, with a range of commands and tests through which memory and I/O may be examined or modified. PCI devices can also be identified and their configuration registers displayed and changed.

VSA allows all Concurrent Technologies' boards in a system to be tested from a single console connected to the System Controller. This console can be a standard VGA screen and keyboard, or a serial terminal connected to COM1 or COM2.

11.2 The VSA Environment

Boards configured for VSA mode of operation can be installed in any slots in the VME chassis. When the system starts up, those boards running in VSA mode will carry out an arbitration sequence on the VME backplane using shared memory on each board involved. One board, normally the board in the slot nearest to or in the System Controller slot, will win this arbitration and act as the Master Test Handler. Other boards which lost the arbitration sequence will operate in a Slave Test Handler mode.

11.2.1 Slot Numbering

Throughout the VSA firmware, boards are identified by their logical slot number. This number does not represent the physical backplane slot. The logical slot number is assigned by the Master Test Handler when it detects a board capable of participating in system testing. Therefore boards from other manufacturers, boards not configured for VSA mode and boards that are seriously damaged will not be detected and included in the numbering scheme. The board which will act as the Master Test Handler will be assigned slot number zero.

In a system containing a faulty board, which is unable to enter its Slave Test Handler, the logical slot numbers will not match the board positions in the rack. The faulty board can be isolated by executing a short Built-In Self-Test (BIST) (e.g. BIST 126) on each board in turn. The POST LED is illuminated while the BIST is executing allowing the faulty board to be quickly identified.

11.2.2 VSA Console Devices

VSA can use the VGA compatible display interface and keyboard for the console device, or a serial terminal may be used connected to COM1 or COM2. VSA automatically detects the users choice of console when the attention, "U" keystroke is entered at the prompt.

For serial consoles VSA will auto-detect the baud rate, though it is recommended that 19,200 Baud or 9,600 Baud be used. The auto-baud function may require the attention key to be pressed more than once in noisy environments, or when lower rates than the recommended ones are used.

Console I/O will only be provided by the Master Test Handler.

11.2.3 Starting the Master Test Handler

VSA mode is selected by setting the Mode switch to the VSA position as indicated in Figure 10-1. The board will enter VSA mode before the BIOS starts displaying sign-on text, so the first console output will be the VSA user attention prompt

When VSA starts, it outputs attention characters to all possible console devices simultaneously; i.e. the default video adapter, COM1 and COM2 ports. On the video adapter this will appear as a series of asterisks "*", on a serial console the appearance of the character will depend on the console's baud rate.

Only the board in the system controller slot can provide console output. This is the Master Test Handler (MTH); if other boards are present they will automatically enter their Slave Test Handlers (STH) and await test execution requests from the Master.

When the attention prompt is displayed, pressing "U" (uppercase "u") on the desired console device will display an option menu. From here the Master Test Handler can be entered, or the board booted back to BIOS mode.

The tests available in VSA mode are described as Built-In Self-Tests (BISTs).

11.2.4 Remote Testing from the System Controller

In a system comprising more than one Concurrent Technologies CPU board, only the system controller board will provide a console interface; however, this board can be used to test the other VSA configured boards through their Slave Test Handlers.

During system startup, the VSA configured system controller will detect all other functional, VSA configured boards. These boards will be identified via the VSA startup screen, together with their logical slot ID.

The default test slot is initially set as slot zero (the system controller). This can be changed using the SLOT command to any valid logical slot. When the default slot is changed, all tests will run on the slave board and the TESTMENU command will return the list of valid BISTs for that board.

11.2.5 Bootloading the BIOS

The board can be booted to BIOS mode from VSA mode using the BPHASE command. Once in BIOS mode, warm boots will confine execution to the BIOS firmware; however, if a cold boot is generated without changing the VSA switch, the board will re-enter VSA mode.

If the system controller board is booted to VSA mode and the "U" command is not entered, the firmware will proceed to boot the board back to BIOS mode.

11.2.6 BIST Execution

BIST execution is started using the TEST command. While a test is executing, no further commands may be entered.

It is possible to specify more than one BIST for execution using the ";" separator, for example:

`T14;T15;T20,4` Execute Test 14, Test 15 and Test 20. Test 20 has a command parameter.

BISTs may be executed more than once, automatically, using the iteration count. Using an iteration count of zero will execute the BIST until the break "Ctrl-C" command is pressed, for example:

`10<T14>` Execute T14 ten times.

`0<T5>` Execute T5 "forever".

The iteration counter can also be used to execute a sequence of tests more than once, for example:

`5<T14;T15;T16>` Execute T14, T15 and T16 five times.

11.3 MTH Command Reference

This section details all of the commands available from the MTH (Master Test Handler) prompt. Commands are divided into General and Utility sections. The list below shows the commands in uppercase letters only, but lowercase letters may also be used.

Where numbers are entered decimal notation is assumed unless the value ends in ‘H’ or ‘h’ In this case the value is assumed to use hexadecimal notation.

11.3.1 Help Screens

Typing HELP at the MTH prompt will give general help for the MTH commands. Help for the utility commands is available with the UTILHELP command.

11.3.2 General Commands

The general commands control BIST execution on the local or a remote test slot.

BPHASE [Short command **B**]

Boot the BIOS firmware on the default slot.

BPHASE # [Short command **B**]
- slot number

Boot the BIOS firmware on the specified slot.

CLEARSUM [Short command **C**]

Clears the pass and fail counts for all BISTs on the default slot.

ID [No short command]

Displays a list of boards in the system, their status and the active default slot number. Boards are identified by logical slot number. Only Concurrent Technologies boards, configured for VSA mode will be identified by this command.

PRINT [Short command **PR**]

Toggles the BIST printing flag. When PRINT is off BIST diagnostic messages are not displayed during testing, only the pass or fail and error code are displayed.

RESET [Short command **R**]

This command can only be applied to a slave board, which can be made to reset and reboot into its Slave Test Handler.

SLOT [Short command **S**]

Displays the default test slot, i.e. the slot on which BISTs will execute. The slot number does not relate to the physical backplane slot, it is a logical slot number assigned by the test handler.

SLOT # [Short command **S**]
- slot number

Changes the default slot number. The slot number does not relate to the physical backplane slot, it is a logical slot number assigned by the test handler.

It is possible to specify an unoccupied slot number with this command; however, a warning message will be displayed and confirmation of the change requested.

SUM [No short command]

Prints the pass and fail counts for all BISTs available on the default slot.

SUM # [No short command]
- test number, in the range 0-255

Prints the pass and fail count, for the BIST indicated, on the default slot.

TEST # [Short command **T**]
- test number, in the range 0-255

Starts BIST execution on the default slot. The test is run without parameters. Further command input is prevented until the BIST completes (or a BIST time-out is generated for a remote slot).

TEST #,p1,p2,… [Short command **T**]
- test number, in the range 0-255
p1,p2 - test parameters (see individual BIST descriptions for details)

Starts test execution on the default slot, the supplied parameters are passed to the BIST

TESTMENU [Short command **TM**]

Displays a list of available BISTs for the default slot, together with their associated test number.

UTILHELP [Short command **U**]

Displays the help screen for the utility commands, described below.

VERSION [Short command **V**]

Prints the firmware version number on the default slot.

11.3.3 Utility Commands

IRO, IRR, ICR, ICW

These commands are reserved for factory testing. They report and modify the state of the VSA board communication data structures.

I**NB** port_address	read a byte from the specified I/O address
INW port_address	read a word from the specified I/O address
IND port_address	read a dword from the specified I/O address
OUTB port_address,data	write a byte to the specified I/O address
OUTW port_address,data	write a word to the specified I/O address
OUTD port_address,data	write a dword to the specified I/O address
DB address,length	read a byte from the specified memory address
DW address,length	read a word from the specified memory address
DD address,length	read a dword from the specified memory address
DQ address,length	read a qword (64-bits) from the specified memory address
SB address,data	write a byte to the specified memory address
SW address,data	write a word to the specified memory address
SD address,data	write a dword to the specified memory address

NOTE: The I/O and memory read and write functions only operate on the local slot, i.e. the Test Master. To read or write I/O and memory on the slave boards: change the default slot number and use the equivalent BIST functions TEST 101 through TEST 104.

TEA toggle Test Error Action flag between QUIT and CONTINUE

SEA toggle Sequence Error Action flag between QUIT and CONTINUE

The last two commands prevent looped BIST execution from halting if an error occurs.

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12 VSA MODE DIAGNOSTICS

This chapter describes the board's initialization into VSA mode and the Tests that can be run from VSA mode. For details of the VSA command line interface, refer to Chapter 11.

Some of these tests are designed to be run when the board is fitted with additional test hardware at the factory, or in conjunction with other boards. When these tests are run by the user, they may fail simply because this additional hardware is not available.

12.1 Initialization Checks

The board will always start executing PC BIOS firmware; however, if the Mode switch is set to the VSA position the BIOS will transfer control to the VSA firmware once it has completed chipset initialization, cache and memory sizing.

The VSA firmware performs additional hardware initialization and some basic functional checks before switching to Protected Mode and entering its master or slave test handler. These functional checks are described below.

12.1.1 Check 16: CPU Alive Check

To test the basic CPU-interconnect access path, the CPU writes the ID of this test to the BIST TEST ID Interconnect register, then reads it back to verify that it was correctly written.

The test fails if the value read is not the same as the value written.

12.1.2 Check 18: Scratchpad RAM Check

The first 192 Kbytes of RAM, the scratchpad, are used by the BIST firmware. This memory area is tested by writing and verifying two rotating test patterns across the scratchpad address range. The first pattern is 0AA55h, the second 055AAh. Each pattern is rotated left two bit positions for each increment of the address; this ensures that consecutive addresses have unique data patterns whether they use 16-, 32- or 64-bit bus fetches.

NOTE: This is the only test carried out on this area of RAM - all other BISTs test only the remaining RAM area.

12.2 BIST Descriptions

The following is a list of the tests that are available in the firmware set installed on this board, together with an overview of the function of each test.

A description of each possible error condition, with its code, is given for each test.

12.2.1 Test 1: Test Initialization Routine

This pseudo-test performs no actual testing of the board. It sets up in RAM several data values, such as RAM size, that are used by later tests. This BIST should always be run at the start of a test session before any other tests are run.

This test will be executed at power-up, and may be invoked thereafter by a Master Test Handler.

12.2.2 Test 2: PROM Check

This BIST performs a checksum test over the VSA firmware EPROM. By default, the range tested is from 0FFF00100h to 0FFF77FFFh.

The test range is configurable by the user of the board: the parameters that control the test are stored in three consecutive 32-bit words at the start of the VSA firmware, i.e. starting at address 0FFF00000h. The parameters are as follows:

0FFF00000h: Checksum Area Start Address
0FFF00004h: Checksum Area Length (in bytes)
0FFF00008h: Expected Checksum Value

A feature of the test is that if the expected checksum value is set to a value of 0FFFFFFFFh (-1 in decimal) then the test will always pass, but will report the actual checksum value to the test master. This is useful for discovering the new checksum value of a modified range.

Note that if the checksum area is defined to cover the three words that control the test, it will not be possible to calculate an expected checksum value.

Test 2 Error codes:

0300h – The checksum test failed

12.2.3 Test 4: Numeric Coprocessor Test

This BIST performs checks on the functions of the numeric coprocessor component of the CPU.

At the start of the test, the coprocessor is re-initialized using an FINIT instruction and the required operating mode set up. Basic arithmetic functions are checked and a deliberate division by zero is attempted in order to generate an exception condition and the associated interrupt.

If the results of the arithmetic operations are incorrect or result in an exception, or if no divide by zero exception is generated the test fails.

Test 4 Error codes:

0401h – error in re-initializing floating-point processor
0402h – computation generated an exception or incorrect result
0403h – exception occurred in floating-point comparison
0404h – divide by zero failed to generate the correct exception status

12.2.4 Test 6: Interconnect Image Check

This BIST reads and verifies the vendor ID and the board name from the Header Record of the local Interconnect Template. The interconnect template is a data structure used by VSA to communicate between boards.

Test 6 Error codes:

0300h – image check failed

12.2.5 Test 7: Off-board Interconnect Access

This BIST searches for a known interconnect record in the interconnect template of the System Controller board. The interconnect template is a data structure used by VSA to communicate between boards.

Test 7 Error codes:

0300h – test failed

12.2.6 Test 9: 8254 PIT Test

This BIST checks the PC compatible, Programmable Interval Timers within the South Bridge chip. To test the secondary PIT (PIT2) see Test 40.

Each timer in turn is initialized with a start count value, then monitored to make sure that it counts successfully.

Test 9 Error codes:

0401h – timer 0 failed to count
0402h – timer 1 failed to count
0403h – timer 2 failed to count

12.2.7 Test 10: 8259A PIC Test

This BIST checks the functionality of the PC compatible Programmable Interrupt Controllers on the board.

Test 10 Error codes:

0402h – interrupt did not occur
0412h – incorrect interrupt occurred

12.2.8 Test 12: Local RAM Fixed Pattern Test

This BIST performs a short test on local RAM. The range of memory to be tested depends upon the test handler from which the BIST was invoked.

When the test is executed from the power-up test handler, it is necessary to limit execution time; therefore the test range is limited to the block of RAM before the video memory hole, i.e. 30000H to 9FFFFH.

When the test is executed from the slave test handler, e.g. during soak testing, the test range is limited to 64 Mbytes; however, each time the BIST is executed it tests a different block. Therefore, over the duration of a soak-test run, the whole of memory will be tested a number of times, but the overall test coverage will be improved for large memory capacity boards.

When the test is executed from the master test handler, the test range is from 1 Mbyte to the top of fitted memory. However, BIST parameters can be used to specify a different test range. Note that the video memory hole between A0000h and BFFFFh must be avoided.

First, the memory under test is initialized to 00000000. Then two “marches” are made through memory with patterns as follows:

pass 1	new=FFFFFFFF	old=00000000
pass 2	new=00000000	old=FFFFFFFF

During the march through the memory range, for every 32-bit word location, first the old pattern is verified, then the new pattern is written and verified.

To reduce execution time this BIST runs from DRAM; however, the area of memory from which the test code executes is first tested by the ROM-based version of the routine.

Test 12 Error codes:

0300h – test failed. For details see accompanying message

12.2.9 Test 13: SCC Access Test

This BIST performs a read-after-write test on each serial channel of the board.

The serial controller’s scratch register is used for this test. A write-then-read of a shifting one value is used to test access to the device. The value is written then read and verified.

Test 13 Error codes:

04x0h – failure on channel x. Accompanying message gives further details

12.2.10 Test 19: NMI Test

This test checks the generation of an NMI interrupt from the front panel switch. The switch “FP Switch Function” on the board must be set to the NMI position.

Test 19 Error codes:

0401h – no interrupt
0402h – wrong interrupt
0403h – wrong interrupt source

12.2.11 Test 20: Universe NMI Test

This BIST checks the ability of the Universe II to generate a NMI to the processor using the software generated interrupt via LINT1.

Test 20 Error codes:

0406h – no interrupt generated or spurious interrupt

12.2.12 Test 22: Local RAM Data and Address Bus Test

This BIST tests RAM data and address buses.

The data bus test verifies that each bit on the data bus can be set and cleared for each memory row.

The address bus test checks that each address line on the bus is connected correctly.

The default memory range under test is from 1 Mbyte to the top of fitted memory.

Test 22 Error codes:

0401h – error on data bus
0402h – error on address bus
0403h – error clearing Memory

12.2.13 Test 23: Local RAM Read/Write Test

This BIST is a simple non-destructive read-complement-write test. The range of memory to be tested depends upon the test handler from which the BIST was invoked.

When the test is executed from the slave test handler, e.g. during soak testing, the test range is limited to 64 Mbytes; however, each time the BIST is executed it tests a different block. Therefore, over the duration of a soak-test run the whole of memory will be tested a number of times, but the overall test coverage will be improved for large memory capacity boards.

When the test is executed from the master test handler, the test range is from 1 Mbyte to the top of fitted memory. However, BIST parameters can be used to specify a different test range. Note that the video memory hole between A0000h and BFFFFh must be avoided.

The test operates on double words throughout the range selected. During the test, PCI Bus Error interrupts are enabled. If one of these should occur the test is aborted and a diagnostic message displayed.

To reduce execution time this BIST runs from DRAM; however, the area of memory from which the test code executes is first tested by the ROM-based version of the routine.

Test 23 Error codes:

0300h – test failed. For details see accompanying message
0402h – PCI bus error occurred

12.2.14 Test 25: Local RAM Dual Address Test

This BIST checks for Dual Addressing in the RAM. The range of memory to be tested depends upon the test handler from which the BIST was invoked.

When the test is executed from the slave test handler, e.g. during soak testing, the test range is limited to 64 Mbytes; however, each time the BIST is executed it tests a different block. Therefore, over the duration of a soak-test run the whole of memory will be tested a number of times, but the overall test coverage will be improved for large memory capacity boards.

When the test is executed from the master test handler, the test range is from 1 Mbyte to the top of fitted memory. However, BIST parameters can be used to specify a different test range. Note that the video memory hole between A0000h and BFFFFh must be avoided.

The BIST proceeds to write the memory address, rotated two bit positions, to each Dword location. When the whole test region has been written, the memory is read back and compared against the expected value. By using the memory address as test data, any incorrect values will identify the dual-addressed memory location.

During the test, the PCI Bus Error interrupts are enabled. If one of these should occur, the test is aborted and a diagnostic message displayed.

To reduce execution time this BIST runs from DRAM; however, the area of memory from which the test code executes is first tested by the ROM-based version of the routine.

Test 25 Error codes:

0300h – test failed; associated message gives details
0402h – PCI bus error occurred

12.2.15 Test 27: Local RAM Execution Test

This BIST executes code from RAM in the selected test region. The range of memory to be tested depends upon the test handler from which the BIST was invoked.

When the test is executed from the slave test handler, e.g. during soak testing, the test range is limited to 64 Mbytes; however, each time the BIST is executed it tests a different block. Therefore, over the duration of a soak-test run the whole of memory will be tested a number of times, but the overall test coverage will be improved for large memory capacity boards.

When the test is executed from the master test handler, the test range is from 1 Mbyte to the top of fitted memory. However, BIST parameters can be used to specify a different test range. Note that the video memory hole between A0000h and BFFFFh must be avoided.

This test copies a small string of code into the selected RAM area and executes out of that RAM. The buffer is first filled with INT3 opcodes, and then the sequence of instructions is copied to the beginning of the buffer. A jump is made to the code, which copies itself to the next available location in the buffer, then overwrites the old copy with INT3 instructions once more. If an error occurs such that it the code jumps into a location outside the instruction sequence, this is trapped via the INT3 instructions.

When the test code reaches the end of the buffer, it returns to the caller and the test has passed.

During the test, the PCI Bus Error interrupts are enabled. If one of these should occur, the test is aborted and a diagnostic message displayed.

Test 27 Error codes:

0300h – test failed: for details see accompanying message
0402h – PCI bus error occurred

12.2.16 Test 28: SCC Interrupt Test

This BIST checks that each serial channel on the board is capable of generating an interrupt.

A null character is transmitted on each channel in turn to generate a transmit interrupt from that channel. If the interrupt occurs, checks are made to ensure that there is a transmit interrupt pending on the serial device. A channel specific interrupt is generated for each channel in turn.

Test 28 Error codes:

04xyh – the error number is encoded in the following way:

x – channel Number for which interrupt was generated.
y – error type:
1 – no interrupt,
2 – wrong interrupt,
3 – no interrupt pending indicated,
4 – no TX interrupt pending.

12.2.17 Test 29: SCC Internal Loopback Test

This BIST performs an Internal Loopback Test on each serial channel of the board.

Each channel in turn is switched into Internal Loopback Mode, and 255 characters are transmitted and received. The data received is checked against the data sent (ascending byte values, 0..254). The test runs in asynchronous mode at 9600 baud.

Test 29 Error codes:

04x1h – timed out waiting for TxRDY
04x2h – timed out waiting for RxRDY
04x3h – data mismatch on compare after write

where x is the channel.

12.2.18 Test 30: SCC External Loopback Test

This BIST performs an External Loopback Test on serial channel A (COM1) of the board.

Channel A should be looped back externally to itself by connecting TxDA to RxDA, DSR and CD to DTR, RTS and CTS together.

The test sequence is identical to the Internal Loopback Test described above, followed by a test in which the modem signals are manipulated independently to check their functionality.

Test 30 Error codes:

04xyh – the error number is encoded in the following way:

x – channel under test
y – error type
1 – timed out waiting for TxRDY
2 – timed out waiting for RxRDY
3 – data mismatch on compare after write
4 – RTS Active, message gives details
5 – RTS Inactive, message gives details
6 – DTR Active, message gives details
7 – DTR Inactive, message gives details

12.2.19 Test 31: 855 Integrated Graphics Device Test

This BIST checks the operation of the Intel 855 Integrated Graphics device

First a register access test is performed to the hardware cursor high and low registers; this uses ports 03D4h and 03D5h. Then the linear video memory is auto-sized and the result reported. Finally, the linear video memory is tested via 16-bit accesses using the address offset as a pattern.

Test 31 Error codes:

0401h – no Intel 855 IGD console available
0402h – failed register test with 055h pattern
0403h – failed register test with 0AAh pattern
0404h – device sub-type unrecognized
0405h – failed linear memory pattern test

12.2.20 Test 32: MPT SCSI/SATA Controller Tests

This BIST tests the LSI 53C1020 single channel SCSI controller on the baseboard as well as any other MPT Fusion SCSI controllers located in the PMC site. If no sub-test is specified, the default, test 0, is performed on all instances of MPT Fusion SCSI controllers that can be detected.

The following sub-tests are available, (D) indicates a test run by default:

0 – Controller Test (D)
1 – Scan for Devices

12.2.20.1 Sub-Test 1: Controller Test

This sub-test checks access to the MPT Fusion SCSI controller(s) and confirms that it's interrupt-based message passing interface is operating correctly.

12.2.20.2 Sub-Test 2: Scan for Devices

This sub-test scans the port of the MPT Fusion SCSI controller(s) for SCSI / SATA hard drives. For each device, the Manufacturer, Model, and Revision are presented as well as the drive capacity, and whether or not the Master Boot Record (MBR) could be detected.

For this test to pass, each SCSI controller port must have at least one drive attached, with a MBR.

12.2.20.3 Syntax

These tests can be performed on a specific instance of MPT Fusion SCSI controller, or on all instances. By default the controller test is performed on all instances.

`t32` – performs controller test on all instances

`t32, 0, 1` – performs controller test on 1st instance only

`t32, 1, 0` – performs 'scan for devices' on all instances

`t32, 1, 2` – performs 'scan for devices' on 2nd instance only.

12.2.21 Test 33: Universe PCI -> VME Test

This BIST performs a basic functional check on the Universe II. First, a write-then-read test is performed on PCI3 slave BS register. Then interrupt generation is tested by performing a posted write to a non-existent VME address.

Test 33 Error codes:

0402h – error in read/write test
0406h – no interrupt or spurious interrupt during test

12.2.22 Test 34: Universe PCI Config Utility

This pseudo test configures a Universe PCI slave image register for off-board VME accesses.

The following parameters are required:

Slave to program	(Default = 3)
Lower Address	(Default = 90000000h)
Upper Address	(Default = 91000000h)
Translation Offset	(Default = 0)
Control Register Value	(Default = 80820000h)

This test does not fail.

12.2.23 Test 35: Universe VME Config Utility

This pseudo test configures a Universe VME slave image register so the board responds to VME accesses.

The following parameters are required:

Slave to program	(Default = 3)
Lower Address	(Default = 90000000h)
Upper Address	(Default = 91000000h)
Translation Offset	(Default = 0)
Control Register Value	(Default = 80520000h)

This test does not fail.

12.2.24 Test 36: VME Bus Byte Swapping

This BIST is used to test the Hardware Byte Swapping Features when reading / writing the VME bus. The test requires another board in the VME rack to test with.

The test works by configuring a Universe PCI slave image for VME bus access, writing known Byte, Word and Double word values to the slave VME board then enabling Byte Swapping in the control register. Quad word values are written and read by 64-bit DMA transfer.

The data is read back and compared with expected values, any discrepancies are reported along with the error codes.

The Universe slave image and Byte swapping is disabled at the end of the test.

When testing is performed using a Concurrent Technologies soak master, this test will operate as a co-operating BIST where two boards perform the Byte Swapping test on each others memory simultaneously.

Test 36 Error Codes:

0410h – error comparing byte 0
0411h – error comparing byte 1
0412h – error comparing byte 2
0413h – error comparing byte 3
0420h – error comparing word 0
0421h – error comparing word 1
0430h – error comparing double word
0440h – error comparing quad word
0441h – error in 64-bit DMA transfer

12.2.25 Test 37: Bus Error Detection

This BIST checks the operation of the VME Bus Error Detection facilities available on the VP 31x/02x board. This BIST is composed of a series of sub-tests. The sub-test number is selected by a BIST parameter; when run without parameters, all sub-tests are performed.

The available sub-tests are listed below, a (D) against the test indicates that it is executed by default when no parameters are supplied.

0 – Perform all default (D) tests
1 – VME Bus Error Detection [by polling] (D)
2 – VME Bus Error Detection [by interrupt] (D)
3 – VME Bus Error Address Capture (D)

12.2.25.1 Sub-Test 1: VME Bus Error Detection [by polling]

This sub-test checks the operation of the VME Bus Error Detection facility. The Universe is configured, for the duration of the sub-test, to map free PCI memory to a non-existent 64k block of VME memory starting at address 0E0000000h. The sub-test reads the VME memory and checks that a VME bus error is detected within 1 ms.

12.2.25.2 Sub-Test 2: VME Bus Error Detection [by interrupt]

This sub-test checks the operation of the VME Bus Error Detection facility. The Universe is configured, for the duration of the sub-test, to map free PCI memory to a non-existent 64k block of VME memory starting at address 0E0000000h. The sub-test reads the VME memory and checks that the VME bus error generates an interrupt within 1 ms.

12.2.25.3 Sub-Test 3: VME Bus Error Address Capture

This sub-test checks the operation of the VME Bus Error Address Capture facility. The Universe is configured, for the duration of the sub-test, to map free PCI memory to a non-existent 64K block of VME starting at address 0E0000000h. The sub-test reads the VME memory and checks that the VME Address Capture Read Register contains same value as the address of the accessed VME memory.

Test 37 Error codes:

0400h – sub-test does not exist
0410h – the Universe peripheral was not found
0411h – the South Bridge peripheral was not found
0420h – unable to clear the “VME Bus Error Detected” flag
0421h – unable to reset the “VME Bus Error Detected” flag
0422h – no VME Bus Error was detected
0423h – the VME Bus Error did not generate an interrupt
0424h – the VME Bus Error generated the wrong interrupt
0430h – timeout during address capture
0431h – wrong captured address

12.2.26 Test 39: ICH Watchdog Test

This BIST checks the watchdog facilities available on this board. The BIST is composed of a series of sub-tests. The sub-test number is selected by a BIST parameter; when run without parameters, a default series of sub-tests is performed.

The available sub-tests are listed below, a (D) against the test indicates that it is executed by default when no parameters are supplied.

0 – Perform all Default (D) Tests
1 – Watchdog Interrupt Test (D)
2 – Watchdog Reset Test

12.2.26.1 Sub-Test 1: Watchdog Interrupt Test

This sub-tests verifies that in normal operation no interrupt (or reset) is generated by the watchdog. The test also verifies the ability of the watchdog to generate an interrupt when its time-out expires.

12.2.26.2 Sub-Test 2: Watchdog Reset Test

This sub-test checks the ability of the watchdog to reset the board when the time-out counter expires. The test first checks that the watchdog can operate without generating a reset when it is being restarted regularly.

NOTE: The successful completion of this BIST will result in the board being reset.

Test 39 Error codes:

0400h – sub-test does not exist
0410h – the watchdog is not hardware enabled
0420h – restarting failed to prevent watchdog time-out
0421h – a spurious interrupt was generated while restarting the watchdog
0422h – no Interrupt was generated restarting when the watchdog was not restarted
0423h – a spurious interrupt was generated when the watchdog was not restarted
0424h – reset was expected, but an interrupt was received
0425h – the board did not reset when the watchdog was not restarted

12.2.27 Test 40: LDT and PIT Test

This BIST checks the operation of the LDT (Long Duration Timer) and the PIT (Periodic Interrupt Timer) facilities available on this board. This BIST is composed of a series of sub-tests. The sub-test number is selected by a BIST parameter; when run without parameters, all sub-tests are performed.

The available sub-tests are listed below, a (D) against the test indicates that it is executed by default when no parameters are supplied.

0 – Perform all default (D) tests
1 – Standard LDT / PIT Functional Test (D)
2 – Enhanced LDT / PIT Functional Test (D)

12.2.27.1 Sub-Test 1: Standard LDT / PIT Functional Test

This sub-test checks the operation of the LDT and all the frequencies of the PIT. The LDT's holding register is set to an appropriate value and the LDT is started. The sub-test checks that a "roll-over" is generated within an appropriate time. This sub-test is then repeated for all the frequencies of the PIT.

12.2.27.2 Sub-Test 2: Enhanced LDT / PIT Functional Test

This sub-test checks the operation of the LDT and all the frequencies of the PIT. The LDT's holding register is set to an appropriate value and the LDT is started. The sub-test checks that a "roll-over" is generated causing an interrupt within an appropriate time. This sub-test is then repeated for all the frequencies of the PIT.

Test 40 Error codes:

0400h – sub-test does not exist
0410h – LDT failed standard test
0411h – PIT failed standard test when programmed frequency = 100Hz
0412h – PIT failed standard test when programmed frequency = 200Hz
0413h – PIT failed standard test when programmed frequency = 500Hz
0414h – PIT failed standard test when programmed frequency = 1kHz
0415h – PIT failed standard test when programmed frequency = 2kHz
0416h – PIT failed standard test when programmed frequency = 5kHz
0417h – PIT failed standard test when programmed frequency = 10kHz
0420h – LDT failed enhanced test
0421h – PIT failed enhanced test when programmed frequency = 100Hz
0422h – PIT failed enhanced test when programmed frequency = 200Hz
0423h – PIT failed enhanced test when programmed frequency = 500Hz
0424h – PIT failed enhanced test when programmed frequency = 1kHz
0425h – PIT failed enhanced test when programmed frequency = 2kHz
0426h – PIT failed enhanced test when programmed frequency = 5kHz
0427h – PIT failed enhanced test when programmed frequency = 10kHz

12.2.28 Test 56: IDE Controller Test

This BIST checks the operation of the embedded IDE controller that forms part of the 6300ESB south bridge.

This test consists of a number of sub-tests, which can be selected via a command line parameter. If the BIST is invoked without parameters, only those tests that exercise the controller are performed. The following sub-tests are available, (D) indicates a test run by default:

0 – Run default tests (D)
1 – Register access test (D)
2 – Controller diagnostics test (D)
3 – Identify disk drive

12.2.28.1 Sub-Test 1: Register Access Test

This sub-test performs a write-then-read check on the controllers internal registers. The sectors-per-track, sector-number and low-cylinder-count registers are tested.

12.2.28.2 Sub-Test 2: Controller Diagnostics Test

This sub-test invokes the IDE controller's internal diagnostic check. If the check fails, the diagnostic error code is displayed.

12.2.28.3 Sub-Test 3: Identify Disk Drive

This sub-test uses the 'Identify Drive' command to interrogate the controller on the disk drive. The manufacturers model name, the physical geometry and the highest supported PIO, DMA and UDMA modes are displayed.

Test 56 Error codes:

0400h – register test miscompare
0401h – controller diagnostics error
0402h – drive identify generated an error
04FFh – disk controller not found

NOTE: An IDE disk drive must be connected for the BIST to operate.

12.2.29 Test 63: PS/2 Mouse Test

This BIST tests the PS/2 port and PS/2 mouse. The PS/2 port test includes opening auxiliary port on keyboard controller, sending echo to auxiliary port and test auxiliary bus.

The PS/2 mouse test resets mouse, reads identify device and echo from PS/2 mouse and tests mouse buttons and moving.

The following sub-tests are available, (D) indicates a test run by default:

0 – Test mouse without error time-out
1 – Test mouse action (D)
2 – Test only the PS/2 port

12.2.29.1 Sub-Test 0: Test mouse without error time-out

This option checks PS/2 port and PS/2 mouse. It displays mouse buttons and moving actions for 10s.

12.2.29.2 Sub-Test 1: Test mouse action

This is default option. Like option one, it does a PS/2 port test and mouse test. Every mouse action (press left or right button, move up, down, left and right) is tested separately. Time-out is 5s for every action.

Test 63 Error codes:

0401h – time-out trying to flush keyboard controller buffer
0402h – keyboard controller did not read auxiliary enable command
0403h – keyboard controller did not read mode command
0404h – keyboard controller did not read mode command data
0405h – no echo from auxiliary port
0406h – wrong echo from auxiliary port
0407h – did not find PS/2 mouse
0408h – PS/2 mouse reported error after reset
0409h – no identify from PS/2 mouse
040Ah – wrong identify from PS/2 mouse
040Bh – no echo from PS/2 mouse
040Ch – wrong echo from PS/2 mouse
040Dh – no ACK from PS/2 mouse
040Eh – received byte from PS/2 mouse is not ACK
040Fh – no data byte from PS/2 mouse
0410h – no data packet from PS/2 mouse
0411h – time-out waiting for test [mouse buttons and mouse moving]
0412h – auxiliary interface test command not read
0413h – time-out waiting for auxiliary interface test result
0414h – interface test fail. Auxiliary clock line stuck high
0415h – interface test fail. Auxiliary clock line stuck low
0416h – interface test fail. Auxiliary data line stuck high
0417h – interface test fail. Auxiliary data line stuck low

12.2.30 Test 64: PC Keyboard Test

This BIST performs checks on the keyboard controller, and also determines whether a keyboard is present.

First, the keyboard controller's output buffer is flushed and a 'keyboard present' test is performed. The keyboard controller is then enabled and initialized and if successful, the keyboard controller's self test and interface test are performed. Finally a keyboard interrupt is generated and verified.

Test 64 Error codes:

0401h – time-out trying to flush keyboard controller buffer
0402h – keyboard controller did not read keyboard enable command
0403h – keyboard controller did not read mode command
0404h – keyboard controller did not read mode command data
0405h – self test command not read
0406h – time-out waiting for self test result
0407h – self test fail
0408h – keyboard controller not ready after self test
0409h – interface test command not read
040Ah – time-out waiting for interface test result
040Bh – interface test fail. Keyboard clock line stuck high
040Ch – interface test fail. Keyboard clock line stuck low
040Dh – interface test fail. Keyboard data line stuck high
040Eh – interface test fail. Keyboard data line stuck low
0410h – error while trying to cause an interrupt
0411h – no keyboard interrupt
0412h – wrong interrupt received

12.2.31 Test 67: Printer Port Test

This BIST checks the PC compatible printer port using a Concurrent Technologies printer test fixture.

A marching 1/0 test is performed on the PORTC and PORTA registers. Then a marching 1/0 test is performed on PORTA via test fixture. Finally, a 1/0 test is performed on PORTB driven by PORTA and PORTC, via the test fixture.

Test 67 Error codes:

0450h - PORTC marching ‘0’ failed
0451h - PORTC marching ‘1’ failed
0452h - PORTA marching ‘0’ failed
0453h - PORTA marching ‘1’ failed
0454h - PORTA marching ‘0’ via test fixture failed
0455h - PORTA marching ‘1’ via test fixture failed
0458h - PORTB write 0h failed
0459h - PORTB write STB = 0 failed
045Ah - PORTB write PINIT = 1 failed
045Bh - PORTB write PSEL = 1 failed
045Ch - PORTB write PORTA D0 = 1 failed
045Dh - PORTB write PORTA D0 = 1 failed

12.2.32 Test 68: Real Time Clock Test

This BIST tests the PC compatible, real time clock. The BIST provides a number of sub-tests, which are selected by a command parameter. If no parameter is supplied the current time and date is displayed, the interrupt signal is tested and the non-destructive NVRAM test performed.

The following sub-tests are available:

0 – Set the date and time
1 – Display time and date, then do interrupt test
2 – Clear content of NVRAM
3 – Display contents of NVRAM
4 – Non-destructive read/write test of NVRAM

12.2.32.1 Sub-Test 0: Set date and time.

Enter 0 followed by:

Hour (0 - 23)
Minute (0 - 59)
Day (1 - 31)
Month (1 - 12)
Year (0 - 99)

12.2.32.2 Sub-Test 1: Display Time and Date, then do Interrupt Test

The RTC periodic interrupt is allowed to interrupt twice to test that the interrupt is acknowledged correctly.

12.2.32.3 Sub-Test 2: Clear Contents of NVRAM

12.2.32.4 Sub-Test 3: Display Contents of NVRAM

12.2.32.5 Sub-Test 4: Non-Destructive Read/Write Test of NVRAM.

The read/write test checks each location of NVRAM (excluding the RTC registers). Each address is tested first with 0x55, then with 0xAA. The contents of NVRAM is saved and restored around the test.

Test 68 Error codes:

0300h – fail - message will describe failure in some detail
04xyh – the error number is encoded in the following way:
x – fault code:
    0 – no interrupt occurred
    1 – wrong interrupt occurred
y – test numbers:
    2 – timer 0 interrupt
    4 – timer 2 interrupt
    5 – first RTC periodic interrupt
    6 – second RTC periodic interrupt
0440h – test pattern 1 fail
0441h – test pattern 2 fail

12.2.33 Test 70: Maxim 6656 Sensor

This BIST checks the operation of the Maxim 6656 Voltage and Thermal Sensor.

This BIST will read and display the following information.

- Ambient temperature
- CPU Temperature
- 12V Power Supply
- 5V Power Supply
- 3.3V Power Supply
- CPU Power Supply Voltage

Test 70 Error Codes:

0421h – the CPU thermal sensor open circuit
0422h – the CPU thermal sensor is reading 0ºC
0423h – the CPU thermal sensor is reading 127ºC
04FFh – the CPU thermal sensor has exceeded its safety limit

12.2.34 Test 72: Intel 8254X GigaBit LAN

This BIST is intended for factory use only.

12.2.35 Test 74: Intel 8254X Front GigaBit I/F Test

This BIST is intended for factory use only.

12.2.36 Test 75: Intel 8254X Local Loopback Test

This BIST is intended for factory use only.

12.2.37 Test 85: Floppy Disk Drive Test

This BIST checks the operation of the PC compatible floppy disk controller and associated hardware. The BIST comprises a number of sub-tests, of which only the Floppy Controller test is run by default. The BIST operates on drive A: by default, however drive B: can be specified by a BIST parameter.

12.2.37.1 Controller Access Test

This sub-test checks access to the floppy disk controller hardware. No disk drive is required for this test.

12.2.37.2 Diskette Access Test

This sub-test checks access to a floppy disk drive by reading a single sector from a floppy disk. The content of the disk is not important; the first 256 bytes of the sector will be displayed on screen.

12.2.37.3 Disk Checksum Test

This sub-test reads the entire contents of a floppy disk and computes the byte checksum (32-bit sum-of-bytes). The computed checksum value is displayed allowing different test disks to be used.

Test 85 Error codes:

0420h - failure during Floppy Controller test
0440h - failure during Disk Access test
0480h - failure during Disk Verify test
04FFh - invalid BIST parameter supplied

These values are modified by adding the following sub-codes to identify the cause of the error:

01h - Error during controller command phase
02h - Error writing data to the controller
04h - Error reading data from the controller
08h - Wrong interrupt received
10h - No interrupt received

12.2.38 Test 90: Intensive Memory Test

This BIST is intended for factory use only.

12.2.39 Test 101: Display Memory Utility

This BIST allows any area of the target board's local memory to be examined and displayed by the test master. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

start address of memory area (default 0)
length of memory area in bytes (default 10h)
data type (1 for byte, 2 for word, and 4 for dword)(default 1)

The results are displayed as hexadecimal values.

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.40 Test 102: Fill Memory Utility

This BIST allows any area of the target board's local RAM to be filled with a constant value by the test master. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

start address of memory area (default 0)
data type (1 for byte, 2 for word, and 4 for dword) (default 1)
length of RAM area in bytes (default 1)
constant value with which to fill the area (default 0)

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.41 Test 103: I/O Read Utility

This BIST allows examination of any I/O register on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

16-bit I/O address (default 0)
data type (1 for byte, 2 for word, and 4 for dword) (default 1)
increment value for the port address (default 1)
number of times to perform an I/O read (default 1)

The result is displayed as a hexadecimal value.

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.42 Test 104: I/O Write Utility

This BIST allows modification of any I/O register on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

16-bit I/O address (default 0)
value to write to register (default 0)
data type (1 for byte, 2 for word, and 4 for dword) (default 1)
increment value for the port address (default 1)
number of times to perform an I/O write (default 1)

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.43 Test 105: Interconnect Read Utility

This BIST allows a local interconnect read to be performed on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameter is:

interconnect register number (16-bit value)

The result is displayed as a hexadecimal value.

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.44 Test 106: Interconnect Write Utility

This BIST allows a local interconnect write to be performed on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

Because this operation is carried out as a local access on the target board, it allows a remote agent to write to interconnect registers for which it would normally have read-only access.

The parameters are:

interconnect register number (16-bit value)
new register value (8-bit value)

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.45 Test 107: Cache Control Utility

This BIST allows the status of DRAM and EPROM caching on the target board to be interrogated or configured. If the utility is invoked without parameters, the default action is to display the state of DRAM and EPROM caching.

The available options are:

0 – Disable DRAM caching
1 – Enable DRAM and EPROM caching
2 – Toggle DRAM caching state
3 – Report DRAM and EPROM caching state (default)
4 – Disable EPROM caching

NOTE: In normal operation, EPROM Caching should not be disabled. When EPROM caching is disabled, ROM-based timing loops are disrupted, which can cause BISTs to time-out or fail.

12.2.46 Test 120: PCI Configuration Utility

This BIST will display, for each device on the PCI bus, the vendor identification number, device identification number and the device revision number. For example:

Bus	Dev	Func	Vendor ID	Device ID	Revision
00	00	00	8086	3580	02
00	00	01	8086	3584	02
00	00	03	8086	3585	02
00	02	00	8086	3582	02
00	02	01	8086	3582	02
..	..	..	....	....	..

NOTE: The revision numbers may change.

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.47 Test 121: PCI Read Utility

This BIST allows PCI configuration registers to be examined on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

Device number	= 0 to 31 - default = 0
Register Offset	= 0 to 255 - default = 0
Data Type	= 1 (Byte), 2 (Word) or 4 (Dword) - default = 2
Length	= number of bytes, words, Dwords
Bus Number	= 0 to 255 - default = 0
Function Number	= 0 to 7 - default = 0

The result is displayed as a hexadecimal value.

This is not a true BIST, but merely provides a utility function, and so always returns a PASS status.

12.2.48 Test 122: PCI Write Utility

This BIST allows PCI configuration registers to be modified on the target board. This utility requires command-line parameters to function correctly, so it should only be run in an interactive manner by a local or remote test master.

The parameters are:

Device number	= 0 to 31 - default = 0
Register Offset	= 0 to 255 - default = 0
Value to write	= ? (Default 0)
Data Type	= 1 (Byte), 2 (Word) or 4 (Dword) - default = 2
Length	= number of bytes, words, Dwords
Bus Number	= 0 to 255 - default = 0
Function Number	= 0 to 7 - default = 0
Verify	= 0 (no verify), 1 (verify by reading back) - default = 0

12.2.49 Test 126: Board Configuration Utility

This pseudo-test displays the board configuration as seen by the processor. It performs no actual testing, and assumes a basic level of operation by the board. The test does not fail.

The test does not run at power-up, though it can be invoked thereafter by a Master Test Handler.

12.2.50 Test 127: Retrieve BIST Information

This BIST is intended to provide information only for factory testing of the board. It does not fail, but returns information in an encoded form for use during automatic testing prior to shipment.

The test is normally run only by a Test Master.

13 SYSTEM MANAGEMENT

13.1 Power Management

The Intel Pentium M processor incorporates a mechanism for changing the processor's operating frequency and core voltage under software control. By making these reductions the board's maximum power consumption is also reduced. See Table A-1 for more details.

The Intel Pentium M processor supports a number of discrete operating frequencies (typically five or six) that vary between 600 MHz and full speed (see Table 13-1). The BIOS provides a Setup menu (**`Advanced | CPU Settings | CPU Operating Frequency`**) that allows the operating frequency of the CPU to be set prior to booting an operating system. By default the CPU will operate at full speed.

1.8 GHz Intel Pentium M Processor 745	1.6 GHz Intel Pentium M Processor	1.4 GHz Intel Pentium M Processor 738
1.8 GHz	1.6 GHz	1.4 GHz
1.6 GHz	1.4 GHz	1.2 GHz
1.4 GHz	1.2 GHz	1.0 GHz
1.2 GHz	1.0 GHz	800 MHz
1.0 GHz	800 MHz	600 MHz
800 MHz	600 MHz	
600 MHz		

Table 13-1 CPU Operating Speed BIOS Options

This mechanism for power reduction allows the board to operate in environments where power capacity is limited (e.g. under battery power), or in systems where cooling airflow is less than adequate. In this last case it may be wise to also consider some of the Thermal Management options available on this board (see Section 13.2).

The operating frequency of the Intel Celeron M processor is fixed and cannot be changed under software control. This processor also does not support the thermal management modes described in Section 13.2.

NOTE: During POST, the BIOS will always report the maximum possible CPU frequency, as specified by the CPU's Brand String.

13.2 Thermal Management

The maximum power dissipation of the Intel Pentium M processor may sometimes be higher than that of previous Mobile Intel Pentium processors. Under typical load conditions, the heatsink (and cooling airflow) will keep the processor die temperature within specification. However, if the board is running CPU-intensive or stress software or if the airflow is inadequate, the heatsink alone may not be able to prevent the processor overheating.

To ensure that the processor always operates within its thermal specifications, it includes several thermal management and protection functions. Each of these is described below. A BIOS setup option is used to select which functions are to be enabled. See Section 13.2.4 for further details.

13.2.1 Thermal Monitor 1 (TM1)

TM1 uses a temperature sensor located near to the hottest part of the processor die. If it detects a critically high temperature a thermal control circuit (TCC) will modulate (i.e. alternately stop and start) the processor core clocks. This causes the processor to halt for short periods and decreases its power consumption, which in turn lowers the die temperature.

The severity of the modulation will increase as the die temperature rises, up to a maximum of about 50%. The TCC will cease modulation when the die temperature has fallen to a non-critical value.

The temperature sensor is individually calibrated by Intel. The TM1 characteristics are also fixed by Intel and cannot be modified.

The drawbacks of TM1 are that it starts to operate at a relatively low temperature (about 90°C) and that it has a low modulation rate, which can produce undesirable software latencies.

TM1 is disabled after Reset and has to be enabled by the BIOS (see Section 13.2.4).

13.2.2 Thermal Monitor 2 (TM2)

TM2 uses the same temperature sensor as TM1. When the TM2 thermal control circuit is triggered, the CPU operating frequency and core voltage will be reduced, causing the power consumption to fall, which in turn lowers the die temperature.

Because a CPU under TM2 control operates continuously, the overall system performance for a given reduction in power consumption is higher than TM1. System latency is also lower when using TM2.

The drawback of TM2 is that changes to the operating frequency will also affect the Time Stamp Counter (TSC) rate and any timing or calculations that use it.

TM2 is disabled after Reset and has to be enabled by the BIOS (see Section 13.2.4).

13.2.3 CPU Thermal Trip

The processor chip also contains a thermal trip circuit. This is intended to protect the processor in the event of a catastrophic cooling failure. If the die temperature reaches approximately 135°C, it shuts down the processor core and asserts the THERMTRIP# signal. Logic on the board responds to this assertion by removing the processor core voltage within a few milliseconds.

A power cycle (i.e. OFF then ON) is required to restore normal operation. The thermal trip circuit is always operational and cannot be disabled.

13.2.4 PC BIOS Setup Options

The PC BIOS Setup Menu provides control over the thermal management functions, using the setting for the **`Advanced | CPU Settings | Thermal Management`** option. It offers three choices, namely:

- Disabled - only the Thermal Trip is enabled
- Thermal Monitor 1 - the CPU's clock modulation mechanism is used to reduce power consumption; the Thermal Trip is enabled
- Thermal Monitor 2 - the CPU operating frequency is lowered to reduce power consumption; the Thermal Trip is enabled

The default setting is "**`Disabled`**".

It may be desirable that some form of thermal management is enabled to handle operation at very high load and high temperature. Under normal conditions, even with high loads, the standard heatsink and specified forced air cooling are adequate to keep the processor operating within its limits even with the Thermal Management option set to **`Disabled`**. The BIOS setup option provides a means to enable additional protection if there is any concern about heat dissipation in the particular system being used.

13.2.5 Processor Thermal Status Indication

The User LED may be programmed to indicate if the processor die has reached the critical temperature at which thermal management is activated. This is done using the User LED Mode option switch. Figure 13-1 shows the location of this switch on the board and its settings.

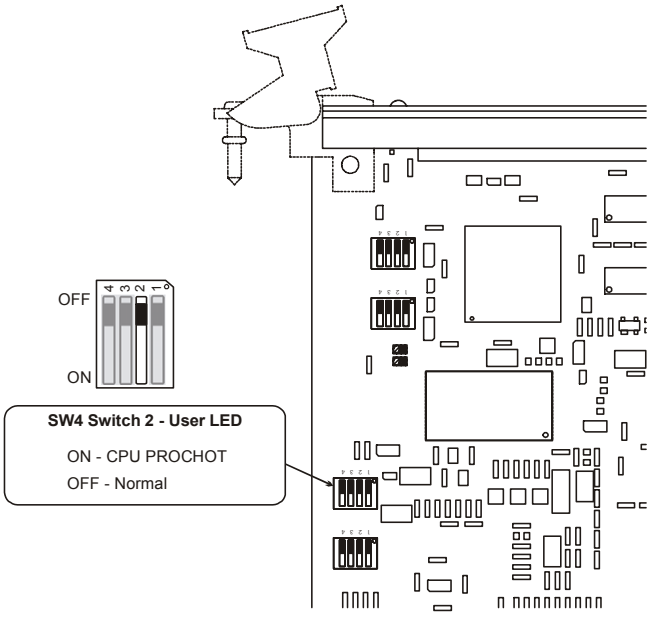


Figure 13-1 User LED Switch

The User LED will also indicate a CPU Thermal trip. See Section 13.2.3 for details.

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A SPECIFICATIONS

A.1 Functional Description

Processor:	• 1.8 GHz, 1.6 GHz or 1.4 GHz Intel Pentium M processor, or 1.0 GHz Intel Celeron M processor.
Level 2 Cache:	• 512 Kbytes on-die RAM operating at core frequency (1.0 GHz processor). • 1024 Kbytes on-die RAM operating at core frequency (1.6 GHz processor). • 2048 Kbytes on-die RAM operating at core frequency (1.8 GHz and 1.4 GHz processor).
Memory:	• 1 Mbytes Flash EPROM for PC BIOS and factory test firmware VSA using socketed Firmware Hub device. • DDR SDRAM 0.5 to 2 Gbytes as defined by order number.
Interfaces:	• 64-bit VME interface utilizing the Tundra Universe II VME PCI bridge, with Endian byte swapping. • Single Ended Wide SCSI interface using the LSI 53C1020. • Two RS232 serial channels using 16550 compatible UARTs. • EIDE/Ultra ATA100 interface via P2 and on-board mass storage option interface. • Two Serial ATA150 interfaces via P0 connector (in selected board configurations only). • Floppy disk interface supporting up to two drives via P2. • Four USB2 interfaces via front panel and P2 connectors; 1.5, 12 and 480 Mbit/s interfaces supported. • Single-width PMC site supporting a 64/32-bit 66/33 MHz PCI interface with 5V or 3.3V signaling. Both 5V and 3.3V power rails are provided. • Expansion to a PMC carrier board. 32-bit, 33 MHz PCI interface with 5V or 3.3V signaling supported. • PS/2 compatible keyboard interface, front panel connections. • PS/2 compatible mouse interface, front panel connections. • 2 Ethernet interfaces using 82546GB Ethernet controller, 10/100/1000 Mbit/s, front panel access via RJ45 connectors. • VGA CRT interface with up to 64 Mbytes of UMA RAM and supporting resolutions up to 2048 x 1536 with up to 16 million colors. Front panel connection. Digital video output. Rear connection via P2. • 2 General Purpose I/O ports.
Peripherals:	• Intel 6300ESB ICH device provides standard PC-AT architecture peripherals. • PC AT Real Time Clock. • 32-bit Long Duration Timer with processor interrupt capability.

NOTE: Interface accessibility is dependent upon the build options and associated breakout boards, refer to the product datasheet for further details.

SPECIFICATIONS

A.2 Environmental Specification

	Standard Temperature (N-Series)	Extended Temperature (E-Series)	Extended Temperature (K-Series)
Temperature Range (operating)	0°C to +55°C	-25°C to +70°C	-40°C to +85°C
Temperature Range (storage)	-40°C to +70°C	-40°C to +70°C	-40°C to +85°C
Airflow (linear feet per minute)	300 LFM	Up to 400 LFM	400 LFM
Relative Humidity (operating)	10% to 90%	10% to 90%	10% to 90%
Relative Humidity (storage)	10% to 90%	10% to 90%	10% to 90%
Humidity Protection	Optional	Optional	Yes

NOTE: If the on-board hard disk drive option is fitted, the operating temperature range will be restricted to +5 to +55ºC and the storage temperature range will be restricted to -40 to +65ºC.

NOTE: If the battery is fitted, the storage temperature range will be restricted to 0 to +70ºC. This is because the 6300ESB ICH device is partially operational when the battery is connected. The battery life will be reduced by storage at high temperatures due to increased self-discharge. It is therefore recommended that the battery be removed during storage.

A.3 Dimensions

Height	23.3cm
Depth	16.0cm
Width	2.0cm
Weight	500g (without Mass Storage Kit fitted)

SPECIFICATIONS

A.4 Electrical Specification

Full speed	Actual speed	+5V +/-5%		+12V +/-5%	-12V +/-5%
		Typical	Maximum	Maximum	Maximum
1.8 GHz	1.8 GHz	6.4A	8.4A	0.00A	0.00A
	1.2 GHz	5.1A	6.3A	0.00A	0.00A
	600 MHz	4.5A	5.4A	0.00A	0.00A
1.6 GHz	1.6 GHz	6.3A	8.8A	0.00A	0.00A
	1.2 GHz	5.2A	6.5A	0.00A	0.00A
	600 MHz	4.8A	5.2A	0.00A	0.00A
1.4 GHz	1.4 GHz	5.1A	6.3A	0.00A	0.00A
	1.0 GHz	4.8A	5.4A	0.00A	0.00A
	600 MHz	4.4A	5.0A	0.00A	0.00A
1.0 GHz	1.0 GHz	4.4A	4.9A	0.00A	0.00A

Table A-1 Voltage and Current Requirements

NOTE: This is for a board with 1 Gbyte DRAM and with no Mass Storage Kit or PMC Modules fitted.

NOTE: +12V supply is provided for the PMC interface. This supply does not need to be present if the PMC module does not require it. Current requirements will be those of the fitted PMC module.

NOTE: - 12V supply is provided for the PMC interface. This supply does not need to be present if the PMC module does not require it. Current requirements will be those of the fitted PMC module.

A.5 Connectors

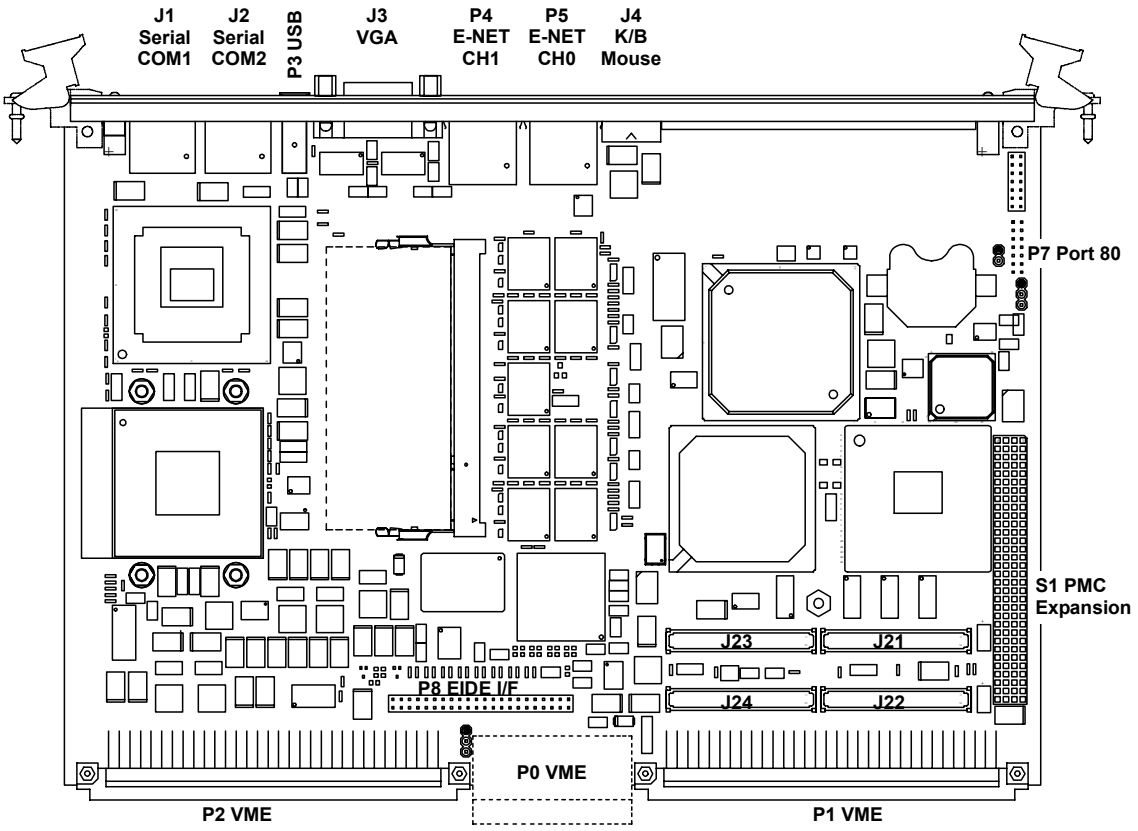


Figure A-1 Connector Layout

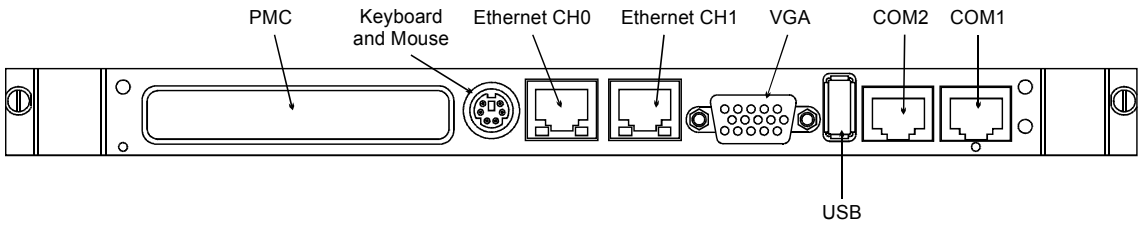


Figure A-2 Front Panel Connectors

A.5.1 VME Interface (P1) Pin-outs

The VME interface connector P1 consists of a 160-pin connector with pins assigned as follows:

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	-	D00	BBSY#	D08	-
2	GND	D01	BCLR#	D09	GND
3	-	D02	ACFAIL#	D10	-
4	GND	D03	BG0IN#	D11	-
5	-	D04	BG0OUT#	D12	-
6	GND	D05	BG1IN#	D13	-
7	-	D06	BG1OUT	D14	-
8	GND	D07	BG2IN#	D15	-
9	-	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	-	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	-
13	-	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	-
15	-	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	-
17	-	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	-
19	-	GND	AM3	A19	-
20	GND	IACK#	GND	A18	-
21	-	IACKIN#	-	A17	-
22	GND	IACKOUT#	-	A16	-
23	-	AM4	GND	A15	-
24	GND	A07	IRQ7#	A14	-
25	-	A06	IRQ6#	A13	-
26	GND	A05	IRQ5#	A12	-
27	-	A04	IRQ4#	A11	-
28	GND	A03	IRQ3#	A10	-
29	-	A02	IRQ2#	A09	-
30	GND	A01	IRQ1#	A08	-
31	-	-12V	VCC_STANDBY	+12V	GND
32	GND	+5V	+5V	+5V	VCC

Table A-2 P1 VME Interface Pin-outs

A.5.2 Auxiliary Connector (P2) Pin-outs (Wide SCSI, Panel Link & EIDE)

The auxiliary connection P2 consists of a 160-pin connector. When the board is factory configured for Wide SCSI and the Panel Link interface the pin assignments are as shown in table A-3.

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	GPIO0	SCSIDB0#	+5V	DRVDEN0	NC
2	GND	SCSIDB1#	GND	DRVDEN1	NC
3	GPIO1	SCSIDB2#	NC	EXT_RST#	IDEDD7
4	GND	SCSIDB3#	A24	INDX#	IDEDD9
5	IDERST#	SCSIDB4#	A25	FDME0#	IDEDD6
6	GND	SCSIDB5#	A26	FDS1#	IDEDD10
7	IDEDD8	SCSIDB6#	A27	FDS0#	IDEDD5
8	GND	SCSIDB7#	A28	FDME1#	IDEDD11
9	NC	SCSIDBP0#	A29	DIR#	IDEDD4
10	GND	GND	A30	STEP#	IDEDD12
11	RFU	GND	A31	WRDATA#	IDEDD3
12	GND	GND	GND	WE#	IDEDD13
13	RFU	TERMPWR	+5V	TRK0#	IDEDD2
14	GND	GND	D16	WP#	IDEDD14
15	RFU	GND	D17	RDDATA#	IDEDD1
16	GND	SCSIATN#	D18	HDSEL#	IDEDD15
17	RFU	GND	D19	DSKCHG#	IDEDD0
18	GND	SCSIBSY#	D20	RFU	IDEDRQ
19	RFU	SCSIACK#	D21	RFU	IDEIOW#
20	GND	SCSIRST#	D22	SCSIDB8#	IDEIOR#
21	GDCCK	SCSIMSG#	D23	SCSIDB9#	IDEDRDY#
22	GND	SCSISEL#	GND	SCSIDB10#	IDEDACK#
23	GDCDAT	SCSICD#	D24	SCSIDB11#	IDEIRQ
24	GND	SCSIREQ#	D25	SCSIDB12#	IDEA1
25	RFU	SCSIIO#	D26	SCSIDB13#	IDEA2
26	GND	RFU	D27	SCSIDB14#	IDEA0
27	USBD1#	RFU	D28	SCSIDB15#	IDECS1#
28	GND	GND	D29	SCSIDBP1#	IDECS0#
29	USBD1	TX2	D30	TX0	IDEACT#
30	GND	TX2#	D31	TX0#	GND
31	NC	TXC	GND	TX1	GND
32	GND	TXC#	+5V	TX1#	VCC

Table A-3 P2 Auxiliary Connector Pin-outs (Wide SCSI, EIDE and Panel Link)

NC = Not Connected

RFU = Reserved for Future Use (do NOT connect to these pins)

CAUTION: Pin D32 is now VCC. On VP101/01x this pin is marked as NC.

A.5.3 Auxiliary Connector (P2) Pin-outs (Narrow SCSI, EIDE & Printer Port)

The auxiliary connection P2 consists of a 160-pin connector. When the board is factory configured for Narrow SCSI, EIDE and the Printer Port interface the pin assignments are as shown in Table A-4.

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	GPIO0	SCSIDB0#	+5V	DRVDEN0	NC
2	GND	SCSIDB1#	GND	DRVDEN1	NC
3	GPIO1	SCSIDB2#	NC	EXT_RST#	IDEDD7
4	GND	SCSIDB3#	A24	INDX#	IDEDD9
5	IDERST#	SCSIDB4#	A25	FDME0#	IDEDD6
6	GND	SCSIDB5#	A26	FDS1#	IDEDD10
7	IDEDD8	SCSIDB6#	A27	FDS0#	IDEDD5
8	GND	SCSIDB7#	A28	FDME1#	IDEDD11
9	NC	SCSIDP#	A29	DIR#	IDEDD4
10	GND	GND	A30	STEP#	IDEDD12
11	RFU	GND	A31	WRDATA#	IDEDD3
12	GND	GND	GND	WE#	IDEDD13
13	RFU	TERMPWR	+5V	TRK0#	IDEDD2
14	GND	GND	D16	WP#	IDEDD14
15	RFU	GND	D17	RDDATA#	IDEDD1
16	GND	SCSIATN#	D18	HDSEL#	IDEDD15
17	RFU	GND	D19	DSKCHG#	IDEDD0
18	GND	SCSIBSY#	D20	IDEIOW#	IDEDRQ
19	RFU	SCSIACK#	D21	IDEIOR#	IDEIOW#
20	GND	SCSIRST#	D22	STROBE#	IDEIOR#
21	GDCCK	SCSIMSG#	D23	PRT_D0	IDEDRDY#
22	GND	SCSISEL#	GND	PRT_D1	IDEDACK#
23	GDCDAT	SCSICD#	D24	PRT_D2	IDEIRQ
24	GND	SCSIREQ#	D25	PRT_D3	IDEA1
25	NC	SCSIIO#	D26	PRT_D4	IDEA2
26	GND	RFU	D27	PRT_D5	IDEA0
27	USBD1#	RFU	D28	PRT_D6	IDECS1#
28	GND	RFU	D29	PRT_D7	IDECS0#
29	USBD1	AFD#	D30	PRT_ACK#	IDEACT#
30	GND	ERR#	D31	PRT_BUSY	GND
31	NC	INIT#	GND	PERR	GND
32	GND	SELECT_I#	+5V	SELECT	VCC

Table A-4 P2 Auxiliary Connector Pin-outs (Narrow SCSI, EIDE & Printer Port)

NC = Not Connected

RFU = Reserved for Future Use (do NOT connect to these pins)

CAUTION: Pin D32 is now VCC. On VP101/01x this pin is marked as NC.

A.5.4 Auxiliary Connector (P2) Pin-outs (EIDE Only)

The auxiliary connection P2 consists of a 160-pin connector. When the board is factory configured for EIDE only the pin assignments are as shown in table A-5.

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	GPIO0	IDERST#	+5V	DRVDEN0	NC
2	GND	IDEDD8	GND	DRVDEN1	NC
3	GPIO1	IDEDD7	NC	EXT_RST#	IDEDD7
4	GND	IDEDD9	A24	INDX#	IDEDD9
5	IDERST#	IDEDD6	A25	FDME0#	IDEDD6
6	GND	IDEDD10	A26	FDS1#	IDEDD10
7	IDEDD8	IDEDD5	A27	FDS0#	IDEDD5
8	GND	IDEDD11	A28	FDME1#	IDEDD11
9	NC	IDEDD4	A29	DIR#	IDEDD4
10	GND	IDEDD12	A30	STEP#	IDEDD12
11	RFU	IDEDD3	A31	WRDATA#	IDEDD3
12	GND	IDEDD13	GND	WE#	IDEDD13
13	RFU	IDEDD2	+5V	TRK0#	IDEDD2
14	GND	IDEDD14	D16	WP#	IDEDD14
15	RFU	IDEDD1	D17	RDDATA#	IDEDD1
16	GND	IDEDD15	D18	HDSEL#	IDEDD15
17	RFU	IDEDD0	D19	DSKCHG#	IDEDD0
18	GND	IDEDRQ	D20	IDEIOW#	IDEDRQ
19	RFU	IDEDRDY#	D21	IDEIOR#	IDEIOW#
20	GND	IDEDACK#	D22	STROBE#	IDEIOR#
21	GDCCK	IDEIRQ	D23	PRT_D0	IDEDRDY#
22	GND	IDEA1	GND	PRT_D1	IDEDACK#
23	GDCDAT	IDEA2	D24	PRT_D2	IDEIRQ
24	GND	IDEA0	D25	PRT_D3	IDEA1
25	NC	IDECS1#	D26	PRT_D4	IDEA2
26	GND	IDECS0#	D27	PRT_D5	IDEA0
27	USBD1#	IDEACT#	D28	PRT_D6	IDECS1#
28	GND	GND	D29	PRT_D7	IDECS0#
29	USBD1	AFD#	D30	PRT_ACK#	IDEACT#
30	GND	ERR#	D31	PRT_BUSY	GND
31	NC	INIT#	GND	PERR	GND
32	GND	SELECT_I#	+5V	SELECT	VCC

Table A-5 P2 Auxiliary Connector Pin-outs (EIDE Only)

NC = Not Connected

RFU = Reserved for Future Use (do NOT connect to these pins)

CAUTION: Pin D32 is now VCC. On VP101/01x this pin is marked as NC.

A.5.5 PMC I/O Connector (P0) Pin-outs

This is a 95-way (5-row x 19-position) IEC 61076-4-101 2mm pitch connector. It carries all 64 I/O signals from the PMC Site and Serial ATA channels 0 and 1. The pin assignments are shown below.

Position	Row F	Row E	Row D	Row C	Row B	Row A
1	GND	-	-	-	-	-
2	GND	-	-		-	-
3	GND	-	-		-	-
4	GND	I/O_1	I/O_2	I/O_3	I/O_4	I/O_5
5	GND	I/O_6	I/O_7	I/O_8	I/O_9	I/O_10
6	GND	I/O_11	I/O_12	I/O_13	I/O_14	I/O_15
7	GND	I/O_16	I/O_17	I/O_18	I/O_19	I/O_20
8	GND	I/O_21	I/O_22	I/O_23	I/O_24	I/O_25
9	GND	SATA0_RX-	SATA0_RX+	GND	SATA0_TX-	SATA0_TX+
10	GND	GND	GND	GND	GND	GND
11	GND	SATA1_RX-	SATA1_RX+	GND	SATA1_TX-	SATA1_TX+
12	GND	I/O_26	I/O_27	I/O_28	I/O_29	I/O_30
13	GND	I/O_31	I/O_32	I/O_33	I/O_34	I/O_35
14	GND	I/O_36	I/O_37	I/O_38	I/O_39	I/O_40
15	GND	I/O_41	I/O_42	I/O_43	I/O_44	I/O_45
16	GND	I/O_46	I/O_47	I/O_48	I/O_49	I/O_50
17	GND	I/O_51	I/O_52	I/O_53	I/O_54	I/O_55
18	GND	I/O_56	I/O_57	I/O_58	I/O_59	I/O_60
19	GND	I/O_61	I/O_62	I/O_63	I/O_64	-

Table A-6 P0 Connector Pin-out

NOTE: This connector is a build time option and is not available on all variants.

A.5.6 VGA Connector (J3) Pin-outs

This connector provides access to the VGA interface. It is a female 15-way high density D-type connector. The pin-out is as follows.

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	RED	6	RED GND	11	-
2	GREEN	7	GREEN GND	12	DDC DATA
3	BLUE	8	BLUE GND	13	HSYNC
4	-	9	-	14	VSYNC
5	GND	10	GND	15	DDC CLOCK

Table A-7 VGA Connector Pin-outs

A.5.7 On-Board Mass Storage Option Connector (P8) Pin-outs

Pin No.	Signal Name	Pin No.	Signal Name
1	IDE_RST#	2	GND
3	SDD7	4	SDD8
5	SDD6	6	SDD9
7	SDD5	8	SDD10
9	SDD4	10	SDD11
11	SDD3	12	SDD12
13	SDD2	14	SDD13
15	SDD1	16	SDD14
17	SDD0	18	SDD15
19	GND	20	3.3V
21	SDREQ	22	GND
23	SDIOW#	24	GND
25	SDIOR#	26	GND
27	SIORDY	28	NC
29	SDDACK#	30	GND
31	IDEIRQS#	32	NC
33	SDA1	34	PDIAG
35	SDA0	36	SDA2
37	SDCS0#	38	SDCS1#
39	ACTIVITY#	40	GND
41	+5V	42	+5V MOTOR
43	GND	44	NC

Table A-8 On-Board Mass Storage Option Interface Pin-outs

A.5.8 PMC Site Connector Pin-outs

Signal assignments on the PMC connectors are shown in Tables A-9, A-10, A-11 and A-12.

Pin No.	Signal Name	Pin No.	Signal Name
1	TCK†	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	-
11	GND	12	+3.3V††
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V (I/O)	20	AD(31)
21	AD(28)	22	AD(27)
23	AD(25)	24	GND
25	GND	26	C/BE(3)#
27	AD(22)	28	AD(21)
29	AD(19)	30	+5V
31	V (I/O)	32	AD(17)
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V (I/O)	46	AD(15)
47	AD(12)	48	AD(11)
49	AD(09)	50	+5V
51	GND	52	C/BE(0)#
53	AD(06)	54	AD(05)
55	AD(04)	56	GND
57	V (I/O)	58	AD(03)
59	AD(02)	60	AD(01)
61	AD(00)	62	+5V
63	GND	64	REQ64#

V (I/O) can be +5V or +3.3 V depending on board configuration,
† pulled low via 4K7Ohm resistor.
†† pulled high via 10KOhm resistor.

Table A-9 PMC J21 Connector Pin-outs

Pin No.	Signal Name	Pin No.	Signal Name
1	+12V	2	TRST†
3	TMS†††	4	TDO(-)
5	TDI†††	6	GND
7	GND	8	-
9	-	10	-
11	+3.3V††	12	+3.3V
13	RST#	14	GND
15	+3.3V	16	GND
17	-	18	GND
19	AD(30)	20	AD(29)
21	GND	22	AD(26)
23	AD(24)	24	+3.3V
25	IDSEL	26	AD(23)
27	+3.3V	28	AD(20)
29	AD(18)	30	GND
31	AD(16)	32	C/BE(2)#
33	GND	34	IDSEL B
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE(1)#	44	GND
45	AD(14)	46	AD(13)
47	M66EN	48	AD(10)
49	AD(08)	50	+3.3V
51	AD(07)	52	REQ B#
53	+3.3V	54	GNT B#
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	EREADY††
59	GND	60	-
61	ACK64#	62	+3.3V
63	GND	64	+3.3V††

† pulled low via 4K7Ohm resistor.
†† pulled high via 10KOhm resistor.
††† pulled high via 4K7Ohm resistor.

Table A-10 PMC J22 Connector Pin-outs

NOTE: IDSEL B, REQ B# and GNT B# are provided for use by dual-function PMC modules or Processor-PMC modules.

NOTE: Pins 58 and 64 are pulled high to suit Processor-PMC modules.

NOTE: JTAG signals are terminated with 4K7Ohm resistors but are unused on the board.

Pin No.	Signal Name	Pin No.	Signal Name
1	-	2	GND
3	GND	4	C/BE(7)#
5	C/BE(6)#	6	C/BE(5)#
7	C/BE(4)#	8	GND
9	V(I/O)	10	PAR64
11	AD(63)	12	AD(62)
13	AD(61)	14	GND
15	GND	16	AD(60)
17	AD(59)	18	AD(58)
19	AD(57)	20	GND
21	V(I/O)	22	AD(56)
23	AD(55)	24	AD(54)
25	AD(53)	26	GND
27	GND	28	AD(52)
29	AD(51)	30	AD(50)
31	AD(49)	32	GND
33	GND	34	AD(48)
35	AD(47)	36	AD(46)
37	AD(45)	38	GND
39	V(I/O)	40	AD(44)
41	AD(43)	42	AD(42)
43	AD(41)	44	GND
45	GND	46	AD(40)
47	AD(39)	48	AD(38)
49	AD(37)	50	GND
51	GND	52	AD(36)
53	AD(35)	54	AD(34)
55	AD(33)	56	GND
57	V(I/O)	58	AD(32)
59	-	60	-
61	-	62	GND
63	GND	64	-

Table A-11 PMC J23 Connector Pin-outs

Pin No.	Signal Name	Pin No.	Signal Name
1	I/O 1	2	I/O 2
3	I/O 3	4	I/O 4
5	I/O 5	6	I/O 6
7	I/O 7	8	I/O 8
9	I/O 9	10	I/O 10
11	I/O 11	12	I/O 12
13	I/O 13	14	I/O 14
15	I/O 15	16	I/O 16
17	I/O 17	18	I/O 18
19	I/O 19	20	I/O 20
21	I/O 21	22	I/O 22
23	I/O 23	24	I/O 24
25	I/O 25	26	I/O 26
27	I/O 27	28	I/O 28
29	I/O 29	30	I/O 30
31	I/O 31	32	I/O 32
33	I/O 33	34	I/O 34
35	I/O 35	36	I/O 36
37	I/O 37	38	I/O 38
39	I/O 39	40	I/O 40
41	I/O 41	42	I/O 42
43	I/O 43	44	I/O 44
45	I/O 45	46	I/O 46
47	I/O 47	48	I/O 48
49	I/O 49	50	I/O 50
51	I/O 51	52	I/O 52
53	I/O 53	54	I/O 54
55	I/O 55	56	I/O 56
57	I/O 57	58	I/O 58
59	I/O 59	60	I/O 60
61	I/O 61	62	I/O 62
63	I/O 63	64	I/O 64

Table A-12 PMC J24 Connector Pin-outs

A.5.9 Ethernet Interface (P4 & P5) Pin-outs

The Ethernet Interfaces use 8-way RJ45 connectors with the following pin-out.

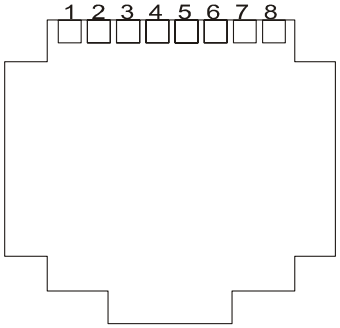


Figure A-3 Ethernet RJ-45 Connector (Front View)

Pin No.	Signal Name
1	DA
2	DA#
3	DB
4	DC
5	DC#
6	DB#
7	DD
8	DD#

Table A-13 Ethernet RJ-45 Connector Pin-outs

A.5.10 Keyboard and Mouse Interface (J4) Pin-outs

The Keyboard and mouse Interfaces use a 6-way Mini-DIN connector with the following pin-out.

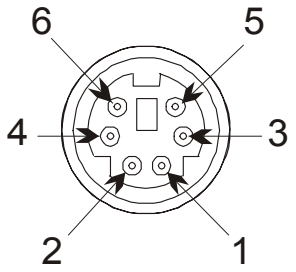


Figure A-4 Keyboard and Mouse Connector

Pin No.	Signal Name
1	KEYBOARD DATA
2	MOUSE DATA
3	KEYBOARD/MOUSE GND
4	KEYBOARD/MOUSE POWER
5	KEYBOARD CLOCK
6	MOUSE CLOCK
Shell	CHASSIS GND

Table A-14 Keyboard and Mouse Connector Pin-outs

A.5.11 USB CH0 Interface (P3) Pin-outs

The front panel USB Interface uses a 4-way USB connector with the following pin-out.

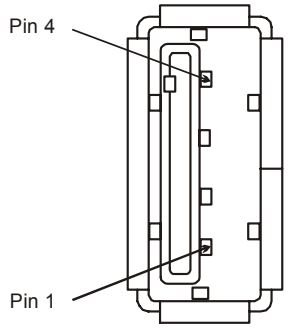


Figure A-5 USB CH0 Connector (Front View)

Pin No.	Signal Name
1	POWER
2	DATA-
3	DATA+
4	GND

Table A-15 USB Connector Pin-outs

A.5.12 Serial Interface (J1 & J2) Pin-outs

The Serial Interfaces COM1 and COM2 use 8-way RJ45 connectors with the following pin-out.

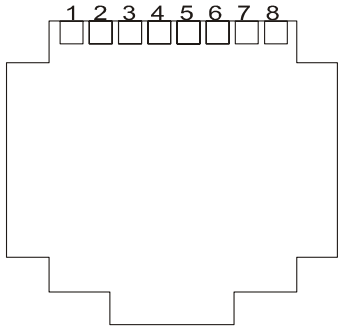


Figure A-6 Serial (COM) RJ-45 Connector (Front View)

Pin No.	Signal Name
1	RTS
2	DTR
3	GND
4	TXD
5	RXD
6	DCD
7	DSR
8	CTS

Table A-16 Serial (COM) RJ-45 Connector Pin-outs

A.5.13 Port 80 (P7) Pin-outs

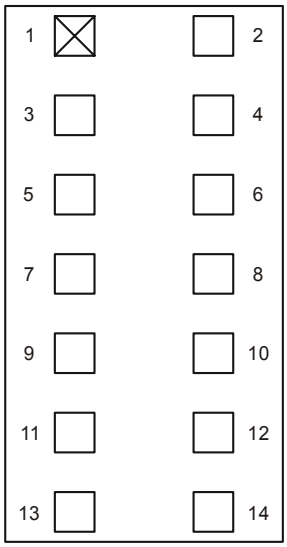


Figure A-7 Port 80 Connector

Pin No.	Signal Name
1	GND
2	XRD#
3	Port 80 WRITE#
4	XWR#
5	D3
6	D7
7	D2
8	D6
9	D1
10	D5
11	D0
12	D4
13	+5V
14	-

Table A-17 Port 80 Connector Pin-outs

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B BREAKOUT MODULES

B.1 Introduction

This section details all the available breakout modules available for use with the VP 34x/02x. Each breakout module provides a means of connecting interface cables to the rear I/O of the VP 34x/02x.

An overview of each breakout module is given with a reference to a pin-out table for each of the connectors identified.

B.2 Breakout Modules List

The following breakout modules are suitable for use with the VP 34x/02x:-

Sales Part No.	Board number (as marked on PCB)
AD VP2/001-10	720-6081-00
AD VP2/001-20	720-6081-01
AD VP2/002-10	720-6088-00
AD VP2/003-10	720-6105-00
AD VP2/003-30	720-6105-02
AD VP2/007-40	720-6137-03

Table B-1 Breakout Modules List

B.3 AD VP2/001-10

The AD VP2/001-10 product is a 96-way P2 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 50-way IDC SCSI header, a 34-way IDC Floppy header, a 26-way printer header, a 3-way External Reset/NMI header, a 3-way 5V header and additional power connection terminals.

This breakout requires one slot width behind the backplane.

B.3.1 Layout

Figure B-1 shows the position of connectors and headers.

The AD VP2/001-10 requires a minimum of 70mm depth behind the VME backplane. This measurement is taken from the mating face of the rear P2 connector.

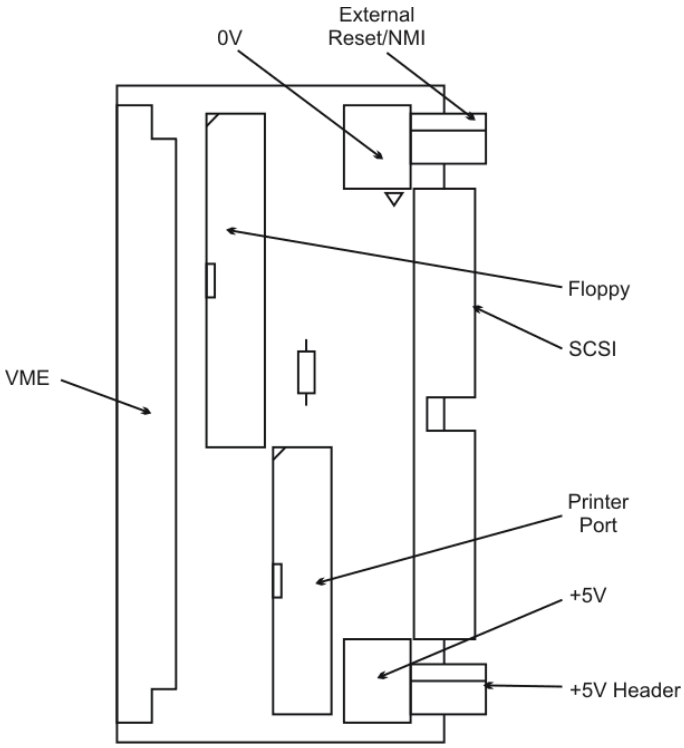


Figure B-1 AD VP2/001-10 P2 Breakout Connectors

B.3.2 Pin-out Tables

Floppy	-	Table B-2
Printer Port	-	Table B-4
SCSI (Narrow)	-	Table B-12
Reset/NMI	-	Table B-5
+5V Header	-	Table B-6

B.4 AD VP2/001-20

The AD VP2/001-20 product is a 96-way P2 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 40-way IDC EIDE header, a 34-way IDC Floppy header, a 26-way printer header, a 3-way External Reset/NMI header, a 3-way 5V header and additional power connection terminals.

This breakout requires one slot width behind the backplane.

B.4.1 Layout

Figure B-2 shows the position of connectors and headers.

The AD VP2/001-20 requires a minimum of 70mm depth behind the VME backplane. This measurement is taken from the mating face of the rear P2 connector.

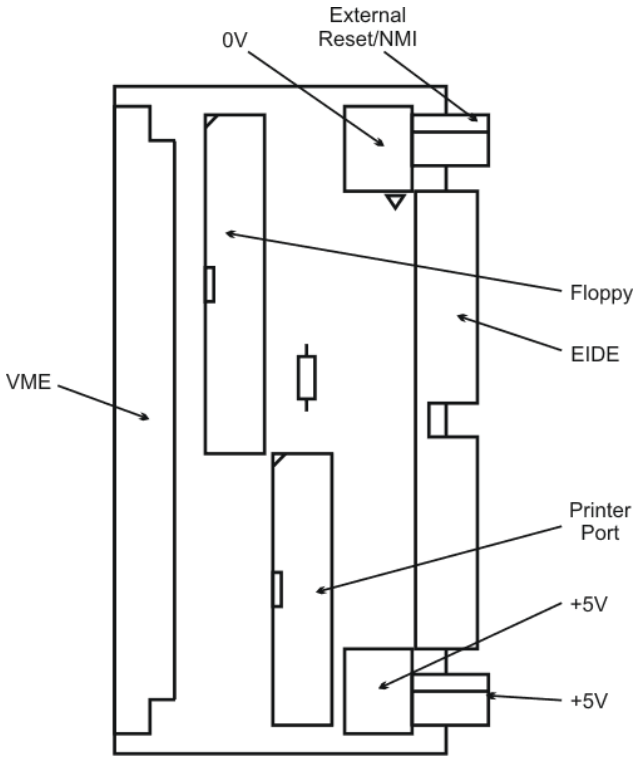


Figure B-2 AD VP2/001-20 P2 Breakout Connectors

B.4.2 Pin-out Tables

Floppy	-	Table B-2
Printer Port	-	Table B-4
EIDE	-	Table B-3
Reset/NMI	-	Table B-5
+5V Header	-	Table B-6

B.5 AD VP2/002-10

The AD VP2/002-10 product is a 160-way P2 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 40-way IDC EIDE header, a 50-way IDC SCSI header,a 34-way IDC Floppy header, a USB connector, a 26-way printer header, a 3-way External Reset/NMI header, a 3-way 5V header and additional power connection terminals.

This breakout requires one slot width behind the backplane.

B.5.1 Layout

Figure B-3 shows the position of connectors and headers.

The AD VP2/002-10 requires a minimum of 82mm depth behind the VME backplane. This measurement is taken from the mating face of the rear P2 connector.

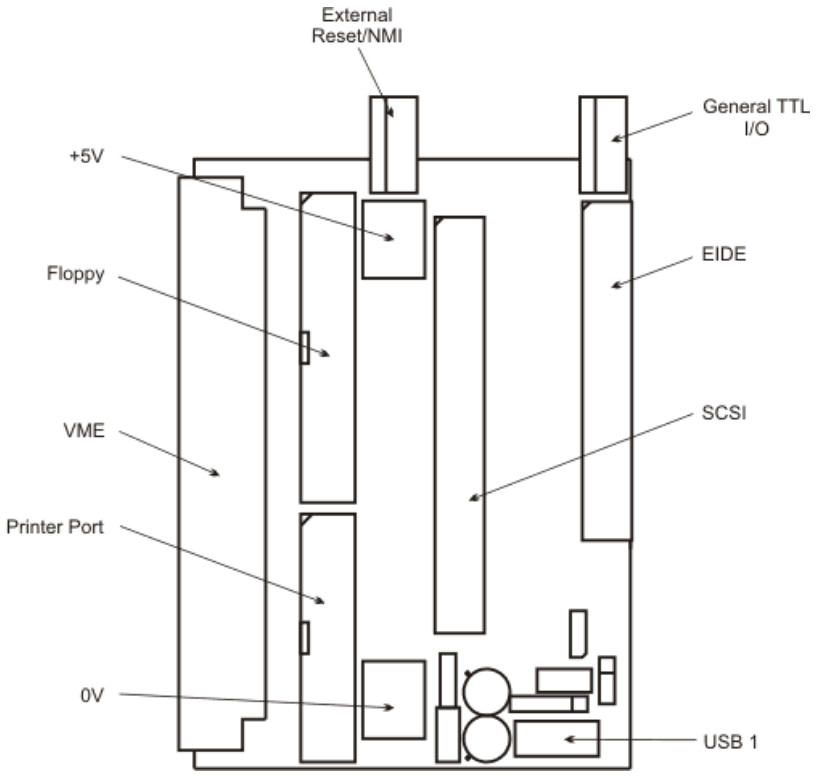


Figure B-3 AD VP2/002-10 P2 Breakout Connectors

B.5.2 Pin-out Tables

Floppy	-	Table B-2
Printer Port	-	Table B-4
SCSI (Narrow)	-	Table B-12
EIDE	-	Table B-3
Reset/NMI	-	Table B-4
General TTL I/O	-	Table B-7
USB 1	-	Table B-8

B.6 AD VP2/003-10

The AD VP2/003-10 product is a 160-way P2 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 68-way right angled female wide SCSI connector, a 40-way IDC EIDE header, a 20-way right angled DFP connector, a 50-way IDC Narrow SCSI header, a 34-way IDC Floppy header, a 4-way right angled USB connector, a 3-way External Reset header, and a 3-way general purpose I/O header.

This breakout requires one slot width behind the backplane.

B.6.1 Layout

Figure B-4 shows the position of connectors and headers.

The AD VP2/003-10 requires a minimum of 90mm depth behind the VME backplane.

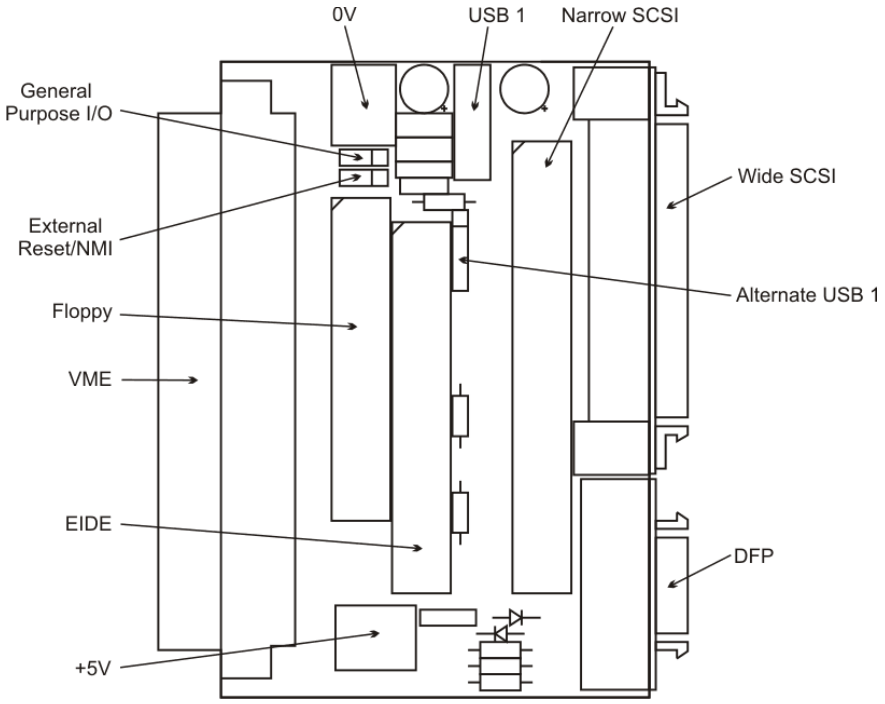


Figure B-4 AD VP2/003-10 P2 Breakout Connectors

B.6.2 Pin-out Tables

Floppy	-	Table B-2
SCSI (Narrow)	-	Table B-12
SCSI (Wide)	-	Table B-13
Reset/NMI	-	Table B-5
General Purpose I/O	-	Table B-7
USB 1	-	Table B-8
Alternate USB 1	-	Table B-9
DFP	-	Table B-11

B.7 AD VP2/003-30

The AD VP2/003-30 product is a 96-way P2 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 68-way right angled female wide SCSI connector, a 20-way right angled DFP connector, a 50-way IDC Narrow SCSI header, a 34-way IDC Floppy header, and a 3-way External Reset header.

This breakout requires one slot width behind the backplane.

B.7.1 Layout

Figure B-5 shows the position of connectors and headers.

The AD VP2/003-30 requires a minimum of 90mm depth behind the VME backplane.

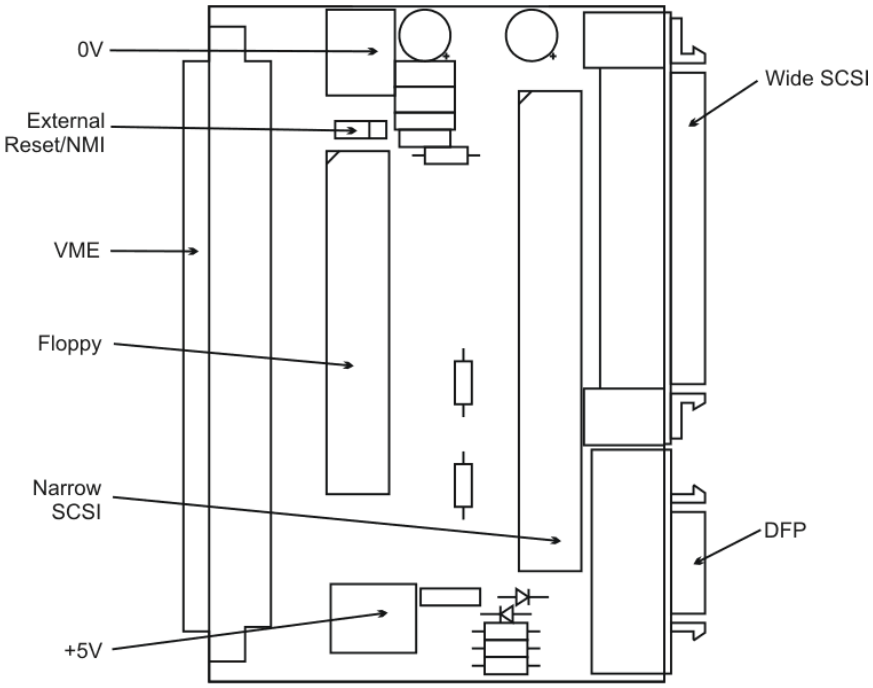


Figure B-5 AD VP2/003-30 P2 Breakout Connectors

B.7.2 Pin-out Tables

Floppy	-	Table B-2
SCSI (Narrow)	-	Table B-12
SCSI (Wide)	-	Table B-13
Reset/NMI	-	Table B-5
DFP	-	Table B-10

B.8 AD VP2/007-40

The AD VP2/007-40 product is a 160-way P2 and P0 backplane breakout for a number of Concurrent Technologies VME boards. It provides a 68-way right angled female wide SCSI connector, a 40-way IDC EIDE header, a 20-way right angled DFP connector, a 50-way IDC Narrow SCSI header, a 34-way IDC Floppy header, three 4-way right angled USB connectors, a 3-way External Reset header, a 3-way general purpose I/O header, and two 34-way headers for PMC I/O.

This breakout requires one slot width behind the backplane.

B.8.1 Layout

Figure B-6 shows the position of connectors and headers.

The AD VP2/007-40 requires a minimum of 90mm depth behind the VME backplane.

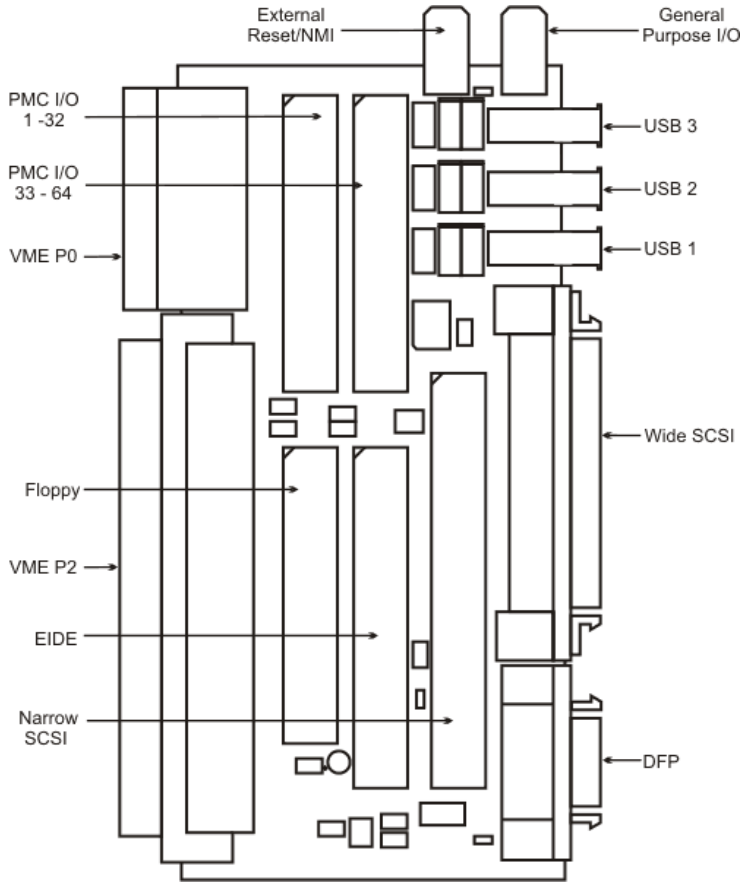


Figure B-6 AD VP2/007-40 P2 Breakout Connectors

B.8.2 Pin-out Tables

Floppy	-	Table B-2
SCSI (Narrow)	-	Table B-12
SCSI (Wide)	-	Table B-13
Reset/NMI	-	Table B-5
General Purpose I/O	-	Table B-7
USB 1, 2, 3	-	Table B-8
DFP	-	Table B-11
PMC I/O 1 to 32	-	Table B-14
PMC I/O 33 to 64	-	Table B-15

B.9 Header/Connector Configuration Tables

The headers and connectors are designed to enable use of standard P.C. Interface cables wherever possible. Detailed below are the pin-outs of the headers and connectors used on the breakout modules.

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	DRVDEN0
3	GND	4	NC
5	GND	6	DRVDEN1
7	GND	8	INDX
9	GND	10	FDME0
11	GND	12	FDS1
13	GND	14	FDS0
15	GND	16	FDME1
17	GND	18	DIR
19	GND	20	STEP
21	GND	22	WRDATA
23	GND	24	WE
25	GND	26	TRK0
27	GND	28	WP
29	GND	30	RDDATA
31	GND	32	HDSEL
33	GND	34	DSKCHG

Table B-2 Floppy 34-way IDC Header

Pin No.	Signal Name	Pin No.	Signal Name
1	IDERST	2	GND
3	IDEDD7	4	IDEDD8
5	IDEDD6	6	IDEDD9
7	IDEDD5	8	IDEDD10
9	IDEDD4	10	IDEDD11
11	IDEDD3	12	IDEDD12
13	IDEDD2	14	IDEDD13
15	IDEDD1	16	IDEDD14
17	IDEDD0	18	IDEDD15
19	GND	20	NC
21	IDEDRQ	22	GND
23	IDEIOW	24	GND
25	IDEOR	26	GND
27	IDEDRDY	28	NC
29	IDEDACK	30	GND
31	IDEIRQ	32	NC
33	IDEA1	34	NC
35	IDEA0	36	IDEA2
37	IDECS1	38	IDECS2
39	IDEACT	40	GND

Table B-3 EIDE 40-way IDC Header

Pin No.	Signal Name	Pin No.	Signal Name
1	STROBE	2	AFD
3	PRT D0	4	ERR
5	PRT D1	6	INIT
7	PRT D2	8	SELECTI
9	PRT D3	10	GND
11	PRT D4	12	GND
13	PRT D5	14	GND
15	PRT D6	16	GND
17	PRT D7	18	GND
19	PRTACK	20	GND
21	PRT BUSY	22	GND
23	PERR	24	GND
25	SELECT	26	GND

Table B-4 Printer 26-way IDC Header

Pin No.	Signal Name
1	GND
2	EXTRST
3	GND

Table B-5 External Reset 3-way Header

Pin No.	Signal Name
1	+5V
2	+5V
3	+5V

Table B-6 5V 3-way Header

Pin No.	Signal Name
1	General Purpose Output
2	GND
3	General Purpose Input

Table B-7 General Purpose I/O Header

Pin No.	Signal Name
1	USB VCC (+5V)
2	USBD-
3	USBD+
4	USB Ground
SCR	SCREEN (SHIELD)

Table B-8 USB Connector

NOTE: USB SCREEN is connected to GND via a 0.1µF Capacitor.

Pin No.	Signal Name
1	USB VCC (+5V)
2	USBD-
3	USBD+
4	USB Ground
5	SCREEN (SHIELD)

Table B-9 USB 5-pin Header

Pin No.	Signal Name	Pin No.	Signal Name
1	TX1	2	TX1
3	GND	4	GND
5	TXC	6	TXC
7	GND	8	DFP VCC (+5V)
9	NC	10	NC
11	TX2	12	TX2
13	GND	14	GND
15	TX0	16	TX0
17	NC	18	Reserved
19	NC	20	NC

Table B-10 DFP Connector (without DDC)

Pin No.	Signal Name	Pin No.	Signal Name
1	TX1	2	TX1
3	GND	4	GND
5	TXC	6	TXC
7	GND	8	DFP VCC (+5V)
9	NC	10	NC
11	TX2	12	TX2
13	GND	14	GND
15	TX0	16	TX0
17	NC	18	HPD
19	DDC DAT	20	DDCCK

Table B-11 DFP Connector (with DDC)

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	2	SCSIDB0
3	GND	4	SCSIDB1
5	GND	6	SCSIDB2
7	GND	8	SCSIDB3
9	GND	10	SCSIDB4
11	GND	12	SCSIDB5
13	GND	14	SCSIDB6
15	GND	16	SCSIDB7
17	GND	18	SCSIDBP
19	GND	20	GND
21	GND	22	GND
23	GND	24	NC
25	GND	26	TERMPWR
27	GND	28	NC
29	GND	30	GND
31	GND	32	SCSIATN
33	GND	34	GND
35	GND	36	SCSIBSY
37	GND	38	SCSIACK
39	GND	40	SCSIRST
41	GND	42	SCSIMSG
43	GND	44	SCSISEL
45	GND	46	SCSICD
47	GND	48	SCSIREQ
49	GND	50	SCSIIO

Table B-12 Narrow SCSI 50-way IDC Header

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	35	SCSIDB12
2	GND	36	SCSIDB13
3	GND	37	SCSIDB14
4	GND	38	SCSIDB15
5	GND	39	SCSIDBP1
6	GND	40	SCSIDB0
7	GND	41	SCSIDB1
8	GND	42	SCSIDB2
9	GND	43	SCSIDB3
10	GND	44	SCSIDB4
11	GND	45	SCSIDB5
12	GND	46	SCSIDB6
13	GND	47	SCSIDB7
14	GND	48	SCSIDBP0
15	GND	49	GND
16	GND	50	GND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	NC	53	NC
20	GND	54	GND
21	GND	55	SCSIATN
22	GND	56	GND
23	GND	57	SCSIBSY
24	GND	58	SCSIACK
25	GND	59	SCSIRST
26	GND	60	SCSIMSG
27	GND	61	SCSISEL
28	GND	62	SCSICD
29	GND	63	SCSIREQ
30	GND	64	SCSIIO
31	GND	65	SCSIDB8
32	GND	66	SCSIDB9
33	GND	67	SCSIDB10
34	GND	68	SCSIDB11

Table B-13 Wide SCSI 68-way Connector

Pin No.	Signal Name	Pin No.	Signal Name
1	I/O 1	2	I/O 2
3	I/O 3	4	I/O 4
5	I/O 5	6	I/O 6
7	I/O 7	8	I/O 8
9	I/O 9	10	I/O 10
11	I/O 11	12	I/O 12
13	I/O 13	14	I/O 14
15	I/O 15	16	I/O 16
17	I/O 17	18	I/O 18
19	I/O 19	20	I/O 20
21	I/O 21	22	I/O 22
23	I/O 23	24	I/O 24
25	I/O 25	26	I/O 26
27	I/O 27	28	I/O 28
29	I/O 29	30	I/O 30
31	I/O 31	32	I/O 32
33	GND	34	GND

Table B-14 PMC I/O 34-way IDC Header (Lines 1- 32)

Pin No.	Signal Name	Pin No.	Signal Name
1	I/O 33	2	I/O 34
3	I/O 35	4	I/O 36
5	I/O 37	6	I/O 38
7	I/O 39	8	I/O 40
9	I/O 41	10	I/O 42
11	I/O 43	12	I/O 44
13	I/O 45	14	I/O 46
15	I/O 47	16	I/O 48
17	I/O 49	18	I/O 50
19	I/O 51	20	I/O 52
21	I/O 53	22	I/O 54
23	I/O 55	24	I/O 56
25	I/O 57	26	I/O 58
27	I/O 59	28	I/O 60
29	I/O 61	30	I/O 62
31	I/O 63	32	I/O 64
33	GND	34	GND

Table B-15 PMC I/O 34-way IDC Header (Lines 33- 64)

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