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Technical Reference Manual for VX 511/06x VME Intel® Core™ 2 Duo Processor Single Board Computer

Manual Order code 550 0036 Rev 02 March 2010

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CONVENTIONS

Throughout this manual the following conventions will apply:

or * after a name represents an active low signal, e.g. INIT# or INIT*
h denotes a hexadecimal number, e.g. FF45h
byte represents 8-bits
word represents 16-bits
dword represents 32-bits

NOTATIONAL CONVENTIONS

NOTE: Notes provide general additional information.

WARNING: Warnings provide indication of board malfunction if they are not observed.

CAUTION: Cautions provide indications of board or system damage if they are not observed.

GLOSSARY OF TERMS

AC'97	Audio CODEC 1997
ACPI	Advanced Configuration and Power Interface
APIC	Advanced Programmable Interrupt Controller
ATA	AT Attachment
BIOS	Basic Input Output System
BMC	Baseboard Management Controller
CMOS	Complementary Metal Oxide Semiconductor
CODEC	Coder / Decoder
CPCI	CompactPCI
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DDR	Double Data Rate
DDR3	Double Data Rate, second generation
DIB	Dual Independent Bus
DIL	Dual In Line
ECC	Error Checking and Correcting
EIDE	Enhanced Integrated Drive Electronics
EMC	Electromagnetic Compatibility
EPROM	Electrically Programmable Read Only Memory
EEPROM	Electrically Erasable Programmable Read Only Memory
FRU	Field Replacement Unit
FWH	Firmware Hub
GLCI	Gigabit LAN Connect Interface
MCH	Memory Controller Hub
ICH	I/O Controller Hub
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
LED	Light Emitting Diode
LFM	Linear Feet per Minute
LPC	Low Pin Count
N/A	Not Applicable or Not Available
NC	Not Connected
NMI	Non Maskable Interrupt
PC-AT	Personal Computer-Advanced Technology
PCI	Peripheral Component Interconnect
PCI-X	PCI Extended
PICMG	PCI Industrial Computer Manufacturers Group
PIC	Programmable Interrupt Controller
PIM	Peripheral Interface Module
PIT	Periodic Interrupt Timer
PMC	PCI Mezzanine Card
POST	Power-on Self Test
PRST	Push Button Reset
RoHS	Restriction of Hazardous Substances
RST	Reset
RTC	Real Time Clock
RTM	Rear Transition Module or Transition Module
SATA	Serial ATA
SDR	Sensor Data Record
SDRAM	Synchronous Dynamic Random Access Memory
SMBus	System Management Bus
SMC	Satellite Management Controller
SMI	System Management Interrupt
SMM	System Management Mode
USB	Universal Serial Bus
XMC	Switched Mezzanine Card

REVISION HISTORY

Revision	Summary of Changes	Date
01	First Release	December 2008
02	Corrections to VXS connector pin-out. Corrections to AD VP2/018-30 switch settings, current figures, etc. Added Appendix C (RC variant). Added MTBF values table. Added AD VP2/024 RTM to Section B. Removed AD 230/001 Flash Disk Module. Shock and Vibration table updated. Addition of Section 2.5.1 – Battery Isolation Strip Removal of Flash Disk option	March 2010

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1 INTRODUCTION

1.1 General

This manual is a guide and reference handbook for engineers and system integrators who wish to use the Concurrent Technologies VX 511/06x ultra high-performance Intel® Core™ 2 Duo processor single board computer. The board has been designed for high-speed multiprocessing applications using a PC-AT™ architecture operating in a VME Bus environment.

The VX 511/06x board is available in several different architecture variants which differ by the amount of fitted DDR3 SDRAM and the rear I/O connector configuration. The processor speed options are listed in Table 1-1.

Processor	Board Variant
2.26GHz Intel® Core™ 2 Duo processor SP9300	VX 511/063
1.86GHz Intel® Core™ 2 Duo processor SL9400	VX 511/062

Table 1-1 Processor Options

The board is available in standard temperature, extended temperature, Ruggedized Air-Cooled and Ruggedized Conduction-Cooled versions. Further details on these options are given in Section 1.2. Further details of other board options are given in Section 1.3. References to the board in this document will use the name VX 511/06x unless they apply only to a specific variant, in which case the full name will be used.

The other configuration options are specified by a two-digit suffix to the board name; refer to the product datasheet for further details (available on www.gocct.com). Further details of the I/O configuration options are given in Section 1.4.

The information contained in this manual has been written to provide users with all the information necessary to configure, install and use the VX 511/06x as part of a system. It assumes that the user is familiar with the VME bus and PC-AT bus architectures and features.

1.2 Standard, Extended Temperature and Ruggedized Options

1.2.1 Standard (N-Series), Extended Temperature (E-Series and K-Series) Options

The VX 511/06x is available as variants which are qualified to either a standard or extended range of operating and storage temperatures. Please see Section A.2 for specifications for the temperature ranges and Section A.3 for the shock and vibration ranges supported by the VX 511/06x. Consult your distributor or Concurrent Technologies directly for further details of the extended temperature options.

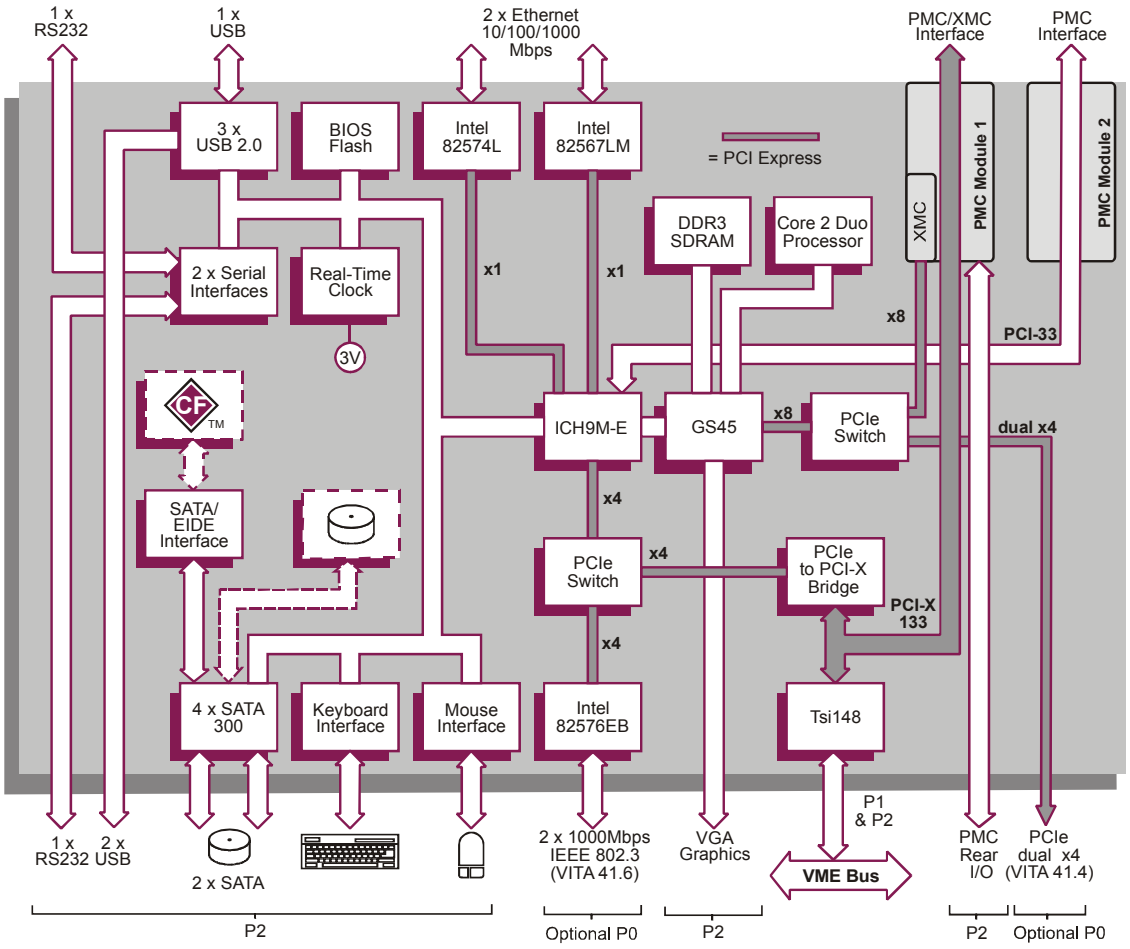


Figure 1-1 Overview of Standard and Extended Temperature Boards

1.2.2 Ruggedized Air-Cooled (RA-Series) Options

The VX 511/06x is available as Ruggedized Air-Cooled variants designated VX 511/061-RA. These offer extended temperature ranges as well as a higher specification for shock and vibration. Please see Section A.2 for specifications on the temperature range and Section A.3 for the shock and vibration ranges supported by the VX 511/061-RA. Consult your distributor or Concurrent Technologies directly for further details of the ruggedized options.

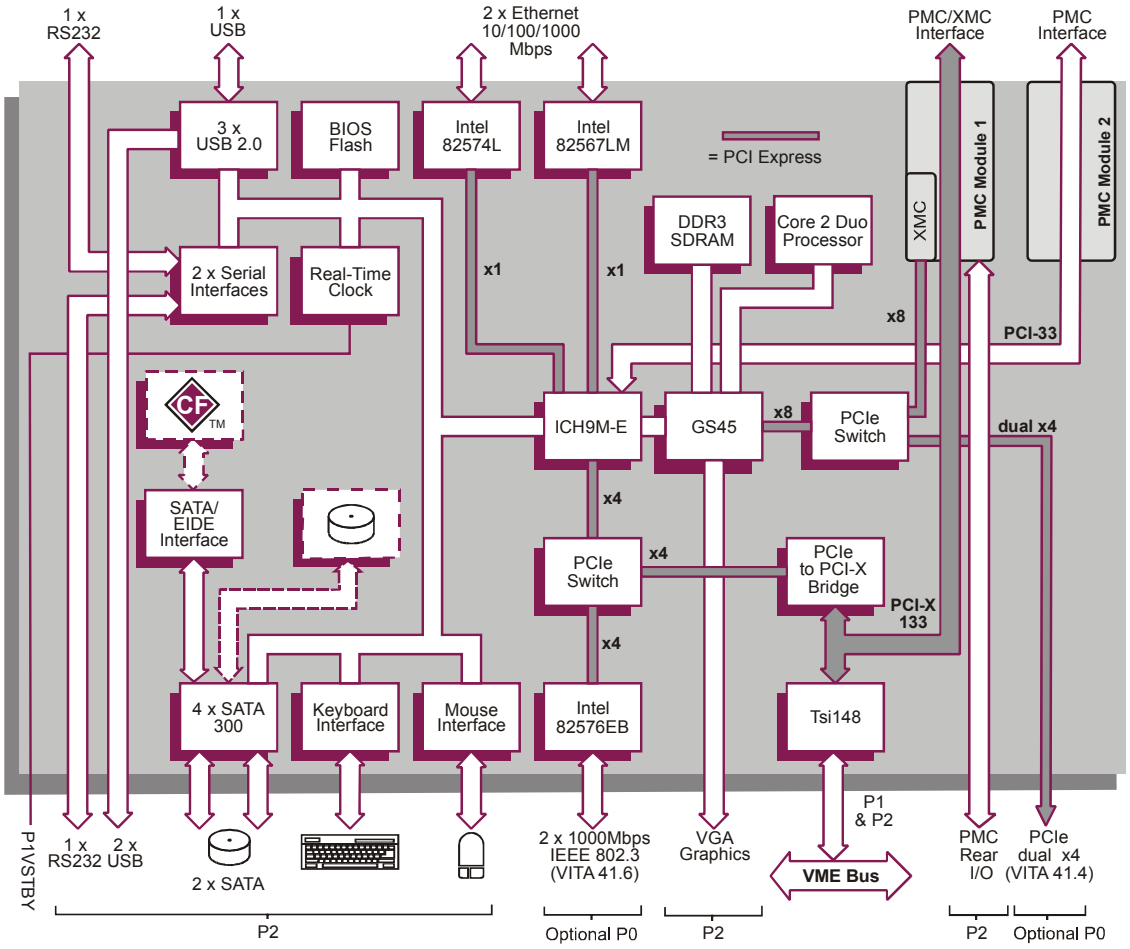


Figure 1-2 Overview of Ruggedized Air-Cooled Boards

1.2.3 Ruggedized Conduction-Cooled (RC-Series) Options

The VX 511/06x is also available as Ruggedized Conduction-Cooled variants designated VX 511/061-RC. These offer extended temperature ranges, a higher specification for shock and vibration and do not require any forced airflow through the chassis. Please see Section A.2 for specifications on the temperature range and Section A.3 for the shock and vibration ranges supported by the VX 511/061-RC.

Some features of the Ruggedized Conduction-Cooled variants are significantly different to the other series of variants, though the primary difference is the absence of front panel connections. If the RC variant is being used, it is recommended that Appendix C be referred to prior to reading the main manual, as Appendix C provides more details of the differences in the RC variant. Consult Concurrent Technologies or your distributor directly for further details.

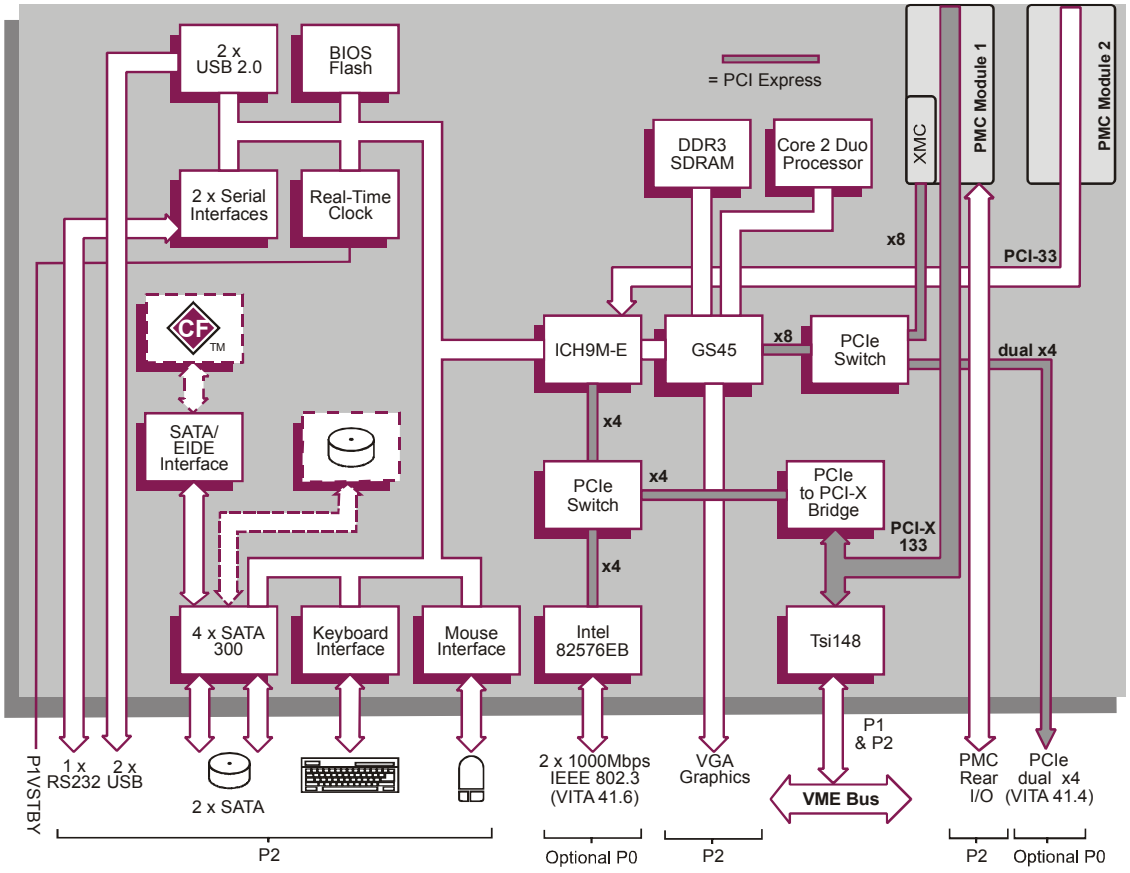


Figure 1-3 Overview of Ruggedized Conduction-Cooled Boards

1.2.4 Differences between Standard, Extended Temperature and Ruggedized Options

Table 1-2 indicates the features supported by the extended temperature and ruggedized boards.

Version	Series	Mass Storage with CompactFlash Card	Mass Storage with 2.5" Hard Disk Drive or 2.5" Flash Drive	Front Panel Interfaces	Battery socket
Standard Temperature	N-Series	✔	✔	✔	✔
Extended Temperature	E-Series	✔	✔	✔	✔
	K-Series	✔	✔	✔	✔
Ruggedized Air-Cooled	RA-Series	✔	✔	✔	✘
Ruggedized Conduction Cooled	RC-Series	✔	✔	✘	✘

Table 1-2 I/O Differences between N, E, K, RA and RC Series

1.3 The VX 511/06x – Main Features

The VX 511/06x is a member of the Concurrent Technologies range of single board computers for the VME bus architecture. It has been designed as a powerful single board computer based upon the Intel Core 2 Duo processor, the Intel® GS45 and ICH9M-E chipset with Internal Gigabit LAN, an Intel® 82576EB dual channel Gigabit Ethernet controller, an Intel® 82574L Gigabit Ethernet controller and a PCI to VME bus bridge chip. It also provides two IEEE 1386.1 PMC (one with XMC) interfaces, two PMC/ XMC expansion carrier interfaces, optional on-board mass storage and interfaces for standard PC-AT based peripherals.

1.3.1 Central Processor

The central processor used on this board is an Intel Core 2 Duo processor, operating internally at 1.86 GHz or at 2.26 GHz.

The Intel Core 2 Duo processor has two high performance execution cores based on the latest Intel® Core™ Microarchitecture. The 64-bit frontside bus is connected to the memory controller at 1066 MHz to provide a maximum transfer bandwidth of 8.3 Gbytes/s. The processors are capable of addressing 64 Gbytes of physical memory all of which is cacheable and 64 Terabytes of virtual memory.

The Intel Core 2 Duo processors are upwardly code-compatible with the other members of the x86 family of microprocessors. They have in-built floating point coprocessors for compatibility with 486 and 386/387 designs. The Intel Core 2 Duo processor also supports Intel® 64 Technology (64-bit computing).

1.3.2 Cache Memories

The Level 1 and Level 2 caches are both implemented on the processor die for maximum performance. Each of the two execution cores has its own Level 1 cache and they share a common Level 2 cache. The Level 1 cache is organized as 32 Kbytes of instruction cache and 32 Kbytes of data cache. The Level 2 cache stores both instructions and data. It operates at the core frequency and is based on the Advanced Transfer Cache architecture from Intel. The Core 2 Duo processor has 6 Mbytes of Level 2 cache.

1.3.3 Chipset

The VX 511/06x uses the Intel GS45 and ICH9M-E chipset. This is comprised of the GS45 Graphic Memory Controller Hub (GMCH) and the ICH9M-E I/O Controller Hub (ICH). They respectively provide North Bridge and South Bridge.

The GS45 GMCH interfaces to the CPU's host bus. It provides a dual-channel DDR3 SDRAM memory controller, high performance graphic controller, a PCIe link and a high speed Direct Management Interface which connects to the ICH9M. It supports concurrent CPU, memory, PCI Express and Hub Interface bus operations.

The ICH9M-E provides several PCIe links for supporting high performance devices. It also provides a 33 MHz 32-bit PCI bus. The Direct Management Interface supports a maximum transfer bandwidth of 2 Gbytes/s.

The ICH9M-E also provides a variety of peripheral functions including Serial ATA (SATA) controllers, USB 2.0 and 1.1 controllers, LPC (Low Pin Count) Bus bridge, SPI bus for BIOS memory, IOAPIC interrupt controller, Real Time clock (RTC) and other legacy PC-AT architectural functions.

The LPC Bus is used to connect to the PC87427 SuperI/O Controller. This device implements two serial ports, keyboard and mouse controller and provides the interface to control the status registers.

1.3.4 SDRAM

The SDRAM controller within the GS45 GMCH supports dual DDR3 1066MHz memory channels. These provide a maximum memory transfer bandwidth of 8.3 Gbytes/s. 6 Gbytes maximum of on-board memory are supported.

1.3.5 PCI Express Busses

The GS45 has an x8-lane PCIe interface which is connected to a 24-lane PLX PCIe switch. The remaining 16 lanes of the switch are configured as one x8-lane and two x4-lane links which are used to support the XMC site and VXS P0 connector. The x8-lane PCIe link connects to the XMC site, this link can also be configured as two x4-lane links. The two ports of x4 PCIe connect to Port A and Port B on P0 as specified for the VXS VITA 41.4 data plane.

The ICH9M-E has an x4-lane PCIe link and two x1-lane links. The x4-lane link connects to a PCIe switch, which connects to a Pericom PCI/PCI-X bridge as well as to an Intel® 82576EB Dual Gigabit SerDes through a PCIe switch. One of the x1-lane links connects to the front Gigabit Ethernet controller. The last x1-lane link is configured as an Internal Gigabit LAN GLCI.

1.3.6 PCI Busses

There are two separate PCI busses on the board, one being 64-bit and one 32-bit. The 64-bit bus is generated from the Pericom PCIe-to-PCI/PCI-X bridges and the 32-bit bus is provided by the ICH9M-E.

The 64-bit bus supports 33/66 MHz in PCI mode and 66/100/133 MHz in PCI-X mode, this connects to the PMC site as well as the Tundra Tsi148 VME-to-PCI Bridge.

The ICH9M-E's 32-bit PCI bus is used to connect to the second PMC site.

1.3.7 EPROM

The board contains a 4 Mbyte SPI Flash device for the BIOS code, fixed data and factory test software.

1.3.8 VME Interface

The VME bus interface is provided by a Tundra Tsi148 VME-to-PCI-X Bridge. The interface will operate in any VME slot. The VME interface is 32/64-bits wide. All modes of access and cycle types are supported, including 2eSST and 2eVME. The board can act as system controller when in the first VME Bus slot.

1.3.9 EIDE Controller

The VX 511/06x has one EIDE interface which connects to a CompactFlash® site. The EIDE interface is implemented with a SATA to EIDE device.

1.3.10 Serial ATA Controllers

The VX 511/06x has three Serial ATA300 interfaces. Two interfaces are available from the rear P2 connector, and one interface is available as an on board connection for a 2.5" SATA hard disk or solid state disk drive.

1.3.11 USB

Three USB 2.0 channels are provided by the board, one via the front panel connector and two via the P2 connector. All three USB channels support both USB 1.1 (1.5 and 12 Mbits/s) and USB 2.0 (480 Mbits/s) operation.

1.3.12 PMC/XMC Interfaces

Two PMC interfaces which support single width PMC modules complying with the IEEE 1361.1 standard are provided. The first PMC site has a 32/64-bit 33/66 MHz PCI or 66/100/133 MHz PCI-X bus interface, and supports 3.3V and 5V signaling. It has an XMC connector with an x8-lane PCI express link. The second PMC site has a 32-bit 33 MHz PCI bus interface, and supports 3.3V and 5V signaling.

The PMC interfaces will also accept dual function and Processor PMC modules. The latter will operate only in non-Monarch mode.

1.3.13 PMC Expansion Carrier Interface

The VX 511/06x supports the AD CR3/PMC PMC Expansion Carrier board. The carrier board supports two single width PMC modules complying with the IEEE 1361.1 standard, in a second backplane slot adjacent to the VX 511/06x. Using the AD CR3/PMC, one PMC site is occupied on the VX 511/06x, and the two additional sites on the carrier board support only 3.3V PCI signaling environments at 33 or 66 MHz.

1.3.14 Ethernet Controllers

A single Intel® 82576EB Gigabit Ethernet controller is used to provide two high performance PCIe-to-Gigabit SerDes interfaces. Both support 1000 Mbits/s only operation. The board can support either VITA 41.6 backplane networking or rear panel Gigabit Ethernet. The rear panel Ethernet interface is not accessible in all board configurations – see Section 1.4 for further details.

An Intel® 82574L Gigabit Ethernet controller is used to provide a high performance PCIe-to-Ethernet interface. An 82567LM PHY is used to connect directly to the ICH9M-E GLCI, and will support Intel AMT. Both of these Gigabit Ethernet interfaces are available on front panel connectors.

1.3.15 Graphics Controller

The VX 511/06x provides analog SVGA graphics using the GS45 integrated graphics controller. This device shares the main memory and offers resolutions up to 2048 x 1536 with 32-bit color support. The SVGA interface is accessed via the Rear P2 connector.

1.3.16 Serial Communications

The VX 511/06x provides two serial data communication channels. These are implemented by the PC87427 SuperI/O Controller and are available via a front panel RJ45 connector and P2. The baud rate clock is generated internally by the device's I/O Controller.

1.3.17 Keyboard and Mouse

The VX 511/06x supports PS/2™ type keyboard and mouse interfaces. These are accessed via the Rear P2 connector.

USB keyboard and mouse are also supported. These devices may either be connected to the USB ports on the RTM, or be connected, via a USB hub, to the front panel USB connector.

1.3.18 Real Time Clock (RTC)

A battery backed RTC device provides PC-AT clock, calendar and configuration RAM functions.

The RTC and BIOS are year 2000 compliant. The clock and configuration RAM functions can be maintained from an external supply for battery free operation if required.

1.3.19 Other Interfaces

The VX 511/06x has 2 TTL compatible I/O pins accessible via P2 which are available for user defined I/O.

1.4 I/O Configuration Options

The VX 511/06x board may be ordered in one of a few hard-wired configurations to support different combinations of rear I/O.

In particular, there are two options available with or without the P0 connector fitted. Not fitting P0 results in the following rear access interfaces being lost: dual Gigabit SERDES backplane networking and two ports x4-lane PCIe data plane. Note that additional interfaces are available on the P2 connector.

Each board is typically used with an appropriate Rear Transition Module (RTM) to provide connections behind the backplane, and the standard options are described in Appendix B. Table 1-3 indicates the interfaces provided by each of these RTMs. The RTMs must be ordered as additional items to the VX 511/06x board.

RTM	VME P2 Connector pins	VME P0 Connector	Serial ATA (SATA)	Gigabit Ethernet	VGA	USB	PMC1 Rear I/O	Keyboard	Mouse	General Purpose I/O	Push button reset	Serial Port COM 2	eSATA
AD VP2/018-10	160		2		✔	2	64-bit	✔	✔	✔	✔	✔	
AD VP2/018-30	160	✔	2	2	✔	2	64-bit	✔	✔	✔	✔	✔	
AD VP2/024-10	160		2*		✔	2	64-bit	✔	✔	✔	✔	✔	2*
AD VP2/024-30	160	✔	2*	1	✔	2	64-bit	✔	✔	✔	✔		2*

Table 1-3 VME RTM Interfaces

Note that all RTMs are fitted with 160-way P2 connectors as many of the I/O interfaces are connected via rows D and Z of the VX 511/06x P2 connector. Some configurations of the VX 511/06x board also use the P0 connector to provide some of the I/O interfaces. In these cases, the appropriate backplane (typically for VXS) will be required to connect the RTMs.

* = SATA and eSATA ports are user-selectable and a maximum of two ports may be selected (e.g. 2 x SATA or 2 x eSATA or 1 x SATA and 1 x eSATA).

1.5 On-board Mass Storage Options

Additional mass storage option kits are available for the VX 511/06x:

- A 2.5 inch SATA hard disk drive of at least 80 Gbytes capacity
- A Flash disk module (CompactFlash) kit

NOTE: The mass storage option kits utilize one of the PMC site areas. It is not possible to fit both a mass storage option kit and a PMC module to the same site simultaneously.

Refer to the VX 511/06x datasheet for ordering information for all these options.

1.6 Compliance to RoHS 2002/95/EC



This product is offered in a form which complies with the RoHS 2002/95/EC directive, including any technology-specific exemptions where applicable. The European Union RoHS 2002/95/EC directive restricts the use of six materials in electronic components and assemblies. Specifically, these materials are Lead (Pb), Mercury (Hg), Cadmium (Cd), Hexavalent Chromium (Cr VI), Polybrominated Biphenyls (PBB) and Polybrominated Diphenyl Ethers (PBDE). Concurrent Technologies is committed to compliance to the RoHS directive.

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2 INSTALLATION

2.1 General

This chapter contains general information on unpacking and inspecting the VX 511/06x after shipment, and information on how to configure board options and install the board into a CompactPCI chassis.

CAUTION: It is strongly advised that an earthing strap should be worn at all times when handling the VX 511/06x and its associated components in order to prevent damage to the board as a result of electrostatic discharge.

CAUTION: Care should be taken when handling the board as the heatsink and some components will be hot during and after use.

The list below outlines the steps necessary to configure and install the board. Each entry in the list refers to a section in this chapter which will provide more details of that stage of the procedure. It is recommended that the board is prepared for installation by following this sequence:-

- Unpack the board - see Section 2.2.
- Locate the board indicators, switches and jumpers- see Section 2.3.
- Check the board jumper and switch settings match the required operating mode - see Section 2.4.
- Fit the battery if required - see Section 2.5.
- Fit a CompactFlash module if required - see Section 2.6.
- Fit any optional mass storage modules - see Section 2.7.
- Fit a PMC/XMC module if required - see Section 2.8.
- Install the board - see Section 2.9.

CAUTION: It is strongly recommended that the user reads all the sections in this chapter before installing the board in a VME backplane, or before fitting a PMC/XMC module. In particular, additional cautionary notes will highlight areas needing special consideration.

2.2 Unpacking and Inspection

A thorough inspection of the package and contents should be carried out immediately after the board is delivered, to check for any damage caused in transit.

CAUTION: If the external packaging is damaged or water-stained, the carrier's agent must be present when the board is unpacked.

Once unpacked, the board should be inspected carefully for physical damage such as loose components. Should the board be damaged, notify Concurrent Technologies or its authorized agent immediately.

2.3 Default Jumper and Switch Settings

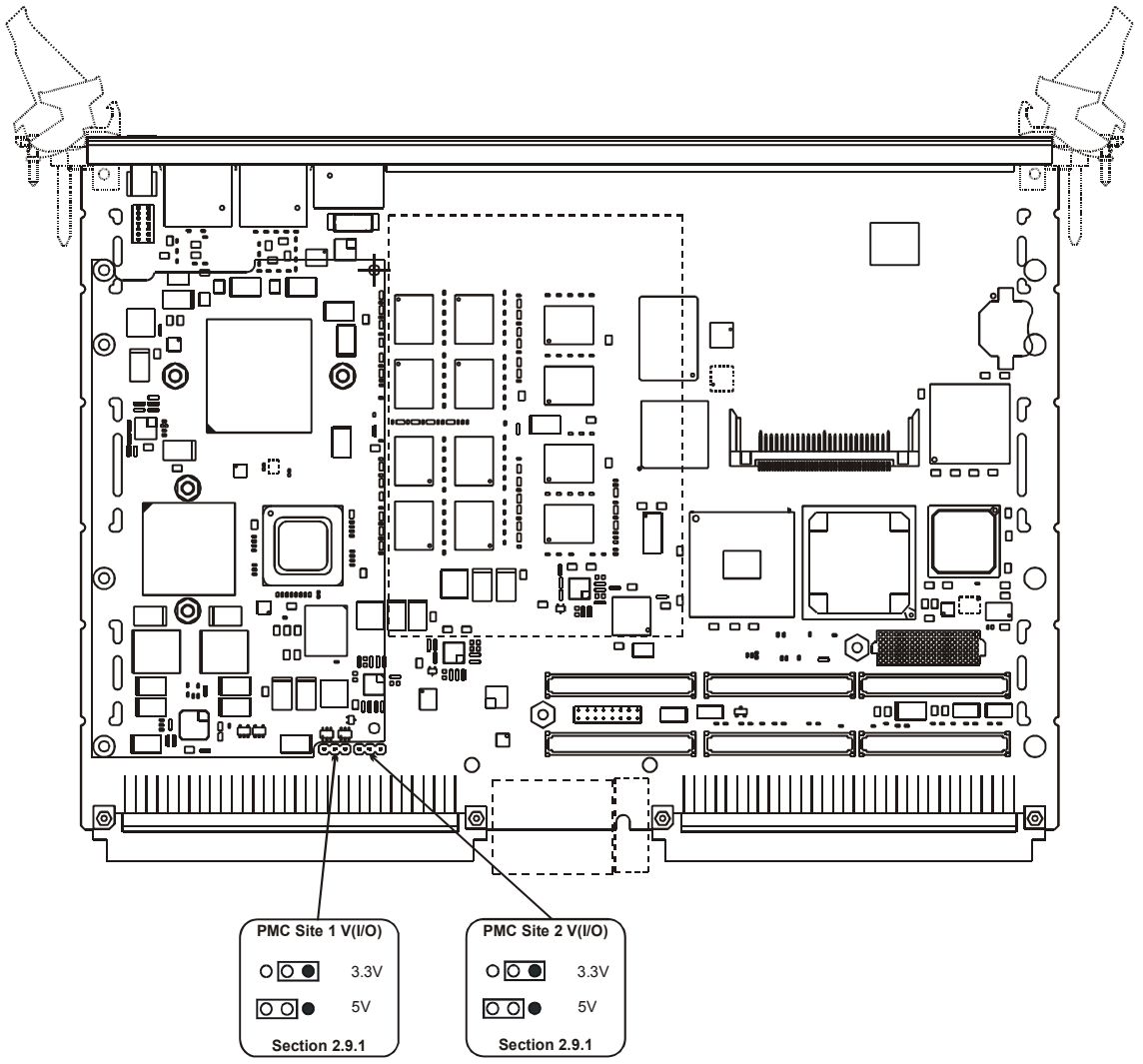


Figure 2-1 Default Jumper Settings (Component Side)

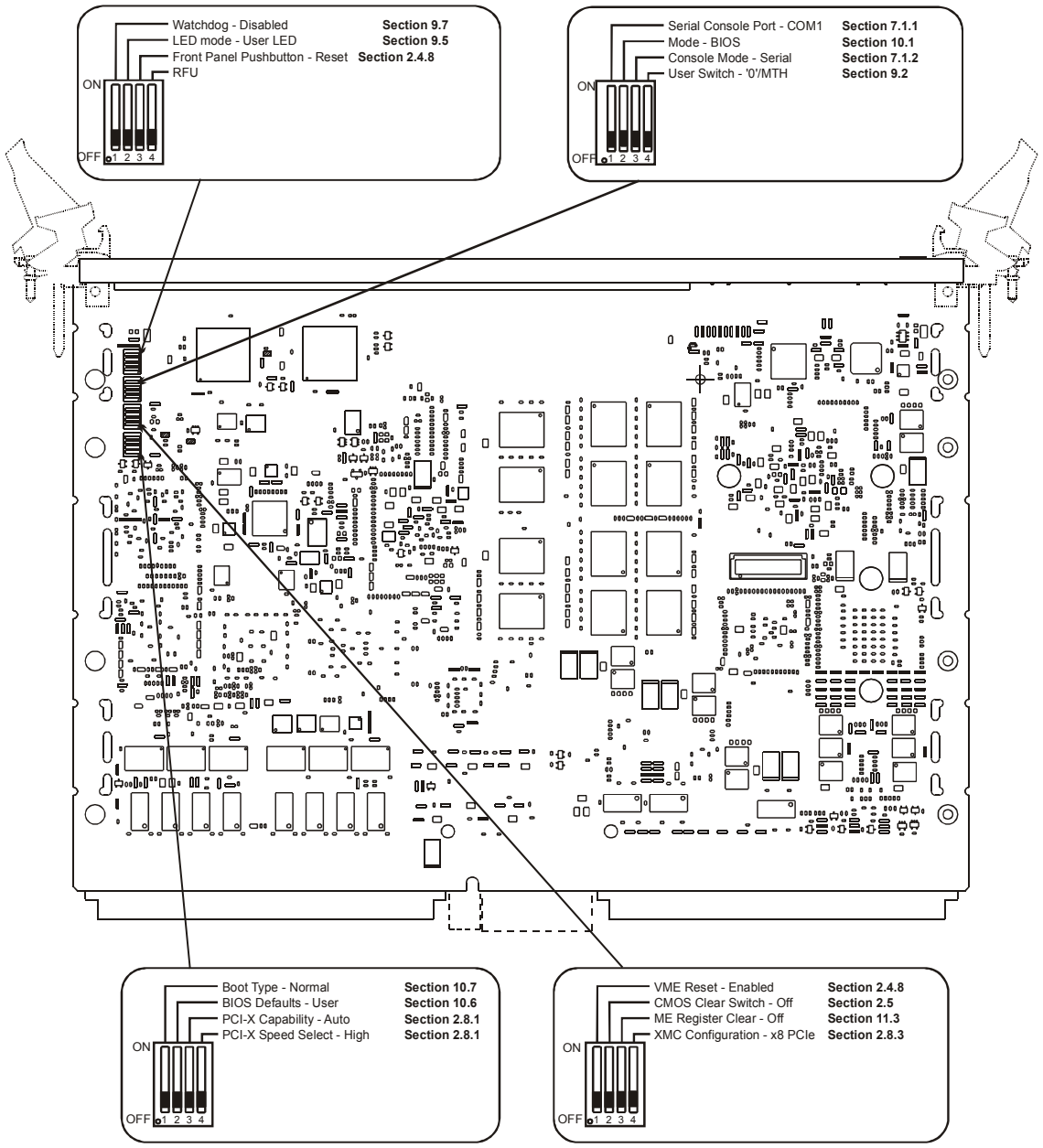


Figure 2-2 Default Switch Settings (Solder Side)

2.4 Front Panel Indicators and Controls (Air-Cooled Variants Only)

LEDs are provided for development and debug on standard, extended temperature and ruggedized air-cooled variants. Ruggedized conduction-cooled variants do not have a front panel fitted; however some of the LEDs are still supported.

When installing or removing the board for the first time or when checking its operation, it can be very useful to note the behavior of the LEDs on the front panel. Figure 2-3 shows the location of the LEDs, and their purpose is outlined below.

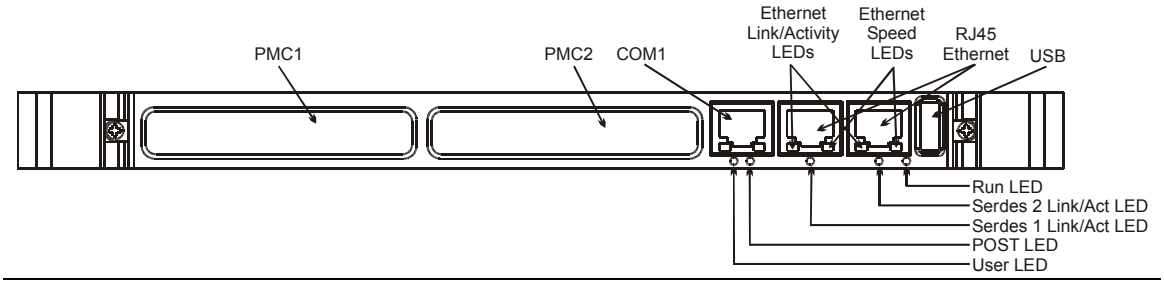


Figure 2-3 Front Panel Indicators and Controls

2.4.1 Run LED (R) Green

The run LED indicates that activity is occurring on either of the internal LPC or 32-bit PCI busses. This allows the user to quickly assess how active the busses are.

2.4.2 POST LED (P) Yellow

The POST LED is used to indicate that a power on self test has failed. This LED will also flash when outputting sound on the speaker interface.

2.4.3 Ethernet Speed LEDs (SP) Yellow

These LEDs indicates the operating speed of the Ethernet interfaces, as follows:

- Off = 10 Mbits/s
- Steady On = 100 Mbits/s
- Flashing = 1000 Mbits/s

2.4.4 Link/Activity LEDs (LK) Green

These LEDs light when connection has been made on the Ethernet interfaces. They will flash to indicate link activity, and during periods of high Ethernet activity the LED may switch off for several seconds.

2.4.5 Disk Activity LED (On board) Orange

This LED lights when there is activity on the on board EIDE interface.

2.4.6 User LED (U) Red

This LED is available for use by user software. It is manipulated via an I/O register. Alternatively, the User LED may be configured to light when the CPU reaches its maximum specified operating temperature. In either mode, the User LED will flash rapidly if the CPU Thermal Trip activates. See Section 11.2 for further details.

2.4.7 SerDes Link/Activity LEDs (S1 and S2)

These LEDs light when connection has been made on Gigabit SerDes (VITA 41.6) or the RTM with Ethernet fitted. They will flash to indicate link activity and, during periods of high Ethernet activity, the LED may be off for several seconds.

2.4.8 Reset Pushbutton

This pushbutton which is available on the RTM can be configured via the Front Panel Switch Function switch to perform one of two functions:

1) a board and/or system reset
2) a local Non-Maskable Interrupt (NMI)

When the Front Panel Switch Function switch is in the "NMI" position, operating the pushbutton causes an NMI to the local CPU.

When the Front Panel Switch Function switch is in the "Reset" position, operating the pushbutton causes a reset locally on the board. If the board is the System Controller, this reset may also be propagated to the VME backplane via the SYSRESET# signal, depending on the setting of the VME Reset Out Enable switch (see below). If the board is not the System Controller, only the board itself will be reset.

The VME Reset Enable switch prevents or disables both the reset action of the front panel pushbutton and the Watchdog Timer expiry event (see Section 9.7) from activating the VME bus reset signal SYSRESET#. When this switch is in the "Disabled" position, the pushbutton reset and Watchdog Timer expiry reset will only act locally on this board. When this switch is in the "Enabled" position, both the pushbutton reset and Watchdog Timer expiry reset will cause a VME bus reset via the SYSRESET# signal. Regardless of the setting of the VME Reset Enable switch, the board will always generate a VME bus reset both from power up (when acting as System Controller) and when the Tsi148 chip has been programmed to do this.

Figure 2-4 shows the location and settings of the VME Reset Enable and Front Panel Switch Function switches.

The board's response to SYSRESET# being activated by another board is also configurable. Status and Control register 2 (see Section 9.4) contains a bit which can be programmed to allow or prevent the backplane SYSRESET# signal causing a reset to the board.

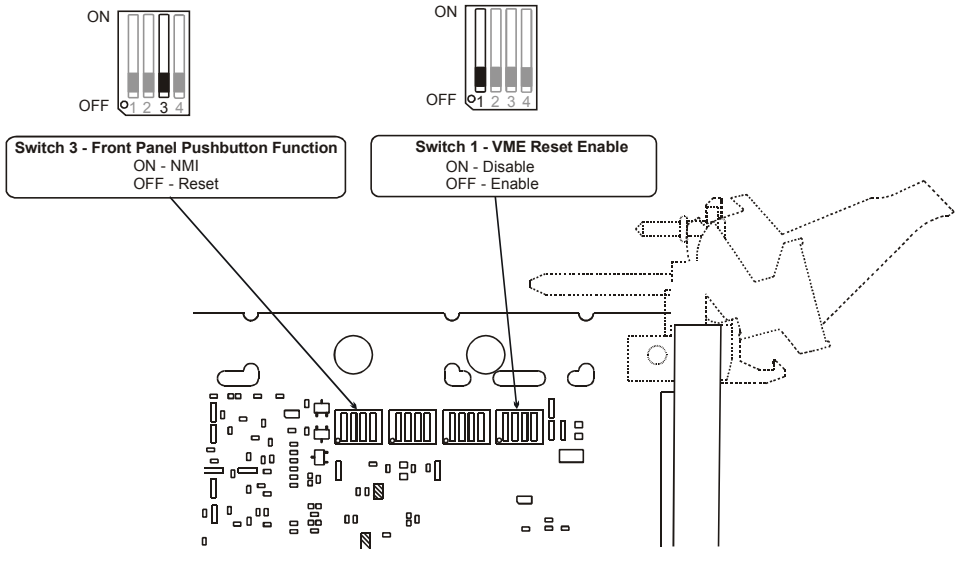


Figure 2-4 Front Panel Pushbutton and VME Reset Switches

2.5 Battery Installation/Replacement

The on-board Real Time Clock and CMOS memory used by the PC BIOS firmware are powered by a 3V Lithium battery when the board is powered off. It is advisable, though not essential, for the battery to be fitted prior to using the board as shown in Figure 2-5. One battery is supplied with the board, but it is not normally fitted when the board is shipped.

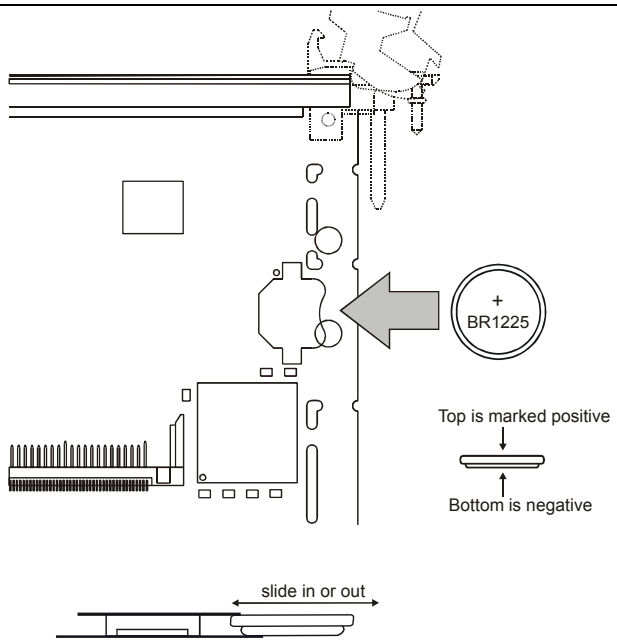


Figure 2-5 Battery Installation

The battery should be replaced when the voltage falls below 2.5V. Depending on how the board is operated and stored, battery life should be approximately 3 years for 33% off time, 2 years for 66% off-time and 1 year for 100% off-time. Battery life expectancy will fall if the battery is subjected to long periods at temperatures of 45°C or above, or if the battery is fitted to a board that is stored in its conductive bag even at room temperature.

Operation without a battery is possible by connecting the VME Bus VCC_STANDBY supply to an external 5V source. The contents of the CMOS memory will be maintained and the Real Time Clock will continue to function as long as the VCC_STANDBY supply is maintained to the board.

NOTE: When replacing the board it is not necessary to remove power from the VCC_STANDBY supply.

CAUTION: When replacing the battery, anti-static precautions must be observed.

WARNING: Dispose of battery properly. DO NOT BURN. The date and time settings will need to be initialized if the battery is disconnected.

Battery



Never dispose of batteries in a fire.
Always dispose of batteries according to local regulations.
Please recycle when possible.
Do not dispose of batteries as household waste.
Always replace battery with manufacturer's recommended type.

2.5.1 Battery Isolation Strip

In order to prevent loss of battery capacity when the battery is fitted while the board is in storage, an insulating strip is available. This strip isolates one of the battery terminals preventing unwanted discharge. The strip is easily fitted and removed as described below.

This strip is supplied with new product. Customers with existing product who require the strip should contact their local sales office.

NOTE: When this strip is fitted, an unpowered board will not retain the Real Time clock or BIOS settings if they have not been saved to Flash/NVRAM.

2.5.1.1 Fitting the Strip

The insulating strip must be fitted into the battery retainer as outlined below. It may be easier to carry out this process without a PMC or XMC card installed in site 2, although it is not necessary to remove the card if one is already fitted.

1) Hold the strip at the labeled end with the fold facing away form the board and slide the other end into the entrance of the battery retainer. Slide the strip in until the end of the strip lines up with the rear of the battery retainer.
2) Place the new battery on top of the strip with the thicker side of the battery facing upwards, and slide it into the battery retainer.
3) Fold the loose end of the strip over the top of the battery retainer toward the center of the board, taking care not to pull it out of the battery retainer. The end may be slipped underneath a PMC or XMC card if one is fitted in site 2. When there is no PMC or XMC card in site 2, the strip should be further creased to keep the loose end as close as possible to the board.
4) Prepare the board as usual, taking care not to push the insulating strip out of the retainer at any stage.

2.5.1.2 Activating the Battery

When the board is to be made ready for use, follow this procedure:

5) Retrieve the loose end of the strip and move it away from the center of the board.
6) Gently pull the strip away from the edge of the board and out of the battery retainer. The strip may be discarded at this stage.
7) To ensure that the battery is still properly located, push the exposed edge of the battery gently toward the center of the board until it is fully inserted in the retainer.

NOTE: The Real Time Clock data will need to be set after the board is powered up.

2.5.2 Clearing the CMOS RAM

If the BIOS setup screens have been used to set up the board for an invalid configuration, or in other fault conditions, it may be useful to be able to reset the contents of the CMOS RAM and Real-Time Clock. In this case, the CMOS Clear switch can be used.

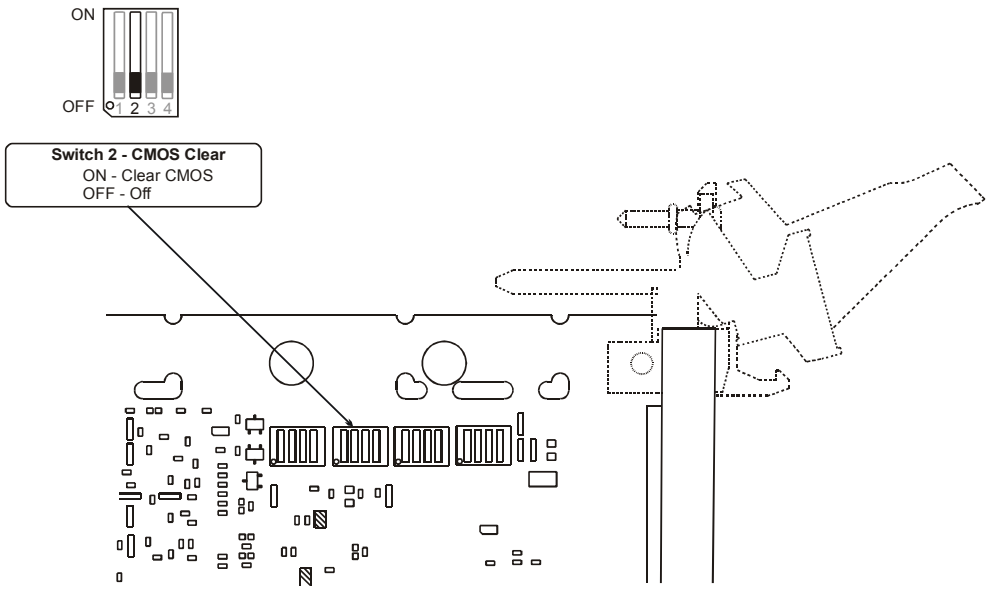


Figure 2-6 CMOS Clear Switch

To clear the CMOS RAM to a known state, switch ON the CMOS Clear switch and apply power. When the board is next powered down switch OFF the CMOS Clear switch, otherwise CMOS RAM will again be reset. After the BIOS settings have been re-configured, they can be saved to Flash EPROM as user default values. See Section 10.6 for more details of this capability, which is very useful when the board is running without a battery or power through VCC_STANDBY.

2.6 Installation of CompactFlash Modules

The VX 511/06x has the option to have a CompactFlash card installed – the site and associated components are shown in Figure 2-7.

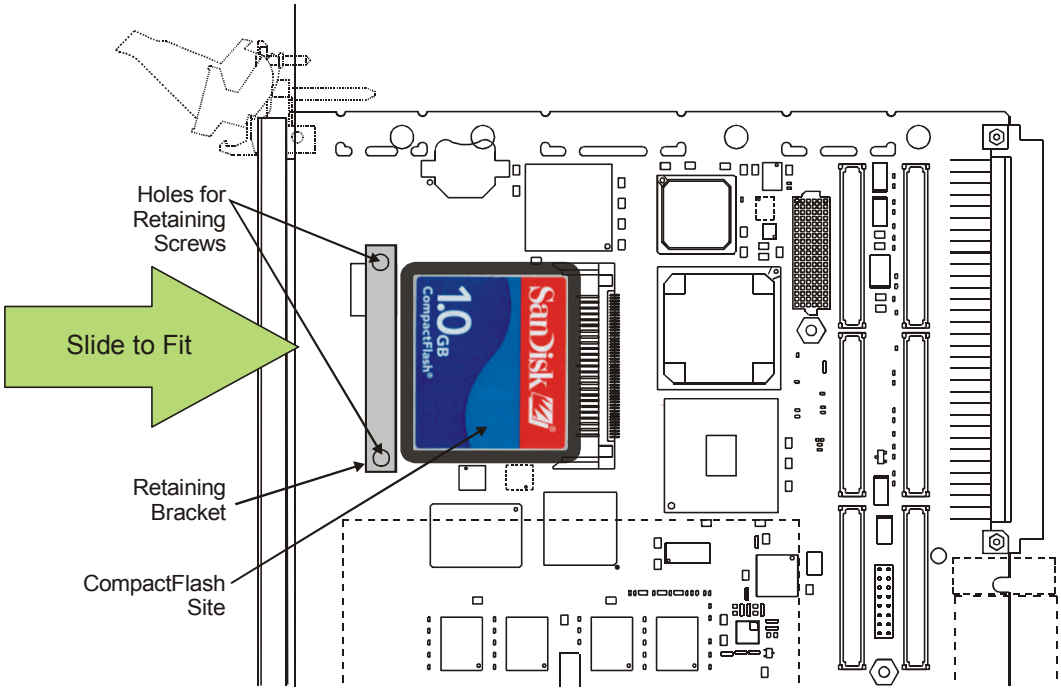


Figure 2-7 Fitting a CompactFlash card

To fit a CompactFlash card:

- Remove the retaining bracket (if fitted) by undoing the two fixing screws and lifting the bracket clear of the board.
- Orient the card so that the connector end is facing the socket and the label side is away from the board.
- Slide the CompactFlash card between the guides until it locks into the connector.
- Refit the retaining bracket (if required) by placing it behind the card and screwing it into place.

Removal of a CompactFlash card is the reversal of the above procedure.

2.7 Installation of On-Board Mass Storage

The mass storage option is fitted to connector pads and is secured via screws and spacers using the four HDD mounting holes and two adapter mounting holes as shown in Figure 2-8 below.

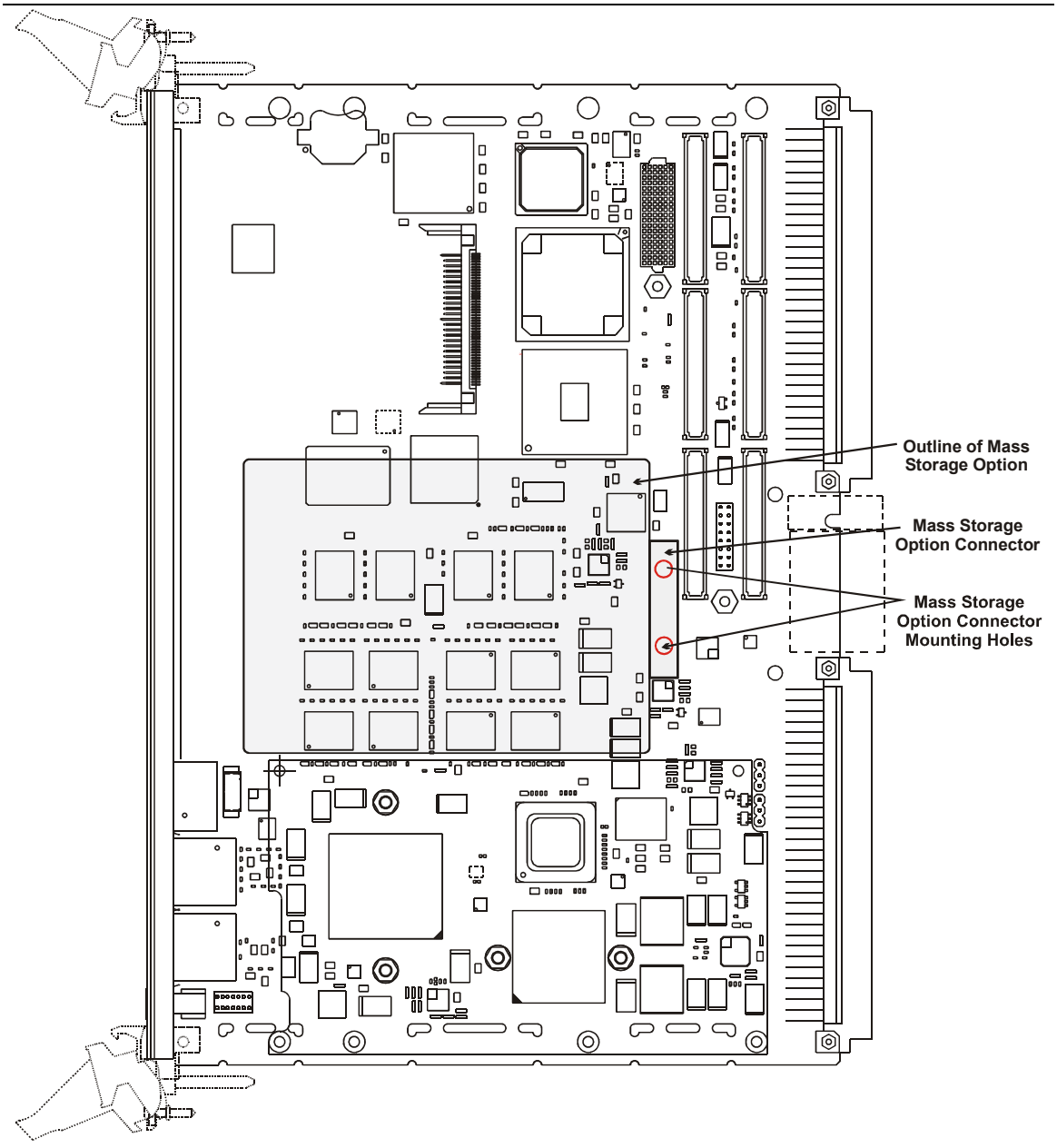


Figure 2-8 Mass Storage Connector and Fixing Screws

2.7.1 Hard Disk Storage Kit (AD 110/001)

The option kit comprises:

- A 2.5 inch SATA disk drive (dependent upon variant ordered)
- An adapter assembly
- Four M3 x 4mm screws
- Four M3 x 5mm pillars
- Two M2 x 6mm screws

The adapter assembly has a 20-way connector on one side and a 22-way SATA connector on the other side. The 22-way SATA connector plugs into the disk drive and the 20-way connector attaches to the base board.

1) If necessary remove the second slot board from the single slot board, using the procedure explained in the board manual
2) Screw the four pillars into the bottom of the disk drive until the pillar and the disk drive meet, i.e. there should be no gap between them. Do not over tighten the pillars.
3) Remove PMC site polarizing key if fitted.
4) Plug the 22-way SATA connector into the disk drive as shown in Figure 2-9 - note the orientation.

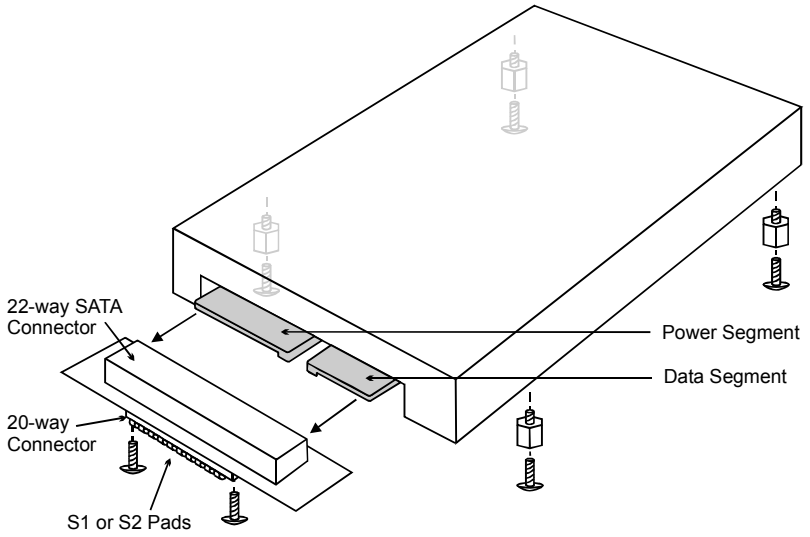


Figure 2-9 Disk Drive Installation

5) Fix the disk drive into position, placing the four M3 screws provided through the appropriate holes in the host board and screwing them into the bottom of the pillars. Do not over tighten the screws.
6) Secure the adapter to the base board using the two M2 screws provided. Do not over tighten the screws.
7) If necessary replace the second slot board onto the single slot board, using the procedure explained in the board's manual.

NOTE: If the board is likely to be subjected to mechanical vibration a suitable thread lock compound applied to the screws should be considered.

2.8 Installation or Removing a PMC or XMC Module

2.8.1 V(I/O) Selection for PMC Modules

The VX 511/06x board provides two jumpers to select 3.3V or 5V V(I/O) independently to both PMC sites. Before installing a PMC module check that the VX 511/06x board PMC V(I/O) is configured to match the requirements and/or configuration of the PMC modules being used. See Figure 2-10.

PMC Site 1 has provision for fitting a polarizing key for 3.3V V(I/O) or 5V V(I/O) PMC modules. Only one key must be fitted, to correspond with the setting for the PMC site 1 V(I/O) jumper. In PMC Site 2, provision is made only for a 5V polarizing key. If a 3.3V V(I/O) PMC module is fitted in this site, the polarizing key should be removed.

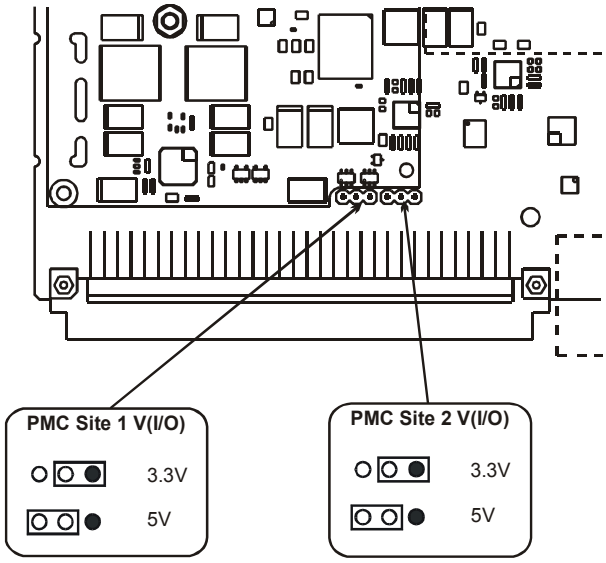


Figure 2-10 PMC Sites V(I/O) Jumpers

CAUTION: Ensure that the jumpers and polarizing keys are configured correctly for the PMC cards being used. Failure to do so may result in damage to the VX 511/06x board or to the PMC cards.

2.8.2 PCI Bus Speed Selection for PMC Modules

The 64-bit PCI bus connecting to the first PMC Site can operate at various bus speeds and modes:- 33 MHz PCI, 66 MHz PCI, 66 MHz PCI-X, 100MHz PCI-X and 133 MHz PCI-X. The speed and mode of the bus are determined by either the type of PMC modules fitted or the setting of option switches as shown in Figure 2-11.

Both switches should normally be in the OFF position. This allows the bus to operate at the optimum speed for the PMC modules fitted, including PCI-X mode when PCI-X capable PMC modules are fitted. If Switch 3 is in the ON position, the bus will always operate in 33 MHz or 66 MHz PCI mode, otherwise it can operate in PCI-X mode up to 133 MHz. If Switch 4 is in the ON position, PCI-X operation is limited to 100 MHz, otherwise it can negotiate up to 133 MHz.

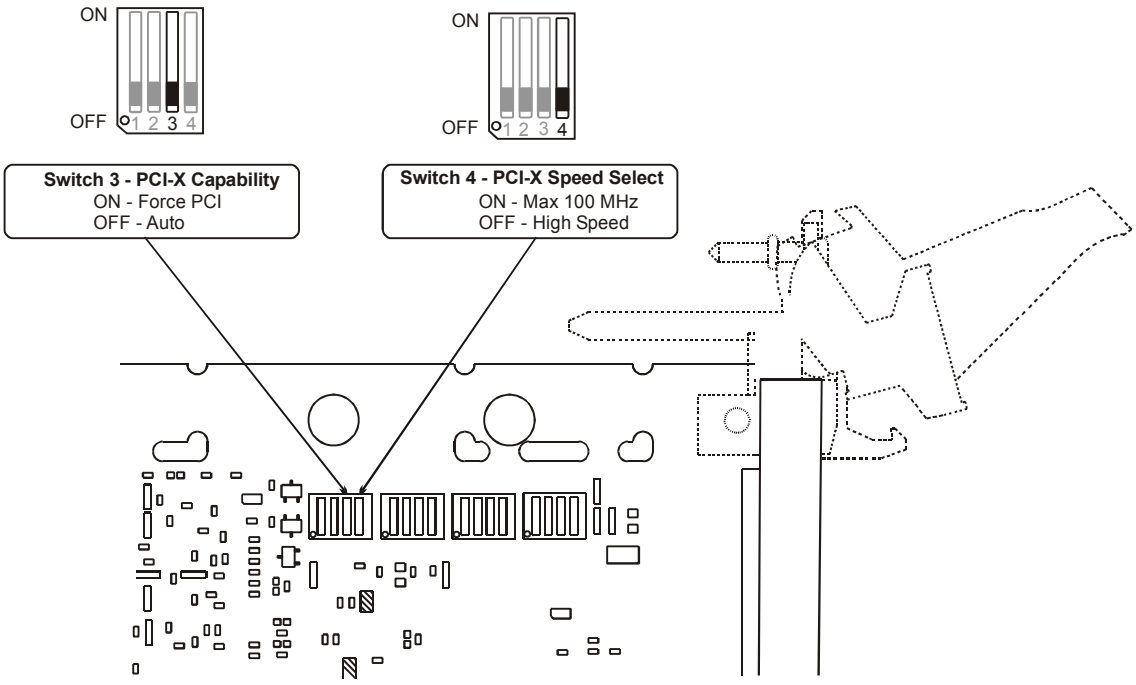


Figure 2-11 PCI Speed Select and Capability Switches

NOTE: The PMC site 1 PCI bus is shared with the Tsi148 PCI-X-to-VME bridge, hence the VME bandwidth may be affected if a PMC module is fitted which can only support lower speeds.

PMC Site 2 can only support 33 MHz PCI operation.

2.8.3 XMC PCIe Lane Width

It is possible to configure the XMC site to accept dual x4-lane PCIe XMC cards by use of SW4-4 (XMC Configuration switch), as shown in Figure 2-12.

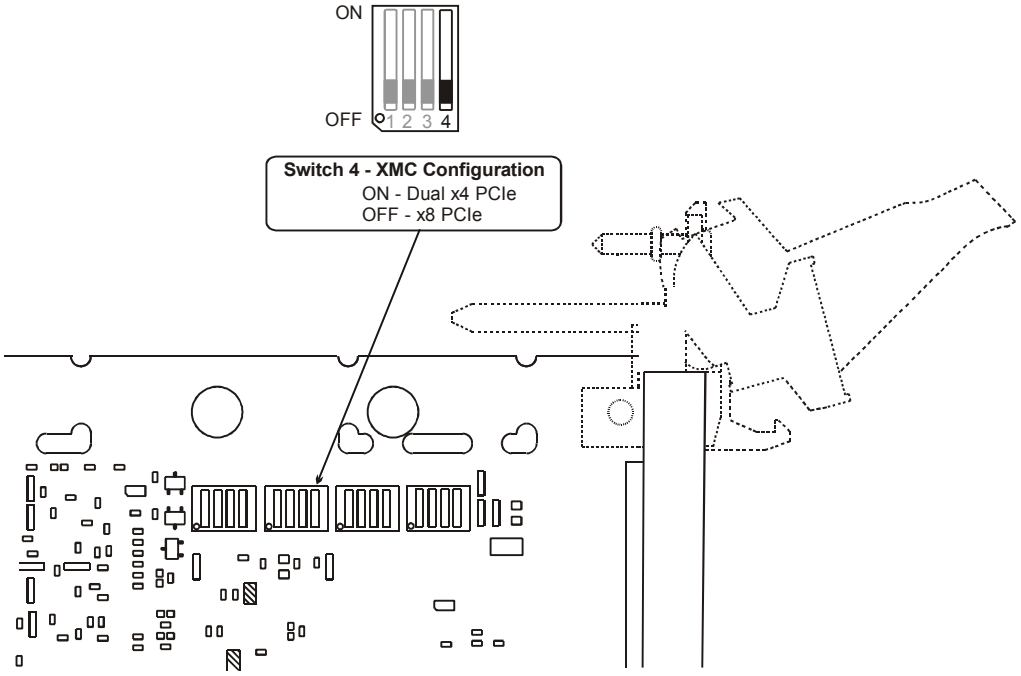


Figure 2-12 XMC Configuration Switch

2.8.4 Installation Instructions (except VX 511/06x-RC)

Figure 2-13 shows the way to install a PMC module on the board. Use the same approach when fitting an XMC module, but first remove the voltage key post, as shown in Figure 2-13.

NOTE: The VX 511/06x board is supplied with PMC blanking plates which must be removed before a new module can be fitted.

NOTE: When using the VX 511/06x, only PMC modules which meet the required standard for shock and vibration should be used.

1) Remove the front panel blanking plate from the appropriate PMC slot on the VX 511/06x.
2) Check that the standoffs are attached to the PMC and then align the front of the PMC with the opening in the front panel of the VX 511/06x.
3) Install the PMC, component side down, aligning the PMC connectors with their mating connectors on the VX 511/06x. Press them together so that the friction from the pins holds the PMC in place.
4) Screw the PMC in place using the four mounting screws.

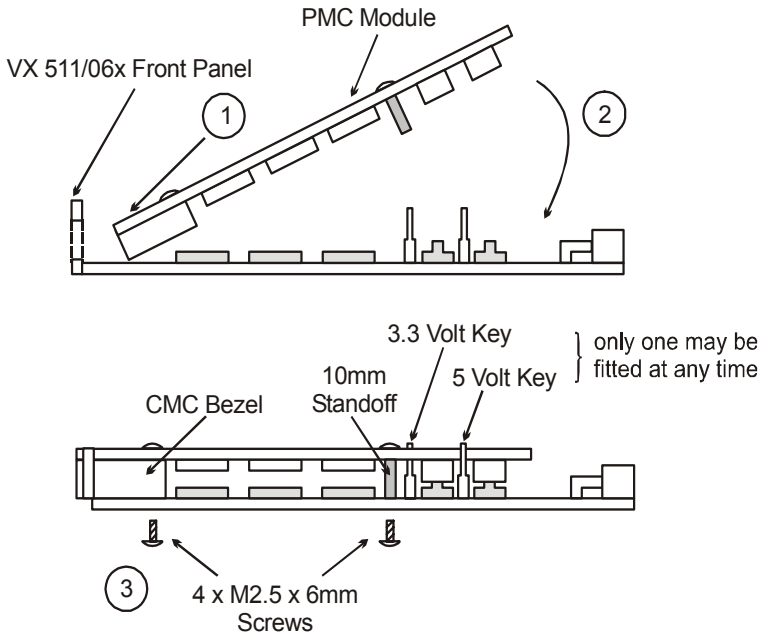


Figure 2-13 PMC/XMC Installation Diagram (except VX 511/06x-RC)

2.9 Installation and Removal (all variants)

Before the board is installed in a VME chassis, check the following points:

When installing a variant of the board which is fitted with a P0 connector into a backplane which does not have the corresponding socket, check to see that no strengthening bars or other tall objects are present on the backplane before inserting the board. If bars or other objects are present then verify that the P0 connector and/or the backplane will not be damaged when the board is fully seated in the slot.

The system Power Supply Unit must have sufficient current capabilities. The board draws current primarily from the +5V rail, and the details are provided in Section A.6. The board can be installed in any standard VME slot. When installed in the first occupied slot the board will become the system controller.

CAUTION: The high supply current requirements of the 2.26 GHz CPU variants of these boards mean that all the available +5V pins on the VME P1 connector must be utilized. It is therefore strongly recommended that this board is installed only in backplanes with 5-row P1 connectors supplying +5V power through all the pins defined in the VME64 specifications. Failure to comply with this recommendation may result in the board malfunctioning or, in extreme cases, board or system damage.

2.9.1 Installation

The board is installed and powered up as follows:

1) Ensure that system power is turned OFF (VCC_STANDBY may be left ON if used).
2) Slide the board into the designated slot, ensuring that the board fits neatly into the runners. For RC variants the wedgelocks may need un-tightening and the handles should be in the closed position.
3) Push the board into the card-cage until the P0, P1 and P2 connectors are firmly located. Use the ejector handles for the final push.
4) Screw the ejector handle retaining bolts into the holes in the chassis, or tighten the wedgelock screws until the board is firmly locked in place.
5) Connect the I/O cables to the connectors on the board's front panel and fix in place with the connectors' retaining screws.
6) If using an RTM, install it at the rear of the backplane and connect the I/O cables.
7) Power-up the system. The following sequence of events should then occur:
    i. The green "RUN" LED and the yellow "POST" LED on the front panel will light.
    ii. The yellow "POST" LED will switch OFF.

If power-up does not follow the sequence described above this will indicate that the board is not operational.

NOTE: This sequence of events assumes the VX 511/06x has Concurrent Technologies standard BIOS firmware and that the board is configured to the factory settings described in Section 2.3.

2.9.2 Removing the Board

To remove the board, shut down the application and operating system software before powering down the system, disconnecting any I/O cables, unscrewing the ejector handle retaining bolts, opening the ejector handles or loosening the wedgelock screws and extracting the board.

CAUTION: The VX 511/06x is not hot swappable. The main system power must be off before attempting to install or remove the board.

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3 SOFTWARE INSTALLATION

In most cases, installing operating system software on the VX 511/06x board follows the same sequence as installing on a PC. However, there are some additional points to note. The sections below summarize the special actions required for a few common operating systems.

3.1 Starting up for the First Time

Many operating systems running on the board will want to use the standard Real Time Clock hardware. To maintain the date and time settings, and several other settings recorded by the PC BIOS, the battery must be fitted (or VCC_STANDBY connected). When the board is first powered up, or at the first power-up after changing the battery, carry out the following steps to set up the board.

1) Fit a battery, if required, as shown in Section 2.5.
2) Make sure that the Console Mode switch is set to the correct state for the console device which will be used (VGA monitor and keyboard, or serial terminal). Most operating systems which install on the target hardware will require a monitor and keyboard during installation, even if they can subsequently be re-configured to use only a serial terminal. See Section 7.1 for details of how to configure the board for this option.
3) Connect any additional modules and peripherals especially any mass storage devices.
4) Connect the console device and power up the board. Wait for the PC BIOS to sign on and run its memory test.
5) When the test finishes, the BIOS may report a setup or date/time setting error. If this occurs, press <**F2**> as soon as possible after the error is reported, and carry out the following:
6) Set the time and date by using the cursor keys to move around the screen and reading the help information in the right-hand screen panel.
7) When the time and date have been set, move the cursor to any other field on the same screen, then press <**F4**> to exit.
8) Press <**y**> to accept the changes and restart.
9) The BIOS will then completely restart and re-run its memory test. This time it should complete and begin bootloading. To proceed with software installation, check that all necessary mass storage devices are connected before continuing with one of the sequences below.

3.2 Bootloading from CD-ROM or Floppy Disk

Operating systems which install on the target hardware will generally install from CD-ROM, or may require both a CD-ROM and floppy disk. Bootloading from floppy disk requires the use of a USB floppy disk drive. To use the floppy disk drive the USB interface must first be enabled in the BIOS. When the board boots and is running the memory test press <**F2**> to enter the BIOS setup.

Enable the USB interface and also select Legacy support. Press <**F4**> to exit and press <**y**> to accept the changes and restart.

To bootload from CD-ROM, use the following procedure:

1) While the BIOS is running its memory test, press <**ESC**>.
2) Wait for the pop-up boot device menu to be displayed.
3) Select the CD-ROM drive using the cursor keys, and then press <**ENTER**>.

3.3 Installing Microsoft® Windows® Operating Systems

Installing these operating systems on the VX 511/06x is generally very similar to installing them on a desktop PC. However, Concurrent Technologies also offers a Board Support Package on CD or DVD (part number CD WIN/BSx-x0) which provides installation and configuration information, including appropriate drivers. Please refer to your supplier for further details or to obtain this package.

SOFTWARE INSTALLATION

3.4 Installing RedHat® Linux®

Installing these operating systems on the VX 511/06x is generally very similar to installing them on a desktop PC. However, Concurrent Technologies also offers a Board Support Package on CD-ROM (CD LNX/BS1-L0) which includes VME bus drivers and additional information. Please refer to your supplier for more details or to obtain this package.

NOTE: If virtualization is to be used, it may be necessary to refer to the Board Support Package for further installation instructions.

4 MASS STORAGE INTERFACES

The VX 511/06x board has four Serial ATA (SATA) interfaces. Two are accessible via the rear P2 connector for connecting mass storage devices. Two are used to support on-board mass storage devices. The first SATA port is converted to EIDE to support an on-board CompactFlash card.

The order in which the PC BIOS firmware bootloads from these drives can be changed via the BIOS Setup screen for Boot.

4.1 Serial ATA Interfaces

The board provides four SATA300 interfaces which support maximum transfer rates of 300 Mbytes/s. Each interface supports connection of a single SATA device.

The BIOS Setup screens for **`Main | SATA Port 1, Main | SATA Port 2, Main | SATA Port 3 and Main | SATA Port 4`** allow the user to see what is connected to these interfaces, and to select some characteristics of the drives manually. Normally the PC BIOS firmware will automatically determine the drive characteristics from the drives themselves.

SATA1 is used to support a CompactFlash card via a SATA to EIDE bridge device. SATA2 is used to support an on-board SATA disk drive. SATA3 and SATA4 are available on the VME P2 connector.

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5 ETHERNET INTERFACES

The VX 511/06x board is fitted with four independent Gigabit Ethernet interfaces, implemented with an Intel 82576EB controller, an Intel 82574L controller, and the Integrated Gigabit LAN on ICH9M-E. The Intel 82576EB is configured as a dual SerDes interface connected to P0 to support VITA 41.6 backplane networking. The other two interfaces are routed to the front panel connectors.

If the system does not support VITA 41.6, the 82576EB can support dual Gigabit Ethernet using an RTM. P0 needs to be fitted on both the base board and the RTM module, and the backplane must have appropriate RJ0 connectors.

By convention in this manual, the front panel Ethernet interfaces are numbered as 1 and 2, and the rear Ethernet interfaces are numbered as 3 and 4. Operating system drivers may renumber these devices to conform to their driver conventions.

It is possible to bootload the board through the Ethernet interfaces by setting appropriate BIOS configuration options. See Section 10.3 for more details.

5.1 Ethernet Channel 2

This Ethernet port is provided directly from ICH9M-E as an integrated Gigabit LAN which supports Intel AMT.

5.2 VITA 41.6 or Rear Panel Ethernet

The Ethernet interfaces available at the P0 connector are configured for Gigabit SerDes only operation. When the board is used with one of the Concurrent Technologies P2/P0 RTMs (see Appendix B), it may be necessary to check and configure switches on that RTM to ensure that the Ethernet connections are routed either only to the P0 connector (VITA 41.6 configuration) or to the rear RJ45 connections (rear panel Ethernet configuration).

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6 VME INTERFACE

The VX 511/06x is fitted with a Tundra Tsi148 PCI-to-VME bus bridge device together with additional support logic. This hardware implements a flexible interface to and from the VME bus with the following key characteristics.

6.1 VME Bus Interface Features

The VX 511/06x can be programmed as a VME master supporting off-board VME memory addressing accessible by any PCI bus master. The VX 511/06x can also be programmed as a VME slave allowing other VME masters to access any PCI bus slave. This access is achieved by programming the appropriate Tsi148 device register. "PCI slave" registers are used for VX 511/06x master accesses and "VME slave" registers for VME accesses to the VX 511/06x.

The VME interface supports A32/A24/A16/MBLT64 addressing modes and D64/D32/D16/D08 (EO) data widths in both user and supervisor address space.

The VME interface performs auto-SysCon detect at power up to provide system controller functionality, if the board is located in the first VME slot. As system controller, the Tsi148 will arbitrate VME mastership of the bus using DEMAND request mode.

The VX 511/06x can act as an interrupt controller for any combination of VME interrupts and can be an interrupter generating either a software interrupt or any of the Tsi148's internal interrupt sources on any IRQ level. All VME interrupts are directly mapped between the Tsi148 registers and the VME bus backplane. Of the PCI INT[A:D] lines, PCI INTA is mapped into the PCI interrupt and PCI INTD is mapped to NMI. PCI INTB and PCI INTC are not used.

The Tsi148 device uses the linear incrementing mode when being accessed by a PCI master. The Tsi148 supports VME mailbox interrupts. See Tsi148 data sheet for further details.

WARNING: VME bus access is allowed to the full VX 511/06x memory map. Care must be taken to ensure that no accesses are made to areas that will corrupt the system memory or the configuration of any of the interfaces.

The PC BIOS firmware fitted to this board includes several setup screens, which allow up to 8 PCI Slave and VME Slave access windows to be configured. The configuration is retained in Flash EPROM and is programmed automatically into the Tsi148 chip when the board starts up. This allows basic access to or from the VME bus to be established without the need to write any operating software for the board, or for the Tsi148 chip. For further details, refer to the BIOS setup screens for the **`Tsi148 | PCI Slave`** and **`Tsi148 | VME Slave`** options.

The VX 511/06x board will assert the VME SYSFAIL signal after a power-on or system reset. In some cases it may be desirable to deactivate this signal early in the boot process, while in others it can be left to the operating software to do this at a later stage. The SYSFAIL signal is controlled by the Tsi148 chip. The PC BIOS provides a user setup option to allow this signal to be deactivated by the BIOS itself during its initialization sequence, or to simply leave it unchanged after the restart. In the latter case, SYSFAIL will remain asserted until the operating software deactivates it. The setup option is provided on the menu for Tsi148.

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7 OTHER INTERFACES

Many additional standard interfaces are provided on the VX 511/06x board. These interfaces consist primarily of those found in a regular desktop or mobile PC, and are outlined below.

7.1 Serial Ports

Two serial interfaces are provided. Serial port COM2 is connected via P2. Serial port COM1 is accessed via a front panel RJ45 connector, and an adapter cable is required to convert to D-type connectors of the appropriate size and gender, such as the CB 232/121-01 or CB 232/121-00.

The serial ports are implemented in the PC chipset used on the board, using standard 16550-style devices. The serial lines may be configured for speeds up to 115kbaud.

7.1.1 PC BIOS Serial Console

With some operating systems, or in some applications, it is preferable to use a serial terminal as an operator console device for the board, in which case it will be necessary to configure the board accordingly. When configured in this mode, the PC BIOS firmware will re-direct its output to a COM port, and similarly will take its input from this port, rather than using the VGA screen and PC keyboard. The Console Mode switch allows selection of this mode, as shown in Figure 7-1.

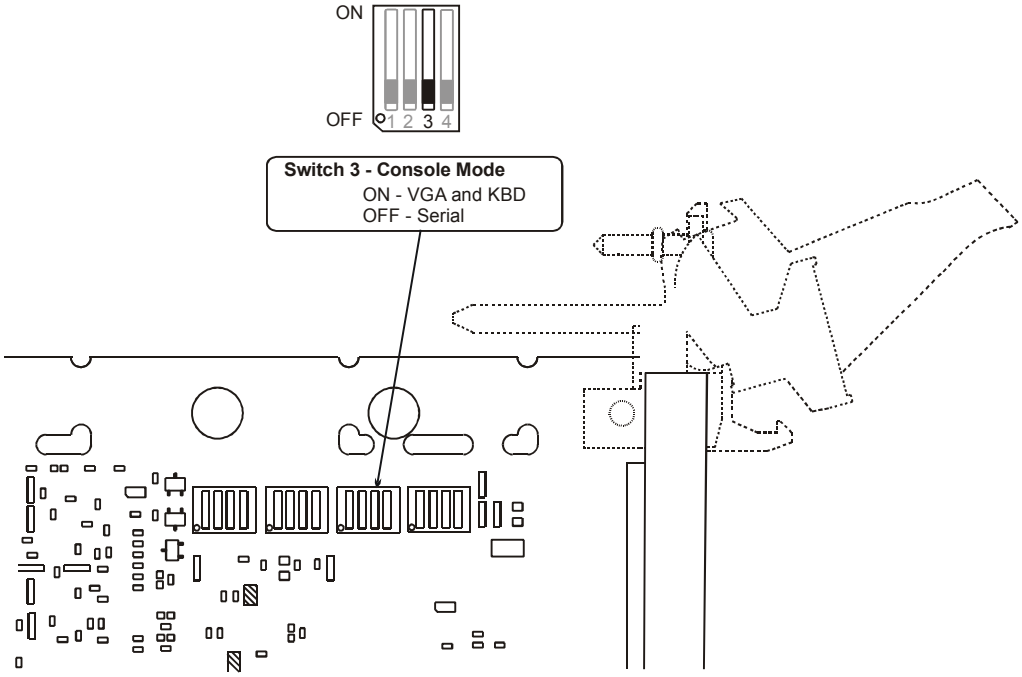


Figure 7-1 Console Mode Switch

The serial line speed used for the Serial Console mode may be selected from the BIOS Setup screen for Main configuration.

7.1.2 PC BIOS Serial Console Port

When the PC BIOS is configured to use a serial port for its console, either COM1 or COM2 can be selected, using the board switch shown in Figure 7-2.

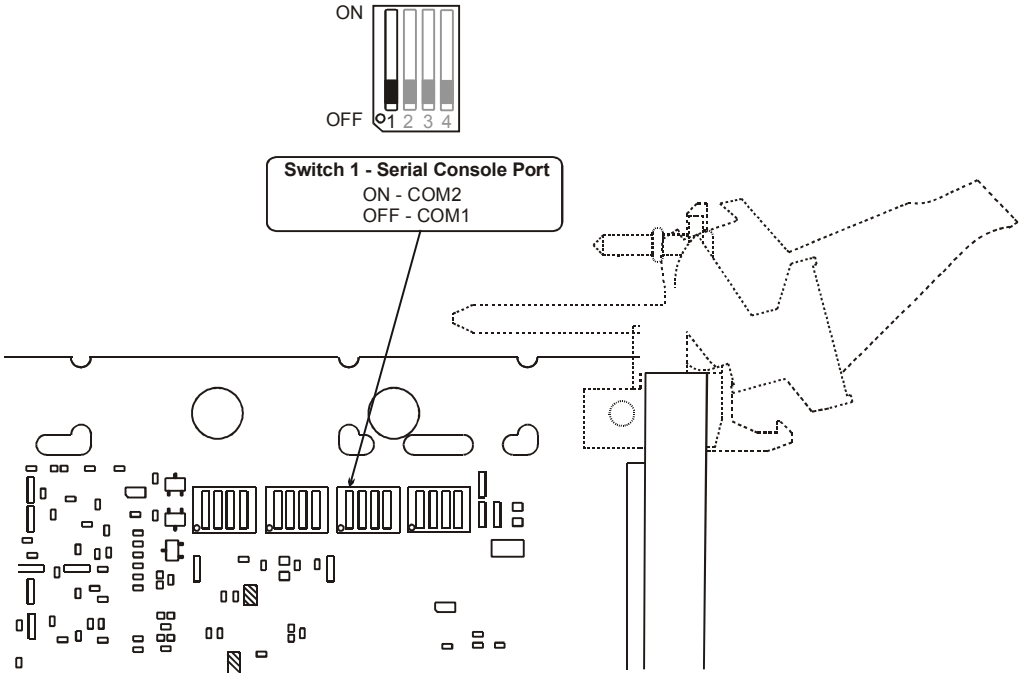


Figure 7-2 Serial Console Port Select Switch

7.2 Keyboard and Mouse Ports

The keyboard and mouse connections are available via P2. This front panel connector also provides a USB interface, which may be used to connect a USB keyboard or mouse.

Power for the keyboard and mouse interfaces is protected by a self-resetting current limiting circuit. To reset this circuit power the board off, remove and replace the faulty keyboard or mouse device, then power up again.

NOTE: External devices that derive power from the keyboard/mouse interface may be used provided that the total current taken by all devices is less than 500mA.

7.3 Graphics (VGA) Controller

The VX 511/06x board contains a graphics controller within the GS45 GMCH. This device uses main memory for graphics RAM and supports many different modes of operation including VGA and SVGA, with resolutions up to 2048x 1536 and color depths up to 24 bits (16 million colors). It also provides both 2D and 3D acceleration. The analog CRT interface from the GS45 is routed to the P2 connector. The digital flat panel interfaces of the GS45 are not used on this board.

See also Section 7.1 for information about how to switch the PC BIOS console device between VGA screen and keyboard, and a serial port.

7.4 Real Time Clock

A conventional PC Real Time Clock is included on this board, and it can be powered by an on-board Lithium battery when main power to the board is removed. See Section 2.5 for more details of how to fit or replace the battery. The clock device also provides 242 bytes of CMOS RAM, in which the PC BIOS keeps much of its setup screen data and other information. To allow for the case where no battery supply is present, the BIOS Setup data can be saved in Flash EPROM and restored as default values when the BIOS runs again at power-up or after reset. See Section 10.5 for further details.

Alternatively the CMOS settings and Real-Time clock can be maintained in the absence of power by connecting a 5V source to the VMEbus VCC_STANDBY input.

7.5 Universal Serial Bus (USB)

Three USB 2.0 interfaces are provided on this board. Two channels are routed to P2, and the third is available at the front panel connector. All three channels can operate at 1.5, 12 or 480 Mbits/s. The PC BIOS firmware supports bootloading via all of these ports.

7.6 Power On Self Test LED/Speaker

The Power On Self Test (POST) LED is connected to the PC Speaker port.

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8 FLASH EPROM AND SDRAM

8.1 Flash EPROM

The VX 511/06x is fitted with one Flash EPROM part, namely a 32 Mbit SPI Flash device. This device is soldered to the board and is programmed at the factory with PC BIOS and factory test firmware. This EPROM will not normally be reprogrammed by the user, but Concurrent Technologies has programming software which allows BIOS updates to be carried out in the field when necessary, perhaps to add new features. Contact Concurrent Technologies for a copy of this software, and for the BIOS reprogramming information, if you believe that such an update is required.

Also programmed into the SPI Flash at the factory is a Recovery BIOS, which allows the board to be restarted in a basic functional mode even if the main BIOS firmware has been corrupted. See Section 10.7 for further details of this feature.

The internal Gigabit Ethernet will also use this SPI flash to store MAC addresses as well as EEPROM contents.

8.2 SDRAM

The VX 511/06x board supports a large amount of DDR3-1066 SDRAM. Soldered memory on board supports up to 6 Gbytes capacity. When more than 4 Gbytes is fitted some memory space may be lost due to memory mapped resources, for example PCIe Extended Configuration address space. Some operating systems can re-map the memory address space to overcome this restriction.

The SDRAM can be accessed from the processor, the local PCI bus, PCIe links and the VME backplane.

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9 ADDITIONAL LOCAL I/O FUNCTIONS

The VX 511/06x supports a variety of I/O functions whose addresses are summarized in Table 9-1.

I/O Address Range	Description
0000-001Fh	DMA Controller (ICH9M-E)
0020-002Dh	Interrupt Controller (ICH9M-E)
002E-002Fh	Configuration Index & Data Registers (SuperI/O)
0030-003Dh	Interrupt Controller (ICH9M-E)
0040-0043h	PIT Timers (ICH9M-E)
0050-0053h	PIT Timers (ICH9M-E)
0060h	Keyboard Controller (SuperI/O)
0061h	NMI Status (ICH9M-E)
0064h	Keyboard Controller (SuperI/O)
0070h	NMI Enable/RTC Address (ICH9M-E)
0071h	RTC Data (ICH9M-E)
0080h	Port 80 Debug Port
0092h	Port 92 Reset Generator (ICH9M-E)
00A0-00A1h	Slave Interrupt Controller (ICH9M-E)
00C0-00DFh	Slave DMA Controller (ICH9M-E)
00F0h	Maths Coprocessor Error
0210-021Fh	Control & Status Registers, Long Duration Timer (CPLDs)
02F8-02FFh	COM2 Serial (Super I/O)
03BC-03BFh	Parallel Port LPT1 (SuperI/O) (Not Used)
03F0-03F7h	Floppy Controller (SuperI/O) (Not Used)
03F8-03FFh	COM1 Serial (SuperI/O)
04D0-04D1h	Interrupt Control (ICH9M-E)
0CF8-0CFFh	PCI Configuration Registers (GS45)
0D00-FFFFh	PCI Free I/O Space

Table 9-1 I/O Address Map

Most of the addresses are standard PC-AT compatible values, but addresses **0210-021Fh** provide custom Status & Control registers for board specific features.

ADDITIONAL LOCAL I/O FUNCTIONS

9.1 Onboard Status & Control Registers

There are 12 byte wide status and control registers. They are accessed directly via the chipset's X-Bus at the following addresses:

- **0210h** for Status & Control Register 0.
- **0211h** for Status & Control Register 1.
- **0212h** for Status & Control Register 2.
- **0213h** for Watchdog Status & Control Register.
- **0214h** for Status & Control Register 3.
- **0218h** for Long Duration Timer LS byte.
- **0219h** for Long Duration Timer Mid Low byte.
- **021Ah** for Long Duration Timer Mid High byte.
- **021Bh** for Long Duration Timer MS byte.
- **021Ch** for Long Duration Timer Status & Control Register.
- **021Eh** for ACPI PM1 Control Register Low Byte.
- **021Fh** for ACPI PM1 Control Register High Byte.

9.2 Status & Control Register 0

This register is at I/O address **0210h**.

7	6	5	4	3	2	1	0
REV 2	**REV 1**	**REV 0**	**RTM DETECT**	**CONSOLE PORT**	**CONSOLE SWITCH**	**USER SWITCH**	**MODE SWITCH**
RO	RO	RO	RO	RO	RO	RO	RO

Bit 0: Mode switch
Used to define the operating mode following a reset. See Section 10.3.

0 = BIOS operation
1 = VSA operation

Bit 1: User switch
Available for user defined purposes in BIOS mode. See Figure 9-1 for the switch settings. In VSA mode this switch selects between MTH and Soak operation during factory testing.

0 = MTH
1 = Soak

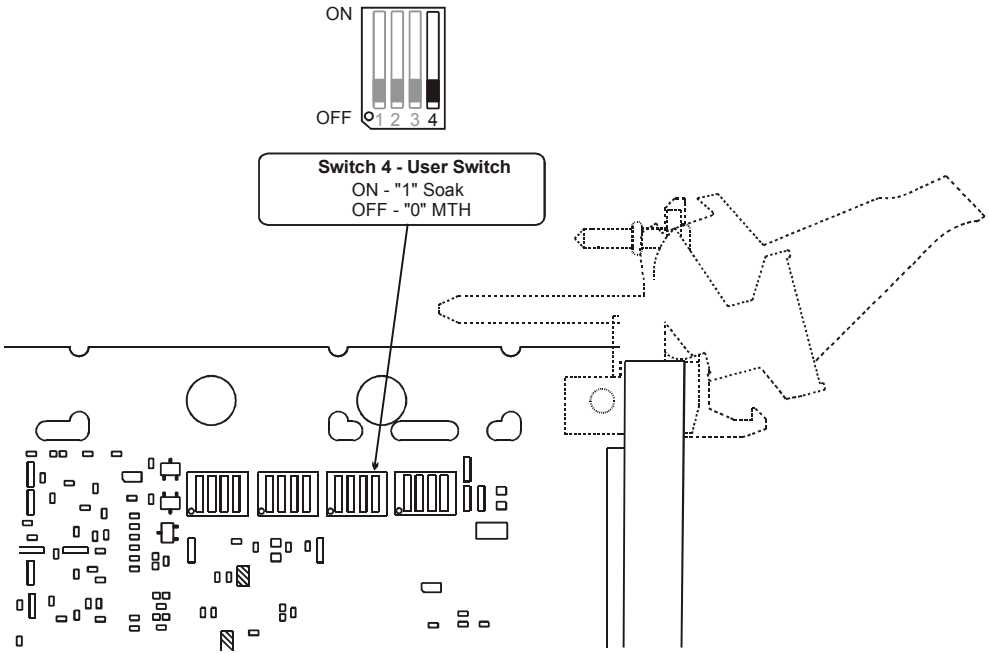


Figure 9-1 User Switch

Bit 2: Console switch
Used to define the BIOS default standard input/output mode. See Section 7.1.1.

0 = input/output via serial port
1 = input via keyboard/output via VGA adapter.

Bit 3: Serial console port switch
Used to select which serial port is used for the serial console. See Section 7.1.2.

0 = COM1 (Front Panel)
1 = COM2 (P2).

Bit 4: RTM detect

Used to detect the RTM connected to P2.

0 = RTM not connected
1 = RTM present.

Bits 7-5: Hardware revision strapping

000 = Rev A
001 = Rev B etc…

9.3 Status & Control Register 1

This register is at I/O address **0211h**.

7	6	5	4	3	2	1	0
PMC1 HIGH SPEED	**PMC1 SPD1**	**PMC1 SPD0**	**PCIE SW FERR**	**XMC FITTED**	**PMC/XMC INIT COMP**	**PMC2 MODULE PRESENT**	**PMC1 MODULE PRESENT**
RO	R/W1	R/W1	RO	RO	RO	RO	RO

Bit 0: PMC1 module present

This bit indicates whether or not a PMC1 module is present on the board in PMC site 1.

0 = PMC module not present
1 = PMC module present.

Bit 1: PMC2 module present

This bit indicates whether or not a PMC2 module is present on the board in PMC site 2.

0 = PMC module not present
1 = PMC module present.

Bit 2: PMC/XMC initialization complete

1 = PMC/ XMC module ready for enumeration
0 = PMC/ XMC module not ready for enumeration.

Bit 3: XMC fitted

Used to report the presence of an XMC module.

0 = not present
1 = present.

Bit 4: PEX8624 switch fatal error status

Used to report Fatal Error Status from the PEX8624 PCIe switch.

0 = fatal error not detected
1 = fatal error detected.

Bits 6-5: PMC site 1 PCI bus mode & frequency

These bits are written by the BIOS after the bus mode and frequency has been determined. Bit 7 of this register determines whether the lower (0) or higher (1) frequency applies.

00 = PCI 25 or 33 MHz
01 = PCI 50 or 66 MHz
10 = PCI-X 50 or 66 MHz
11 = PCI-X 100 or 133 MHz

Bit 7: PMC site 1 high bus frequency

Used in conjunction with bits 6 & 5 to determine the bus speed for PMC1.

0 = lower speed
1 = higher speed.

9.4 Status & Control Register 2

This register is at I/O address **0212h**.

7	6	5	4	3	2	1	0
FP_NMI	**TSI_NMI**	**ICH_NMI**	**BDFAIL**	**VME RESET INTERRPT ENABLE**	**PB RESET ENABLE**	**RFU**	**RFU**
RC	RO	RO	RO	RW	RW	RO	RO

Bits 1-0: Reserved

Bit 2: Push Button reset enable

This bit determines whether RTM or on board push button reset can cause board reset (or NMI). See Section 2.4.8.

0 = Push Button disabled
1 = Push Button enabled

Bit 3: VME reset input enable

This bit determines whether VME backplane reset can cause a board reset. It is ignored if the board is in the System Controller slot. See Section 2.4.8.

0 = disable VME backplane reset
1 = enable VME backplane reset

Bit 4: BDFAIL value

This bit provides a value of a pulled up signal driven by the TSI148 device.

0 = value read
1 = value read.

Bit 5: ICH_NMI from the ICH9M is the cause of NMI

This bit is set by the ICH9M and should be cleared by writing to the appropriate ICH9M register.

0 = ICH_NMI has occurred
1 = ICH_NMI has not occurred.

Bit 6: TSI_NMI signal from the PCI-to-VME Bridge is the cause of NMI

This bit is set by the TSI148 and should be cleared by writing to the appropriate TSI148 register.

0 = TSI_NMI has occurred
1 = TSI_NMI has not occurred

Bit 7: Front panel switch is the cause of NMI

0 = event has not occurred
1 = event has occurred

9.5 Status & Control Register 3

This register is at I/O address **0214h**.

7	6	5	4	3	2	1	0
USER LED MODE	**USER LED**	**GPIO 1 DIR**	**GPIO 0 DIR**	**RFU**	**RFU**	**GPIO 1 DATA**	**GPIO 0 DATA**
RO	RW	RW	RW	RO	RO	RW	RW

Bits 1-0: GPIO data

Data written to these bits will be output on the GPIO pins when the direction is set for output. Reads of these bits will read the data present on the GPIO pins. If the direction is set for input and no external device is connected to the pin then the data will read as a one. There are switches on GPIO1 & 0 to enable them to be used as software option inputs.

See also Section 9.10 regarding the Extended General Purpose Inputs supported by selected RTMs.

Bits 3-2: Reserved

Reads as 0

Bits 5-4: GPIO direction

These bits set the data direction for the GPIO pins.

0 = pin is an input
1 = pin is an output

Bit 6: User LED

Used to activate or get the status of the User LED; is write enabled when bit 7 is 1.

0 = the LED is OFF
1 = the LED is ON

Bit 7: User LED Mode switch

Used to select the function of the USER LED. See Section 11.2.5.

0 = Processor Hot Mode
1 = User Mode

9.6 APCI Control Registers

Two 8-bit registers are supported for use by APCI power management functions. Their dedicated function is beyond the scope of this manual, but the outlines of both registers are shown below.

9.6.1 ACPI PM1 Control Register Low Byte

This register is at I/O address **021Eh**. It provides a minimal power management interface. Refer to the ACPI Specification document for further details.

7	6	5	4	3	2	1	0
RESERVED FOR ACPI					**GBL_RLS**	**BM_RLD**	**SCI_EN**
RW	RW	RW	RW	RW	RO	RO	RO

Bit 0: SCI_EN
This bit is fixed at 0.

Bit 1: BM_RLD
This bit is fixed at 0.

Bit 2: GBL_RLS
This bit is fixed at 0.

Bits 7-3: Reserved for use by ACPI driver

9.6.2 ACPI PM1 Control Register High Byte

This register is at I/O address **021Fh**. It provides a minimal power management interface. Refer to the ACPI Specification document for further details.

7	6	5	4	3	2	1	0
RESERVED FOR APCI		**SLP_EN**	**SLP_TYPx**			**IGNORE**	**ACPI RSVD**
RO	RO	RW	RW			RO	RW

Bit 0: Reserved for use by ACPI driver

Bit 1: Ignored by ACPI software
This bit is fixed at 0.

Bits 4-2: Sleep type

Bit 5: Sleep enable
Write 1 to this bit to assert SMI.

Bits 7-6: Reserved in ACPI specification
These bits are fixed at 0.

9.7 Watchdog Timer

The VX 511/06x board includes a hardware Watchdog timer which can be used by the operating software to monitor the normal operation of the system. The timer is enabled by a board switch (see Figure 9-2) and controlled by software. Once enabled it must be restarted at regular intervals. If it is not restarted for a period of approximately 1 second, the timer will expire and cause a Non-Maskable Interrupt or reset to the local processor.

The watchdog timer facility is provided by a Maxim MAX705 power-on reset supervisor chip and additional hardware. Details of how it is used are provided in the following sections, starting with a description of the I/O register provided for this purpose.

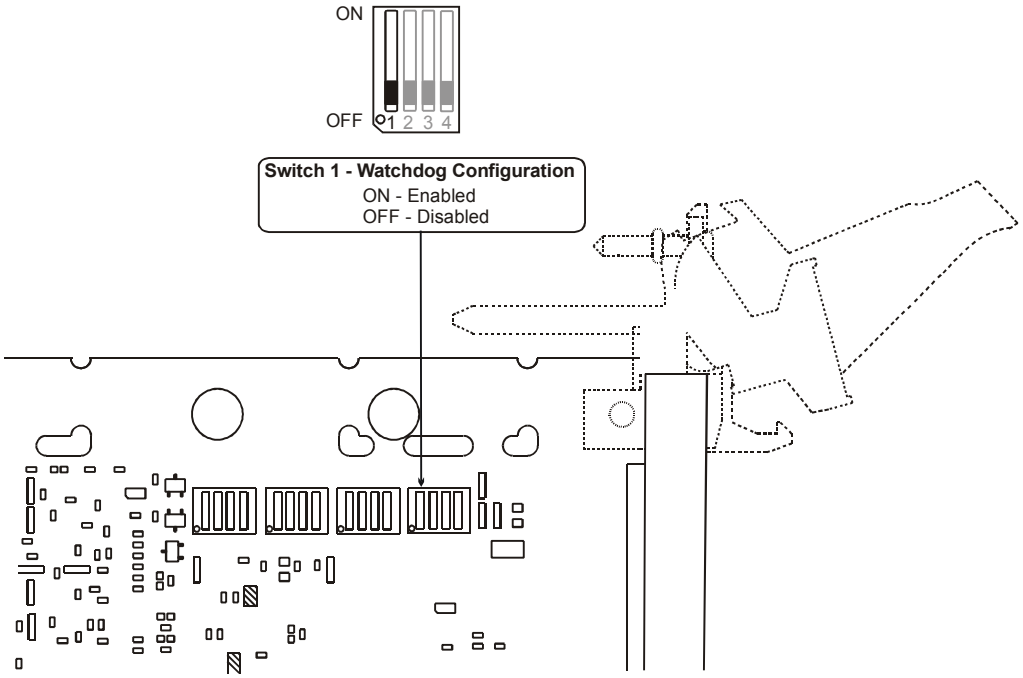


Figure 9-2 Watchdog Configuration Switch

9.7.1 Watchdog Status & Control Register

This register is at I/O address **0213h**.

7	6	5	4	3	2	1	0
RFU	**SYS. RESET ENABLE**	**S/W ENABLE**	**ENABLE LINK**	**STATUS RESET**	**NMI/RESET**	**PAT (1)**	**PAT (2)**
RW	RW	RW	RO	RO	RW	RW	RW

Bits 1-0: Watchdog 'PAT' bits
Refer to the following description on how to use the watchdog (Sections 9.7.2 to 9.7.4)

Bit 2: Select Watchdog action
This bit selects the following actions when the watchdog times out:

0 = generate an NMI (default)
1 = generate a board or system reset

Bit 3: Watchdog status
This bit can be used to determine if the watchdog was the source of an NMI or reset. A valid watchdog restart will set this bit to 'watchdog OK' if the watchdog had previously timed out.

0 = watchdog OK (default)
1 = watchdog timed out

Bit 4: Watchdog enable switch status
0 = watchdog is under software control
1 = watchdog disabled in hardware

Bit 5: Watchdog software enable
0 = watchdog disabled (default)
1 = watchdog enabled

Bit 6: Watchdog system reset enable
0 = local reset only (default)
1 = local and system reset.

Watchdog action (Bit 2) must be set to '1' for this bit to have any effect. If both bits 6 and 2 are set to 1 and the watchdog timer expires, and the board is acting as system controller, the VMEbus SYSRESET# will be activated depending on the setting of the VME System Reset Enable switch (see Section 2.4.8).

Bit 7: Reserved
Reads as 0.

9.7.2 Enabling and Disabling the Watchdog Timer

The watchdog circuitry contains features to safeguard against accidental use through faulty or unintended software actions. To enable the watchdog the following sequence of events needs to be performed.

1) Read the Watchdog Status & Control register. Check the status of the watchdog enable switch (bit 4). If it reads 'low' then proceed to step 2. If it reads 'high' then the watchdog cannot be enabled in software.
2) Set bits 1 & 0 to the complement of each other (i.e. 0,1 or 1,0) and at the same time set bit 5 'high'.
3) Write the new value back.
4) Complement bits 1 & 0. Write the new value to the Watchdog Status & Control register.
5) Repeat step 4.

Once the watchdog has been enabled, it can be disabled by repeating the above procedure with bit 5 set 'low'.

9.7.3 Using the Watchdog Timer

Once enabled, the watchdog timer must be restarted at regular intervals to prevent it expiring. The maximum interval is pre-set to 1 second. This is a function of the watchdog chip and cannot be changed. If the watchdog timer is not restarted within this time it will time out and cause a reset or NMI depending on the state of bit 2 of the Watchdog Status & Control register. To restart the watchdog the complement of the lower two bits needs to be written into the Watchdog Status & Control register. These two bits must also be the complement of each other i.e. 0,1 or 1,0. Writing any other value or the same value will not restart the watchdog. If the watchdog time-out is configured to generate a board reset and a time-out occurs the watchdog circuit will also be reset. The watchdog must be enabled to be re-enabled after a reset has occurred. This has been done to allow operating systems software to boot after a reset without having to keep the watchdog from timing out during this period. The watchdog status bit will not be cleared; this must to be done by enabling and restarting the watchdog. The reason for this is to preserve the status of the watchdog timeout to allow software to determine the source of an NMI or if a reset was caused by the watchdog.

NOTE: Once an erroneous value has been written into the watchdog register it will take two further writes using the correct values to restart the watchdog again. Therefore, when changing any bit in the register whilst the watchdog is enabled, bits 1 & 0 should be complemented.

NOTE: The actual time-out of the watchdog chip can vary between 1s and 2.25s. To guarantee correct operation on all boards the restart interval should be less than 1s.

9.7.4 Programming the Watchdog Timer

The following functions show how to use the watchdog facility available through the Status and Control registers.

It is worth noting that the Software Enable bit in the Watchdog Status and Control register does not read back the value last written; it is the output from the error checking logic, so it will not read back as enabled until two watchdog restarts have been performed (equally it will not display disabled until two further restarts have been performed).

```
/* Status and control registers */

#define STATCTL_BASE        0x0210

#define WATCHDOG_STATCTL    (STATCTL_BASE + 4)
#define     WD_PAT_MASK         0x03
#define     WD_PAT_1            0x02
#define     WD_PAT_2            0x01
#define     WD_ACTION_MASK      0x04
#define     WD_ACTION_NMI       0x00
#define     WD_ACTION_RST       0x04
#define     WD_STATUS           0x08
#define     WD_HW_DISABLE       0x10
#define     WD_SW_ENABLE        0x20


/*****************************************************************************
 * vEnableWatchdog: configure the watchdog for NMI or RESET on timeout
 *
 * RETURNS: none
 */

void vEnableWatchdog
(
    UINT8   bTimeoutAction  /* action on timeout: NMI or Reset */
)
{
    UINT8   bTemp;


    bTemp = inbyte (WATCHDOG_STATCTL);

    bTemp &= ~WD_ACTION_MASK;   /* set watchdog timeout action */
    bTemp |= bTimeoutAction;

    bTemp |= WD_SW_ENABLE;      /* software enable of watchdog */
    bTemp &= ~WD_PAT_MASK;      /* clear the pat bits */

    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_1);   /* set and pat twice */
    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_2);
    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_1);

} /* vEnableWatchdog () */


/*****************************************************************************
 * vDisableWatchdog: de-configure the watchdog and disable
 *
 * RETURNS: none
 */

void vDisableWatchdog (void)
{
    UINT8   bTemp;
    bTemp = inbyte (WATCHDOG_STATCTL);

    bTemp &= ~WD_ACTION_MASK;       /* set watchdog action to NMI */
    bTemp |= WD_ACTION_NMI;
```

```
    bTemp &= ~WD_SW_ENABLE;         /* software disable the watchdog */

    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_1);   /* set and pat twice */
    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_2);
    outbyte (WATCHDOG_STATCTL, bTemp | WD_PAT_1);

} /* vDisableWatchdog () */


/*****************************************************************************
 * vRestartWatchdog: restart the watchdog to prevent timeout
 *
 * Bits 1:0 of the Watchdog status / control register are inverted before
 * writing back.
 *
 * RETURNS: none
 */

void vRestartWatchdog (void)
{
    UINT8   bTemp;
    UINT8   bPat;

    bTemp = inbyte (WATCHDOG_STATCTL);

    bPat = (~bTemp) & WD_PAT_MASK;  /* get complement of bits 1:0 */
    bTemp &= ~WD_PAT_MASK;          /* clear the bits 1:0 in data */
    bTemp |= bPat;                  /* set new bits */

    outbyte  (WATCHDOG_STATCTL, bTemp);

} /* vRestartWatchdog () */
```

9.8 Long Duration Timer / Periodic Interrupt Timer

The Long Duration Timer (LDT) consists of a 32-bit free running counter with a 32-bit holding register and a status & control register. It may be used by user software to timestamp events to a resolution of 1 microsecond. The counter bytes are laid out in little-endian format to permit multi-byte read/write operations. The status & control register controls the operation of the LDT. A 32-bit holding register is provided to ensure stable count values are read. Read operations return the holding register byte values. A read operation on the low byte of the counter causes the count value to be transferred to the holding register. Hence, the low byte should be read first to ensure a stable count value.

The counter may be preset by writing to the registers. The counter bytes may be written independently. The counter should be stopped before writing to it or the outcome may be indeterminate. The counter registers are cleared at power-on, but not by subsequent reset operations. If necessary, the LDT can be cleared by writing zero to all four counter bytes. An interrupt may be generated when the counter rolls over (from FFFFFFFFh to zero). This occurs approximately every 72 minutes (1 MHz clock).

The LDT doubles as a simple Periodic Interrupt Timer (PIT). It offers 7 fixed interrupt rates, namely: 100, 200, 500, 1,000, 2,000, 5,000 and 10,000 Hz (1 MHz clock). The mode / interrupt rate is set by three bits in the LDT status & control register.

NOTE: If the LDT clock frequency is not 1 MHz (i.e. HF Clock = 4 MHz), the above rates should be scaled accordingly.

In PIT mode, the counter counts up to a pre-determined maximum value and then goes back to zero. To ensure a full first interval, the low and mid-low bytes of the counter should be cleared before the counter is started.

9.8.1 Long Duration Timer / Periodic Interrupt Timer Low Byte

This register is at I/O address **0218h**.

7	6	5	4	3	2	1	0
LDT7	**LDT6**	**LDT5**	**LDT4**	**LDT3**	**LDT2**	**LDT1**	**LDT0**
RW	RW	RW	RW	RW	RW	RW	RW

Bits 7-0: Low byte of LDT / PIT

Reading this register causes the current value of the LDT to be transferred to a holding register. This allows a stable 4 byte count to be read. The low byte of the holding register is returned by the read.

Writing to this register loads a value into the low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.8.2 Long Duration Timer / Periodic Interrupt Timer Mid-low Byte

This register is at I/O address **0219h**.

7	6	5	4	3	2	1	0
LDT15	**LDT14**	**LDT13**	**LDT12**	**LDT11**	**LDT10**	**LDT9**	**LDT8**
RW	RW	RW	RW	RW	RW	RW	RW

Bits 7-0: Mid-low byte of LDT / PIT

Reading this register returns the mid-low byte of the holding register. Writing to this register loads a value into the mid-low byte of the LDT / PIT counter. The counter should be stopped when writing or the result will be indeterminate.

9.8.3 Long Duration Timer / Periodic Interrupt Timer Mid-high Byte

This register is at I/O address **021Ah**.

7	6	5	4	3	2	1	0
LDT23	**LDT22**	**LDT21**	**LDT20**	**LDT19**	**LDT18**	**LDT17**	**LDT16**
RW	RW	RW	RW	RW	RW	RW	RW

Bits 7-0: Mid-high byte of LDT

Reading this register returns the mid-high byte of the holding register. Writing to this register loads a value into the mid-high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.8.4 Long Duration Timer / Periodic Interrupt Timer High Byte

This register is at I/O address **021Bh**.

7	6	5	4	3	2	1	0
LDT31	**LDT30**	**LDT29**	**LDT28**	**LDT27**	**LDT26**	**LDT25**	**LDT24**
RW	RW	RW	RW	RW	RW	RW	RW

Bits 7-0: High byte of LDT

Reading this register returns the high byte of the holding register. Writing to this register loads a value into the high byte of the LDT counter. The counter should be stopped when writing or the result will be indeterminate.

9.8.5 LDT / PIT Status & Control Register

This register is at I/O address **021Ch** and it controls the operation of the LDT.

The LDT clock signal is obtained from the SuperI/O controller HF Clock output. The HF Clock is derived from an internal 48 MHz signal. A programmable divider within the SuperI/O controller gives a choice of HF Clock frequencies. The HF Clock frequency is further divided by 4 or 128 before being fed to the LDT clock input. The following clock frequencies are available:

HF Clock / 4: 12 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, 1.5 MHz, 1 MHz, 750 kHz.
HF Clock / 128: 375 kHz, 187.5 kHz, 125 kHz, 93.75 kHz, 62.5 kHz, 46.875 kHz, 31.25 kHz, 23.4375 kHz

NOTE: The BIOS will configure the SuperI/O and LDT for a 1 MHz clock frequency.

7	6	5	4	3	2	1	0
RFU	**RFU**	**CLOCK SELECT**	**INTERRUPT FLAG**	**MODE 2**	**MODE 1**	**MODE 0**	**RUN**
RO	RO	RW	RC	RO	RW	RO	RW

Bit 0: LDT / PIT run

This bit controls whether the LDT / PIT runs or is stopped.

0 = stop (default)
1 = run

Bits 3-1: LDT / PIT mode

These bits set the mode of the timer as follows:

0 0 0 = LDT
0 0 1 = PIT 100 Hz
0 1 0 = PIT 200 Hz
0 1 1 = PIT 500 Hz
1 0 0 = PIT 1,000 Hz
1 0 1 = PIT 2,000 Hz
1 1 0 = PIT 5,000 Hz
1 1 1 = PIT 10,000 Hz

NOTE: The above PIT rates require LDT CSR bit 5 = 0 and the HF Clock output from the SuperI/O controller to be 4 MHz. This results in an LDT clock frequency of 1 MHz.

Bit 4: LDT / PIT interrupt flag

The interrupt flag is active whenever the timer is running. It is set if the LDT RUN bit is set AND either the LDT rolls over or the PIT interval expires. It can be cleared by writing to the register with a 0 in its bit position. This should be done in the LDT / PIT interrupt service routine.

0 = LDT / PIT interrupt has not occurred
1 = LDT / PIT interrupt has occurred

Bit 5: LDT / PIT clock source

This bit selects the clock source for the LDT / PIT as follows:

0 = SuperI/O HF Clock / 4 (1 MHz)
1 = SuperI/O HF Clock / 128 (31.25kHz)

Bits 7-6: Reserved

Set to 0.

9.8.6 Programming the LDT/PIT

The following code fragments illustrate how the system software, by using the on-board hardware, can create accurate time delays and measure elapsed times, accurate to 1µs, irrespective of the CPU's operating frequency.

The LDT and PIT control registers and operational modes are defined thus:

```
#define TIMER_BYTE_0            (0x0218U)
#define TIMER_BYTE_1            (0x0219U)
#define TIMER_BYTE_2            (0x021AU)
#define TIMER_BYTE_3            (0x021BU)
#define CONTROL_STATUS          (0x021CU)

#define INTERRUPT_MASK          (0x10U)
#define INTERRUPT_ENABLE        (0x10U)
#define INTERRUPT_DISABLE       (0x00U)
#define INTERRUPT_SET           (0x10U)
#define INTERRUPT_RESET         (0x00U)

#define TIMER_ROLLOVER          (0x10U)

#define MODE_MASK               (0x0EU)
#define MODE_PIT_10000Hz        (0x0EU)
#define MODE_PIT_5000Hz         (0x0CU)
#define MODE_PIT_2000Hz         (0x0AU)
#define MODE_PIT_1000Hz         (0x08U)
#define MODE_PIT_500Hz          (0x06U)
#define MODE_PIT_200Hz          (0x04U)
#define MODE_PIT_100Hz          (0x02U)
#define MODE_LDT                (0x00U)

#define MODE_RUN_MASK           (0x01U)
#define MODE_RUN_GO             (0x01U)
#define MODE_RUN_STOP           (0x00U)
```

The following code fragment illustrates how a simple delay of 10ms is implemented.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);

/* wait until the PIT rolls over ... */

while (inbyte (CONTROL_STATUS) & TIMER_ROLLOVER) == 0)
    ; /* do nothing ... */

/* reset the PIT "rollover" flag ... */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

It is possible to implement delays of 5ms, 2ms, 1ms, 500µs, 200µs and 100µs by utilizing other PIT modes.

The PIT can generate an interrupt whenever the PIT rolls over. The system programmer must initialize the interrupt vector, enable PIC interrupts, etc. The following code fragment shows the basic interrupt handling function.

```
static volatile signed long int dCounter;

#pragma interrupt (vInterruptHandler)
static void far vInterruptHandler (void)
{
    /*
     * clear the source of the interrupt by resetting the rollover
     * flag, thus:
     */

    outbyte (CONTROL_STATUS, inbyte (CONTROL_STATUS) & ~INTERRUPT_MASK);

    /*
     * perform the relevant actions to acknowledge the interrupt
     * in the PIC, etc ...
     */

    dCounter--;
}
```

The following code fragment used in conjunction with the previous code fragment illustrates another method of implementing a timed delay. The `dCounter` variable is declared to be volatile which prevents any C compilers, which conform to the ANSI standard, from optimizing accesses to the `dCounter` variable.

```
outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_PIT_100Hz | MODE_RUN_GO);
dCounter = 500;   /* 500 * (1 / 100) == 5 seconds */

/*
 * install the interrupt for the PIT counter, modify the
 * PIC settings, etc. and ensure interrupts are enabled.
 */

while (dCounter > 0)
    ; /* do nothing ... */

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
```

The following code fragment uses the LDT to measure the elapsed time to a resolution of 1ms. In this example, the LDT is zeroed at the start of the test and so there is no need to subtract the LDT's initial value from its final value.

```
static UINT32 dElapsedTime;

outbyte (CONTROL_STATUS, MODE_RUN_STOP);
outbyte (TIMER_BYTE_0, 0);
outbyte (TIMER_BYTE_1, 0);
outbyte (TIMER_BYTE_2, 0);
outbyte (TIMER_BYTE_3, 0);
outbyte (CONTROL_STATUS, MODE_LDT | MODE_RUN_GO);

/*
 * perform action to be timed ...
 */
outbyte (CONTROL_STATUS, MODE_STOP);
dElapsedTime  =  (UINT32) inbyte (TIMER_BYTE_0);
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_1)) << 8;
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_2)) << 16;
dElapsedTime |= ((UINT32) inbyte (TIMER_BYTE_3)) << 24;
printf ("Elapsed time = %u.%06u seconds\n",
         dElapsedTime / 1000000U, dElapsedTime % 1000000U);
```

The TIMER_BYTE_0, TIMER_BYTE_1, TIMER_BYTE_2 and TIMER_BYTE_3 control registers are at successive addresses and form a 32-bit register in "little endian" format. It is possible to read and write the timer's value in a single 32-bit I/O operation. For example, to read the timer's value, the following C statement suffices.

```
dCounterValue = inlong (TIMER_BYTE_0);
```

9.9 POST LED / Speaker

The POST LED is controlled via the speaker port. The POST LED replaces a PC speaker and is programmed in the same way a speaker would be programmed. The board also outputs the speaker port via a high current open collector driver on the P2 connector for connection to an external speaker if required.

9.10 Extended GP Inputs

The VX511/06x board itself supports two GPIO signals, either of which can be an input or an output, and are controlled via Status and Control Register 3 (see Section 9.5). These two signals are accessible directly on all the available RTMs via pin headers. On the AD VP2/024 or similar RTMs, the same two GPIO pins can also be used as I²C data and clock pins (GPIO0 and GPIO1 respectively). This I²C port is connected to a PCA8574 I/O expander module which takes input from the 8 GP input signals set by DIP switches.

The I/O expander has I²C address 20h and supports two 8-bit registers: an output mode register, and an input status register which reports the GP input switch status. Standard I²C write and read commands are used to access these registers. The output mode register is used simply to set the operating mode of the I/O expander, so need only be written once with a value of 0FFh. Subsequently a single I²C read command should be issued. This puts the I/O expander into a mode where all subsequent 8-bit I²C transfers return the state of the GP input switches. The state of all 8 pins is latched on the I²C acknowledge bit.

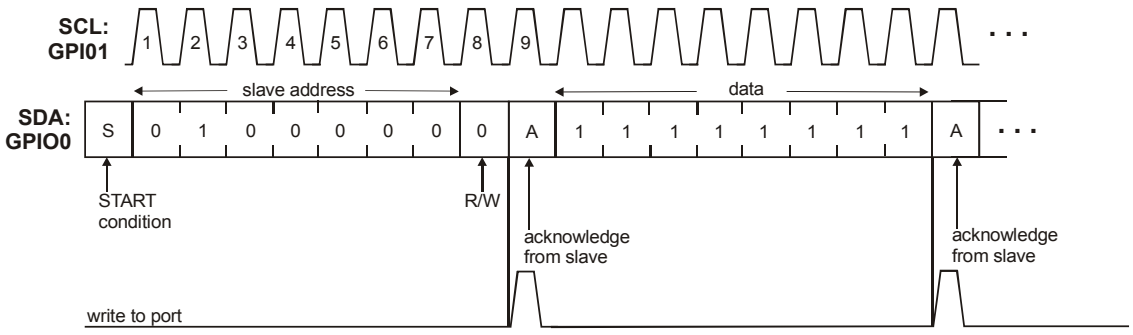


Figure 9-3 Extended GPI Initialization Timing

The write sequence is initiated by a START condition, and then followed by 7 bits of slave address + 1 bit operating command, which is '0' for a Write operation. The slave will acknowledge this address + command octet by pulling the SDA line to logic low. The next octet written to the SDA line indicates activation of the pull-up of each GPI bits; in this case all bits should be set to '1'.

Once the device is initialized, the status on each GPI pin as set by the corresponding DIP switch can be read using the following sequence:

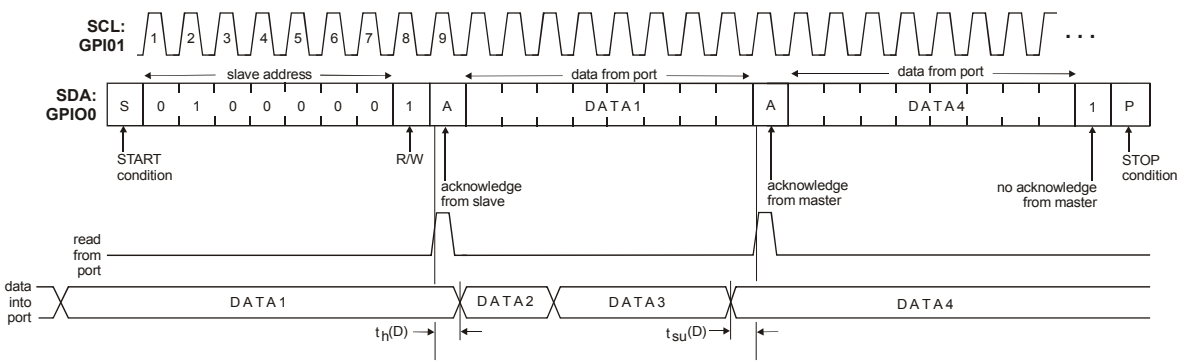


Figure 9-4 Extended GPI Read Timing

The read sequence is initiated by a START condition followed by 7 bits of slave address + 1 bit operating command, which is '1' for a Read operation. The slave will acknowledge this address + command octet by pulling the SDA line to logic low. The next octet read from the SDA line is the GPI status sampled during the Acknowledge cycle. This data is then acknowledged by the Master. Subsequent data reads also can be done without initiating the address + command octet. This could be used to de-bounce the GPI state.

The maximum clock speed for SCL is 400 kHz. The minimum data setup time ($t_{SU}(D)$) is 0 µS, and the minimum data hold time ($t_H(D)$) is 4 µS.

The following example code illustrates how the eight DIP switches on an AD VP2/024 may be read by the VX 511/06x. The code below is written for clarity, rather than providing an optimal solution. When using this code, an operating system specific version of `ioDelay()` must be provided that ensures SCL does not operate faster than 400 kHz.

Prior to reading the DIP switch data, the I^2C link and I/O Expander must be initialized by a call to `vx511gpioInit()`, then data may be read via calls to `vx511gpioRead()`. The example code for functions `vx511gpioRead()` and `vx511gpioWrite()` does not include logic to detect fault conditions where no ACK is received from the I/O expander.

9.10.1 Declarations

The following definitions are referenced throughout the example code below.

```
/* defines */

#define I2C_ADDR           (0x20 << 1)   // address of device on I2C bus

#define I2C_READ           0x01          // read and write bit
#define I2C_WRITE          0x00          //

#define PORT_80            0x0080        // BIOS diagnostic port

#define VX511_SC3          0x0214        // Status and Control register 3
#define  SC3_DATA          0x01          // GPIO0 = I2C data
#define  SC3_CLK           0x02          // GPIO1 = I2C clock
#define  SC3_DATA_DIR      0x10          // 0 = input, 1 = output
#define  SC3_CLK_DIR       0x20          //     -"-

/* typedefs */

typedef unsigned char      UINT8;
```

9.10.2 Programming Interface Functions

The following function provides a trivial example illustrating how to configure and read from the AD VP2/024 General Purpose Inputs.

```
void readVx511Gpi (void)
{
       UINT8  b;

       vx511gpioInit ();

       b = vx511gpioRead ();
       printf ("GPI = %02X\n", (int)b);

} /* readVx511Gpi () */
```

The `vx511gpioInit()` and `vx511gpioRead ()` functions provide the programming interface to the GPI hardware.

```
/*******************************************************************************
 * vx511gpioInit: initialize the GPIO interface for input
 *
 * RETURNS: none
 */
void vx511gpioInit (void)
{
       i2cInitPort ();            // set I2C port initial I/O states
       vx511gpioWrite (0xFF);     // all outputs set high for use as inputs

} /* vx511gpioInit () */

/*******************************************************************************
 * vx511gpioRead: read data from the GPIO interface
 *
 * RETURNS: byte data
 */
UINT8 vx511gpioRead (void)
{
       UINT8  temp = 0;
       UINT8  data = 0;
       int    i;

       /* Send the Control byte = Slave Address + R/W bit */

       do {
              i2cSetDataOut ();          /* send "Start" */
              i2cStart ();

              /* Send device address - MSBit first */

              for (i = 7; i >= 0; i--)
                     i2cPutBit (I2C_ADDR | I2C_READ, i);

              i2cSetDataIn ();           /* check for ACK */
              i2cGetBit (&temp, 0);

       } while ((temp & 0x01) != 0);

       /* Read the data and ACK */

       i2cSetDataIn ();
```

```
            for (i = 7; i >= 0; i--)          /* MSBit first */
                  i2cGetBit (&data, i);

            i2cSetDataOut ();                 /* drive ACK */
            i2cPutBit (1, 0);

            /* Send "Stop" */

            i2cSetDataOut ();
            i2cStop ();

            return (data);

      } /* vx511gpioRead () */
```

9.10.3 Local Functions

The `vx511gpioWrite()` function is used only during initialization of the GPI interface. The AD PP2/024 does not support General Purpose outputs (GPO).

```
/*******************************************************************************
 * vx511gpioWrite: write data to the GPIO interface
 *
 * RETURNS: none
 */
static void vx511gpioWrite (UINT8 data)
{
       UINT8  temp = 0;
       int    i;

       /* Send the Control byte = Slave Address + R/W bit */

       do {
              i2cSetDataOut ();          /* send "Start" */
              i2cStart ();

              /* Send device address - MSBit first */

              for (i = 7; i >= 0; i--)
                     i2cPutBit (I2C_ADDR | I2C_WRITE, i);

              i2cSetDataIn ();           /* check for ACK */
              i2cGetBit (&temp, 0);

       } while ((temp & 0x01) != 0);

       /* Write the data and read ACK */

       i2cSetDataOut ();

       for (i = 7; i >= 0; i--)          /* MSBit first */
              i2cPutBit (data, i);

       i2cSetDataIn ();                  /* check for ACK */
       i2cGetBit (&temp, 0);

       /* Send "Stop" */

       i2cSetDataOut ();
       i2cStop ();

} /* vx511gpioWrite () */
```

ADDITIONAL LOCAL I/O FUNCTIONS

The following functions drive the low-level port operations required to implement the I^2C protocol used to communicate with the PCA8574.

The function `ioDelay()` must be modified by the user to ensure the I^2C clock frequency does not exceed 400kHz.

```
/*****************************************************************************
 * ioDelay (): delay to ensure I2C clock toggles at <= 400KHz, i.e. 2.5uS
 *             minimum delay period
 */

static void ioDelay (void)
{
       inportb (PORT_80);         /* dumy I/O read */

} /* ioDelay (); () */


/*****************************************************************************
 * i2cInitPort: configure I2C data and clock lines as output
 */

static void i2cInitPort (void)
{
       UINT8  p_data;             /* port data */

       p_data = inportb (VX511_SC3);

       p_data = p_data | SC3_DATA | SC3_CLK;
       outportb (VX511_SC3, p_data);

       p_data = p_data | SC3_DATA_DIR | SC3_CLK_DIR;
       outportb (VX511_SC3, p_data);

} /* i2cInitPort () */

/*****************************************************************************
 * i2cSetDataOut: configure I2C data line as output
 */

static void i2cSetDataOut (void)
{
       UINT8  p_data;             /* port data */

       p_data = inportb (VX511_SC3);
       outportb (VX511_SC3, p_data | SC3_DATA_DIR);
       ioDelay ();

} /* i2cSetDataOut () */

/*****************************************************************************
 * i2cSetDataIn: configure I2C data line as input
 */

static void i2cSetDataIn (void)
{
       UINT8  p_data;             /* port data */

       p_data = inportb (VX511_SC3);
       outportb (VX511_SC3, p_data & ~SC3_DATA_DIR);
       ioDelay ();

} /* i2cSetDataIn () */
```

```
/*****************************************************************************
 * i2cStart: send an I2C start sequence on the wire
 *
 * CLK _____/   \___
 *
 * DAT =_/     \_____
 */

static void i2cStart (void)
{
       UINT8  p_data;                    /* port data */

       p_data = inportb (VX511_SC3);     /* get current port state */
       ioDelay ();

       p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = no change */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data | SC3_DATA;       /* CLK = 0, DATA = 1 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data | SC3_CLK;        /* CLK = 1, DATA = 1 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data & ~SC3_DATA;      /* CLK = 1, DATA = 0 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = 0 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

} /* i2cStart () */

/*****************************************************************************
 * i2cStop: send an I2C stop sequence on the wire
 *
 * CLK ____/   \___
 *
 * DAT =_____/_____
 */

static void i2cStop (void)
{
       UINT8  p_data;                    /* port data */

       p_data = inportb (VX511_SC3);     /* get current port state */
       ioDelay ();

       p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = no change */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data & ~SC3_DATA;      /* CLK = 0, DATA = 0 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data | SC3_CLK;        /* CLK = 1, DATA = 0 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data | SC3_DATA;       /* CLK = 1, DATA = 1 */
       outportb (VX511_SC3, p_data);
       ioDelay ();

       p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = 1 */
```

```
        outportb (VX511_SC3, p_data);
        ioDelay ();

} /* i2cStop () */

/*****************************************************************************
 * i2cPutBit: write a single data bit on the I2C wire
 *
 *          __      __
 * CLK ___/  \____/
 *
 *                 _____
 * DAT =_______/          Data = 0 then 1
 *
 * Data is in 'bit_num' of 'data'. CLK = 0 on entry, must be 0 on exit
 */

static void i2cPutBit
(
        UINT8  data,              /* byte value currently being transmitted */
        int    bit_num            /* bit position to write to device */
)
{
        UINT8  p_data;            /* port data */

        p_data = inportb (VX511_SC3);     /* get current port state */
        ioDelay ();

        p_data = p_data & ~SC3_DATA;      /* CLK = 0, DATA = data[bit_num] */

        if ( ((data >> bit_num) & 0x01) != 0 )
                p_data = p_data | SC3_DATA;

        outportb (VX511_SC3, p_data);
        ioDelay ();

        p_data = p_data | SC3_CLK;        /* CLK = 1, DATA = no change */
        outportb (VX511_SC3, p_data);
        ioDelay ();

        p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = no change */
        outportb (VX511_SC3, p_data);
        ioDelay ();

} /* i2cPutBit () */

/*****************************************************************************
 * i2cGetBit: read a single data bit from the I2C wire
 *
 *          __      __
 * CLK ___/  \____/
 *
 *                 _____
 * DAT =_______/          Data = 0 then 1
 *
 * Put data in 'bit_num' via 'data_ptr', do not modify remainder. CLK = 0 on
entry
 * must be 0 on exit.
 */

static void i2cGetBit
(
        UINT8* data_ptr,     /* pointer to byte value currently being received */
        int    bit_num       /* position to store bit read from device */
)
{
        UINT8  p_data;       /* port data */

        p_data = inportb (VX511_SC3);     /* get current port state */
        ioDelay ();

        p_data = p_data | SC3_CLK;        /* CLK = 1, DATA = input */
        outportb (VX511_SC3, p_data);
```

```
        ioDelay ();

        p_data = inportb (VX511_SC3);     /* read data */
        ioDelay ();

        *data_ptr = (*data_ptr) & ~(1 << bit_num);     /* assume return data = 0
*/

        if ((p_data & SC3_DATA) != 0)     /* if 1, then set bit */
              *data_ptr = (*data_ptr) | (1 << bit_num);

        p_data = p_data & ~SC3_CLK;       /* CLK = 0, DATA = may change */
        outportb (VX511_SC3, p_data);
        ioDelay ();
```

This page is intentionally unused.

10 PC BIOS

The VX 511/06x is fitted with PC BIOS firmware that performs many of the functions of a standard desktop PC. It also includes additional features specifically tailored for the VME bus environment. In addition to the core BIOS firmware, the board is fitted with BIOS Extensions for VGA interface, and remote bootload capability via any of the on-board Ethernet channels. To improve the flexibility of the board, some of these features may be selectively enabled or disabled by an operator using BIOS setup menus. Many of the features provided by the PC BIOS are unlikely to be adjusted by the user, but there are several options which many users will find helpful. Some of these are already referenced in other sections of this manual, but the remainder of this chapter will describe some other commonly-used options. More information about each of the options available is provided in the Help box of the BIOS setup menus.

10.1 Entering the PC BIOS

The startup mode of the board may be selected using the Mode switch, but can be either of the following: PC BIOS mode (the factory default setting), which generally follows the behavior of a desktop PC, and VSA mode (a more flexible and comprehensive testing mode), which can be used for system or board testing. Figure 10-1 shows the location of the switch on the board and its settings.

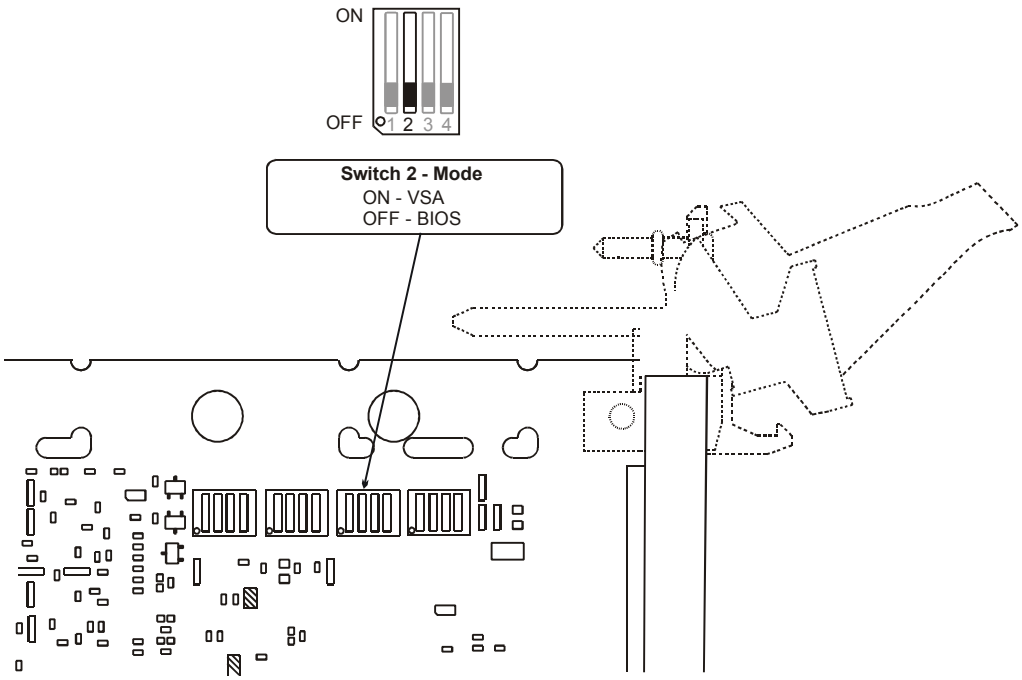


Figure 10-1 Mode Switch

VSA mode may be exited either by operator command, or by allowing the board to proceed through the VSA startup sequence without intervention. In either case, the board will enter PC BIOS mode and continue as if this mode had been selected with the switch. When the board is reset, it will restart in the switch-selected operating mode.

PC BIOS

Operator communication with the PC BIOS is normally through the VGA display and a separate keyboard. This can be reconfigured with on-board switches to use a serial terminal connected to the COM1 or COM2 ports as described in Section 7.1. A VT100-compatible serial terminal or emulator program should be used. By default the serial line is programmed to operate at 9600 Baud with 8 data bits, 1 stop bit and no parity (8N1). There is no flow control. For fast terminals, the baud rate can be increased via the **`Serial Console Baud Rate`** field of the **`Main | Boot Options`** Setup menu.

10.2 The PC BIOS Startup Sequence

When the board starts up without operator intervention, it will run a basic POST sequence, including a DRAM test. The full DRAM test will be omitted on subsequent restarts if the BIOS configuration settings have not been changed. Once the DRAM test has completed, the board will try to bootload application software from any attached mass storage medium or through one of the Ethernet interfaces. When the PC BIOS starts after changing the battery, losing battery power or after using the CMOS Clear switch, it may report a CMOS Checksum Error or some other problem. This will be followed by a prompt to the operator to press to continue or to enter Setup mode. If no key is pressed within approximately five seconds, the PC BIOS will continue with its normal startup sequence. It will also re-calculate the CMOS Checksum to prevent this error occurring again at a subsequent restart.

Pressing <**F2**> at any time during the PC BIOS startup sequence will result in the BIOS Setup menu being entered. The Setup menu is extensive, and is provided with context-sensitive help information which is displayed in the right-hand panel on screen.

NOTE: When <**F2**> is pressed, a few seconds may elapse before the BIOS Setup menu appears. The PC BIOS will always run BIOS Extensions for any PMC modules it detects before responding to a keypress.

10.3 Boot device selection

10.3.1 The Setup Boot Menu

The order in which the PC BIOS searches for a bootable medium is pre-configured but may be altered by the operator using the Boot setup menu. When the order is changed using this menu it will be retained in battery-backed non-volatile memory so that the order is maintained after a restart. Changes to the device boot order can also be saved to Flash memory as part of the User Default settings.

The boot menu is divided into two parts: bootable devices and excluded devices. Devices can be moved between the two lists using the <**X**> key. The 'bootable devices' menu has room for up to eight entries, therefore on boards with many add-in bootable devices it may be necessary to move unwanted entries into the 'excluded' list before the required device can be added to the 'bootable' list.

Once a device has been added to the 'bootable' list, the <**+**> or <-> keys can be used to raise or lower its relative priority in the boot order. Finally, these settings can be saved via the **`Exit`** menu.

10.3.2 The One-time Boot Menu

It is also possible to specify a one-time override of the boot device when the board starts, by pressing <**ESC**>. This will result in a pop-up menu appearing. The appropriate boot device may be selected from a list by using the cursor keys and pressing <**ENTER**>, but this is not retained in non-volatile memory, so the correct device must be re-selected if necessary at a subsequent restart.

NOTE: When <**ESC**> is pressed, a few seconds may elapse before the boot device selection menu appears. The PC BIOS will always run BIOS Extensions for any PMC modules it detects before responding to a key press.

10.3.3 PXE Boot

The Ethernet channels require their BIOS Extension firmware to be enabled before they can be used as boot devices. BIOS setup options are provided to control whether or not the board runs the BIOS Extensions for the Ethernet channels or the on-board PMC site. The PXE Boot Firmware field of the appropriate device menu must be used to enable or disable the BIOS Extension. The device menus are accessible from **`Main | Boot Options`**.

The Ethernet boot firmware allows remote booting using PXE. The PXE protocols are defined by Intel and further information can be obtained from: http://developer.intel.com.

NOTE: The BIOS has limited space available for Extension ROMs. If a PMC or XMC module containing extension firmware is fitted to the board, it may be necessary to disable the PXE firmware extension before the PMC or XMC firmware can be loaded.

10.4 PCI Bus Resource Management

The bus structure of the VX 511/06x is complex. There are two on-board PCI busses, namely:

A 32-bit bus which connects the ICH9M to the PMC site 2 and operates at 33 MHz with 3.3V or 5V signaling levels.

A 64-bit bus which connects a PCIe-to-PCI-X bridge to PMC Site 1 as well as Tsi148. The 64-bit bus normally operates with 3.3V signaling levels and runs at 66 MHz in PCI Bus mode or 133 MHz in PCI-X mode. This may be slowed to 33 MHz if a PMC module is fitted. The bus can also operate at 100 MHz in PCI-X mode by setting some board switches (see Section 2.8.2).

10.4.1 PCI Express Links

The GS45 GMCH provides an 8-lane PCIe link which connects to the upstream side of a PCIe switch. The switch provides up to two downstream PCIe links:

- One x8-lane link to PMC Site 1 XMC connector
- Two x4-lane links to VXS P0 for VITA 41.4

The ICH9M provides two PCIe links, connected as follows:

- One x4-lane link to the PCIe switch, where the downstream is connected to the PCIe-to-PCI-X bridge and 82576EB Dual SerDes controller
- One x1-lane link to the 82574L Ethernet controller

The last PCIe lane on ICH9M-E is configured for the Integrated Gigabit LAN function.

The PCIe links appear as virtual PCI-to-PCI bridges. The endpoint devices appear as device 0 on the corresponding virtual PCI bus.

10.4.2 PCI Resource Allocation

The PC BIOS initializes all devices on the local PCI bus, and allocates appropriate memory address ranges, I/O address ranges, and interrupt routings for all these devices. This process is automatic as part of the BIOS “Plug-and-play” setup. The Intel chipset allows for a flexible allocation of many PCI bus interrupts to the available interrupt inputs on the PC-compatible interrupt controllers provided on the board. The PC BIOS uses this feature to program default settings which it considers appropriate for the combination of on-board devices and any device fitted to the PMC sites.

The interrupt controller in the ICH9M-E can operate in two basic modes, namely PIC (or Non-APIC) mode and APIC mode. PIC mode corresponds to the legacy PC interrupt structure. APIC mode provides additional interrupts and several functional improvements.

Table 10-1 lists the allocation of the various PCI and PCIe devices to interrupt inputs on the ICH9M-E ICH. These allocations are fixed and cannot be changed by the user.

ICH Interrupt Input	Device(s)
PIRQA	GS45 Graphics ICH9M-E Ethernet 82574 Ethernet 82576 Ethernet Channel 0 PMC Site 1 INTC
PIRQB	PMC Site 1 INTD TSI148 INTA 82576 Ethernet Channel 1
PIRQC	PMC Site 1 INTA
PIRQD	PMC Site 1 INTB XMC Site
PIRQE	PMC Site 2 INTA
PIRQF	PMC Site 2 INTB
PIRQG	PMC Site 2 INTC
PIRQH	PMC Site 2 INTD

Table 10-1 PCI Device Interrupt Allocations

Table 10-2 lists the typical interrupt structure in PIC mode. A total of 15 usable interrupts are available. The actual allocation of PCI bus interrupts to available interrupt controller inputs will depend on both the default “Plug-and-play” settings programmed by the PC BIOS, and the way in which the user has overridden them using the Setup screens. When more than one PCI bus interrupt is routed to the same interrupt controller input, that input will remain active while any of the sources connected to it are active.

Interrupt	Device(s)
IRQ0	Timer 0
IRQ1	Keyboard
IRQ2	Slave PIC
IRQ3	Serial Port COM2
IRQ4	Serial Port COM1
IRQ5	Long Duration Timer
IRQ6	PCI device interrupt
IRQ7	PCI device interrupt
IRQ8	Real Time Clock
IRQ9	PCI device interrupt
IRQ10	PCI device interrupt
IRQ11	PCI interrupt
IRQ12	Mouse
IRQ13	Floating Point Error
IRQ14	Primary IDE
IRQ15	Secondary IDE

Table 10-2 Interrupt Structure in PIC Mode

Table 10-3 lists the typical interrupt structure in APIC mode. A total of 24 interrupts are available. The ICH9M interrupt inputs PIRQA – PIRQH are mapped to IRQ16 – IRQ23 respectively.

Interrupt	Device(s)
IRQ0	Legacy PIC Interrupt
IRQ1	Keyboard
IRQ2	Timer 0
IRQ3	Serial Port COM2
IRQ4	Serial Port COM1
IRQ5	Long Duration Timer
IRQ6	
IRQ7	
IRQ8	Real Time Clock
IRQ9	
IRQ10	
IRQ11	
IRQ12	Mouse
IRQ13	Floating Point Error
IRQ14	Primary IDE
IRQ15	Secondary IDE
IRQ16	PIRQA
IRQ17	PIRQB
IRQ18	PIRQC
IRQ19	PIRQD
IRQ20	PIRQE
IRQ21	PIRQF
IRQ22	PIRQG
IRQ23	PIRQH

Table 10-3 Interrupt Structure in APIC Mode

10.4.3 PCI Device IDs

Each PCI bus, and each device on an individual PCI bus, has a unique ID. The VX 511/06x bus and device IDs are listed in Table 10-4. Bus numbers identified by a letter are assigned by the BIOS and can change depending upon fitted optional devices, e.g. XMC or PMC card, and/or BIOS CMOS settings.

Device	Bus	ID	PCI Function Code	Vendor ID	Device ID
GS45 – DRAM controller	0	0	0	8086h	2A40h
Host to PCIe bridge	0	1	0	8086h	2A41h
Internal graphics controller	0	2	0	8086h	2A42h
Internal graphics controller	0	2	1	8086h	2A43h
Gigabit Ethernet Controller	0	25	0	8086h	294Ch
ICH9M – USB UHCI #0	0	26	0	8086h	2937h
ICH9M – USB UHCI #1	0	26	1	8086h	2938h
ICH9M – USB UHCI #2	0	26	2	8086h	2939h
ICH9M – USB EHCI	0	26	7	8086h	293Ch
ICH9M – x4 PCIe Link	0	28	0	8086h	2940h
ICH9M – x1 PCIe Link	0	28	4	8086h	2948h
ICH9M – USB UHCI #0	0	29	0	8086h	2934h
ICH9M – USB UHCI #1	0	29	1	8086h	2935h
ICH9M – USB UHCI #2	0	29	2	8086h	2936h
ICH9M – USB EHCI	0	29	7	8086h	293Ah
DMI to PCI Bus bridge	0	30	0	8086h	2448h
LPC bus bridge	0	31	0	8086h	2917h
SATA controller	0	31	2	8086h	2928h
SMBus Controller	0	31	3	8086h	2930h
SATA controller	0	31	5	8086h	292Dh
PEX 8624 - Upstream	1	0	0	10B5h	8624h
PEX 8624 – Down VXS PA	2	0	0	10B5h	8624h
PEX 8624 – Down VXS PB	2	1	0	10B5h	8624h
PEX 8624 – Internal	2	4	0	10B5h	8624h
PEX 8624 – Down XMC	2	8	0	10B5h	8624h
PES12T3 – Upstream	7	0	0	111Dh	8061h
PES12T3 – Down PCI-X	8	2	0	111Dh	8061h
PES12T3 – Down SerDes	8	4	0	111Dh	8061h
PI7C9X130	9	0	0	12D8h	E130h
Tsi148 VME bridge	10	5	0	10E3h	0148h
82576EB Ch 0	11	0	0	8086h	10E7h
82576EB Ch 1	11	0	1	8086h	10E7h
82574L Ethernet	12	0	0	8086h	10D3h

Table 10-4 PCI Device Numbers

10.5 Local Image Allocation

Boards fitted with 4 Gbytes or more of SDRAM no longer have a convenient 'hole' in the address map where Tsi148 Local Slave Images can be mapped. Therefore the BIOS must reserve a block of address space for this purpose.

The BIOS provides three options for reserving memory:

Slave images are configured through the existing Setup menu options. The BIOS then reserves just enough memory to map the enabled slave images and will automatically assign addresses to them.

The BIOS reserves a fixed-size block of address space. The size of the reserved block is specified through the **`VMEBus | LSI Reserved Size`** setup option.

A combination of 1 and 2 where images are configured according to Setup menu options, but the BIOS reserves a larger address block as specified by **`LSI Reserved Size`**.

The BIOS reserves memory by increasing the size of the block used by PCI devices, i.e. the top of DRAM is lowered.

For all three options, the BIOS creates a data-structure in SDRAM that defines details of the reserved memory as follows:

```
/* Header part */

UINT32 vmeRes_header = 'EMV$';    /* signature, '$' in LSB */
UINT8  vmeRes_version = 0x01;     /* version of structure */
UINT8  vmeRes_length;             /* total length of structure */
UINT16 vmeRes_reserved = 0;

/*  Version 1 payload */

UINT32 vmeRes_mem_base;           /* physical address of reserved block */
UINT32 vmeRes_mem_size;           /* size (in bytes) of reserved block */
UINT32 vmeRes_image_0_base;       /* base address of enabled LSI images */
UINT32 vmeRes_image_1_base;
UINT32 vmeRes_image_2_base;
UINT32 vmeRes_image_3_base;
UINT32 vmeRes_image_4_base;
UINT32 vmeRes_image_5_base;
UINT32 vmeRes_image_6_base;
UINT32 vmeRes_image_7_base;
```

Software requiring details of this reserved memory block can locate this structure by searching for the signature bytes between addresses 0xE0000 and 0xFFFFF.

10.6 User Selectable NVRAM Defaults

The BIOS provides a facility through which the user can save preferred setup option settings to Flash memory. Then, if the BIOS detects that the contents of NVRAM is corrupt, the user can elect to restore the contents from the saved settings, rather than loading factory configured defaults. This facility also allows the board to operate without fitting the battery, but with NVRAM settings different to the factory defaults.

The **`Save User Defaults`** option in the BIOS setup **`Exit`** menu is used to write the current NVRAM settings to Flash memory. When settings are saved to Flash memory, the current BIOS date and time will also be stored; this allows the board to start operating with an appropriate date and time.

NOTE: Saving settings to Flash memory may take a number of seconds to complete.

The NVRAM restore feature is controlled by the BIOS Defaults switch (see Figure 10-2). When the BIOS detects that the NVRAM contents are corrupt, NVRAM settings will be restored from Flash memory (provided that valid settings have been saved). The switch selects between a user saved setting or the factory-configured defaults. If no user setting has been saved then the factory-configured defaults will be used.

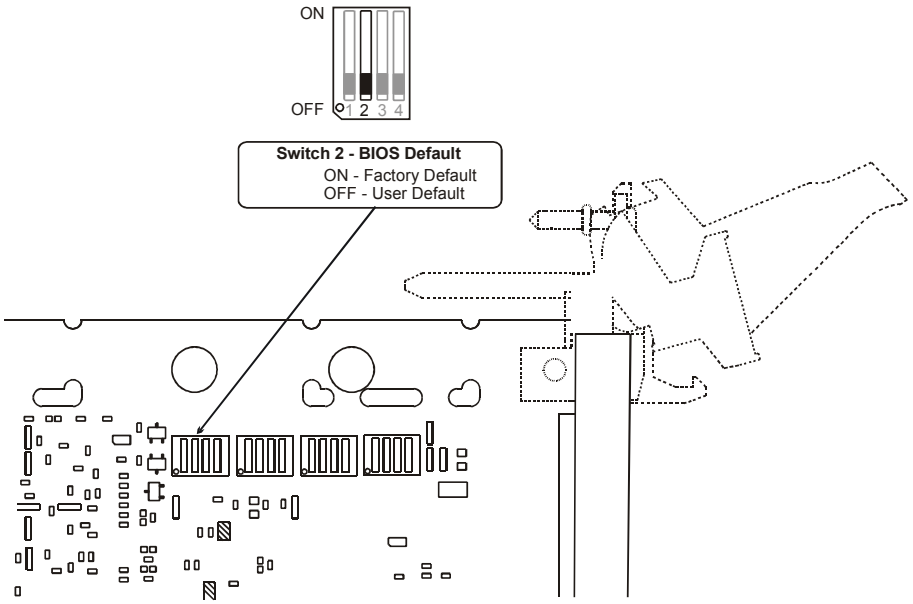


Figure 10-2 BIOS Default Switch

To configure and save preferred NVRAM settings:

- Configure the BIOS in the usual manner via the setup menus
- Reboot the board and allow it to proceed through to the bootloader without error
- Reboot the board and enter Setup
- From the **`Exit`** menu, select **`Save User Defaults`**
- Set the BIOS Defaults switch to enable the restore feature

NOTE: If the board is ever returned to the factory for repair the saved NVRAM settings may be changed or invalidated.

10.7 The Recovery BIOS

In the unlikely event that the board's BIOS ROM contents becomes corrupted and it is not possible to perform the normal BIOS update procedure, the board provides a minimal Recovery BIOS that will allow the board to boot from a specially prepared floppy disk or USB memory stick and restore a known-good BIOS image.

The Recovery BIOS is located in a special sector in the BIOS ROM that is protected from accidental erasure by hardware means. When a BIOS update is performed, the Recovery BIOS does not get updated.

When power is applied to the board, or when the board is reset, the CPU starts to execute the Recovery BIOS. From here a checksum test is performed on the first 64 Kbytes of the main BIOS to ensure that it is intact. When the checksum is validated, control passes to the main BIOS and the board boots normally. If the checksum test fails, the BIOS recovery process is invoked automatically.

The BIOS recovery process can also be forced using the Boot Type switch see Figure 10-3.

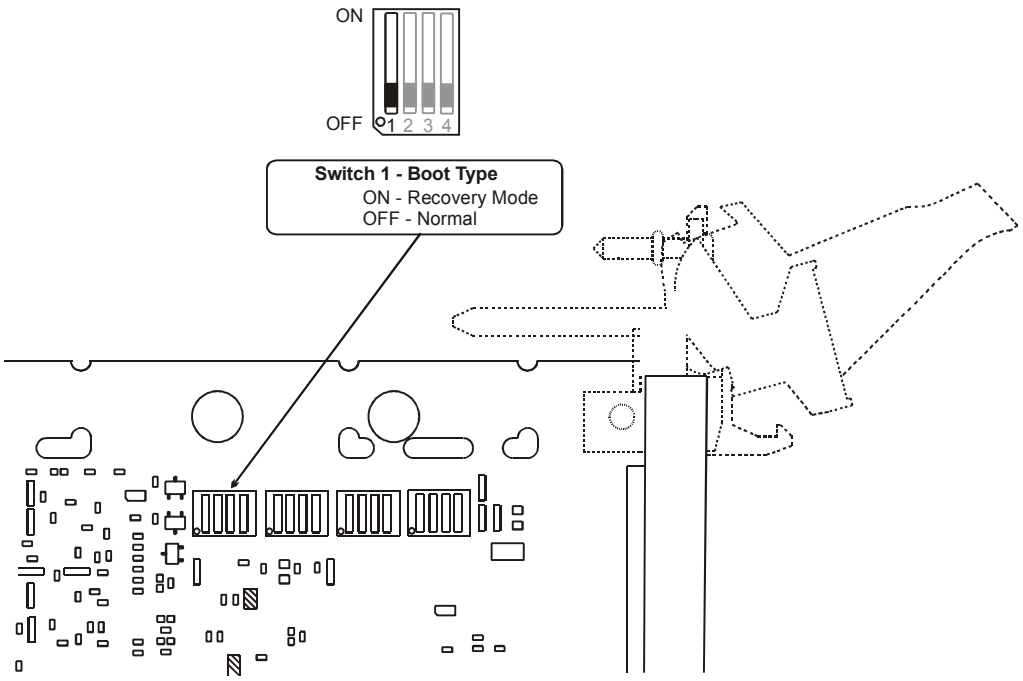


Figure 10-3 Boot Type Switch

The recovery BIOS will indicate its progress via a serial terminal connected to COM1 or COM2 as determined by the Console Port Select switch (see Figure 7-2). If selected, COM1 will be configured for RS232 mode. VGA output is not supported.

The recovery BIOS requires a specially prepared disk image; a suitable recovery disk image can be obtained from Concurrent Technologies, if required.

10.8 VXS PCIe Non-Transparent Bridge Setup

The PLX8624 PCIe switch that implements the VITA 41.4 backplane PCIe links allows one port to be configured as a Non-Transparent (NT) bridge. BIOS V2.09 adds support for enabling the NT bridge function of the switch and configuring the PCI base address registers (BARs) on either side of the NT bridge.

The NT bridge Setup options are located under the VXS PCIe top-level menu. The **`VXS PCIe | NT Port`** option enables the NT bridge function and specifies which VXS port connects via the NT bridge. This can be set to Port-B, Port-A or Disabled; the default is "Disabled".

When the NT port is enabled (for either port) two sub-menus are revealed that allow configuration of up to four BAR registers each for the Virtual (local CPU) and Link (VXS) interfaces to the NT bridge. For each BAR, options are provided for enabling the BAR, specifying the decode size, translation address and prefetchable status. In addition, BAR2 and BAR4 can be configured as 64-bit addressable, (though the BIOS only supports mapping to 32-bit addresses).

The BIOS maintains a single set of NT port settings, so these can be directly transferred between Port-A and Port-B.

NOTE: VXS Port-A connects to port-1 of the PLX8624 and VXS Port-B connects to port-0.

10.8.1 Virtual Interface

The Virtual Interface BARs give the local CPU access to the VXS PCIe interface. The term 'virtual' is used because the PCI bus to which the NT bridge connects exists only within the PEX8624 PCIe switch.

Four 32-bit BAR registers are provided by the Virtual Interface. BAR2 and BAR4 can optionally be configured for 64-bit address decode; however when this feature is enabled the adjacent BAR (3 or 5) is used for the upper address bits and is not available for configuration.

10.8.2 Link Interface

The Link Interface BARs give a device on the VXS PCIe interface access to the local board memory.

Four 32-bit BAR registers are provided by the Link Interface. BAR2 and BAR4 can optionally be configured for 64-bit address decode; however when this feature is enabled the adjacent BAR (3 or 5) is used for the upper address bits and is not available for configuration.

10.8.3 NT Bridge Address Translation

The NT bridge forms PCI addresses by concatenating the least significant bits from the CPU generated address and the most significant bits from the BAR translation address; the contribution from each part is fixed and is determined by the BAR size.

The translation address must be a multiple of the BAR size, which in turn must be a power of two. The BAR Setup option for **`Image Size`** allows selection from a series of pre-configured sizes, the option for **`Xlate Address`** allows the address to be specified directly.

The following example illustrates the address translation mechanism for a CPU access via the NT bridge Virtual Interface to VXS Port-A. The same principle applies in the reverse direction.

VI BAR2 size:	**`0x00200000`**	2Mbytes
VI BAR2 translation address:	**`0x12800000`**	specified by User via Setup
VI BAR2 PCI address:	**`0xDC400000`**	allocated by the BIOS
CPU address:	**`0xDC509834`**	generated by driver or application
Offset within BAR2:	**`0x00109834`**	
Address on VXS Port-A:	**`0x12909834`**	BAR2 offset + translation address

The BAR translation address can be configured (or changed) by an application program, however the BAR size must be specified before the PCI bus is enumerated by the BIOS (or re-enumerated by an operating system.

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11 SYSTEM MANAGEMENT

11.1 Power Management

The Intel Core 2 Duo processor incorporates a mechanism for changing the processor's operating frequency and core voltage under software control. By making these reductions the board's maximum power consumption is also reduced substantially.

The Intel Core 2 Duo processor supports a number of discrete operating frequencies that vary between 0.8 GHz and full speed (see Table 11-1). The BIOS provides a Setup menu (**`Advanced | Advanced Processor Options | CPU Operating Frequency`**) that allows the operating frequency of the CPU to be set prior to booting an operating system. By default the CPU will operate at full speed.

1.86 GHz Intel Core 2 Duo Processor SL9400	2.26 GHz Intel Core 2 Duo Processor SP9300
	2.26 GHz
1.86 GHz	1.6 GHz
0.8 GHz	0.8 GHz

Table 11-1 CPU Operating Speed BIOS Options

This mechanism for power reduction allows the board to operate in environments where power capacity is limited (e.g. under battery power), or in systems where cooling airflow is less than adequate. In this last case it may be wise to also consider some of the Thermal Management options available on this board (see Section 11.2).

NOTE: During POST, the BIOS will always report the maximum possible CPU frequency, as specified by the CPU's Brand String.

11.2 Thermal Management

The maximum power dissipation of the Intel Core 2 Duo processor may sometimes be higher than that of previous Intel processors. Under typical load conditions, the heatsink (and cooling airflow) will keep the processor die temperature within specification. However, if the board is running CPU-intensive or stress software or if the airflow is inadequate, the heatsink alone may not be able to prevent the processor overheating.

To ensure that the processor always operates within its thermal specifications, it includes several thermal management and protection functions. Each of these is described below. A BIOS setup option is used to select which functions are to be enabled. See Section 11.2.4 for further details.

11.2.1 Thermal Monitor 1 (TM1)

TM1 uses a temperature sensor located near to the hottest part of each CPU core on the processor die. If a sensor detects a critically high temperature a thermal control circuit (TCC) will modulate (i.e. alternately stop and start) the core clocks for the associated CPU core. This causes the CPU core to halt for short periods and decreases its power consumption, which in turn lowers the die temperature. Note that TM1 operates independently on each of the CPU cores.

The severity of the modulation will increase as the die temperature rises, up to a maximum of about 50%. The TCC will cease modulation when the die temperature has fallen to a non-critical value.

The temperature sensor is individually calibrated by Intel. The TM1 characteristics are also fixed by Intel and cannot be modified.

The drawbacks of TM1 are that it starts to operate at a relatively low temperature (about 90°C) and that it has a low modulation rate, which can produce undesirable software latencies.

TM1 is disabled after Reset and has to be enabled by the BIOS (see Section 11.2.4).

11.2.2 Thermal Monitor 2 (TM2)

TM2 uses the same temperature sensor as TM1. When the TM2 thermal control circuit is triggered, the CPU operating frequency and core voltage will be reduced, causing the power consumption to fall, which in turn lowers the die temperature.

Because a CPU under TM2 control operates continuously, the overall system performance for a given reduction in power consumption is higher than TM1. System latency is also lower when using TM2.

The drawback of TM2 is that changes to the operating frequency will also affect the Time Stamp Counter (TSC) rate and any timing or calculations that use it.

TM2 is disabled after Reset and has to be enabled by the BIOS (see Section 11.2.4).

11.2.3 CPU Thermal Trip

The processor chip also contains a thermal trip circuit. This is intended to protect the processor in the event of a catastrophic cooling failure. If the die temperature reaches approximately 125°C, it shuts down the processor core and asserts the THERMTRIP# signal. Logic on the board responds to this assertion by removing the processor core voltage within a few milliseconds.

A power cycle (i.e. OFF then ON) is required to restore normal operation. The thermal trip circuit is always operational and cannot be disabled.

11.2.4 PC BIOS Setup Options

The PC BIOS Setup Menu provides control over the thermal management functions, using the setting for the **`Advanced | Advanced Processor Options | Thermal Control Circuit`** option. It offers four choices, namely:

- Disabled - only the Thermal Trip is enabled
- Thermal Monitor 1 - the CPU's clock modulation mechanism is used to reduce power consumption; the Thermal Trip is enabled
- Thermal Monitor 2 - the CPU operating frequency is lowered to reduce power consumption; the Thermal Trip is enabled
- Thermal Monitor 2 + Thermal Monitor 1 – Thermal Monitor 2 will be used during normal operation, however if this fails to keep the operating temperature to an acceptable level TM1 will be invoked in addition.

The default setting is "Disabled".

It may be desirable that some form of thermal management is enabled to handle operation at very high load and high temperature. Under normal conditions, even with high loads, the standard heatsink and specified cooling are adequate to keep the processor operating within its limits even with the Thermal Management option set to Disabled. The BIOS setup option provides a means to enable additional protection if there is any concern about heat dissipation in the particular system being used.

11.2.5 Processor Thermal Status Indication

The User LED may be programmed to indicate if the processor die has reached the critical temperature at which thermal management is activated. This is done using the User LED Mode option switch. Figure 11-1 shows the location of this switch on the board, its settings and default position.

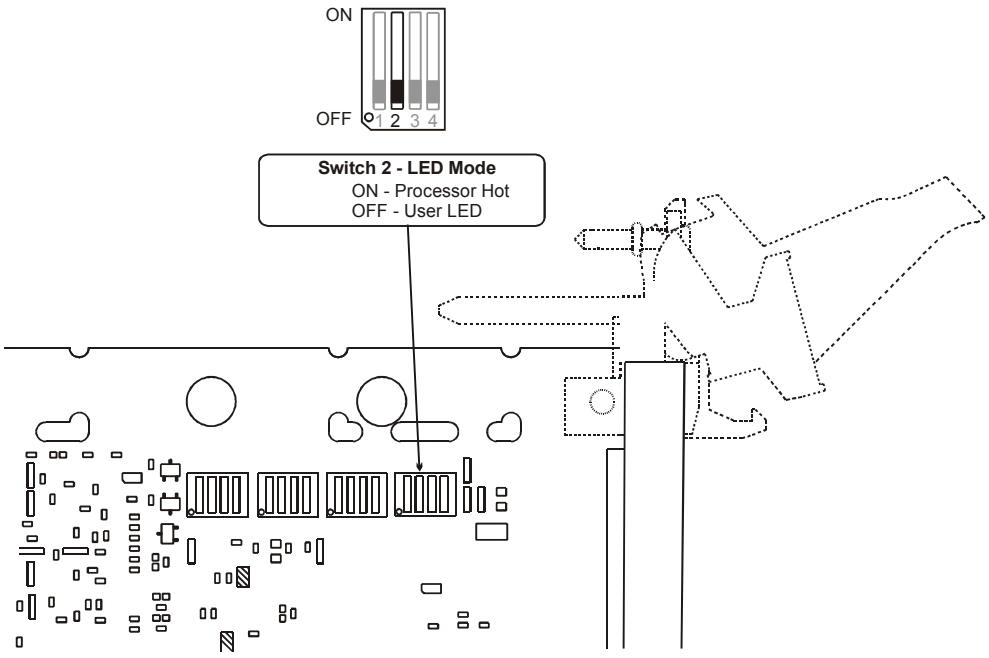


Figure 11-1 LED Mode Switch

11.3 Management Engine

The GS45 chipset includes a Management Engine (ME) that is involved in various power management and other tasks, particularly related to Intel AMT. If problems occur with these functions it is possible to reset the interface from the Core 2 Duo processor to the ME by setting the ME Register Clear switch shown in Figure 11-2 to the Clear Register position. Once the board has been powered up with the switch in the Clear Register position, the switch should be returned to the OFF position to ensure normal operation.

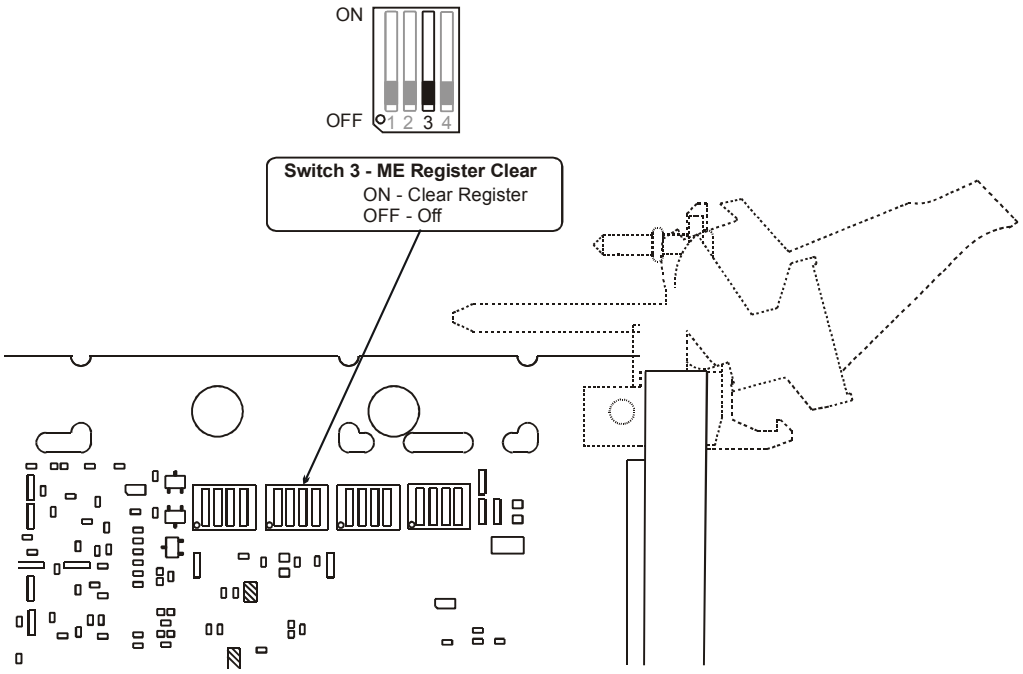


Figure 11-2 ME Register Clear Switch

A SPECIFICATIONS

A.1 Functional Description

Processor:	• 1.86 GHz or 2.26 GHz Intel Core 2 Duo processor on 45 nm process.
Level 1 Cache:	• 32 Kbytes instruction cache and 32 Kbytes data cache.
Level 2 Cache:	• 6 Mbytes on-die RAM operating at core frequency.
Memory:	• 4 Mbyte SPI Flash EPROM for PC BIOS and other firmware. • Up to 6 Gbytes DDR3-1066 SDRAM as defined by order number.
Interfaces:	• 64-bit VME interface utilizing the Tundra Tsi148 VME-to-PCI-X bridge supporting up to 2eSST and 2eVME. • Dual x4-lane PCIe links connected to P0 to support VXS VITA 41.4 backplane control plane. • One RS232 serial channel via front panel connector using 16550 compatible UART. Limited set of signals. • One RS232 serial channel via rear P2 connector using 16550 compatible UART. Full set of signals. • Two SATA300 interfaces via rear P2 connector • One SATA300 to support on-board mass storage option interface. • PS/2 keyboard and mouse interfaces via rear P2 connector. • One USB interface via front panel connector and two USB interfaces via rear P2 connector. USB 1.1 (1.5 and 12 Mbits/s) and USB 2.0 (480 Mbits/s) operation are supported. • One single-width PMC site supporting 64/32-bit 66/33 MHz PCI or 66/100/133 MHz PCI-X interface with 3.3V or 5V signaling. Both 5V and 3.3V power rails are provided. • One single-width PMC site supporting 32-bit 33 MHz PCI interface with 3.3V or 5V signaling. Both 5V and 3.3V power rails are provided. • An 8-lane XMC interface on PMC Site 1. • Two Gigabit Ethernet interfaces using 82574L and 82567LM Ethernet controllers with 10/100/1000 Mbits/s connections via front panel. Ethernet port 2 using 82567LM also will support Intel AMT. • Two Gigabit SERDES interface using 82576EB Ethernet controllers with 10/100/1000 Mbits/s connections via rear P0 to support Backplane networking specify by VXS VITA 41.6. Optionally the SERDES can be used to support Rear panel Gigabit Ethernet port using specific RTM. • External Push Button Reset input via rear P2. • Two general purpose I/O via rear P2.
Peripherals:	• Intel ICH9M-E device providing standard PC-AT architecture peripherals. • PC-AT Real Time Clock. • 32-bit Periodic Interval Timer with processor interrupt capability.

SPECIFICATIONS

A.2 Environmental Specifications

	Standard Temperature (1.86 GHz, N-Series)	Standard Temperature (2.26 GHz, N-Series)	Extended Temperature (1.86 GHz, E-Series)	Extended Temperature (1.86 GHz, K-Series)	Ruggedized Air-Cooled (1.86 GHz, RA-Series)	Ruggedized Conduction-Cooled (1.86 GHz, RC-Series)
Temperature Range (operating)	0°C to +55°C	0°C to +55°C	-25°C to +70°C	-40°C to +85°C	-40°C to +75°C	-40°C to +85°C
Temperature Range (storage)	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C	-50°C to +100°C	-55°C to +105°C
Temperature Rate of Change	2°C / min	2°C / min	2°C / min	2°C / min	7°C / min	7°C / min
Airflow (linear feet per minute)	300 LFM	400 LFM	400 LFM	400 LFM	300 LFM	Conduction Cooled
Relative Humidity (operating)	5% to 95%	5% to 95%	5% to 95%	5% to 95%	5% to 95%	5% to 95%
Relative Humidity (storage)	5% to 95%	5% to 95%	5% to 95%	5% to 95%	5% to 95%	5% to 95%
Humidity Protection	Optional	Optional	Optional	Yes	Yes	Yes
Altitude (operating)	0 to 15,000 ft (0 to 4,572m)	0 to 15,000 ft (0 to 4,572m)	0 to 15,000 ft (0 to 4,572m)	0 to 15,000 ft (0 to 4,572m)	-1,000 to 33,000 ft (-305 to 10,058m)	-1,000 to 50,000 ft (-305 to 15,240m)
Altitude (storage)	0 to 50,000 ft (0 to 15,240m)	0 to 50,000 ft (0 to 15,240m)	0 to 50,000 ft (0 to 15,240m)	0 to 50,000 ft (0 to 15,240m)	-1,000 to 50,000 ft (-305 to 15,240m)	-1,000 to 50,000 ft (-305 to 15,240m)

Table A-1 Environmental Specifications

NOTE: If the on-board hard disk drive option is fitted (N-Series), the operating temperature range will be restricted to +5 to +55ºC and the storage temperature range will be restricted to -40 to +65ºC.

NOTE: If the battery is fitted, the storage temperature range will be restricted to –20°C to +70ºC. This is because the ICH9M-E device is partially operational when the battery is connected. The battery life will be reduced by storage at high temperatures due to increased self-discharge. It is therefore recommended that the battery be removed during storage.

NOTE: The RC-Series operating temperature range refers to the temperature at the board edge.

A.3 Shock and Vibration Specification

	Standard Temperature (N-Series)	Extended Temperature (E-Series)	Extended Temperature (K-Series)	Ruggedized Air-Cooled (RA-Series)	Ruggedized Conduction Cooled (RC-Series)
Shock (operating)	20g, 11ms, ½ sine	20g, 11ms, ½ sine	20g, 11ms, ½ sine	40g, 11ms, ½ sine	40g, 11ms, ½ sine
Shock (non-operating)	30g, 11ms, ½ sine	30g, 11ms, ½ sine	30g, 11ms, ½ sine	40g, 11ms, ½ sine	40g, 11ms, ½ sine
Vibration - sinusoidal (operating)	2g at 5Hz to 2kHz	2g at 5Hz to 2kHz	2g at 5Hz to 2kHz		
Vibration - sinusoidal (non-operating)	3g at 5Hz to 2kHz	3g at 5Hz to 2kHz	3g at 5Hz to 2kHz		
Random Vibration (operating)				+3dB/octave (5Hz to 100Hz) 0.04 g^2/Hz, (10Hz to 1kHz); -6dB/octave (1kHz to 2kHz)	+3dB/octave (5Hz to 100Hz) 0.1 g^2/Hz (10Hz to 1kHz); -6dB/octave (1kHz to 2kHz)

Table A-2 Shock and Vibration Specifications

NOTE: All the above figures are for boards without an on-board hard disk mass storage option.

A.4 MTBF Values

Board Variant	Test used	Temperature	Environment	MTBF
VX 511/062-53RA	MIL 217	25°C	Ground benign	105,141 hrs

Table A-3 MTBF Values

A.5 Dimensions (All variants)

Height	23.3cm
Depth	16.0cm
Width	2.0cm
Weight	Not exceeding 750g (without Mass Storage Kit fitted) 720g (RA-Series) 720g (RC-Series)

NOTE: Several variants of the VX 511/06x are supplied with different heat sinks. While 750g represents the heaviest combination, other permutations may give a lighter overall weight.

SPECIFICATIONS

A.6 Electrical Specification

Full Speed	Actual Speed	+5V +5%/-3% Typical	+5V +5%/-3% Maximum	+12V +/-5% Maximum	-12V +/-5% Maximum
2.26 GHz	2.26 GHz	8.0A	10.1A	0.00A	0.00A
	800 MHz	6.0A	7.1A	0.00A	0.00A
1.86 GHz	1.86 GHz	6.6A	8.4A	0.00A	0.00A
	800 MHz	5.7A	6.6A	0.00A	0.00A

Table A-4 Voltage and Current Requirements

NOTE: This is for a board with 3 Gbytes SDRAM and with no Mass Storage Kit or PMC Modules fitted.

NOTE: Peak currents during startup are 7.4A for the 2.26 GHz CPU at full speed and 6.8A for the 1.86 GHz CPU at full speed.

NOTE: +/- 12V supplies are provided for the PMC interface. These supplies do not need to be present if the PMC module does not require them. Current requirements will be those of the fitted PMC module.

CAUTION: The high supply current requirements of the 2.26 GHz CPU variants of these boards mean that all the available +5V pins on the VME P1 connector must be utilized. It is therefore strongly recommended that this board is installed only in backplanes with 5-row P1 connectors supplying +5V power through all the pins defined in the VME64 specifications. Failure to comply with this recommendation may result in the board malfunctioning or, in extreme cases, board or system damage.

NOTE: The VX 511/06x-RA and VX 511/06x-RC both use the 1.86 GHz CPU.

Variant	Max power dissipation per PMC or XMC module	Max current @ 3.3V per PMC or XMC module	Max current @ 5V per PMC or XMC module	Max current @ 5V for both PMC/XMC sites combined	Max current @ +12V per PMC or XMC module	Max current @ -12V per PMC or XMC module
VX 511/06x (All Variants)	15W	4A	3A	4A (Limit of 4A total from backplane)	0.5A	0.2A

Table A-5 Maximum Current Requirements for PMC/XMC modules

A.7 Connectors (All Variants except RC)

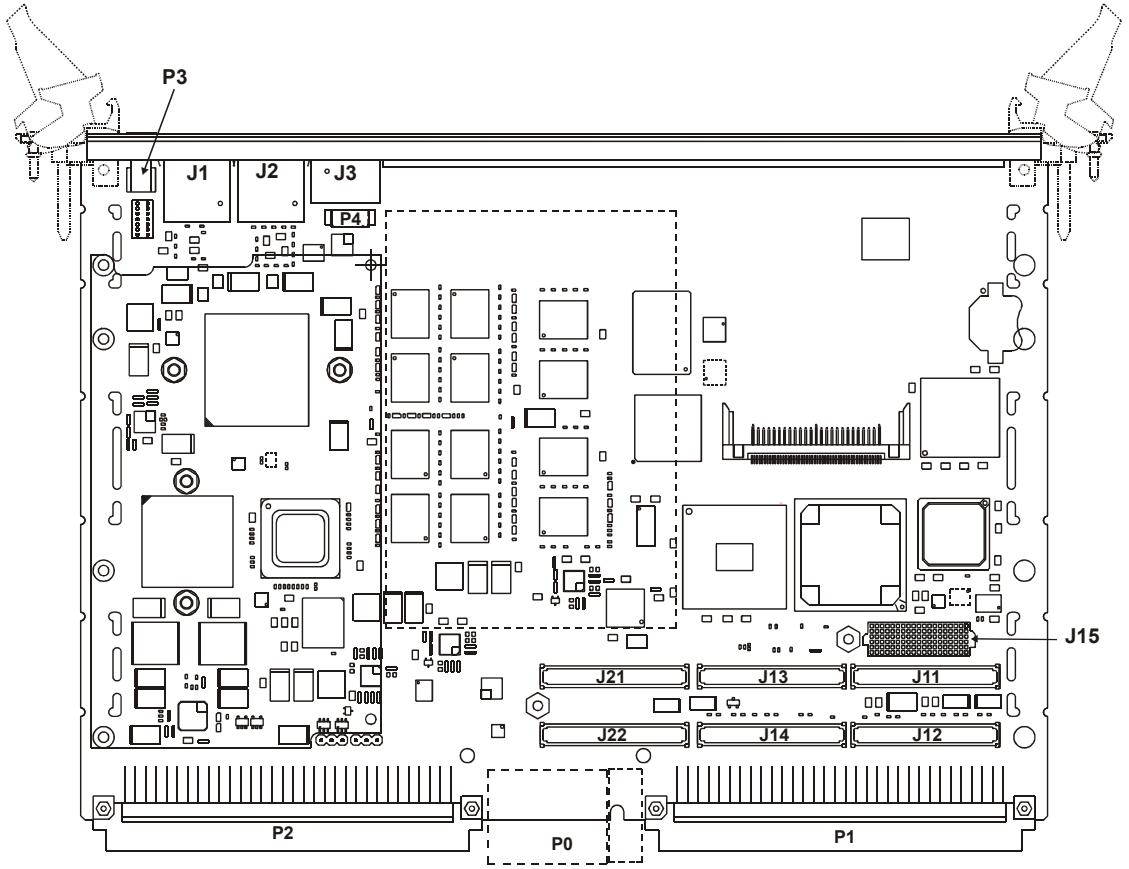


Figure A-1 Connector Layout – Component Side

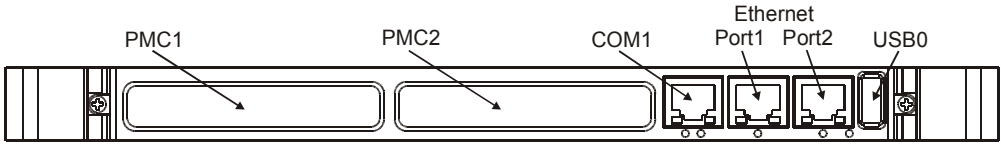


Figure A-2 Connector Layout – Front Panel

A.7.1 VME Interface P1 Pin-out

The VME interface P1 is via a 160-pin connector with signals assigned as follows:

Pin No.	Row Z	Row A	Row B	Row C	Row D
1	-	D00	BBSY#	D08	-
2	GND	D01	BCLR#	D09	GND
3	-	D02	ACFAIL#	D10	-
4	GND	D03	BG0IN#	D11	-
5	-	D04	BG0OUT#	D12	-
6	GND	D05	BG1IN#	D13	-
7	-	D06	BG1OUT	D14	-
8	GND	D07	BG2IN#	D15	-
9	-	GND	BG2OUT#	GND	GAP#
10	GND	SYSCLK	BG3IN#	SYSFAIL#	GA0#
11	-	GND	BG3OUT#	BERR#	GA1#
12	GND	DS1#	BR0#	SYSRESET#	-
13	-	DS0#	BR1#	LWORD#	GA2#
14	GND	WRITE#	BR2#	AM5	-
15	-	GND	BR3#	A23	GA3#
16	GND	DTACK#	AM0	A22	-
17	-	GND	AM1	A21	GA4#
18	GND	AS#	AM2	A20	-
19	-	GND	AM3	A19	-
20	GND	IACK#	GND	A18	-
21	-	IACKIN#	-	A17	-
22	GND	IACKOUT#	-	A16	-
23	-	AM4	GND	A15	-
24	GND	A07	IRQ7#	A14	-
25	-	A06	IRQ6#	A13	-
26	GND	A05	IRQ5#	A12	-
27	-	A04	IRQ4#	A11	-
28	GND	A03	IRQ3#	A10	-
29	-	A02	IRQ2#	A09	-
30	GND	A01	IRQ1#	A08	-
31	-	-12V	VCC_STANDBY	+12V	GND
32	GND	+5V	+5V	+5V	VCC

Table A-6 VME Interface P1 Pin-out

A.7.2 Auxiliary Connector P2 Pin-out

The auxiliary connection P2 consists of a 160-pin connector with signals assigned as follows:

Pin No.	Column Z	Column A	Column B	Column C	Column D
1	TXD2#	PMC_IO(1)	VCC	PMC_IO(2)	3V3
2	GND	PMC_IO(3)	GND	PMC_IO(4)	SATA3_TX+
3	RXD2#	PMC_IO(5)	VME_RETRY#	PMC_IO(6)	SATA3_TX-
4	GND	PMC_IO(7)	VME_A(24)	PMC_IO(8)	GND
5	RTS2	PMC_IO(9)	VME_A(25)	PMC_IO(10)	SATA3_RX-
6	GND	PMC_IO(11)	VME_A(26)	PMC_IO(12)	SATA3_RX+
7	CTS2	PMC_IO(13)	VME_A(27)	PMC_IO(14)	GND
8	GND	PMC_IO(15)	VME_A(28)	PMC_IO(16)	SATA4_TX+
9	DTR2	PMC_IO(17)	VME_A(29)	PMC_IO(18)	SATA4_TX-
10	GND	PMC_IO(19)	VME_A(30)	PMC_IO(20)	GND
11	DSR2	PMC_IO(21)	VME_A(31)	PMC_IO(22)	SATA4_RX-
12	GND	PMC_IO(23)	GND	PMC_IO(24)	SATA4_RX+
13	DCD2	PMC_IO(25)	VCC	PMC_IO(26)	GND
14	GND	PMC_IO(27)	VME_D(16)	PMC_IO(28)	USBP1+
15	RI2	PMC_IO(29)	VME_D(17)	PMC_IO(30)	USBP1-
16	GND	PMC_IO(31)	VME_D(18)	PMC_IO(32)	GND
17	TM_RST#	PMC_IO(33)	VME_D(19)	PMC_IO(34)	USBP2-
18	GND	PMC_IO(35)	VME_D(20)	PMC_IO(36)	USBP2+
19	VGA_DDCCK	PMC_IO(37)	VME_D(21)	PMC_IO(38)	BKP_RST#
20	GND	PMC_IO(39)	VME_D(22)	PMC_IO(40)	VCC_USB1
21	VGA_DDCDT	PMC_IO(41)	VME_D(23)	PMC_IO(42)	VCC_USB2
22	GND	PMC_IO(43)	GND	PMC_IO(44)	GND
23	VGA_RED	PMC_IO(45)	VME_D(24)	PMC_IO(46)	KBD_CLK
24	GND	PMC_IO(47)	VME_D(25)	PMC_IO(48)	KBD_DAT
25	VGA_GREEN	PMC_IO(49)	VME_D(26)	PMC_IO(50)	TM_DET#
26	GND	PMC_IO(51)	VME_D(27)	PMC_IO(52)	MS_CLK
27	VGA_BLUE	PMC_IO(53)	VME_D(28)	PMC_IO(54)	MS_DAT
28	GND	PMC_IO(55)	VME_D(29)	PMC_IO(56)	SPKR
29	VGA_HSYNC	PMC_IO(57)	VME_D(30)	PMC_IO(58)	GPIO0
30	GND	PMC_IO(59)	VME_D(31)	PMC_IO(60)	GPIO1
31	VGA_VSYNC	PMC_IO(61)	GND	PMC_IO(62)	GND
32	GND	PMC_IO(63)	VCC	PMC_IO(64)	VCC

Table A-7 Auxiliary Connector P2 Pin-out

NOTE: The serial I/O Tx and Rx pins act either as single-ended signals for RS232.

A.7.3 VXS Connector P0 Pin-out

This is a 105-way (7-row x 15-position) high speed differential connector. It carries backplane PCIe (VITA 41.4) as well as SERDES (VITA 41.6) interfaces on both Port A and Port B. The signal assignments conform to the mapping defined in the VITA 41.4 and VITA 41.6 standards and are shown below.

Pin	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	-	GND	PA_TX0-	PA_TX0+	GND	PA_RX0-	PA_RX0+
2	GND	PA_TX1-	PA_TX1+	GND	PA_RX1-	PA_RX1+	GND
3	-	GND	PA_TX2-	PA_TX2+	GND	PA_RX2-	PA_RX2+
4	GND	PA_TX3-	PA_TX3+	GND	PA_RX3-	PA_RX3+	GND
5	-	GND	SA_TX-	SA_TX+	GND	SA_RX-	SA_RX+
6	GND	-	-	GND	-	-	GND
7	-	GND	-	-	GND	-	-
8	GND	-	-	GND	-	-	GND
9	-	GND	-	-	GND	-	-
10	GND	-	-	GND	-	-	GND
11	PEN# *	GND	SB_TX-	SB_TX+	GND	SB_RX-	SB_RX+
12	GND	PB_TX0-	PB_TX0+	GND	PB_RX0-	PB_RX0+	GND
13	-	GND	PB_TX1-	PB_TX1+	GND	PB_RX1-	PB_RX1+
14	GND	PB_TX2-	PB_TX2+	GND	PB_RX2-	PB_RX2+	GND
15	-	GND	PB_TX3-	PB_TX3+	GND	PB_RX3-	PB_RX3+

Table A-8 VXS Connector P0 Pin-out

NOTE: This connector is a build time option and is not available on all variants.

* - Refer to VITA 41.0

Pins 1-4 and 12-15 in rows A-F are defined in VITA 41.4.

Pins 5 and 11 in rows A-F are defined in VITA 41.6.

A.7.4 Serial Interface J3 Pin-out

The serial interface J3 uses an RJ45 connector for COM1 in RS232 mode, with signals assigned as follows:

Pin No.	Signal Name	Direction
1	RTS - Request To Send	Output from board
2	DTR - Data Terminal Ready	Output from board
3	RETURN (GND)	
4	TX - Tx Data	Output from board
5	RX - Rx Data	Input to board
6	DCD - Carrier Detect	Input to board
7	DSR - Data Set Ready	Input to board
8	CTS - Clear To Send	Input to board

Table A-9 Serial Interface J3 Pin-out

A.7.5 PMC Site Connector Pin-outs

Signal assignments on the PMC connectors are shown in Tables A-10, A-11, A-12 and A-13.

Pin No.	Signal Name	Pin No.	Signal Name
1	-	2	-12V
3	GND	4	INTA#
5	INTB#	6	INTC#
7	BUSMODE1#	8	+5V
9	INTD#	10	-
11	GND	12	+3.3V††
13	CLK	14	GND
15	GND	16	GNT#
17	REQ#	18	+5V
19	V (I/O)	20	AD(31)
21	AD(28)	22	AD(27)
23	AD(25)	24	GND
25	GND	26	C/BE(3)#
27	AD(22)	28	AD(21)
29	AD(19)	30	+5V
31	V (I/O)	32	AD(17)
33	FRAME#	34	GND
35	GND	36	IRDY#
37	DEVSEL#	38	+5V
39	GND	40	LOCK#
41	SDONE#	42	SBO#
43	PAR	44	GND
45	V (I/O)	46	AD(15)
47	AD(12)	48	AD(11)
49	AD(09)	50	+5V
51	GND	52	C/BE(0)#
53	AD(06)	54	AD(05)
55	AD(04)	56	GND
57	V (I/O)	58	AD(03)
59	AD(02)	60	AD(01)
61	AD(00)	62	+5V
63	GND	64	REQ64#
V (I/O) can be +5V or +3.3 V depending on board configuration, †† pulled high via 10KΩ resistor.			

Table A-10 PMC Connector J11 and J21 Pin-out

Pin No.	Signal Name	Pin No.	Signal Name
1	+12V	2	-
3	-	4	-
5	-	6	GND
7	GND	8	-
9	-	10	-
11	+3.3V††	12	+3.3V
13	RST#	14	GND
15	+3.3V	16	GND
17	-	18	GND
19	AD(30)	20	AD(29)
21	GND	22	AD(26)
23	AD(24)	24	+3.3V
25	IDSEL	26	AD(23)
27	+3.3V	28	AD(20)
29	AD(18)	30	GND
31	AD(16)	32	C/BE(2)#
33	GND	34	IDSEL B
35	TRDY#	36	+3.3V
37	GND	38	STOP#
39	PERR#	40	GND
41	+3.3V	42	SERR#
43	C/BE(1)#	44	GND
45	AD(14)	46	AD(13)
47	M66EN	48	AD(10)
49	AD(08)	50	+3.3V
51	AD(07)	52	REQ B#
53	+3.3V	54	GNT B#
55	PMC-RSVD	56	GND
57	PMC-RSVD	58	EREADY††
59	GND	60	-
61	ACK64#	62	+3.3V
63	GND	64	+3.3V††
†† pulled high via 10KΩ resistor.			

Table A-11 PMC Connector J12 and J22 Pin-out

NOTE: REQ B# and GNT B# are provided for use by dual-function PMC modules or Processor-PMC modules on J12 only, they are no connect on J22.

Pin No.	Signal Name	Pin No.	Signal Name
1	-	2	GND
3	GND	4	C/BE(7)#
5	C/BE(6)#	6	C/BE(5)#
7	C/BE(4)#	8	GND
9	V(I/O)	10	PAR64
11	AD(63)	12	AD(62)
13	AD(61)	14	GND
15	GND	16	AD(60)
17	AD(59)	18	AD(58)
19	AD(57)	20	GND
21	V(I/O)	22	AD(56)
23	AD(55)	24	AD(54)
25	AD(53)	26	GND
27	GND	28	AD(52)
29	AD(51)	30	AD(50)
31	AD(49)	32	GND
33	GND	34	AD(48)
35	AD(47)	36	AD(46)
37	AD(45)	38	GND
39	V(I/O)	40	AD(44)
41	AD(43)	42	AD(42)
43	AD(41)	44	GND
45	GND	46	AD(40)
47	AD(39)	48	AD(38)
49	AD(37)	50	GND
51	GND	52	AD(36)
53	AD(35)	54	AD(34)
55	AD(33)	56	GND
57	V(I/O)	58	AD(32)
59	-	60	-
61	-	62	GND
63	GND	64	-

Table A-12 PMC Connector J13 Pin-out

Pin No.	Signal Name	Pin No.	Signal Name
1	I/O 1	2	I/O 2
3	I/O 3	4	I/O 4
5	I/O 5	6	I/O 6
7	I/O 7	8	I/O 8
9	I/O 9	10	I/O 10
11	I/O 11	12	I/O 12
13	I/O 13	14	I/O 14
15	I/O 15	16	I/O 16
17	I/O 17	18	I/O 18
19	I/O 19	20	I/O 20
21	I/O 21	22	I/O 22
23	I/O 23	24	I/O 24
25	I/O 25	26	I/O 26
27	I/O 27	28	I/O 28
29	I/O 29	30	I/O 30
31	I/O 31	32	I/O 32
33	I/O 33	34	I/O 34
35	I/O 35	36	I/O 36
37	I/O 37	38	I/O 38
39	I/O 39	40	I/O 40
41	I/O 41	42	I/O 42
43	I/O 43	44	I/O 44
45	I/O 45	46	I/O 46
47	I/O 47	48	I/O 48
49	I/O 49	50	I/O 50
51	I/O 51	52	I/O 52
53	I/O 53	54	I/O 54
55	I/O 55	56	I/O 56
57	I/O 57	58	I/O 58
59	I/O 59	60	I/O 60
61	I/O 61	62	I/O 62
63	I/O 63	64	I/O 64

Table A-13 PMC Connector J14 Pin-out

A.7.6 XMC Connector J15 Pin-out

Pin No.	Row A	Row B	Row C	Row D	Row E	Row F
1	PET0p0	PET0n0	+3.3V	PET0p1	PET0n1	+5V
2	GND	GND	PULL DOWN	GND	GND	RESET#
3	PET0p2	PET0n2	+3.3V	PET0p3	PET0n3	+5V
4	GND	GND	PULL DOWN	GND	GND	PULL UP
5	PET0p4	PET0n4	+3.3V	PET0p5	PET0n5	+5V
6	GND	GND	PULL UP	GND	GND	+12V
7	PET0p6	PET0n6-	+3.3V	PET0p7	PET0n7	+5V
8	GND	GND	PULL UP	GND	GND	-12V
9	-	-	-	-	-	+5V
10	GND	GND	-	GND	GND	GA0
11	PER0p0	PER0n0	MBIST#	PER0p1	PER0n1	+5V
12	GND	GND	GA1	GND	GND	PRSNT#
13	PER0p2	PER0n2-	+3.3V	PER0p3	PER0n3	+5V
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	-	PER0p5	PER0n5	+5V
16	GND	GND	PULL UP	GND	GND	MSCL
17	PER0p6	PER0n6	-	PER0p7	PER0n7	-
18	GND	GND	-	GND	GND	-
19	REFCLK+	REFCLK-	-	WAKE#	-	-

Table A-14 XMC Connector J15 Pin-out

NOTE: The terminology in the above table matches that used in the XMC specification, VITA 42.3. The PET0xx signals are used to receive data from the XMC module (i.e. they are the XMC module's transmit signals). The PER0xx signals are used to send data to the XMC module (i.e. they are the XMC module's receive signals).

A.7.7 Ethernet Interfaces J1 and J2 Pin-outs

The Ethernet interfaces (J1 and J2) use 8-way RJ45 connectors with signals assigned as follows:

Pin No.	Signal Name
1	DA
2	DA#
3	DB
4	DC
5	DC#
6	DB#
7	DD
8	DD#

Table A-15 Ethernet Interfaces J1 and J2 Pin-out

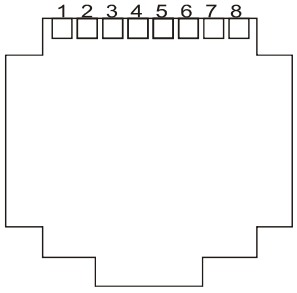


Figure A-3 Ethernet Interfaces J1 and J2 Pin Map

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B REAR TRANSITION MODULES

B.1 Introduction

This section details Rear Transition Modules (RTMs) available for use with the VX 511/06x. Each RTM provides a means of connecting interface cables to the rear I/O of the VX 511/06x.

All RTMs utilize a 5-row P2 for rear I/O connection. For a 3-row backplane only the PMC rear I/O interface is available.

An overview of each RTM is given with references to the pin-out tables for each of the connectors identified.

B.2 RTM List

The following RTMs are suitable for use with the VX 511/06x:-

Sales Part No.	Board Number (as marked on PCB)
AD VP2/018-10	721-6238-10
AD VP2/018-30	721-6238-11
AD VP2/024-10	721-6268-10
AD VP2/024-30	721-6268-11

Table B-1 RTM List

REAR TRANSITION MODULES

B.3 AD VP2/018-10

The AD VP2/018-10 is a 160-way P2 RTM for the VX 511/06x. It provides two SATA ports, a PS/2 combined keyboard and mouse connector, two USB connectors, one VGA connector, one 68-way SCSI-3 style socket for PMC I/O, one 10-way IDC header and one DB9 connector for serial ports (RS232), header pins for Speaker and header pins for General Purpose I/O. Switches are provided to configure the Automatic VGA Detection, GPI00 and GPI01 and selected pins on the PMC I/O connectors.

This RTM requires one slot width and a minimum of 115mm behind the backplane.

B.3.1 Layout

Figure B-1 shows the locations of the connectors, headers and switches. Figure B-2 describes the switch settings.

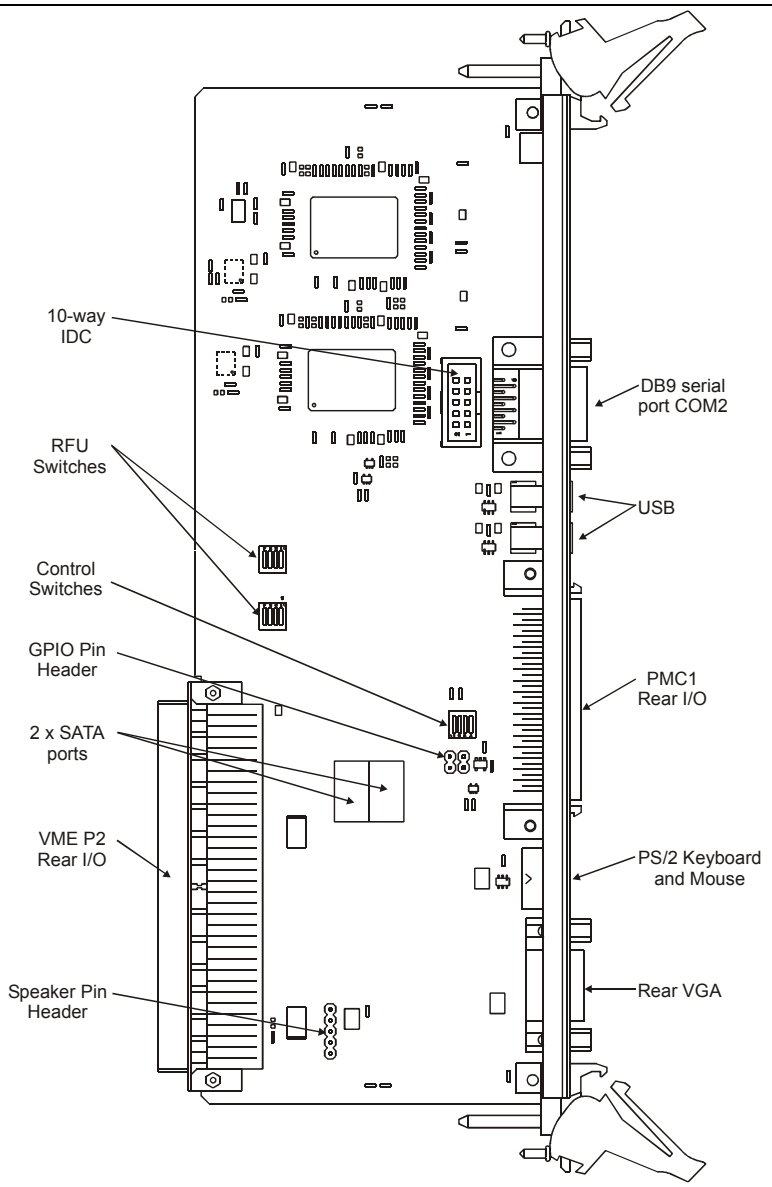


Figure B-1 AD VP2/018-10 RTM - Connectors and Switches

B.3.2 Pin-out Tables

USB0 and USB1	Table B-2
Keyboard and Mouse	Table B-3
Serial I/O	Table B-5
DB9 Serial COM port	Table B-6
GPIO	Table B-7
PMC I/O	Table B-8
VGA	Table B-9
Speaker	Table B-10
SATA 3 and 4	Table B-11

B.3.3 Switch Settings

Pins 19 and 53 of the PMC I/O connectors have no function on this board and are normally not connected. However, to improve signal quality on the connecting cable it may be preferable to connect these pins to ground. The PMC I/O Ground switch shown in Figure B-2 allows the user to do this.

The GPIO switches shown in Figure B-2 provide a configurable input as described in Section 9.5.

In order to detect a VGA monitor during start up there is an automatic switch provided to give an artificial 75Ω load to the VGA_GREEN signal. A switch, as shown in Figure B-2, is available to disable this feature.

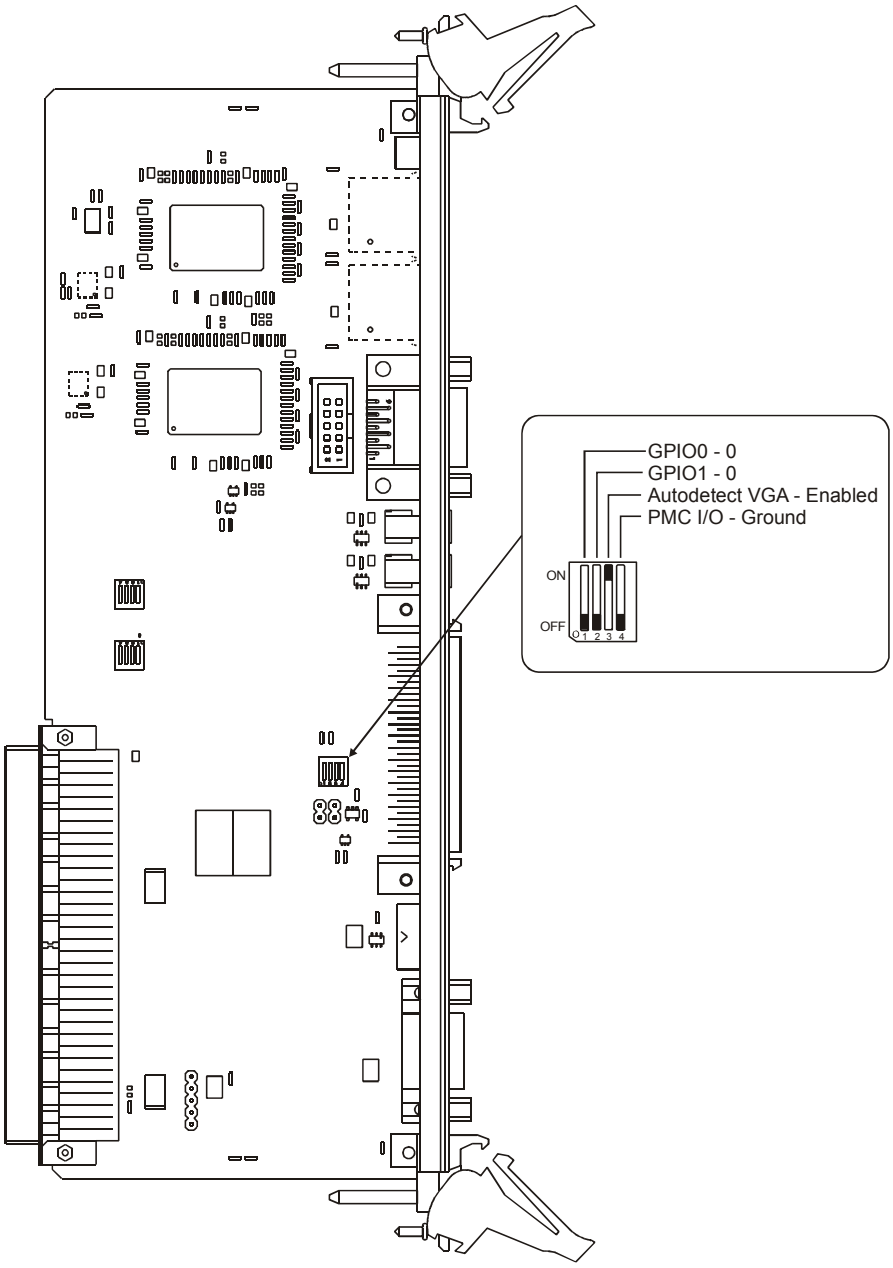


Figure B-2 AD VP2/018-10 RTM - Switch Settings

B.4 AD VP2/018-30

The AD VP2/018-30 is a 160-way P2 plus P0 RTM for the VX 511/06x. As well as all interfaces available on the AD VP2/018-10, it provides two RJ45 1000 Mbits/s Ethernet connectors and additional switches for Ethernet signal routing.

This RTM requires one slot width and a minimum of 115mm behind the backplane.

B.4.1 Layout

Figure B-3 shows the locations of the connectors, headers and switches. Figure B-4 shows the switch settings.

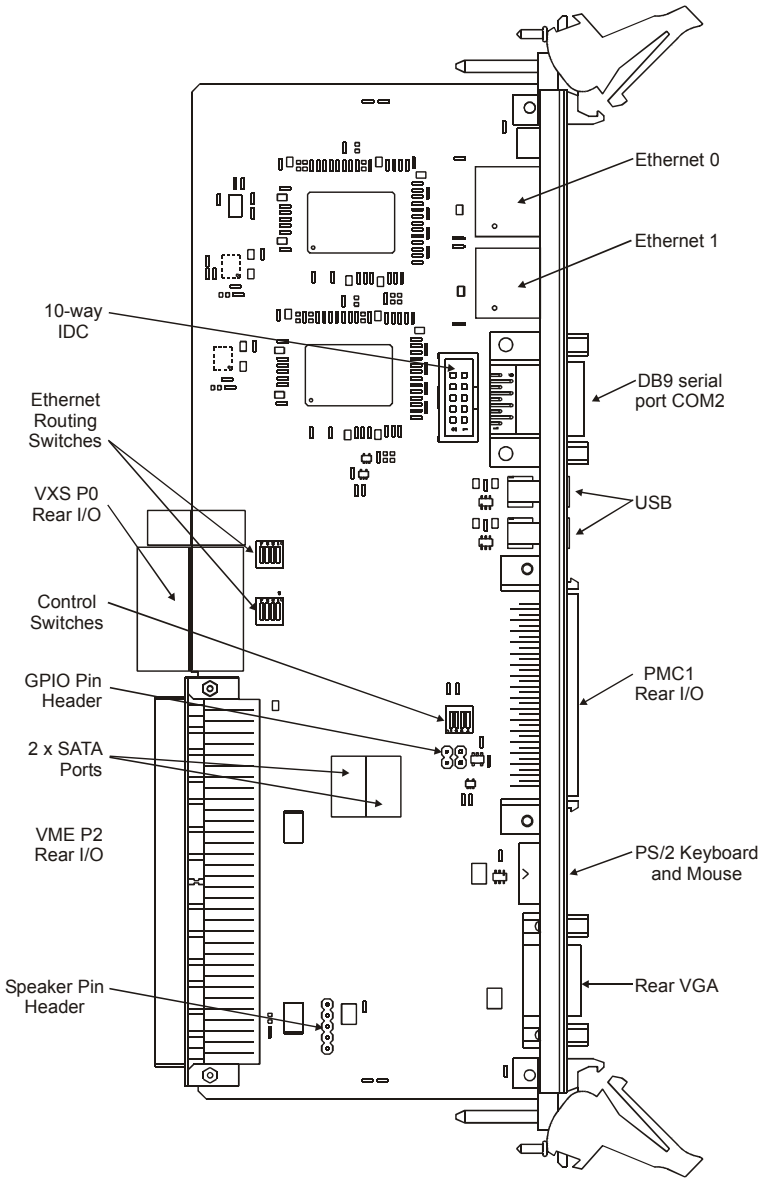


Figure B-3 AD VP2/018-30 RTM - Connectors and Switches

B.4.2 Pin-out Tables

USB0 and USB1	Table B-2
Keyboard and Mouse	Table B-3
Ethernet RJ-45	Table B-4
Serial I/O	Table B-5
DB9 Serial COM port	Table B-6
GPIO	Table B-7
PMC I/O	Table B-8
VGA	Table B-9
Speaker	Table B-10
SATA 3 and 4	Table B-11

B.4.3 Switch Settings

Pins 19 and 53 of the PMC I/O connectors have no function on this board and are normally not connected. However, to improve signal quality on the connecting cable it may be preferable to connect these pins to ground. The PMC I/O Ground switch shown in Figure B-4 allows the user to do this.

The GPIO switches shown in Figure B-4 provide a configurable input as described in Section 9.5.

In order to detect a VGA monitor during start up there is an automatic switch provided to give a visible 75Ω load to the VGA_GREEN signal during start up. A switch, shown in Figure B-4, is available to disable this feature.

Additional switches, as shown in Figure B-4, are provided to route Ethernet signals to the rear RJ45 connectors instead of being used for Backplane networking (VITA 41.6).

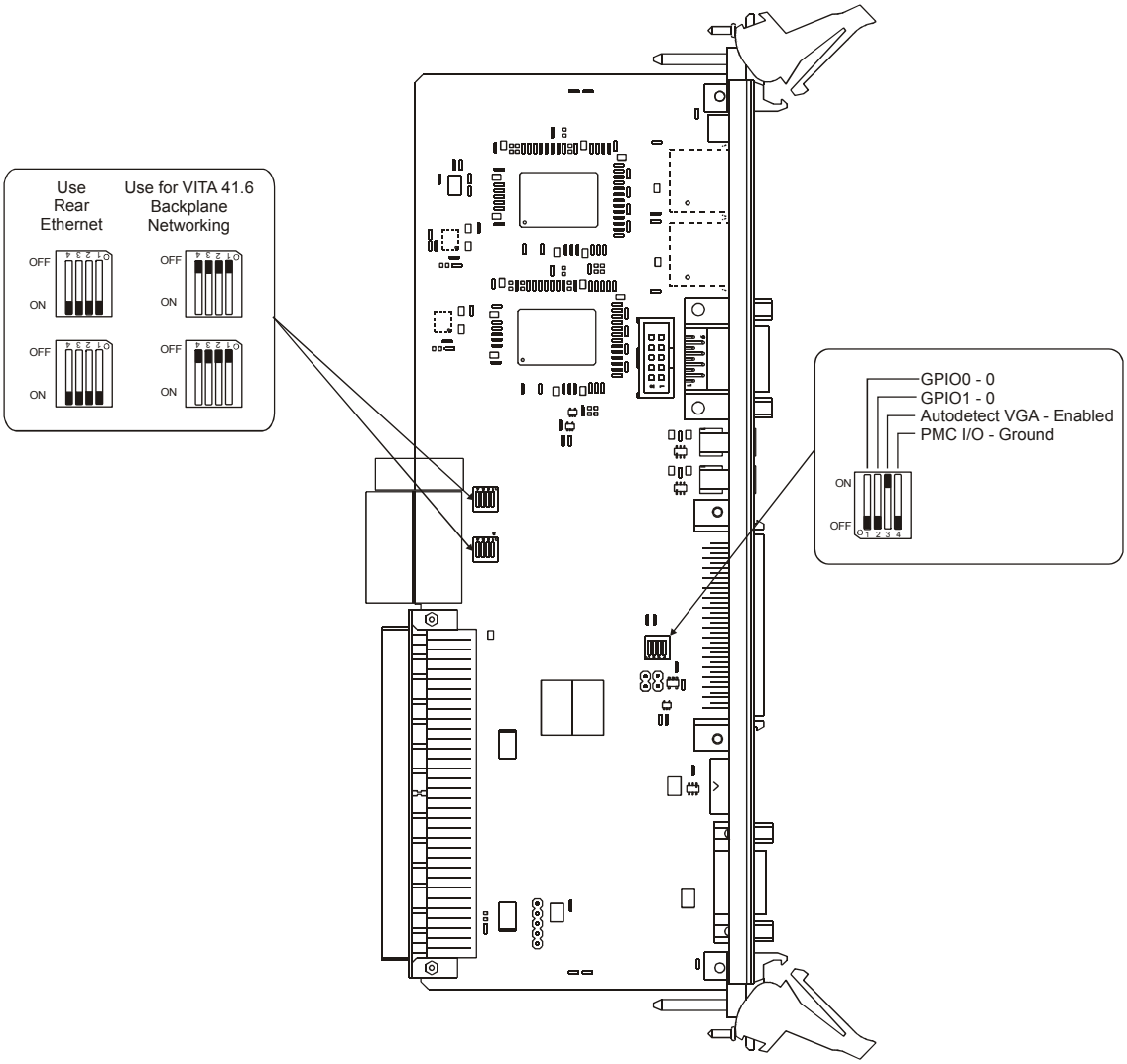


Figure B-4 AD VP2/018-30 RTM - Switch Settings

B.5 AD VP2/024-10

The AD VP2/024-10 is a 160-way P2 RTM for the VX 511/06x. It provides two on-board SATA ports (which are individually selectable and can be re-routed to front panel eSATA ports), one PS/2 combined keyboard and mouse connector, two USB connectors, one VGA graphic connector, one 68-way SCSI-3 style socket for PMC I/O, one 10-way IDC header and one DB9 for serial port (RS232 level), header pins for Speaker, header pins for two GPIOs and two optional DIP switches for extended GPIO (using the two GPIO pins and the software driver – see Section 9.10 for more details).

This RTM requires one slot width and a minimum of 115mm behind the backplane.

B.5.1 Layout

Figure B-5 shows the locations of the connectors, headers, jumpers and switches. Figure B-6 describes the switch settings.

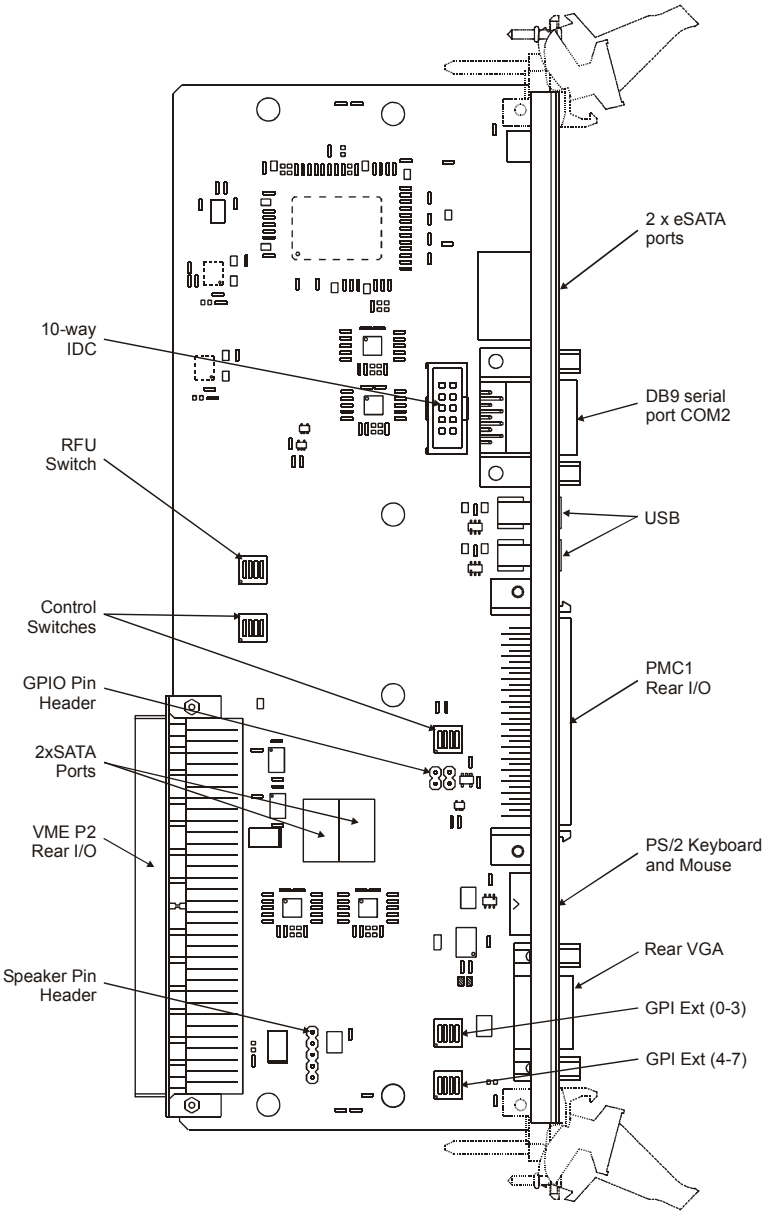


Figure B-5 AD VP2/024-10 RTM – Connector Layout

B.5.2 Pin-out Tables

USB0 and USB1	Table B-2
Keyboard and Mouse	Table B-3
Serial I/O	Table B-5
DB9 Serial COM port	Table B-6
GPIO	Table B-7
PMC I/O	Table B-8
VGA	Table B-9
Speaker	Table B-10
SATA 3 and 4	Table B-11
eSATA 3 and 4	Table B-12

B.5.3 Switch settings

Pins 19 and 53 of the PMC I/O connectors have no function on this board and are normally not connected. However, to improve signal quality on the connecting cable it may be preferable to connect these pins to ground. The PMC I/O Ground jumpers shown in Figure B-6 allow the user to do this.

The GPIO switch shown in Figure B-6 provides a configurable input as described in Section 9.5.

The optional 8-bit GPI switches provide additional General Purpose Inputs as described in Section 9.10.

In order to detect the VGA monitor properly during start-up, there is an automatic detection switch to give artificial 75Ω to the VGA_GREEN signal. A switch as shown on the Figure B-6 is provided to disable this feature.

The SATA signals from the VME P2 connector may be routed independently for each port to either the front panel eSATA connector or the on-board SATA connector.

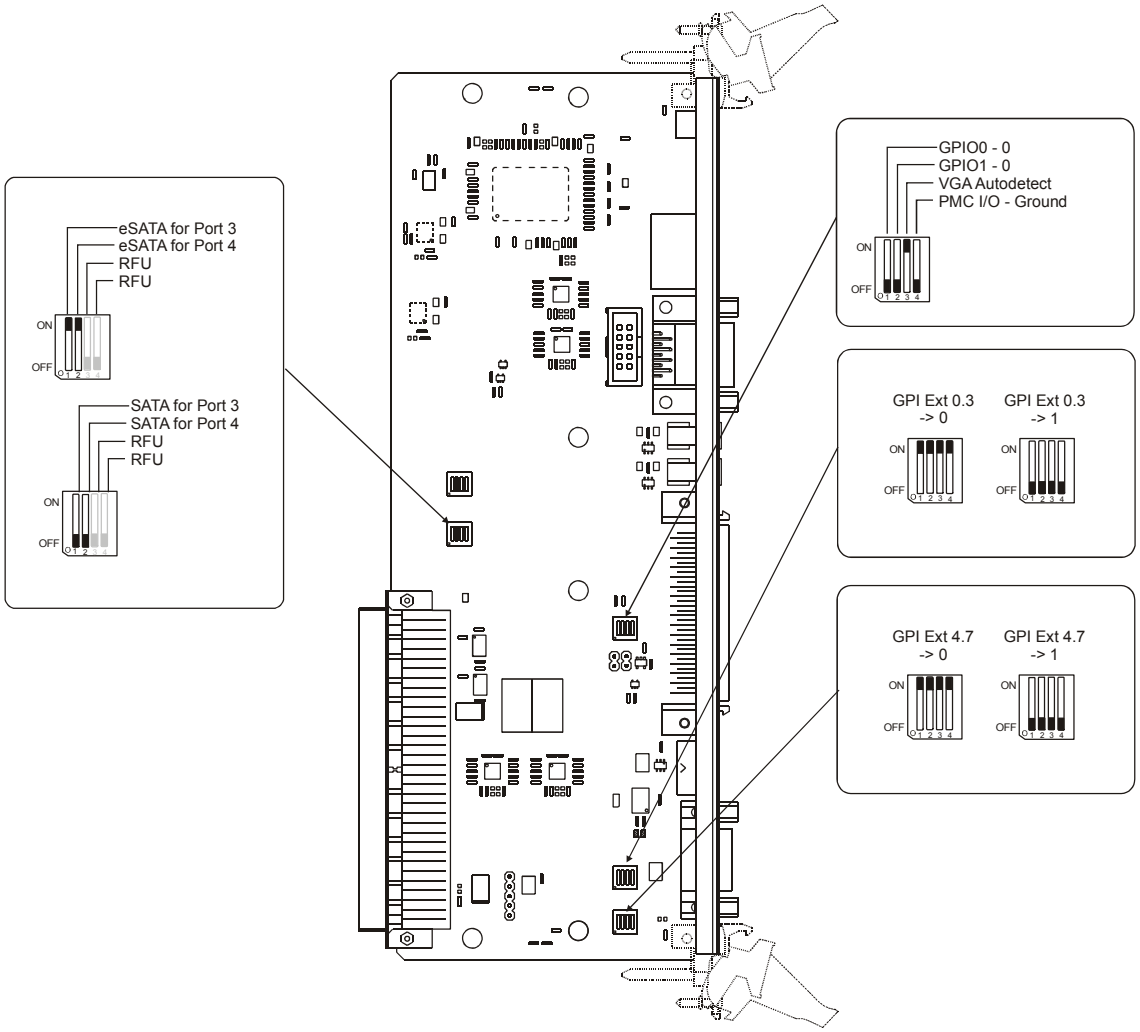


Figure B-6 AD VP2/024-10 RTM - Switch Settings

B.6 AD VP2/024-30

The AD VP2/024-30 is a 160-way P2 plus P0 backplane RTM for the VX 511/06x. It provides the same interfaces as the AD VP2/024-10 plus an additional RJ45 1000 Mbits/s Ethernet connector with additional switches for Ethernet signal routing.

This RTM requires one slot width and a minimum of 115mm behind the backplane.

B.6.1 Layout

Figure B-7 shows the locations of the connectors, headers, jumpers and switches. Figure B-8 describes jumper and switch settings.

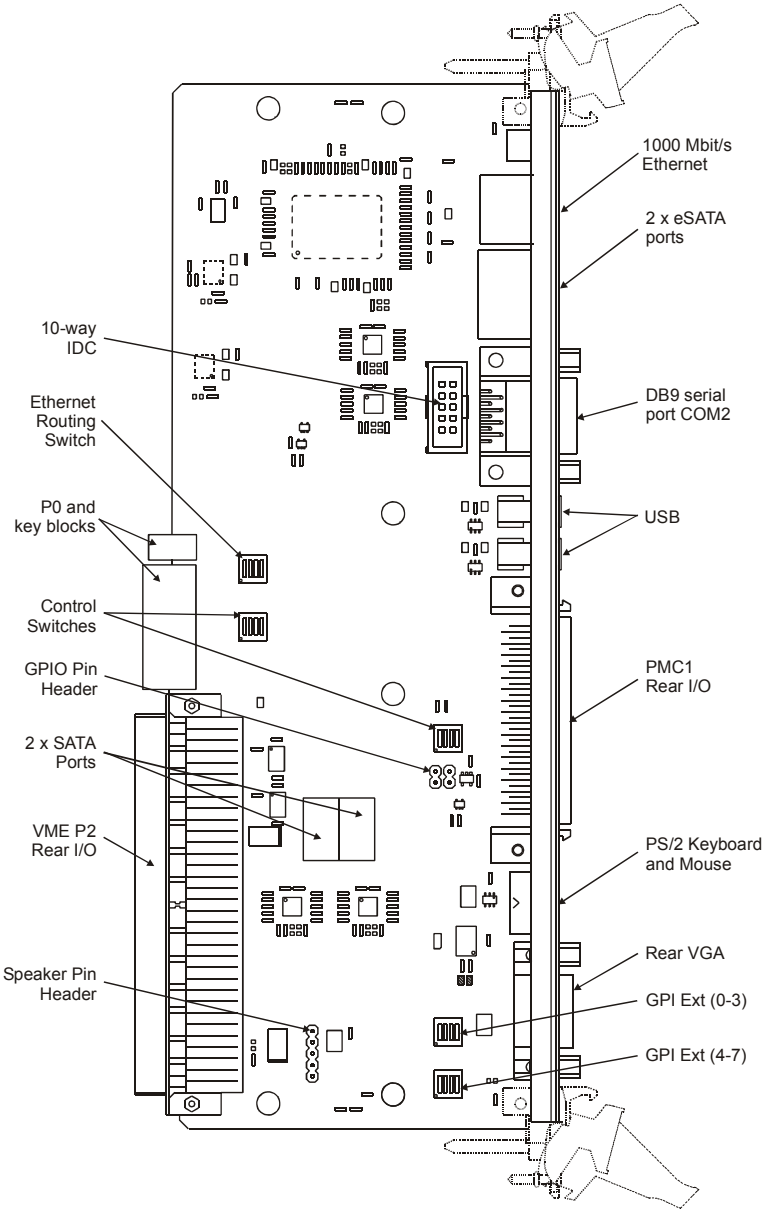


Figure B-7 AD VP2/024-30 RTM – Connector Layout

B.6.2 Pin-out Tables

USB0 and USB1	Table B-2
Keyboard and Mouse	Table B-3
Ethernet RJ45	Table B-4
Serial I/O	Table B-5
DB9 Serial COM port	Table B-6
GPIO	Table B-7
PMC I/O	Table B-8
VGA	Table B-9
Speaker	Table B-10
SATA 3 and 4	Table B-11
eSATA 3 and 4	Table B-12

B.6.3 Switch settings

Additional switches, as shown on Figure B-8, are provided to route Ethernet signals to the rear RJ45 Ethernet instead of backplane networking.

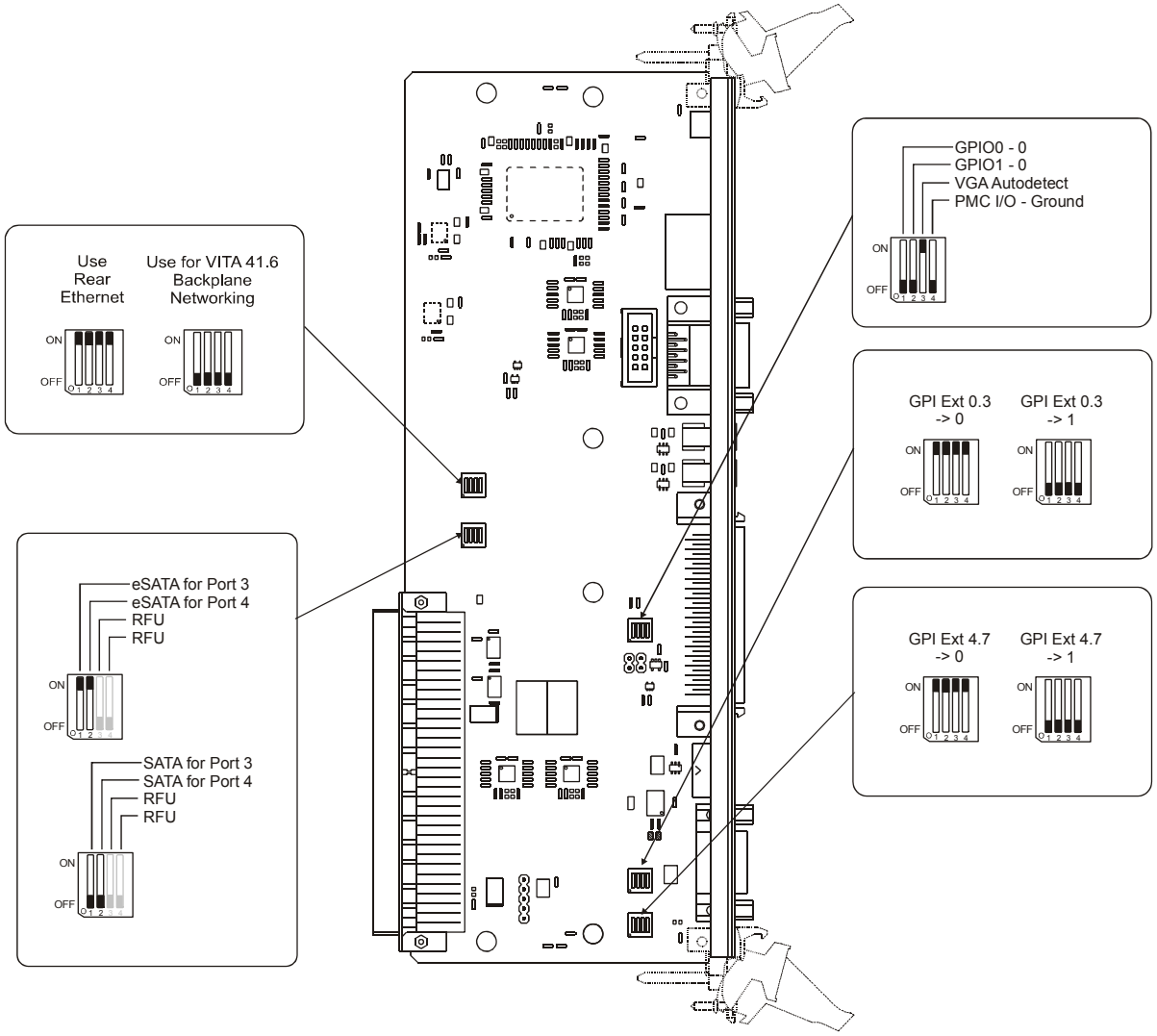


Figure B-8 AD VP2/024-30 RTM - Switch Settings

B.7 Header/Connector Pin-out Tables

The headers and connectors are designed to enable use of standard P.C. interface cables wherever possible. Detailed below are the pin-outs of the headers and connectors used on the RTMs.

Pin No.	Signal Name
1	USB_VCC
2	USBD-
3	USBD+
4	USB GND
SHIELD	CHASSIS GND

Table B-2 USB Connectors

Pin No.	Signal Name
1	KBD_DATA#
2	MS_DATA#
3	GND
4	KBD_PWR
5	KBD_CLOCK#
6	MS_CLOCK#
SHELL	CHASSIS GND

Table B-3 Keyboard and Mouse Connector

Pin No.	Signal Name
1	DA
2	DA#
3	DB
4	DC
5	DC#
6	DB#
7	DD
8	DD#

Table B-4 Ethernet RJ-45 Connectors

Pin No.	Signal	Pin No.	Signal
1	DCD	2	DSR
3	RX	4	RTS
5	TX	6	CTS
7	DTR	8	RI
9	RETURN	10	RETURN

Table B-5 Serial I/O IDC Headers

Pin No.	Signal	Pin No.	Signal
1	DCD	6	DSR
2	RX	7	RTS
3	TX	8	CTS
4	DTR	9	RI
5	RETURN		

Table B-6 DB9 Serial COM port

Pin No.	Signal
1	GPIO0
2	GPIO1
3	GND
4	GND

Table B-7 GPIO Pins

Pin No.	Signal Name	Pin No.	Signal Name
1	I/O 1	35	I/O 2
2	I/O 3	36	I/O 4
3	I/O 5	37	I/O 6
4	I/O 7	38	I/O 8
5	I/O 9	39	I/O 10
6	I/O 11	40	I/O 12
7	I/O 13	41	I/O 14
8	I/O 15	42	I/O 16
9	I/O 17	43	I/O 18
10	I/O 19	44	I/O 20
11	I/O 21	45	I/O 22
12	I/O 23	46	I/O 24
13	I/O 25	47	I/O 26
14	I/O 27	48	I/O 28
15	I/O 29	49	I/O 30
16	I/O 31	50	I/O 32
17	I/O 33	51	I/O 34
18	-	52	-
19	GND†	53	GND†
20	I/O 35	54	I/O 36
21	I/O 37	55	I/O 38
22	I/O 39	56	I/O 40
23	I/O 41	57	I/O 42
24	I/O 43	58	I/O 44
25	I/O 45	59	I/O 46
26	I/O 47	60	I/O 48
27	I/O 49	61	I/O 50
28	I/O 51	62	I/O 52
29	I/O 53	63	I/O 54
30	I/O 55	64	I/O 56
31	I/O 57	65	I/O 58
32	I/O 59	66	I/O 60
33	I/O 61	67	I/O 62
34	I/O 63	68	I/O 64
† a switch is provided to either leave these pins disconnected or to connect them to ground. See Sections B.3.3, B.4.3. and B.5.3.			

Table B-8 PMC I/O Connectors (68-way D-Type)

Pin No.	Signal Name
1	Analog Red Output
2	Analog Green Output
3	Analog Blue Output
4	-
5	Ground
6	Analog Ground
7	Analog Ground
8	Analog Ground
9	-
10	Ground
11	-
12	DDC Data
13	Horizontal Sync
14	Vertical Sync
15	DDC Clock

Table B-9 VGA Connector Pin-outs

Pin No.	Signal
1	VCC
2	GND
3	NC
4	SPKR
5	NC

Table B-10 PC Speaker Header

Pin No.	Signal Name	Pin No.	Signal Name
1	GND	8	GND
2	SATA0_TX+	9	SATA1_TX+
3	SATA0_TX-	10	SATA1_TX-
4	GND	11	GND
5	SATA0_RX-	12	SATA1_RX-
6	SATA0_RX+	13	SATA1_RX+
7	GND	14	GND

Table B-11 SATA Connector Pin-out

Pin No.	Signal Name	Pin No.	Signal Name
1	GND (0V)	8	GND (0V)
2	eSATA0 Tx+	9	eSATA1_TX+
3	eSATA0 Tx-	10	eSATA1_TX-
4	GND (0V)	11	GND (0V)
5	eSATA0 Rx-	12	eSATA1_RX-
6	eSATA0 Rx+	13	eSATA1_RX+
7	GND (0V)	14	GND (0V)

Table B-12 eSATA Connector Pin-out

C.1 Introduction

The main manual provides information relating to all air-cooled variants of the VX 511/06x, namely N-Series, E-Series, K-Series and RA-Series. The Ruggedized Conduction-Cooled (RC-Series) has significant differences to the other Series of products and for clarity these differences are detailed in this Appendix. However, the RC-Series has much in common with the other variants and the main body of this manual still applies for all aspects not covered in this Appendix.

C.2 Ruggedized Conduction-Cooled (RC-Series) Features

Figure C-1 shows an overview of the ruggedized conduction-cooled board.

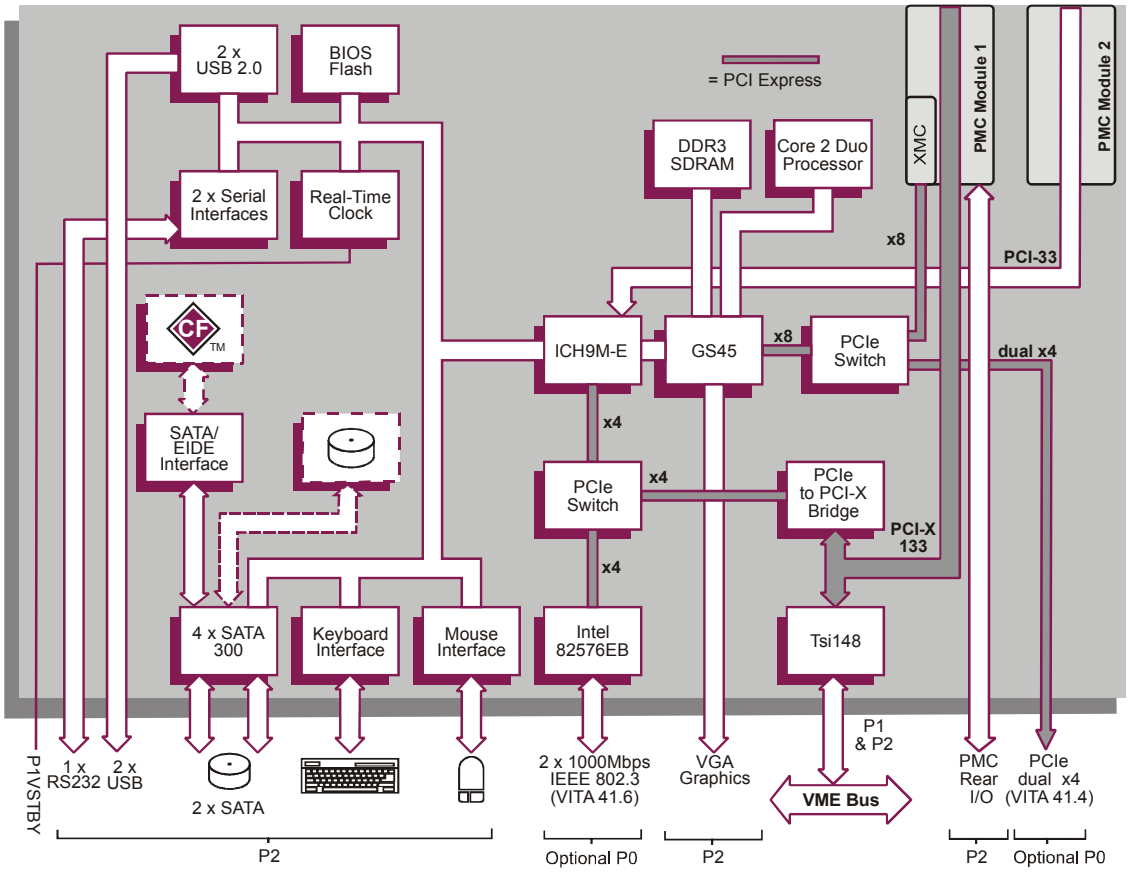


Figure C-1 Overview of Ruggedized Conduction-Cooled Boards

RC-SERIES

The main VX 511/06x features that are detailed in section 1.3 apply to the RC-Series except for the differences detailed below:

1) RC-Series are only available with 1.86 GHz Intel Core 2 Duo processors.
2) There are no front panel interface connectors; therefore functions that are usually accessible via the front panel are not supported. However, the circuits for these functions may still be present and firmware may still report their presence. The removal of the front panel specifically changes the RC features to the following:-
   - One RS232 serial port is provided via P2 connector, COM1 is not supported.
   - Two USB ports via P2 connector.
   - Ethernet channel 1 and 2 are not available and are switched off by the BIOS. Ethernet channels 3 and 4 are available via P0.
   - No on-board battery for the real-time clock and BIOS CMOS settings is provided. There is provision to use VME bus VCC_STANDBY supply for maintaining the clock and settings when board power is removed, see Section 2.5.
   - The PMC/XMC sites only accept modules designed for conduction cooling.
   - PMC sites V(I/O) settings are factory configured.

C.3 RC-Series Installation

Section 2 of this manual specifies the overall process of board configuration, installation and extraction, but there are some areas of the process which are unique for the RC-Series, and these are detailed in the following sections.

C.3.1 Board Front Edge LED Indicators

Figure C-3 shows the location and purpose of the LEDs situated along the bottom side of the board's front edge. See Section 2.4 for a description of these LEDs.

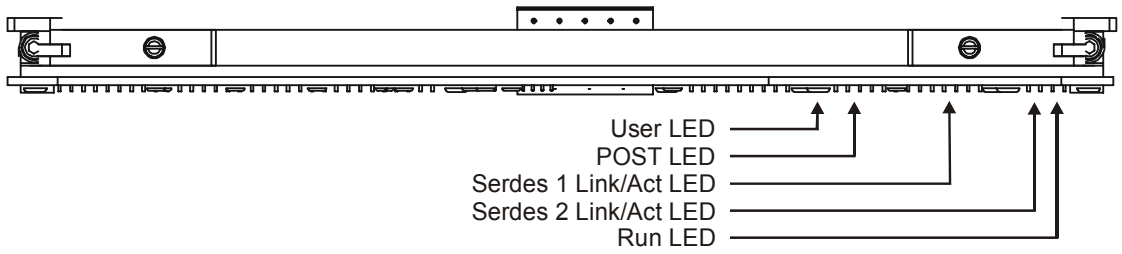


Figure C-2 RC Variant – Front Edge LED Indicators

C.3.2 Configuration for PMC or XMC module

For the PMC sites PCI bus mode and speed selection, see Section 2.8.2.

The VX 511/06x-RC board has a soldered jumper wire to select 3.3V or 5V V(I/O) to both PMC sites – default selection is by product order code as indicated on the VX 511/06x-RC datasheet. Before installing a PMC module check that the board's PMC V(I/O) is configured to match the requirements and/or configuration of the PMC Modules being used.

NOTE: When V(I/O) is configured for 5V, both PMC sites will have voltage polarizing keys in the 5V position. When V(I/O) is configured for 3.3V, PMC site 1 will have a polarizing key fitted in the 3.3V position and PMC site 2 will have no polarizing key fitted.

C.3.3 Installation Instructions for XMC and PMC modules

NOTE: Only PMC or XMC modules which have been designed for conduction cooling should be used with the VX 511/06x-RC. These can normally be identified by a conduction strip along the front, middle and rear of the PMC or XMC, which will conduct heat generated by the module into the VX 511/06x-RC.

NOTE: When using the VX 511/06x-RC, only PMC or XMC modules which meet the required standard for shock and vibration should be used.

NOTE: To improve cooling, a thermal conducting paste can be applied to contact the surfaces of the PMC or XMC module and base board conduction frame.

NOTE: To improve mechanical retention, apply a thread lock compound to all screws.

1) For XMC installations, remove the polarizing key, if fitted.
2) Check that the standoffs are attached to the PMC or XMC. Align the standoffs and the holes at the front, middle and rear of the PMC or XMC with the matching holes on the VX 511/06x-RC
3) Lower the PMC or XMC, component side down, fitting the connectors into their mating connectors on the VX 511/06x-RC. Press them together so that the friction from the pins holds the PMC or XMC in place.
4) Screw the PMC or XMC in place using 5 mounting screws in the top of the front panel, 5 along the conducting strip and 2 on the underside of the board in the standoffs.

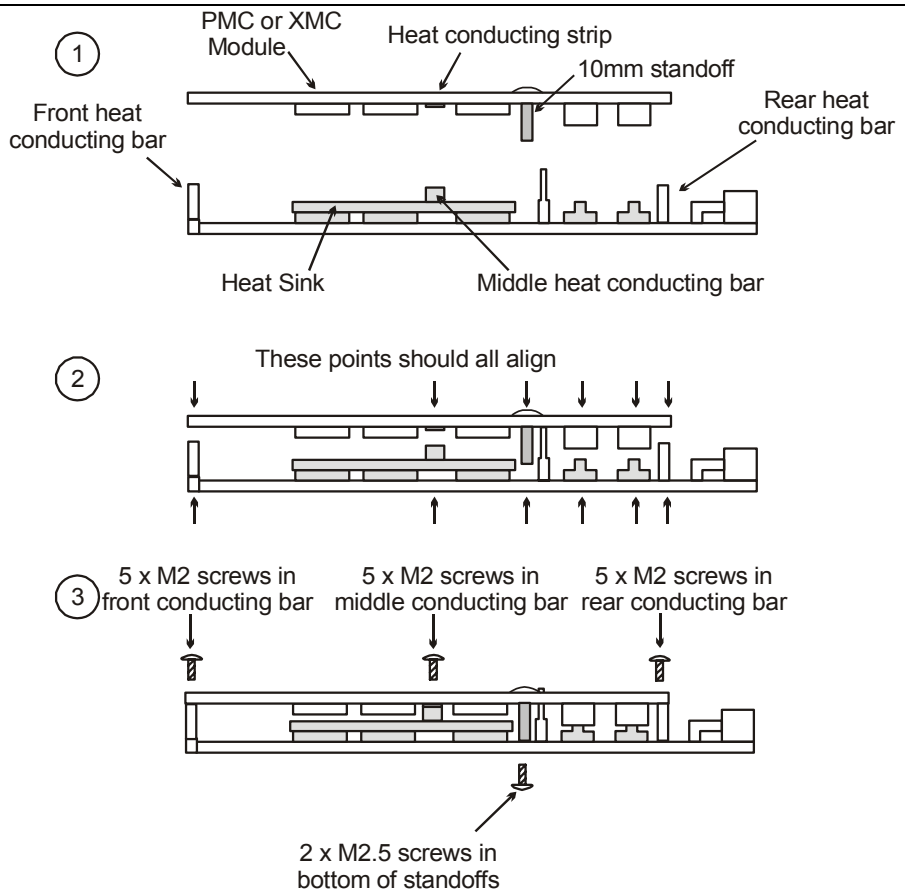


Figure C-3 RC Variant - PMC/XMC Installation Diagram

C.4 Specification

The product specifications in Section A apply to the RC-Series except for the functional description and connector layout which are detailed below.

C.4.1 Functional Description

Processor:	• 1.86 GHz Intel Core 2 Duo processor on 45 nm process.
Level 1 Cache:	• 32 Kbytes instruction cache and 32 Kbytes data cache.
Level 2 Cache:	• 6 Mbytes on-die RAM operating at core frequency.
Memory:	• 4 Mbyte SPI Flash EPROM for PC BIOS and other firmware. • Up to 6 Gbytes DDR3-1066 SDRAM as defined by order number.
Interfaces:	• 64-bit VME interface utilizing the Tundra Tsi-148 VME-to-PCI-X bridge supporting up to 2eSST and 2eVME. • Dual x4-lane PCIe links connected to P0 to support VXS VITA 41.4 backplane control plane. • One RS232 serial channel via rear P2 connector using 16550 compatible UART. Full set of signals. • Two SATA300 interfaces via rear P2 connector. • One SATA300 to support on-board mass storage option interface. • PS/2 keyboard and mouse interfaces via rear P2 connector. • Two USB interfaces via rear P2 connector. Both USB 1.1 (1.5 and 12 Mbits/s) and USB 2.0 (480 Mbits/s) operation are supported. • One single-width PMC site supporting 64/32-bit 66/33 MHz PCI or 66/100/133 MHz PCI-X interface with 3.3V or 5V signaling. Both 5V and 3.3V power rails are provided. • One single-width PMC site supporting 32-bit 33 MHz PCI interface with 3.3V or 5V signaling. Both 5V and 3.3V power rails are provided. • One 8-lane XMC interface on PMC Site 1. • Two Gigabit SERDES interface using 82576EB Ethernet controllers with 10/100/1000 Mbits/s connections via rear P0 to support backplane networking according to VXS VITA 41.6. Optionally the SERDES interfaces can be used to support rear panel Gigabit Ethernet port using an appropriate RTM. • External Push Button Reset input via rear P2. • Two general purpose I/O via rear P2.
Peripherals:	• Intel ICH9M-E device providing standard PC-AT architecture peripherals. • PC-AT Real Time Clock. • 32-bit Periodic Interval Timer with processor interrupt capability.

C.4.2 Connectors

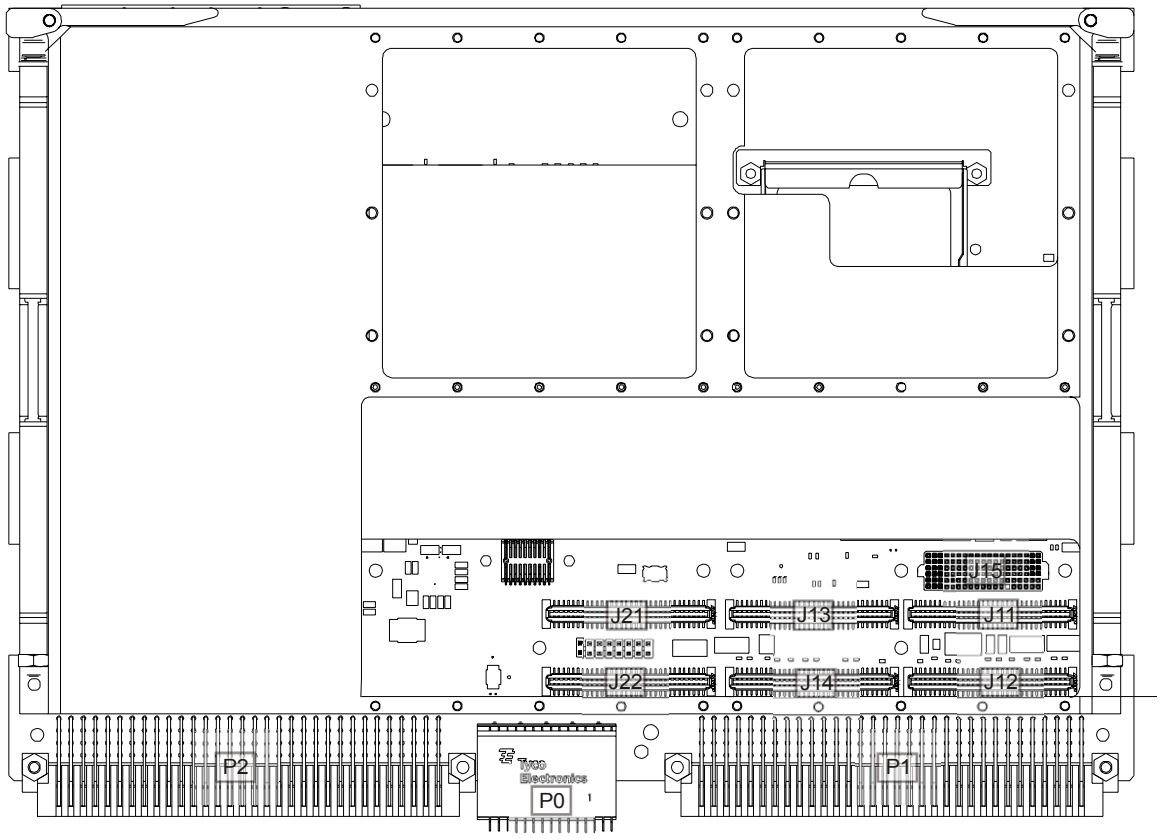


Figure C-4 RC Variant - Connector Layout

See Appendix A for an explanation of connector functions and the pin-out specifications.

D INTERFACE CHARACTERISTICS

This section describes the electrical characteristics of the various interfaces on the P0 and P2 connectors. The connector pin-out tables are given in Sections A.7.2 and A.7.3. This information is provided to enable custom backplanes or RTMs to be designed. For standard signals defined by VXS VITA 41.4, refer to this standard for details – more information is available at http://www.vita.com/specifications.html.

D.1 Ethernet

The VX 511/062-RC provides two Gigabit Ethernet interfaces. Both interfaces support SERDES (1000BASE-BX). They conform to standard IEEE 802.3 specifications with the exception of the isolation voltage being limited to 50V. This limitation is due to the isolation voltage rating of the P0 connector and signal trace spacing on the VX 511/062-RC board.

The 1000BASE-BX differential pair signals on P0 are named SA_TX+/- and SA_RX+/- for the first port and SB_TX+/- and SB_RX+/- for the second port.

Ethernet signal levels are defined in Part 3 of the Ethernet specification. This is available on the IEEE web site as standard IEEE 802.3 at URL is http://standards.ieee.org/getieee802.

The following guidelines apply to backplane routing of the Ethernet signals:-

- Route as differential pairs with 100Ω ±10% differential impedance.
- Route on a GND referenced layer.
- Minimize the number of vias and avoid layer changes if possible.
- Avoid impedance discontinuities such as stubs or bends sharper than 45°.
- Match signal lengths within a pair to within 50 mils (1.25 mm).
- Maintain 50 mils (1.25 mm) separation between pairs.
- Maintain 100 mils (2.54 mm) separation from other signals and from reference plane edges.

INTERFACE CHARACTERISTICS

D.2 General Purpose I/O

The VX 511/062-RC board provides two General Purpose Input and Output (GPIO) signals on the P2 connector. These signals connect to a Xilinx XC95144XL CPLD on the VX 511/062-RC board. They may be independently programmed as either inputs or outputs.

The GPIO signals have the following characteristics:-

- The input and output levels are 3.3V CMOS. The signals are 5V tolerant when programmed as inputs. Refer to the CPLD datasheet for details of output drive capability.
- The signals have 10k ohm pull-up resistors to 3.3V and clamp diodes to VCC (5V) and GND.

The XC95144XL datasheet is available on the Xilinx web site. The URL is http://www.xilinx.com.

The GPIO is a non-critical interface and there are no specific backplane routing guidelines.

D.3 Keyboard & Mouse

The VX 511/062-RC board provides PS/2 keyboard and mouse interfaces on the P2 connector. The signals are described in Table D-1.

Signal	P2 Pin	Direction	Signal Levels	Details
KBD_DAT	D24	Bidirectional	Note 1	Keyboard data
KBD_CLK	D23	Bidirectional	Note 1	Keyboard clock
MS_DAT	D27	Bidirectional	Note 1	Mouse data
MS_CLK	D26	Bidirectional	Note 1	Mouse clock

Table D-1 Keyboard & Mouse Interface Signals

NOTES:
1) The signals are open drain and have 5KΩ pull-up resistors to 5V on the VX 511/062-RC board.
2) A 5V supply is required to operate the keyboard and/or mouse.

The PS/2 keyboard and mouse are non-critical interfaces and there are no specific backplane routing guidelines.

D.4 PMC Rear I/O

The VX 511/062-RC board provides PMC rear I/O on the P2 connector with 64-bits of rear I/O from PMC site 1.

The rear I/O signals from PMC site 1 are routed on the VX 511/062-RC board as differential pair signals with a differential impedance of 100Ω. The pairs are formed from PMC_IO(1) and PMC_IO(2), PMC_IO(3) and PMC_IO(4), and so on. Track lengths are loosely matched in the range 140 mm to 158 mm.

Signal directions and signal levels depend upon the PMC or XMC modules that are fitted.

It is not possible to offer backplane routing guidelines as this is PMC/XMC module and application dependent.

D.5 SATA

The VX 511/062-RC provides two SATA interfaces on the P2 connector. Each interface consists of differential pairs called SATA3_XX± for the first port and SATA4_XX± for the second port. The interfaces are implemented in the ICH9 chip and support second generation SATA operation (i.e. 3.0 Gbits/s signaling).

SATA signal levels are defined in the SATA specification which is available on the Serial ATA International Organization web site at http://www.serialata.org.

The following guidelines apply to backplane routing of the SATA signals:-

- Route as differential pairs with 100Ω ±10% differential impedance.
- Route on a GND referenced layer.
- Minimize the number of vias and avoid layer changes if possible.
- Avoid impedance discontinuities such as stubs or bends sharper than 45°.
- Match signal lengths within a pair to within 10 mils (0.25 mm).
- Maintain 50 mils (1.25 mm) separation between pairs.
- Maintain 100 mils (2.54 mm) separation from other signals and from reference plane edges.

The VX 511/062-RC board has AC coupling capacitors on the SATA signals. However, if a SATA device (such as a SATA repeater or a SATA-to-IDE bridge) is to be located directly on the backplane, then the backplane must provide the necessary AC coupling capacitors. This consideration does not apply to SATA drives, as they will already be fitted with AC coupling capacitors.

D.6 Serial Ports

The VX 511/062-RC provides one serial port on the P2 connector. This port supports the full set of modem control signals, which are buffered to RS232 levels.

The COM serial port signals are described in Table D-2.

Signal	P2 Pin	Direction	Signal Levels	Details RS232
TXD2#	Z1	Output	RS232	Transmit Data
RXD2#	Z3	Input	RS232	Receive Data
RTS2	Z5	Output	RS232	Request to Send
CTS2	Z7	Input	RS232	Clear to Send
DTR2	Z9	Output	RS232	Data Terminal Ready
DSR2	Z11	Input	RS232	Data Set Ready
DCD2	Z13	Input	RS232	Data Carrier Detect
RI2	Z15	Input	RS232	Ring Indication

Table D-2 COM Serial Port Signals

The RS232 specifications are available on the Electronic Industries Alliance web site at http://www.eia.org.

An Intersil ISL4241E is used to buffer the signals, and the ISL4241E datasheet is available on the Intersil web site at http://www.instersil.com.

The serial port signals are low speed and are not critical. For RS232 operation there are no specific backplane routing guidelines.

D.7 USB

The VX 511/062-RC board provides two USB interfaces on the P2 connector. Each USB interface consists of a differential signal pair, named USBP1± and USBP2±. The interfaces are implemented in the ICH9 chip, support both USB 1.1 and USB 2.0 operation and can operate at 1.5 Mbits/s, 12 Mbits/s or 480 Mbits/s.

The USB specification is available on the USB Implementers Forum web site. The URL is http://www.usb.org/home.

The following guidelines apply to backplane routing of the USB signals:-

- Route as differential pairs with 90Ω ±10% differential impedance.
- Route on a GND referenced layer.
- Minimize the number of vias and avoid layer changes if possible.
- Avoid impedance discontinuities such as stubs or bends sharper than 45°.
- Match signal lengths within a pair to within 100 mils (2.54 mm).
- Maintain 20 mils (0.5 mm) separation between pairs.
- Maintain 100 mils (2.54 mm) separation from other signals.
- Maintain 100 mils (2.54 mm) separation from reference plane edges.

The VX 511/062-RC board does not have any ESD protection circuitry on the USB signals. Consideration should be given to providing ESD protection circuitry on the backplane. For maximum effectiveness, the protection circuitry is normally located as close as possible to the external connector.

There are no specific routing guidelines for the VCC_USBn (USB power) connections, but the traces should be capable of carrying up to 500mA current with a minimal voltage drop.

D.8 VGA Graphics

The VX 511/062-RC board provides a VGA graphics interface on the P2 connector. The VGA signals are described in Table D-3.

Signal	P2 Pin	Direction	Signal Levels	Details
VGA_RED	Z23	Output	0.7V pp	Analog Red video signal. The VX 511/062-RC board provides a 75Ω termination resistor to GND on this signal. The signal also has low pass filtering and clamp diodes between 1.5V and GND.
VGA_GREEN	Z25	Output	0.7V pp	Analog Green video signal. The VX 511/062-RC board provides a 75Ω termination resistor to GND on this signal. The signal also has low pass filtering and clamp diodes between 1.5V and GND.
VGA_BLUE	Z27	Output	0.7V pp	Analog Blue video signal. The VX 511/062-RC board provides a 75Ω termination resistor to GND on this signal. The signal also has low pass filtering and clamp diodes between 1.5V and GND.
AGND	Z24, Z26, Z28	Ground	GND	Ground for Analog video signals.
VGA_VSYNC	Z31	Output	TTL	Vertical sync signal. The VX 511/062-RC board provides a 33Ω series termination resistor on this signal.
VGA_HSYNC	Z29	Output	TTL	Horizontal sync signal. The VX 511/062-RC board provides a 33Ω series termination resistor on this signal.
VGA_DDCCK	Z19	Bidirectional	5V I^2C	DDC clock signal. This is an Open Drain signal. The VX 511/062-RC board provides a 150Ω series resistor, a 2.4kΩ pull-up resistor to VCC and a voltage limiting circuit on this signal.
VGA_DDCDT	Z21	Bidirectional	5V I^2C	DDC data signal. This is an Open Drain signal. The VX 511/062-RC board provides a 150Ω series resistor, a 2.4kΩ pull-up resistor to VCC and a voltage limiting circuit on this signal.

Table D-3 VGA Interface Signals

The VGA specification was originally defined in the IBM PS/2 Video Subsystem Technical Reference Manual 1992. This document is out of print. The following web page contains a link to a scanned copy of the original manual: http://www.mcamafia.de/pdf/pdfref.htm

The following guidelines apply to backplane routing of the VGA signals.

Signal	Routing Guidelines
VGA_RED VGA_GREEN VGA_BLUE	Route traces with 75Ω ±10% characteristic impedance. Route on an AGND referenced layer or partial layer. Maintain 100 mils (2.54 mm) separation from other interface signals. Maintain 100 mils (2.54 mm) separation from reference plane edges.
AGND	These ground signals should be the reference plane for the analog RGB signals. Connect all three AGND signals. The AGND reference plane should not be connected to GND. This separation should be maintained all along the signal path to the final connector and then to the display device.
VGA_VYNC	Maintain 100 mils (2.54 mm) separation from other signals. Maintain 100 mils (2.54 mm) separation from reference plane edges.
VGA_HSYNC	
VGA_DDCCK	No specific routing guidelines.
VGA_DDCDT	

Table D-4 Guidelines for VGA Interface Signals

D.9 Power On Self Test/Speaker

The Power On Self Test (POST) indication is connected to the PC Speaker port on the Intel ICH9 chipset. A connection for this port is made available via the VME P2 connector. This connection is driven by an open-collector device and can drive a speaker of 32Ω or 64Ω impedance.

D.9.1 Electrical Characteristics

This section describes the electrical characteristics of the speaker output. The speaker output signal is described in Table D-5. Connect the –ve terminal of the speaker to the speaker output and the +ve terminal of the speaker to VCC.

Signal	P2 Pin	Direction	Signal Levels	Details
SPKR	D28	Output	5V Open Collector	Signal connects to VCC via a 100Ω series resistor and has clamp diodes to GND and VCC.

Table D-5 Speaker Signals

The speaker output is a non-critical interface and there are no specific RTM or backplane routing guidelines.

D.10 External Reset

The VX 511/06x supports the VME Push Button Reset input on P2. This signal is normally wired in the backplane to the System Controller slot only. However, it provides a means of resetting a VX 511/06x board in any slot. The External Reset switch (SW2-3) controls the action of this signal. See Section 2.4.8 for further details.

D.10.1 Electrical Characteristics

The External Reset signal (named BKP_RST# on pin D19 of connector P2) is wired to a MAX706 supervisor device on the VX 511/06x. Hence, there is no need for the user to debounce this signal or to provide a minimum active period. The External Reset signal is an open collector input with a 10KΩ pull-up resistor to the 5V rail. To activate the reset, connect the signal to ground or drive it low.

The MAX706 datasheet is available on the Maxim web site. The URL is http://www.maxim-ic.com.

The External Reset input is a non-critical interface and there are no specific RTM or backplane routing guidelines.

D.11 Rear Transition Module Present

This is an active low input signal named TM_DET# on pin D25 of the P2 connector. When asserted, it indicates that the RTM is present.

This signal connects to a Xilinx XC95144XL CPLD on the VX 511/062-RC, and has the following characteristics:-

- The input and output levels are 3.3V CMOS. The signals are 5V tolerant when programmed as inputs. Refer to the CPLD datasheet for details of output drive capability.
- The signals have 10k ohm pull-up resistors to 3.3V and clamp diodes to VCC (5V) and GND.

The XC95144XL datasheet is available on the Xilinx web site. The URL is http://www.xilinx.com.

The GPIO is a non-critical interface and there are no specific backplane routing guidelines.

D.12 Reset Output from ICH9

This 3.3V signal, named TM_RST# on pin Z17 of the P2 connector, is driven by a NC7SZ125 buffer via a 33Ω series termination resistor

The datasheet for the NC7SZ125 buffer is available on the Fairchild website at http://www.fairchildsemi.com.

This is a non crtical signal and there are no specific backplane routing guidelines.

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