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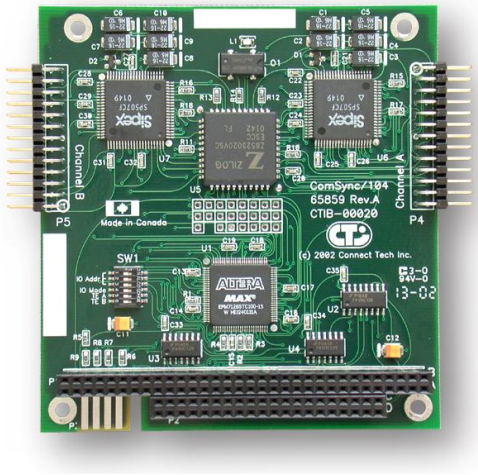
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Connect Tech Inc.
Industrial Strength Communications

ComSync/104

PC/104 serial communications
User Manual



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Customer Support Overview

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In the event that the reseller is unable to resolve your problem, our highly qualified support staff can assist you. Our support section is available 24 hours a day, seven days a week on our website at:
www.connecttech.com/sub/support/support.asp. See the contact information section below for more information on how to contact us directly. Our technical support is always free.

Contact Information

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Telephone/Facsimile
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Telephone: 800-426-8979 (North America only)
Telephone: 519-836-1291 (Live assistance available 8:30 a.m. to 5:00 p.m. EST, Monday to Friday)
Facsimile: 519-836-4878 (on-line 24 hours)

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Submit your technical support questions to our customer support engineers via the **Support Center** on the Connect Tech website.

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Introduction

The Connect Tech Inc. ComSync/104 is a 2 channel Synchronous/Asynchronous Serial Adapter card for PC/104 Bus systems.

The card utilizes the features and functionality of the Zilog 85230 ESCC , along with an innovative I/O structure, to provide the user with full featured SYNC/ASYNC communications.

Features

- Zilog 85230 clocked at 19.6608 MHz, allowing bit rates up to 4.9 Mbps
- Innovative I/O structure featuring basic and enhanced I/O
- Choice of seven software selectable electrical interfaces: RS-232, RS-422, RS-449, EIA-530, EIA-530/A, V.35 and X.21
- Support four software programmable DMA (Direct Memory Access) channels with TC (Terminal Count) interrupt
- 85230 Register Bit Cloning
- Available security features
- Software selectable IRQ on PC/104 bus, and Master Interrupt Enable
- Software selectable Shared IRQ and Pull-Down modes (Rev C and later)
- RS485 Mode support (Rev C and later)
- Available Industrial Temperature operating range of -40 to 85 degrees Celsius (-40 to 185 degrees F) at a reduced clock rate (14.7456 MHz)

Figure 1: ComSync/104 board layout preceeding Revision C

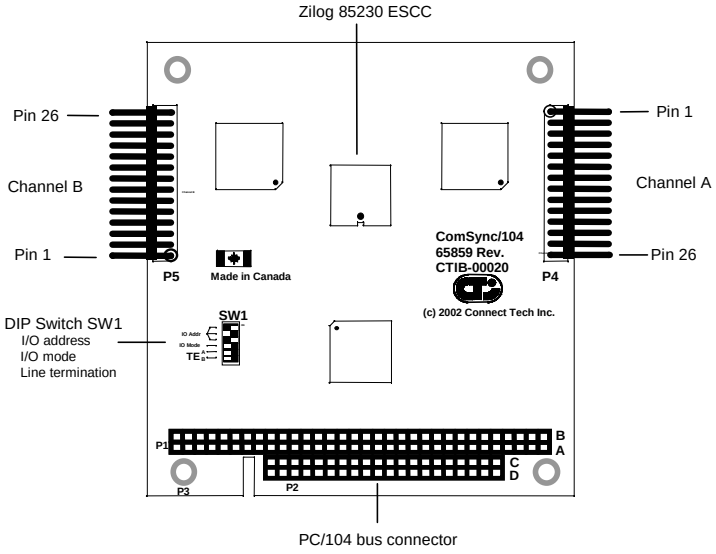
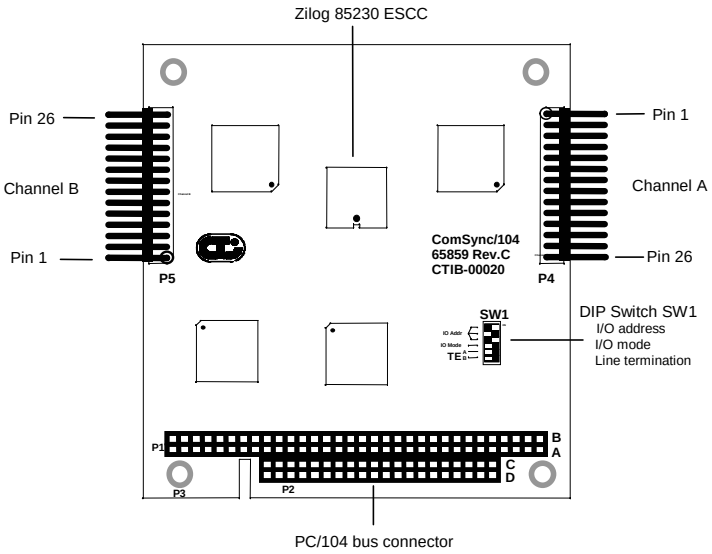


Figure 2: ComSync104 Revision C/D board layout



Hardware Installation

Be sure to configure all dip-switch settings prior to the physical installation of your ComSync/104 adapter into your PC/104 stack.

Innovative I/O Structure

The innovative I/O structure supports either a Basic mode or Enhanced mode of I/O interfacing. The Basic mode decodes 16 (eight prior to Revision C) consecutive I/O addresses of which 10 are used, which supports the ESCC along with Control and Status functions.

The Enhanced mode is 64 consecutive I/O addresses which supports the Basic mode plus an additional I/O region which allows the ESCC registers to be read/written in one PC/104 Bus cycle. The following table shows the I/O Map.

Table 1: I/O Map

I/O Address (Offset)	Function Name	Bit Definitions (Write)		Bit Definitions (Read)	
0	Channel(A) Data [1]	0 » 7	85230 Data register	0 » 7	85230 Data register
1	Channel(A) Control [1]	0 » 7	85230 Control register	0 » 7	85230 Control register
2	Channel(B) Data [1]	0 » 7	85230 Data register	0 » 7	85230 Data register
3	Channel(B) Control [1]	0 » 7	85230 Control register	0 » 7	85230 Control register
4	Status and Control	0 1 2 3 » 5 6 7	DTR(A) [2] DTR(B) Security Feature Enable IRQ Selection DMA Enable (B) DMA Enable (A)	0 1 2 3 4 5 6 7	DSR(A) DSR(B) Security Feature Enable 85230 INT pin I/O mode TC Interrupt[3] DMA Enable (B) DMA Enable (A)
5	TC & Security	any	Clear TC Interrupt [3]	0 » 7	Security Function
6	85230 Control	any	Resets 85230 and Register Bit Clones [5]	0 » 7	85230 Interrupt Acknowledge
7	Misc Control	0 » 2 3 » 5 6 7	Line Interface Mode (A) Line Interface Mode (B) Master Interrupt Enable WAIT/TC Enable [4]	0 » 2 3 » 5 6 7	Line Interface Mode (A) Line Interface Mode (B) Master Interrupt Enable WAIT/TC Enable [4]
8 [8]	IRQ Control	0 1 2 3 » 5 6 7	Shared IRQ Enable IRQ Pull-Down Enable Reserved IRQ Selection [9] Master Interrupt Enable [10] Software IRQ [11]	0 1 2 3 » 5 6 7	Shared IRQ Enable IRQ Pull-Down Enable Reserved IRQ Selection Master Interrupt Enable Software IRQ
9 [8]	RS485 Control	0 » 3 4 » 7	RX and TX RS485 Modes [7] Reserved	0 » 3 4 » 7	RX and TX RS485 Modes [7] Reserved
0x20 » 0x2F [6]	Channel(A) Registers	0 » 7	Register Write data	0 » 7	Register Read data
0x30 » 0x3F [6]	Channel(B) Registers	0 » 7	Register Write data	0 » 7	Register Read data

Notes

[1] See Zilog ESCC user manual for description of functionality.

[2] DTR control from this I/O point is only valid when the **/DTR//REQ** pin of the ESCC is programmed for use as a DMA request.

[3] TC is the Terminal Count signal from the PC/104 Bus, which occurs at the end of a DMA transfer.

[4] When the **/W//REQ** pin of the ESCC is programmed as a WAIT function, this bit enables WAIT states to occur on the PC/104 Bus. When both channels are programmed to operate in DMA mode, this bit becomes a TC Interrupt Enable.

[5] 85230 Registers bits which are cloned.

[6] Only when Enhanced Addressing mode is enabled.

[7] Refer to description below for bit meanings.

[8] I/O Offsets [8] and [9] are only available on Revision C (or later) cards.

[9] IRQ Selection can be set at I/O Offset [8] and [4] (same bit numbers).

[10] Master Interrupt Enable can be set at I/O Offset [8] and [7] (same bit number).

[11] Software IRQ will cause the card to generate an IRQ and is mostly used for testing.

DMA Support

To allow fast data reception and transmission, the ComSync/104 supports four DMA channels; each one is assigned to one of the ESCC DMA Request pins. Each channel of the ESCC has 2 request pins which can be programmed as either a combined receive/transmit request or as separate receive and transmit requests (see the ESCC Users Manual for much more detail).

The I/O of this card will support a DMA Enable for each Channel of the ESCC. The DMA support is organized as follows:

Table 2: DMA Support

PC/104 DMA signals	85230 DMA pin	85230 Channel	85230 Register Bit	Enable Bit	Function
DRQ0 / DACK0#	/DTR//REQA	A	WR14.2 = 1	I/O(4).7	Transmit DMA
DRQ1 / DACK1#	/W//REQA	A	WR1.6 = 1	I/O(4).7	Receive or Transmit DMA
DRQ2 / DACK2#	/DTR//REQB	B	WR14.2 = 1	I/O(4).6	Transmit DMA
DRQ3 / DACK3#	/W//REQB	B	WR1.6 = 1	I/O(4).6	Receive or Transmit DMA

Note: If a Floppy drive is installed in the system then DRQ2/DACK2# are used and should not be used for the ComSync/104.

85230 Register Bit Cloning

Various features of the ComSync/104 board are set up when certain register bits of the ESCC are programmed. This feature is extremely convenient and reduces the redundancy of setup functions. When certain bits are written to ESCC registers, the card keeps a copy of those bits to perform the setup of card features. These Register bits are cloned for each channel of the ESCC, to perform the following functions:

Table 3: Register Bit Cloning

ESCC Register Bit(s) Cloned	Function on ESCC	Function on Card
WR11.2	TRxC pin as an Input or Output (Reset state is an Input)	Controls the direction of the TRxC(±) pins of the Line Interface to match the setting of the ESCC.
WR4.[5,4,3,2]	Various SYNC modes which require the SYNC pin to be an Input (Reset to Async mode).	Controls the direction of the SYNC(±) pins of the Line Interface to match the setting of the ESCC. (SYNC is an input when External SYNC is selected or Async mode is selected. All other times SYNC is an Output).
WR1.6	Changes functionality of the /W//REQ pin (Reset state is the WAIT function).	When programmed to the WAIT function, and the **WAIT Enable** [I/O(7).7] bit is ON, the card will generate wait states onto the PC/104 Bus during Data reads or writes (using the IOCHRDY signal). **USE EXTREME CAUTION WHEN USING THIS MODE, INFINITE WAIT PERIODS CAN OCCUR!** When programmed for the REQ function the ESCC pin becomes the DMA signal DRQn
WR14.2	Changes the functionality of the /DTR//REQ pin (Reset state is the DTR function).	When programmed to the DTR function, the DTR(±) signals on the line interface are supplied by the ESCC (WR5.7) and the DMA signal DRQn is disabled. When programmed to the REQ function, the ESCC pin becomes the DMA signal DRQn, and the DTR(±) line interface signals are provided by the I/O(4).0,1 bits.

Security Feature

Due to the specialized nature of this product, users may wish to "Secure" their software to the use of the CTI hardware. This is similar to the use of a "Software Security Dongle" (sometimes attached to a Parallel port of a PC). The function is implemented by CTI engineers (with customer input) and can be customer specific. It is programmed into the PLD logic component on the card during manufacturing.

The security feature is enabled by setting I/O (4).2, setting the required security bits (this is customer specific), and then reading back the result from I/O (5). When finished with the security feature, the bit at I/O (4).2 is cleared to return to normal operation.

When the security feature is enabled the following functions are inhibited:

- Master Interrupt Enable cannot be changed.
- WAIT states are disabled (IOCHRDY will not activate on PC/104 bus cycles).
- WAIT Enable cannot be changed.
- Line Interface Mode cannot be changed for either channel.

Note: The function which can be programmed is limited in scope and is NOT as fully featured as one would find on a typical "Security Dongle", but it is usually sufficiently cryptic to slow down pirates.

Software Selectable IRQs

There are eight IRQ numbers which can be selected by software along with a Master Interrupt Enable as follows:

Table 4: IRQs

Master Enable I/O (7).6	Setting I/O (4).3 » 5	IRQ Selected (Enabled)
1	0	3
1	1	5
1	2	7
1	3	9
1	4	10
1	5	11
1	6	12
1	7	15

Since the interrupt is programmable, the card powers-up with all interrupt driving circuits tri-stated. During software initialization of the card, both channels of the ESCC should be set up first, then the desired interrupt should be programmed and finally the Master Interrupt Enable bit set [I/O (7).6]. At this point the chosen IRQ signal will be driven inactive (low). When the SCC generates an interrupt, the selected IRQ will be driven active (high) by the card. When the interrupt has been serviced, the IRQ signal will return to the inactive state. (The IRQ signal is never tri-stated during this process).

On most PC/104 buses the IRQ signals are positive edge activated with a pull-up resistor on the IRQ signal (usually located on the PC/104 CPU module). Therefore, it is possible to generate a "phantom" interrupt when the Master Interrupt Enable bit is turned off. During the shutdown of the card (when a software driver is stopped or disabled by the operating system), the interrupt should first be disconnected/disabled from the operating system and then the Master Interrupt Enable bit turned off. A false interrupt can be prevented in this way.

Shared IRQ (Revision C and proceeding)

The Selected IRQ can be shared between multiple ComSync/104 cards. This shared IRQ mechanism is designed using the guidelines in the PC/104 Specification V 2.5, appendix C. To enable Shared IRQ, turn On the Shared IRQ Enable bit I/O (8).0. When this bit is On, the IRQ signal will be tri-stated when it is inactive and driven high when active. A pull-down resistor is required on the IRQ signal to allow it to operate correctly (See IRQ Pull-Down).

IRQ Pull-Down (Revision C and proceeding)

As noted in the Shared IRQ section, the chosen IRQ requires a pull-down resistor (1K) in order to operate correctly. There can be only one pull-down resistor for each shared IRQ. To enable the pull-down, turn On the pull-down Enable bit, I/O (8).1. This activates a 1K pull-down (to GND) resistor on the programmed IRQ. Remember if you have two or more cards sharing an IRQ, only one of them should have the pull-down enabled.

Software Selectable Line Interface Modes

The Serial Line Interface utilizes Sipex devices SP507 (on Revision A and B cards) or SP508 (on Revision C and proceeding cards). Refer to the data sheet for these devices for all electrical characteristics of the interface.

The Line Interface Mode is software selectable for each Channel. The following Modes are available:

Table 5: Line Interface Mode Settings

Signal	Pin#		Line Interface Mode Settings (binary values) I/O address offset 7: bits 0, 1, 2 are for Channel A & bits 3, 4, 5 are for Channel B							
	26 Pin Header	25 pin D-Sub	000	001	010	011	100	101	110	111
TX+	2	14	V.11	V.11	V.11	V.11	V.35[6]	V.11	[1]	[1]
TX-	3	2	V.11	V.11	V.11	V.11	V.35[6]	V.11	V.28	[1]
RX+	6	16	V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]	V.11[5]	[2]	[2]
RX-	5	3	V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]	V.11[5]	V.28	[2]
DTR+	20	23	V.11	[1]	V.11	V.11	[1]	V.11	[1]	[1]
DTR-	14	20	V.11	V.10	V.11	V.11	V.28	V.11	V.28	[1]
RTS+	12	19	V.11	V.11	V.11	V.11	[1]	V.11	[1]	[1]
RTS-	7	4	V.11	V.11	V.11	V.11	V.28	V.11	V.28	[1]
CTS+	25	13	V.11	V.11	V.11	V.11	[2]	V.11	[2]	[2]
CTS-	9	5	V.11	V.11	V.11	V.11	V.28	V.11	V.28	[2]
DSR+	18	22	V.11	[2]	V.11	V.11	[2]	V.11	[2]	[2]
DSR-	11	6	V.11	V.10	V.11	V.11	V.28	V.11	V.28	[2]
DCD+	19	10	[2]	[2]	[2]	[2]	[2]	[2]	[2]	[2]
DCD-	15	8	V.10	V.10	V.10	V.10	V.28	V.10	V.28	[2]
RTxC+	17	9	V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]	V.11[5]	[2]	[2]
RTxC-	8	17	V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]	V.11[5]	V.28	[2]
SYNC+[3]	21	11	V.11	V.11	V.11	V.11	[1]	V.11	[1]	[1]
[4]			V.11	V.11	V.11	V.11	[2]	V.11	[2]	[2]
SYNC-[3]	22	24	V.11	V.11	V.11	V.11	V.28	V.11	V.28	[1]
[4]			V.11	V.11	V.11	V.11	V.28	V.11	V.28	[2]
TRxC+[3]	23	12	V.11	V.11	V.11	V.11	V.35[6]	V.11	[1]	[1]
[4]			V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]]	V.11[5]	[2]	[1]
TRxC-[3]	4	15	V.11	V.11	V.11	V.11	V.35[6]	V.11	V.28	[1]
[4]			V.11[5]	V.11[5]	V.11[5]	V.11[5]	V.35[6]	V.11[5]	V.28	[1]
GND	1, 13	1, 7	GND	GND	GND	GND	GND	GND	GND	GND

Notes:

[1] Tri-State

[2] Hi-Z, resistance >= 10K Ω to GND

[3] When Signal is an Output.

[4] When Signal is an Input

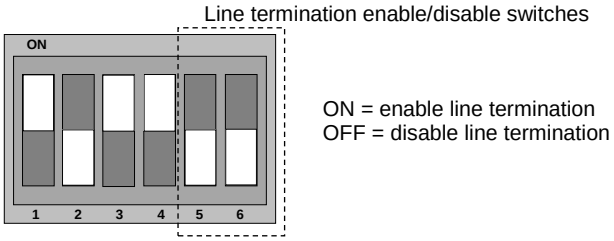
[5] 120 Ω termination resistor is applied between the (+) and (-) signals.

[6] V.35 Termination Network is applied between the (+) and (-) signals.
V.10 = RS-423
V.11 = RS-422
V.28 = RS-232
V.35 = V.35

Line Termination

The multi-mode transceiver provides line termination networks built into the chip. Switches 5 and 6 on DIP switch SW1 disable or enable these networks for channels A and B on the ComSync/104. Please contact Connect Tech support for more information concerning these line termination networks. Please refer to the Line Interface Mode table listed above concerning the ComSync/104 signal assignments and related notes.

Figure 3: Line Termination
DIP switch – SW1



This example shows the default setting with RX, RTxC and TRxC Receiver Terminations disabled:

SW1-5 is set OFF for Channel A
SW1-6 is set OFF for Channel B

RS485 Modes (Revision C and proceeding)

The ESCC can manipulate the /RTS signal to perform a variety of Line Transceiver enabling, and other signaling, related to operation in either asynchronous or SDLC modes. Refer to sections 4.2.1 and 4.4.1 of the Zilog ESCC manual. Also see the description for registers WR5.1, WR7.2 and WR10.2 for additional information about RTS control operations on the ESCC. The card allows the RTS signal to control the Line Transceivers for the TX and RX (TX± and RX±) signals only. A two-wire (Half Duplex) or four-wire (Multi-Drop) style of interface can be achieved.

Note: The ESCC does not control RTS completely autonomously; software is required to perform some of the RTS control.

Table 6: Control Bits

I/O Offset 9 Control Bit	Function	RTS State	Operation
0	RX-RTS Enable, Channel A Allow RTS to control RX Enable [1]	On (RTS = low)	RX Receiver will be disabled
		Off (RTS = high)	RX Receiver will be enabled
1	TX-RTS Enable, Channel A Allow RTS to control TX Tri-State	On (RTS = low)	TX Driver will be enabled
		Off (RTS = high)	TX Driver will be Tri-stated
2	RX-RTS Enable, Channel B Allow RTS to control RX Enable [1]	Same as above	Same as above
3	TX-RTS Enable, Channel B Allow RTS to control TX Tri-State	Same as above	Same as above

Notes

[1] The RX Enable control bit function will only operate if the TX Enable bit is also On.

Examples

Half Duplex Setup
To create this setup, both the RX-RTS Enable and TX-RTS Enable bits should be turned on, for the desired channel. For example: Bits 0 and 1 for Channel A, Bits 2 and 3 for Channel B.

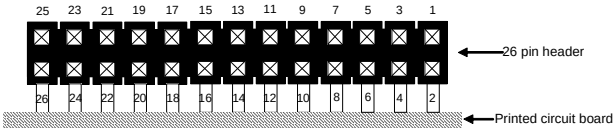
Multi-Drop
To create this setup, only the TX-RTS Enable bit should be turned on, for the desired channel. For example: Bit 1 for Channel A, bit 3 for Channel B.

I/O Connect Pin Assignments

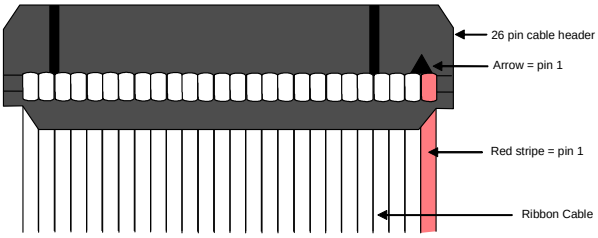
Table 7: Pin Assignments

Header Pin #	DB-25 Pin #	Signal	Header Pin #	DB-25 Pin #	Signal
1	1	GND	14	20	DTR-
2	14	TX+	15	8	DCD-
3	2	TX-	16	21	---
4	15	TRXC-	17	9	RTXC+
5	3	RX-	18	22	DSR+
6	16	RX+	19	10	DCD+
7	4	RTS-	20	23	DTR+
8	17	RTXC-	21	11	SYNC+
9	5	CTS-	22	24	SYNC-
10	18	---	23	12	TRXC+
11	6	DSR-	24	25	---
12	19	RTS+	25	13	CTS+
13	7	GND	26	---	---

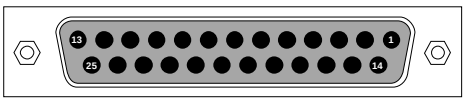
View facing 26 pin header



Top view of DB-25 cable



Female DB-25 Connector



I/O Address and I/O Mode Setup

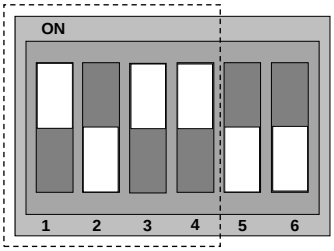
The Base I/O Address and the I/O mode are selected via a miniature Dip Switch. When the Basic mode is selected the card only decodes eight consecutive addresses. If Enhanced Mode is used, then 64 consecutive addresses are used. The following are the selections:

Table 8: I/O Address Selection

SW1				**Base I/O Address**
1	**2**	**3**	**4**	
Off	Off	Off	X	0x100
On	Off	Off	X	0x140
Off	On	Off	X	0x200
On	On	Off	X	0x240
Off	Off	On	X	0x280
On	Off	On	X	0x300
Off	On	On	X	0x340
On	On	On	X	0x380
X	X	X	Off	Basic Mode
X	X	X	On	Enhanced Mode

DIP switch- SW1

Base I/O address & enhanced I/O setup switches



This example shows the default setting:

Base I/O address = 0x300
Enhanced I/O Mode = ON

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