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Find the *Contemporary Controls PCA66-TPB* at our website: ***Click HERE***

PCA66

ARCNET® Network Interface Modules for ISA Bus Computers

INSTALLATION GUIDE

INTRODUCTION

The PCA66 series of ARCNET network interface modules (NIMs) links ISA compatible computers with the ARCNET local area network (LAN).

ARCNET is classified as a token-bus LAN operating at 2.5 Mbps while supporting 255 nodes. Interfacing ARCNET to a host computer usually requires a NIM which plugs into the host computer's bus.

The PCA66 incorporates the newer COM90C66 ARCNET controller chip with enhanced features over the earlier generation ARCNET chips. New performance and integration enhancements include command chaining operation and an internal 2K x 8 RAM buffer. For most AT compatibles there is usually no requirement for wait-state arbitration.

Each PCA66 module has two LEDs on the board. The green LED indicates that the module is transmitting data on the network and the yellow LED indicates bus access to the module. The PCA66 also has an external DIP switch so that node addresses can be easily reassigned without removing the module.

There are five versions of the PCA66 ARCNET NIM. The PCA66-CXS supports coaxial star configurations requiring external active or passive hubs. The PCA66-CXB supports coaxial bus configuration usually requiring no hubs. Other versions include the PCA66-FOG which supports fiber optic cable with either ST or SMA connectors. The PCA66-TPB supports twisted-pair bus cabling using RJ-11 or screw terminal connectors.

CONTEMPORARY CONTROLS®

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SPECIFICATIONS

Environmental
Operating temperat 0°C to +60°C
Storage temperature: –40°C to +85°C

Data Rate
2.5 Mbps

Dimensions
4.20" x 6.50"
(106 mm x 165 mm)

Shipping Weight
1 lb. (.45 kg)

Memory Mapping
Supports memory mapping of RAM buffer and boot PROM on selected 16K segments within the lower 1 MB address space. Module decodes 24 bits of memory addressing.

I/O Mapping
Supports I/O mapping on selected 16-byte boundaries

Interrupt Lines
Supports strapping of IRQ2/9, 3, 4, 5, 6, 7, 10, 11, 12, 14 or 15

Compatibility
PCA66 series NIMs are compliant with ANSI/ATA 878.1 and IEEE P996 Personal Computer Bus Standard Draft 2.2, dated July 1990.

Regulatory Compliance
CE Mark
FCC Part 15 Class A

POWER REQUIREMENTS

Model	+5 V	–12 V
PCA66-CXS	200 mA	20 mA
PCA66-CXB	200 mA	50 mA
PCA66-FOG-SMA	300 mA	N/A
PCA66-FOG-ST	300 mA	N/A
PCA66-TPB	200 mA	50 mA

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INSTALLATION

Once configuration is complete, the PCA66 can be installed in any AT compatible, 16-bit, ISA computer bus. With the power removed from the computer, remove the cover of the computer exposing the motherboard and expansion slots (connectors). Care should be taken when installing the PCA66 because both it and the exposed computer motherboard are sensitive to electrostatic discharge. To prevent inadvertent damage, touch the metal case of the internal power supply to discharge yourself then proceed to remove the PCA66 from its protective ESD package. Remove the backplate of the computer adjacent to the desired slot (connector). The PCA66 can then be inserted into this slot by applying a downward even pressure until it stops and is firmly seated into the connector. The PCA66 backplate can be secured to the computer by installing the small screw used to attach the original backplate. Installation is completed by replacing the computer's cover.

CONFIGURING JUMPER SETTINGS

I/O Address Map

I/O address space is selected in blocks of 16 contiguous bytes. A total of eight blocks can be selected using select pins IOS2-IOS0. These select lines are decoded and used to select a 12 bit register which is compared to address lines A15-A4. The user has a choice of eight I/O address blocks to choose from. Refer to Table 1 for I/O map selection and Figure 1 for the E2 jumper locations. To program the I/O address block, select the desired I/O address range from Table 1 and install jumpers at the corresponding I/O select lines at block location E2. The default setting is 0300. If a jumper is not to be used, simply move the jumper to one side of the jumper block so that only one pin is covered.

IOS2	IOS1	IOS0	I/O ADDRESS RANGE
■	■	■	0260-026F
■	■		0290-029F
■		■	02E0-02EF
■			02F0-02FF
	■	■	0300-030F
	■		0350-035F
		■	0380-038F
			03E0-03EF

■ = Install Jumper

Table 1 — I/O Map Selection

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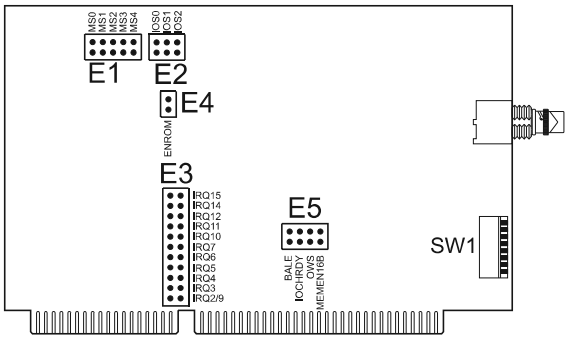


Figure1 — PCA66 Jumper Locations

Internal Reset Logic

Special processor circuitry is included to guarantee smooth operation during reset. In order to eliminate conflicts with other memory elements, internal RAM is hidden until a valid node ID is loaded in the register. System software can determine when to enable the internal memory.

A new provided option enables memory without requiring a software reset. This mode supports memory mapped environments where the driver does not issue a software reset. Installing a jumper on the MEMEN16B location of the E5 jumper block will default the PCA66 to 16-bit mode and enable memory access. If a jumper is not to be used, simply move the jumper to one side of the block so that only one pin is covered. Refer to Figure 1 for the E5 jumper block locations.

Internal RAM

The configuration register contains the I/O access bit which determines whether the RAM will be configured for sequential I/O mapped accesses or memory mapped accesses. Additionally, the decode mode bit allows the choice of 8K or 16K block of ROM if set for I/O mapped access, or the choice of the activation of the MEMCS16 signal upon access to 2K or 128K of RAM if set for memory mapped access.

When the device is configured for a 16-bit data bus, the on-chip RAM is seen by the processor as 1K x 16 rather than 2K x 8.

Although sequential I/O mapped memory accesses require more steps than memory mapped accesses, I/O mapped is just as efficient as memory mapped and does not require the large block of memory in the host addressing space that memory mapped does. On the other hand, memory mapped access is more flexible and allows the processor to analyze data and make decisions without emptying the entire packet into system memory.

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Memory Mapped RAM Access

The memory mapped mode implements the traditional mapping to an ARCNET PROM and RAM buffer into a single 16K memory segment. Memory space is required for the 2K RAM buffer and the 8K PROM. To accommodate these two requirements, a 16K segment must be selected from the PC host address space. Pins MS4-MS0 are decoded in order to generate a 9-bit register value that is compared to address bus lines A19-A11 in order to select a 16K segment. Within the selected 16K segment, the PROM occupies the upper 8K of the selected segment and is accessed when A13 equals a logic 1. The 2K RAM is enabled when A13 equals a logic 0. The actual location of the 2K RAM within the 8K portion depends upon the decoding of address lines A11 and A12 and the programming of MS0 and MS1. Refer to Table 2 for the RAM and PROM address values. To program the memory address block, select the desired memory address range from Table 2 and install jumpers at the corresponding memory select lines at block location E1. Refer to Figure 1 for the E1 jumper block location. The default setting is D:0000. If a jumper is not to be used, simply move the jumper to one side of the jumper block so that only one pin is covered.

To ensure that the PROM and RAM do not conflict with extended memory, the PCA66 decodes address lines A23-A20 and only qualifies the PROM and RAM within the lower 1MB page.

Internal processor latches go transparent on BALE high and latch on BALE low. If all addresses being used are already latched or valid for the entire duration of the cycle, then the BALE signal may be tied to a logic “1.” If BALE is tied high or left disconnected, the address is latched by only the second latch-stage. If BALE is connected to the bus, the address is latched by both the first and second stage latches. To utilize the BALE signal, insert a jumper at the corresponding position at jumper E5. Refer to Figure 1 for the E5 jumper block location. If a jumper is not to be used, simply move the jumper to one side of the block so that only one pin is covered.

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MS4	MS3	MS2	MS1	MS0	RAM ADDRESS RANGE	PROM ADDRESS RANGE
■	■	■	■	■	C:0000-C:07FF	C:2000-C:3FFF
■	■	■	■		C.0800-C:0FFF	C:2000-C:3FFF
■	■	■		■	C:1000-C:17FF	C:2000-C:3FFF
■	■	■			C:1800-C:1FFF	C:2000-C:3FFF
■	■		■	■	C:4000-C:47FF	C:6000-C:7FFF
■	■		■		C:4800-C:4FFF	C:6000-C:7FFF
■	■			■	C:5000-C:57FF	C:6000-C:7FFF
■	■				C:5800-C:5FFF	C:6000-C:7FFF
■		■	■	■	C:C000-C:C7FF	C:E000-C:FFFF
■		■	■		C:C800-C:CFFF	C:E000-C:FFFF
■		■		■	C:D000-C:D7FF	C:E000-C:FFFF
■		■			C:D800-C:DFFF	C:E000-C:FFFF
■			■	■	D:0000-D:07FF	D:2000-D:3FFF
■			■		D:0800-D:0FFF	D:2000-D:3FFF
■				■	D:1000-D:17FF	D:2000-D:3FFF
■					D:1800-D:1FFF	D:2000-D:3FFF
	■	■	■	■	D:4000-D:47FF	D:6000-D:7FFF
	■	■	■		D:4800-D:4FFF	D:6000-D:7FFF
	■	■		■	D:5000-D:57FF	D:6000-D.7FFF
	■	■			D:5800-D:5FFF	D:6000-D:7FFF
	■		■	■	D:8000-D:87FF	D:A000-D:BFFF
	■		■		D:8800-D:8FFF	D:A000-D:BFFF
	■			■	D:9000-D:97FF	D:A000-D:BFFF
	■				D:9800-D:9FFF	D:A000-D:BFFF
		■	■	■	D:C000-D:C7FF	D:E000-D:FFFF
		■	■		D:C800-D:CFFF	D:E000-D:FFFF
		■		■	D:D000-D:D7FF	D:E000-D:FFFF
		■			D:D800-D:DFFF	D:E000-D:FFFF
			■	■	E:0000-E:07FF	E:2000-E:3FFF
			■		E:0800-E:0FFF	E:2000-E:3FFF
				■	E:1000-E:17FF	E:2000-E:3FFF
					E:1800-E:1FFF	E:2000-E:3FFF

■ = Install Jumper

Table 2 — User Configuration of Memory Map

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Sequential I/O Mapped RAM Access

In the I/O mapped mode, only the PROM is memory mapped while occupying a 16K address space instead of 8K. In this mode a 16Kx8 PROM can be used instead of the 8Kx8 PROM. The RAM buffer is then accessed through the I/O address space. Table 2 can still be used to determine PROM addressing realizing that the PROM occupies the RAM space as well.

Wait-State Details

In the typical computer, bus speed is slower than that of the CPU speed so that peripherals will be able to keep up with the machine. In many cases, the peripheral will need additional delays to be able to keep up and will, therefore, use the IOCHRDY signal to tell the processor whether or not it is ready to continue. The use of the IOCHRDY signal effectively "slows down" the bus. To use this signal insert the IOCHRDY jumper.

The COM90C66 is quick enough to take advantage of the maximum bus speed of most AT compatibles. The function employs the use of the 0WS signal and guarantees the fastest microprocessor cycles. The use of the 0WS signal effectively "speeds up" the bus.

Upon power up, the COM90C66 defaults to the non-zero wait-state mode. The 0WS mode can be easily configured by writing a logic "0" into bit 2 of the configuration register.

For machines with faster buses, the COM90C66 can be configured to negate the IOCHRDY line for the minimal period of time necessary. If the IOCHRDY signal is used, it is negated for one XTAL1 clock for RAM and internal register cycles. With the optional PROM on board, this may require a slower cycle to accommodate its access time even if the device is configured for zero wait-state mode.

Either the 0WS jumper or the IOCHRDY jumper may be used (but not both), depending upon the speed of the bus. In the case where the user does not need to "slow down" or "speed up" the bus, neither signal should be used. In this case, the wait-state bit of the configuration register should be reset to logic "0" to configure the PCA66 for zero wait-state, but the 0WS signal should not be connected to the bus. Refer to Figure 1 for the location of the E5 jumper block.

If your host computer requires the use of the IOCHRDY or 0WS signals, they can be enabled by installing/ removing the jumper in the corresponding location at jumper block location E5.

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PROM Enable

The PROM can be enabled by inserting a jumper at location E4 entitled ENROM. If memory mapped mode is selected and the PROM is disabled, the RAM buffer occupying a 2K segment of memory will be the only device selected in memory mapped mode.

Interrupts

A total of eleven interrupts are available for selection. Invoke the desired interrupt by installing a jumper corresponding to the selected interrupt at jumper block location E3. Only one interrupt can be selected at any one time. The default interrupt setting is IRQ5. Refer to Figure 1 for the E3 jumper block location.

Indicator Lights

There is a dual LED located at the PCA66 backplate. The yellow LED indicates that the PCA66 is being accessed via its I/O address. The green LED indicates that the PCA66 is transmitting ARCNET traffic on the network.

Node ID Switch

An 8-bit DIP switch is used to set the ARCNET node address. Any value except zero is a valid ARCNET node address. If zero is set in the switches, the ARCNET LAN adapter will disable its transmitter and not join the network until a non-zero node ID is set via software. The RAM buffer cannot be accessed when the node ID is zero.

The node ID switch SW1 is read left to right (when viewing the printed circuit board in a horizontal plane with components on top) with the MSB to the far left (position 1) and the LSB to the far right (position 8). A logic “1” occurs when the switch is moved away from the board (switch is opened). Figure 2 shows the node ID switch. In this example, the switch is set to hexadecimal address F5.

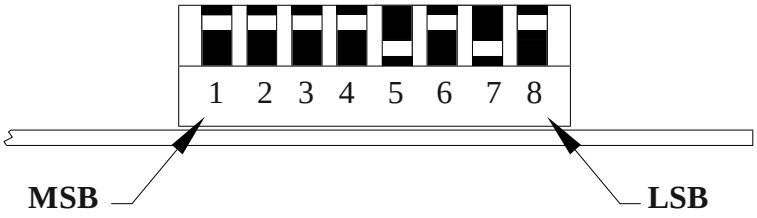


Figure 2 — Node ID Switch

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FIELD CONNECTIONS

The type and style of field connectors depends upon the cabling option selected. Cabling options are identified by a suffix designation applied to the family model number.

-CXS Coaxial Star

In a two node system, simply connect the two -CXS NIMs together using RG-62/u coaxial cable. The length of cable cannot exceed 2000 feet.

If more than two NIMs are used on a network, either an active or passive hub is required. With passive hubs, a maximum of four NIMs can be interconnected. Unused ports on the passive hub must be terminated with a 93 ohm (nominal) resistor. The maximum length between a passive hub port and a NIM is 100 feet.

Active hubs provide overall better performance than passive hubs since greater distances can be achieved along with a degree of isolation. Connect each NIM to a port on the hub using RG-62/u coaxial cable. This length of cable cannot exceed 2000 feet nor can the length of cable between two cascaded hubs exceed 2000 feet. However, up to ten hubs can be cascaded thereby providing an overall cable length of 22,000 feet. Unused ports on active hubs need not be terminated.

-CXB Coaxial Bus

For hubless systems, the -CXB transceiver can be used. NIMs are interconnected with RG-62/u cables and BNC Tee connectors. Each -CXB NIM represents a high impedance connection in both the powered and unpowered states. Therefore, passive termination must be applied to both ends of a bus segment. Use BNC style 93 (nominal) ohm resistors at each end. The maximum segment length is 1000 feet and the maximum number of NIMs that can be connected to a segment is eight.

To extend a bus segment beyond 1000 feet, an active hub is required. If the hub port is of the -CXS type, connection can be made if a few simple rules are followed. Only connect this bus segment at the end of a segment. Do not connect the hub to the middle of a segment since the hub port is not of the high impedance type. Do not terminate the end which attaches to the hub port since a -CXS port effectively terminates the end of a bus segment. Simply remove the BNC Tee connector and terminator from the segment end and attach the cable directly to the hub port. The opposite segment end still requires termination if no hub connection is being made.

Fiber Optic (-FOG, -ST, -SMA)

The fiber optic option is designated -FOG; however, a further designation is required in order to specify the type of connector. The -FOG-ST uses the ST style connector while the -FOG-SMA uses the SMA style connector. Cable

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sizes of 50, 62.5 or 100 micron duplex cable can be used with either connector.

Fiber optic connections require a duplex cable arrangement. Only star and distributed star topologies are supported. Two unidirectional cable paths provide the duplex link. There are two devices on each NIM. One device, colored light gray, is the transmitter and the other, dark gray, is the receiver. Remember that “light goes out of the light (gray).” To establish a working link between a NIM and another NIM or a hub to a NIM, the transmitter of point A must be connected to a receiver at point B. Correspondingly, the receiver at point A must be connected to a transmitter at point B. This establishes the duplex link. Up to 2 km of 62.5 µm fiber optic cable can be used per segment.

Twisted-Pair (-TPB)

The twisted-pair option uses both RJ-11 and screw terminal type connectors. This -TPB version utilizes RJ-11 style jacks capable of accepting either 6 position, 4-pin or 6 position, 6-pin mating connectors. Only the inner-most pair is connected. The 4 position polarized screw terminal connector provides a daisy chain configuration where pins 1 and 3 and 2 and 4 are bussed together for ease of cabling. Refer to Figure 3 and Table 3 for the RJ-11 connector pin assignments and Figure 4 and Table 4 for screw terminal connector pin assignments. Follow these pin assignments when mixing RJ-11 and screw terminal connectors. The -TPB is polarity sensitive requiring that corresponding signal wires at each NIM be connected together.

Wiring between NIMs is accomplished in a daisy-chain fashion with point-to-point cables connecting the various NIMs to create a bus segment. The end NIMs will have one vacant RJ-11 socket which is to hold the RJ-11 style 100 ohm terminator required to terminate the end points of the bus segment. Use twisted-pair cable and observe polarity. Modular plugs must be installed on this cable such that they do not invert the signals. Most satin cable does not twist the pairs nor maintain signal polarity. Do not use this cable. Up to eight -TPB NIMs can be connected to one segment which cannot exceed 400 feet in length.

The overall distance of a twisted-pair network can be expanded beyond 400 feet if hubs are used. Use a hub port that supports a balanced twisted-pair signal (-TPS) or use a BALUN. Contemporary Controls (CC) recommends a Mux Labs BALUN (available from CC under the part number BALUN) connected to a -CXS port on a MOD HUB expansion module. The BALUN converts the balanced twisted-pair signals to single-ended signals suitable to the -CXS port. A more direct approach is to use a MOD HUB expansion module with a -TPS port. The -TPS port has an internal BALUN and provides an identical RJ-11 connection as the BALUN. Unfortunately, the signal sense is inverted from the -TPB module so that an inverted cable

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connection is required to either the BALUN or -TPB port. Connect either of these devices to one of the end NIMs on the segment. This requires the removal of the terminator at that end. The BALUN or -TPS port provides the termination.

Modular Connector Pin Assignments	
6-Contacts	
Pin	Usage
1	Not Available
2	Not Used
3	Line- (Phase B)
4	Line+ (Phase A)
5	Not Used
6	Not Available

Table 3 — Modular Connector Pin Assignments for -TPB

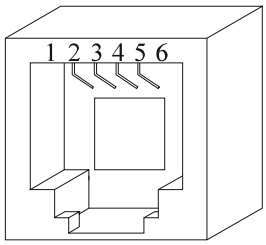


Figure 3 — Modular Jack Numbering Orientation

Screw Terminal Connector Pin Assignments	
Pin	Usage
1	Line+ (Phase A)
2	Line- (Phase B)
3	Line+ (Phase A)
4	Line- (Phase B)

Table 4 — Screw Terminal Connector Pin Assignments for -TPB

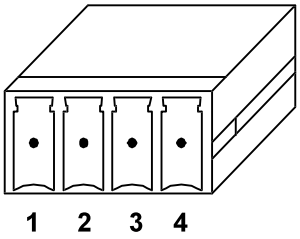


Figure 4 — Screw Terminal Connector Numbering Orientation

Electromagnetic Compatibility

The PCA66 series complies with Class A radiated and conducted emissions as defined by FCC part 15 and EN55022. This equipment is intended for use in non-residential areas.

Warning

This is a Class A product as defined in EN55022. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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Warranty

Contemporary Controls (CC) warrants its product to the original purchaser for one year from the product's shipping date. If a CC product fails to operate in compliance with its specification during this period, CC will, at its option, repair or replace the product at no charge. The customer is, however, responsible for shipping the product; CC assumes no responsibility for the product until it is received. This warranty does not cover repair of products that have been damaged by abuse, accident, disaster, misuse, or incorrect installation.

CC's limited warranty covers products only as delivered. User modification may void the warranty if the modification damages the product, in which case this warranty does not cover repair or replacement.

This warranty in no way warrants suitability of the product for any specific application.

More warranty information can be found on our web site www.ccontrols.com.

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