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## CVXI-1149.1 VXIbus BOUNDARY SCAN CONTROLLER BOARD

- **COMPATIBLE WITH THE IEEE STANDARD 1149.1 (JTAG) SERIAL TEST BUS**
- **SIX SERIAL SCAN TEST BUSES AND 64 BITS PARALLEL I/O**
- **VXIbus C-SIZE and B-SIZE MODULES, REGISTER BASED**
- **USER PROGRAMMABLE SCAN TEST CLOCK RATES UP TO 15 MHZ**
- **INTERNAL OR EXTERNAL SCAN TEST CLOCK SOURCE**
- **SCAN DATA UP TO  $2^{32}$  BITS IN LENGTH**
- **BASED ON THE TI SN74ACT8990 TEST BUS CONTROLLER**
- **PROGRAMMABLE VXIbus INTERRUPTER**
- **SERIAL DATA CAN BE SYNCHRONIZED TO OTHER VXIbus MODULES VIA TTLTRG LINES**



The CVXI-1149.1 VXIbus Boundary Scan Controller Board provides an interface between the VXIbus and any JTAG compatible target. The CVXI-1149.1 is designed to control the operation of an IEEE standard 1149.1 (JTAG) test access ports by generating the proper signals under software control to interface with the target devices. Up to six test access ports can be controlled, each connecting the CVXI-1149.1 card with a four signal cable to the boundary scanned target system. By

controlling the JTAG bus, boundary scan operations per IEEE-1149.1 can be instructed by the software. The user is able to command target circuitry Built-In-Self-Test (BIST), verify PCB interconnects, perform functional testing and debug without the need for manual probing. Furthermore, device internal functions that are not accessible to external probing can be accessed through the JTAG interface, enabling fault isolation within the device itself.

## WHAT IS IEEE 1149.1?

The IEEE 1149.1 test bus and boundary scan architecture allows an IC, and similarly a board or system, to be controlled via a standard four-signal interface. Each IEEE 1149.1 compliant IC incorporates a feature known as boundary scan that allows each functional pin of the IC to be controlled and observed via the four-wire interface. Test, debug, or initialization patterns can be loaded serially into the appropriate IC(s) via the IEEE 1149.1 test bus. This allows IC, board, or system functions to be observed or controlled without actual physical access.

The IEEE 1149.1 test bus is comprised of two main elements: a Test Access Port (TAP), which interfaces internal IC logic with the external world via a four-signal (optionally five-signal) bus; and a boundary scan architecture, which defines standard boundary cells to drive and receive data at the IC pins. The IEEE 1149.1 spec also defines both mandatory and optional opcodes and test features. The test bus signals are: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), Test Data Out (TDO), and the optional Test Logic Reset (TRST). The IEEE 1149.1 specification also specifies that the ICs can be connected in either a ring or star configuration.

## GENERAL OVERVIEW

The CVXI-1149.1 Boundary Scan Controller is designed to control the operation of an IEEE Standard 1149.1 (JTAG) scan test path by taking commands from the host computer and generating the proper signals to interface with the target device(s). The host computer can be an embedded VXIbus computer or an external host that controls the VXI chassis via a VXI slot 0 controller. The target(s) can be moved from any stable state to another stable state, loaded with instructions, and resulting test data scanned out to be read by the Host. Four EVENT pins are provided to allow real-time interaction between the CVXI-1149.1 and its target(s). The EVENT pins can be configured to generate VXIbus interrupt requests and/or assert TTL triggers whenever a user-definable condition is present.

A 32-bit counter can be preset to allow a predetermined number of clock cycles or instruction executions to occur and can be programmed to set an interrupt flag when it reaches a count of zero.

Two 16-bit serial buffers (read and write) are implemented for the VXIbus interface.

The CVXI-1149.1 implements all the low-level functions, enabling the host to use higher-level abstraction such as states of IEEE Standard 1149.1 for control, variables

indicating command finish, buffer full or empty for status, and strings and buffers for data.

The CVXI-1149.1 may connect without external logic to six parallel chains of IEEE Standard 1149.1 targets, each with its own separate TMS signal. The parallel chains share one or two TDI signals, one TDO signal, and one TRST signal and TCK signal.

The CVXI-1149.1 has four event detectors and two 16-bit event counters to support asynchronous functions. The CVXI-1149.1 can connect to the target via a re-timed link with up to 31 bits of delay. This may be required when the clock rate is high and either the target is at a distance or the link involves fanout or buffer/driver devices.

The CVXI-1149.1 is an A16/D16 VXIbus slave device and interrupter with a 16-bit data bus. The critical VXIbus interface timing is independent of the JTAG clock period.

The major functions of the CVXI-1149.1 are controlled by specific commands:

The **STATE** command controls the target interface and target state diagrams. It can change the state to any stable state.

The **EXECUTE** command causes the target to execute instructions that have been shifted into it. It uses the Run-Test/Idle state, and can execute instructions for a fixed time or until an event occurs.

The **SCAN** command circulates data among targets and transfers data between the CVXI-1149.1 and targets. It uses the Shift-IR or Shift-DR states, and also the read and write buffers.

## PROGRAMMABLE CLOCK

The CVXI-1149.1 card TCK clock output to the JTAG compatible target system is programmable by the user's software. The user is able to select either INTERNAL on-board XTAL oscillator or EXTERNAL target supplied clock.

The INTERNAL clock circuitry includes a programmable clock divider logic. Any one of sixteen different divide values, from divide by 2 to divide by 32, can be selected. Using the on-board 30 MHz XTAL oscillator, TCK rates of 937.5 KHz to 15 MHz are user selectable.

In case other clock rates are required, the user can select the EXTERNAL clock source and provide the clock signal from the target system. Optionally, the user can install his own XTAL oscillator chip into the XTAL oscillator socket that is provided on the CVXI-1149.1 card.

A single-step mode is also provided to enable the user to fully control the TCK signal high and low states. When the single step mode is selected, the EXTERNAL clock source and the on-board XTAL oscillator are not being used. Instead, the software write operations to the appropriate bit in the COMMAND register toggle the TCK signal and result in user controlled clock signal. The programmer is able to single-step through the JTAG environment in a fully static mode of operation. This feature is very useful for debugging software drivers and integrating complex JTAG compatible test systems.

## PARALLEL INPUT/OUTPUT PORTS

The board contains 32 TTL compatible parallel inputs and 32 TTL compatible parallel outputs. The input and output signals are organized in 16 bit parallel ports. Each of the parallel input and output ports is directly accessible by the host computer by reading or writing the appropriate VXI A16 register.

The 32 parallel outputs are driven by four tri-state octal buffers, 8 outputs per buffer. The outputs of each of the buffers can be put into tri-state under software control. The command register includes four Output Enable bits, each bit controls one octal output buffer.

The input and output ports can be used to control and sense various non-JTAG functions in the target system. These ports are useful for testing of target systems that incorporate a mixture of JTAG and non-JTAG compatible hardware.

## JTAG COMPATIBLE LOGIC

The CVXI-1149.1 contains two JTAG compatible 74BCT8244 octal buffers that are connected in parallel with the TTLTRG Trigger Input Select Register, which is a 16 bit parallel output port. The serial test busses of the 74BCT8244 devices are daisy chained and then connected to one of the six on-board serial test busses.

In normal mode of operation, these devices can be used as read-back buffers. Data written to the Trigger-In select register port can be read-back from the particular A16 register assigned to these octal buffers. In the diagnostics mode, the normal operation of the octal buffers is inhibited and the Test Access Port circuitry is enabled to scan the device's I/O boundary.

The user is able to program the Trigger-in Select register with arbitrary data, then read it back via the JTAG serial interface and verify that the data scanned matches the actual data presented at the buffer input pins.

This feature provides extensive self-test capabilities to the CVXI-1149.1 board and enables the user to exercise his software and test this "simple" JTAG compatible circuitry before attempting to connect to more complicated target systems.

## INTERRUPTS AND TRIGGERS

The 74ACT8990 test bus controller INTR interrupt request signal can be configured by the user to drive one of the seven VME/VXI interrupts and one of the eight VXIbus TTLTRG trigger lines. The INTR signal is a programmable interrupt request that is set by external event signals and/or internal 74ACT8990 conditions. Refer to the 74ACT8990 data sheet for additional details regarding the operation of the INTR signal and the various programming options for this powerful feature.

The use of interrupts and triggers is an important feature for synchronizing the target system with the CVXI-1149.1 card and for synchronizing multiple VXI modules, including multiple CVXI-1149.1 cards. EVENT signals can detect an asynchronous event in the target system and consequently start or stop serial JTAG data transmission or reception. External events can

also be programmed to generate an interrupt request to the host computer or trigger multiple VXIbus modules.

### VME/VXIbus INTERFACE

**The CVXI-1149.1 is an A16/D16 VME/VXIbus compatible slave module. The card is designed to accept A16 mode address modifiers 29 hex and 2D hex. The card occupies 64 bytes (32 words) of VXI/VME address space which is equivalent to a 40 hex address block. The card address within the A16 address space is set by an 8 bit dip switch that selects one of 256 address blocks from C000 hex to FFC0 hex in 40 hex increments.**

**All the on-board registers are 16 bits wide and are accessed via D16 data transfer cycles on the VME/VXI bus.**

## FRONT PANEL INDICATORS

The **Reset** red LED indicates that the card is in reset and the on-board logic is disabled. This LED is driven directly from the Reset bit (00) of the VXI control register and is under software control.

The **Extclk** green LED indicates that an external JTAG clock source is programmed by the user.

The **Selfst** green LED indicates that the target interface is in tri-state and that the on-board loop-back option is selected (usually during self-test).

## A16 REGISTERS

Thirty two 16 bit registers are provided that configure and control the operation of the CVXI-1149.1 card. The registers are located in the A16 address space within a 40 hex address block that is selected by the 8 bit logical address dip switch.

### ADDRESS

#### OFFSET REGISTER

#### READ/WRITE

00	VXI ID Register	Read
02	VXI Device Type	Read
04	VXI Status/Control	Read/Write
06	Trigger-In select register	*Read/Write
08	Digital I/O Port #1	Read/Write
0A	Digital I/O Port #2	Read/Write
0C	Configuration Register #1	Read/Write
0E	Configuration Register #2	Read/Write
10-3E	74ACT8990 Registers	Read/Write

\* Note: Read-back register is implemented using two JTAG compatible 74BCT8244 devices.

## CVXI 1149.1 SPECIFICATIONS

### POWER SUPPLY

+5 V @ 2.0 AMPS MAX.

### OPERATING TEMPERATURE

0 TO + 70° C

### SIZE

C Size VXI 13.4" x 9.2" x 1.2"

B Size VXI 6.3" x 9.2" x 0.8"

## INCLUDED WITH MODULE

- CVXI-1149.1 Boundary Controller Card
- Self-Test Software Diskette, Including Source Code (IBM PC compatible)
- User's Manual.

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