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Find the *Corelis CVXI-1149.1/IM* at our website: ***Click HERE***

# CORELIS

# CVXI-1149.1/IM™

## Intelligent VXIbus Boundary-Scan Controller

- **Eight IEEE-1149.1 (JTAG) Test Access Ports with high current source and sink capability**
- **High performance 32-bit RISC processor based architecture for maximum test throughput**
- **Programmable test clock TCK rates up to 35 MHz, or external**
- **Dual-port shared RAM provides direct access from VXIbus to data memory for faster test vector downloads**
- **Real-time on-the-fly PASS/ FAIL error detection of scan results**
- **Programmable TDI receive skew to compensate for test cable length delay**
- **Support for remote and/or multidrop testing using differential line drivers and receivers on two Test Access Ports**
- **No host overhead time in serializing boundary-scan data and post processing results**
- **Integrated 64 Digital I/Os for parallel test vector generation and external device synchronization**
- **Single slot C-Size VXI module, Message-based device with shared RAM**
- **Fully compatible with ScanExpress and ScanPlus family of products**




## Overview

The CVXI-1149.1/IM Intelligent VXIbus Boundary-Scan Controller Board is a member of Corelis ScanPlus family of scan-based test, analysis, and diagnostic tools. It provides an Intelligent interface, with memory-behind-the-pin architecture, between the VXIbus and any JTAG compatible device, board, or system Unit Under Test (UUT). The board was designed to minimize the house-keeping and low-level details required by the host, and maximize the test and diagnostics throughput.

The CVXI-1149.1/IM controls the operation of an IEEE Std 1149.1 (JTAG) scan test path by taking commands from the host computer and generating the proper signals to interface with the UUT device(s). The host computer can be an embedded VXIbus computer or an external host that controls the VXI chassis via a VXI slot-0 controller. The boundary-scan UUT(s) can be moved from any stable state to another stable state, loaded with instructions and scan data, and resulting test data scanned out to be read by the host. External inputs are provided to allow real-time interaction between the CVXI-1149.1/IM and its UUT(s). Various user-defined condi-

tions can be programmed to generate VXI bus interrupt requests, assert TTL triggers, and/or alter the digital I/O vector outputs. This supports the 'sync-on-capture' and 'sync-on-update' capabilities.

The CVXI-1149.1/IM also interacts with Corelis CVXI-SCANIO/616, boundary-scan controlled parallel I/O, as well as with any existing parallel digital pattern generator and recorder. The CVXI-1149.1/IM module supports the JTAG 'sample' operation through external trigger inputs. This feature is useful for synchronizing the module to external pattern generators. It also allows testing edge connectors of UUT's and other I/Os that can not be sampled or driven via the boundary-scan chain.

The CVXI-1149.1/IM serializes test vectors, previously loaded to the TDO memory, transfers them to the UUT and stores the UUT responses as raw data, or as post-processed data. Up to eight test access ports can be controlled, each connecting the CVXI-1149.1/IM card with a five-wire signal to the boundary-scanned UUT system.

The configuration and operation of the CVXI-1149.1/IM is controlled through the use of VXIbus Word Serial Protocol commands and shared memory control structure. Serial test data is stored to and retrieved from the on-board 4M bytes (optional 16M bytes) of dual-port (shared) RAM. The CVXI-1149.1/IM embedded processor controls and operates the module using internal registers.

The CVXI-1149.1/IM on-board 4M byte memory is shared by the internal CPU and the VXIbus with memory arbitration being handled automatically by the module. In addition to storing the serial test vectors, the RAM can be downloaded with special pre-processing and/or post-processing function codes that are application specific, such as test macro functions that were implemented in existing non-VXIbus scan testers. Using this dual port shared access technique, tests requiring extremely long test patterns are possible. If needed, the pattern memory can be expanded to a total of 16 Mbytes. Test data formats are used that employ a compression algorithm that maximizes storage usage and minimizes download time.

The on-board 32-bit embedded RISC processor manipulates the data prior to sending and handles all the low-level protocol details locally at the board level. Also, it processes received data and prepares only the relevant information for the host. The host would then read the post-processed data directly from the dual port memory.

The CVXI-1149.1/IM is able to command UUT circuitry Built-In-Self-Test (BIST), verify PCB interconnects, and perform functional testing and debug without the need for manual probing. Furthermore, device internal functions that are not accessible to external probing can be accessed through the JTAG interface, enabling fault isolation within the device itself.

The extensive hardware capabilities of the CVXI-1149.1/IM allow full utilization of the Corelis ScanPlus™ and ScanExpress™ Boundary-Scan Software solutions which include Automatic Test Pattern Generation, diagnostics, and parallel test vectors imported from most EDA software environments as well as a library of high-level routines that can be linked to a user's own development environment.

## System Architecture

To accomplish sustained test speeds of up to 35 MHz without the need to insert PAUSE states or stop the TCK, the CVXI-1149.1/IM is equipped with a large number of performance enhancing features. Figure 1 shows a block diagram of the key components that make up the boundary-scan controller hardware.

Specifically, the following design features contribute to the high performance of the CVXI-1149.1/IM boundary-scan controller:

### Shared RAM VXI Access

The entire 4 Mbyte (optionally 16 Mbytes) of pattern memory is implemented as dual access shared RAM. As such, it is directly available to both the VXI bus as a relocatable memory mapped area, and to the on-board 32-bit RISC processor. Memory access and arbitration is handled automatically in hardware to ensure minimum memory access times without the need for processor or software overhead. This allows new test patterns to be loaded through the VXI bus while the test controller is executing current tests.

### RISC Processor

The CVXI-1149.1/IM boundary-scan test controller is equipped with a 32-bit RISC processor to support high-speed operation without host intervention. The on-board firmware program is loaded from EPROM at start-up and executed from a fast RAM. Macro commands called directives can be pre-loaded by the host computer via the VXI bus for execution by the firmware. Status information is available to the host to monitor progress. Optionally, the VXIbus interrupter capability can be used to notify the host of program completion or test failures.

### High-Level Test Bus Controllers

A pair of proprietary boundary-scan multi-tap test bus controllers is used to supply serialized scan data to two out of eight Test Access Ports simultaneously. Each test bus controller uses an independent programmable clock generator and can be synchronized to external events. External clocking is available as well for synchronous operation with other testers or the unit under test.

The test bus controllers take care of parallel to serial conversion of the scan pattern data and generate the proper test controller states using the TMS and TDO signals. TDI data is shifted in and converted to parallel format for transfer to the results buffer. The use of FIFO's, in addition to other proprietary techniques, on each multi-tap test controller ensures continuous test data streams at up to 35 MHz TCK speeds. This is collision-free with any concurrent VXIbus activity. Thus, EXTEST and BIST operations whose test patterns exceed the size of the on-board pattern memory, may be host fed with upcoming data in background.

### On-the-fly Error Detection and Pattern Matching

Expected results data can be downloaded to the pattern memory

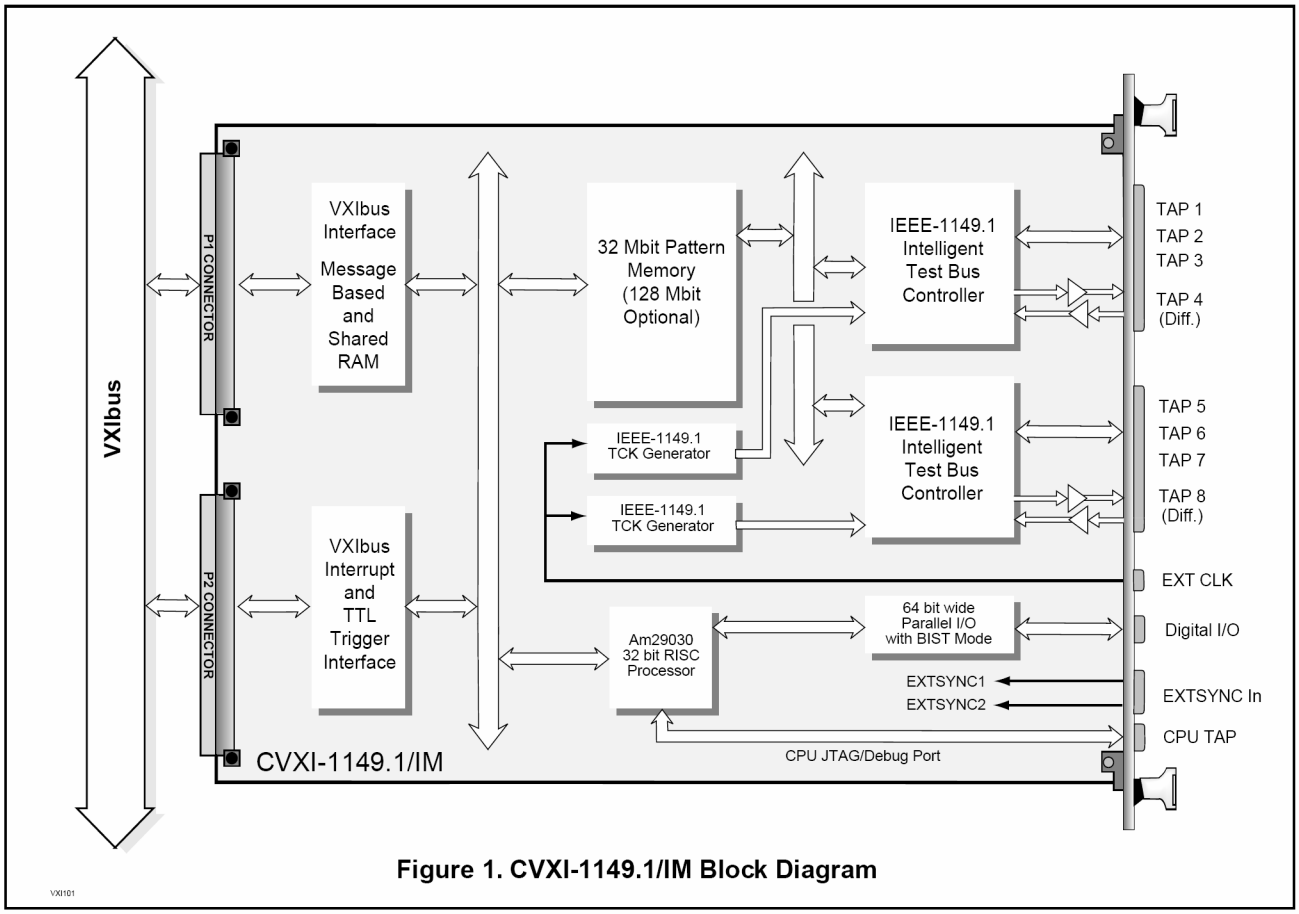



**Figure 1. CVXI-1149.1/IM Block Diagram**

for on-the-fly test result comparison. The outcome of such comparisons can be used to generate an interrupt to the VXI host controller. At this time the host controller can unload either all results, or a subset consisting of failure data only. Optional masking of results data is possible as well in order to screen relevant data only. This cuts down considerably on post processing requirements.

## Deep On-Board Memory

By equipping the CVXI-1149.1/IM with fast on-board dual-port memory that is directly mapped in the VXI memory space, very long test patterns can be clocked out to the UUT without the need to reload data. The standard 4 Mbyte pattern buffer allows vector lengths of up to 32 Mbits if no results data is needed. Optionally, the available memory depth can be increased to 16 Mbytes (128 Mbits). This allows sufficient vector depth to handle UUT self-test applications involving complex ASIC's.

Scan pattern data structures are supported by the on-board processor which hold background and multiple overlay segments. This compression scheme maximizes the reuse of static portions of the scan patterns, with only variations over time needing extra storage. The processor reconstructs the complete bit stream in real-time during the UUT test cycle.

## Multiple Ports

The CVXI-1149.1/IM supports eight individual IEEE-1149.1 ports, each capable of managing multiple scan chains. At any time, two out of these eight TAPs can run simultaneously using separate TCK speeds, operated by the two main controllers. Ports that are switched out during a given scan are kept in a static state. In this way, the connected scan chain's status is preserved until operation of its TAP resumes. This allows tests to be performed on UUT systems containing up to eight individual scan chains. It also supports test cycles of up to eight single TAP targets at a time.

The two concurrent multi-tap controllers multiplex scan transactions between their four ports as required. Clock rates may be programmably altered to suit each TAP port as its controller prepares to drive it. Each UUT TAP is unaffected by the activity of the other three in the controller's group, since it is held in a stable state while others run.

All non-differential scan outputs are TTL level buffered signals capable of sinking/sourcing 64/32 mA of current and driving 50 Ohm terminated transmission lines. To minimize ground bounce and undershoot, noise suppression circuitry is added to each test access port.

Of the eight available test access ports, two are equipped with differential line drivers/receivers. This accommodates multi-drop hierarchical scan topologies such as the multi-drop Scan Bridge architecture used by National Semiconductor.

## Programmable Clock Delay

To compensate for propagation delay in long test cables between the CVXI-1149.1/IM

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boundary-scan tester and the UUT, a programmable delay can be enabled between the active TCK edge and the sampling of the unit under test's TDO data. This reduces the possibility of sampling errors caused by long cable delays when running at high clock rates.

The on-board processor provides an automatic calibration feature to determine optimum delay parameters for each TAP port. These values may be passed up to the host, which in turn may use them (or supply its own) at card setup configuration time. A unique delay characterization may be programmed for each port, being invoked automatically as the processor switches from one to another.

## VXI Compatibility

The CVXI-1149.1/IM is contained on a C-size VXI card, conforms to VXI system specification 1.4, and is controlled using word serial protocol messages and shared RAM. It can be used in conjunction with an embedded computer slot zero controller, or through an IEEE-488.2 or MXI/ VXI interface. Figures 2 and 3 show typical system configurations.

## Parallel I/O and SCANIO Modules

To accommodate various test environments, the CVXI-1149.1/IM is also equipped with 64 bi-directional digital I/O lines organized in 8-bit words. Each group of 8 bits can be tri-stated under software control, defining it as input rather than output. Port access can be accomplished under programmed embedded processor control. Parallel I/O operation may also be controlled through a JTAG scan chain on a dedicated TAP port. Thus, management of this feature may be accomplished as part of the scanning cycle. In this way, the parallel I/O data can be synchronized with scan test vectors.

The availability of digital I/O enhances the CVXI-1149.1/IM by providing control capability of the unit under test. It also serves as an additional set of test access points to the unit under test that can be used to verify operation of nodes that are not visible from the boundary-scan chain.

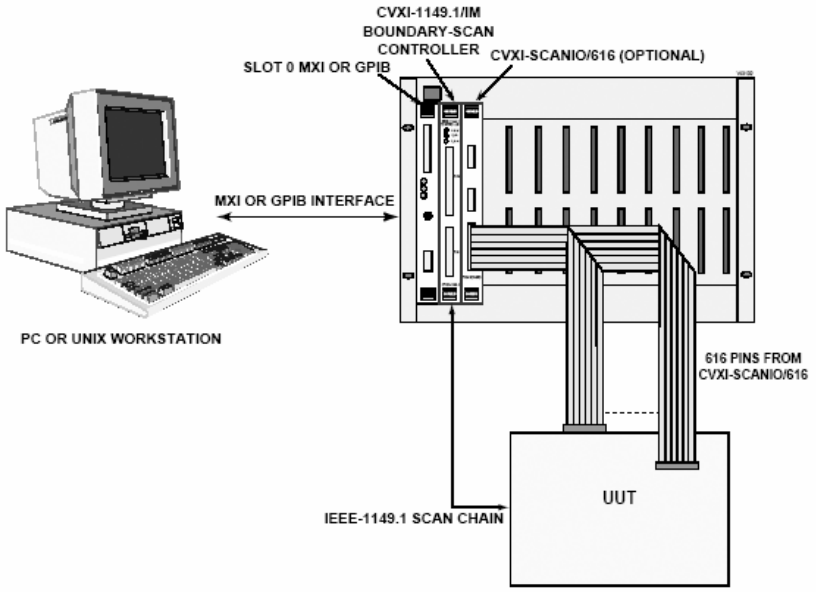



Figure 2. Typical MXI and GPIB Configuration

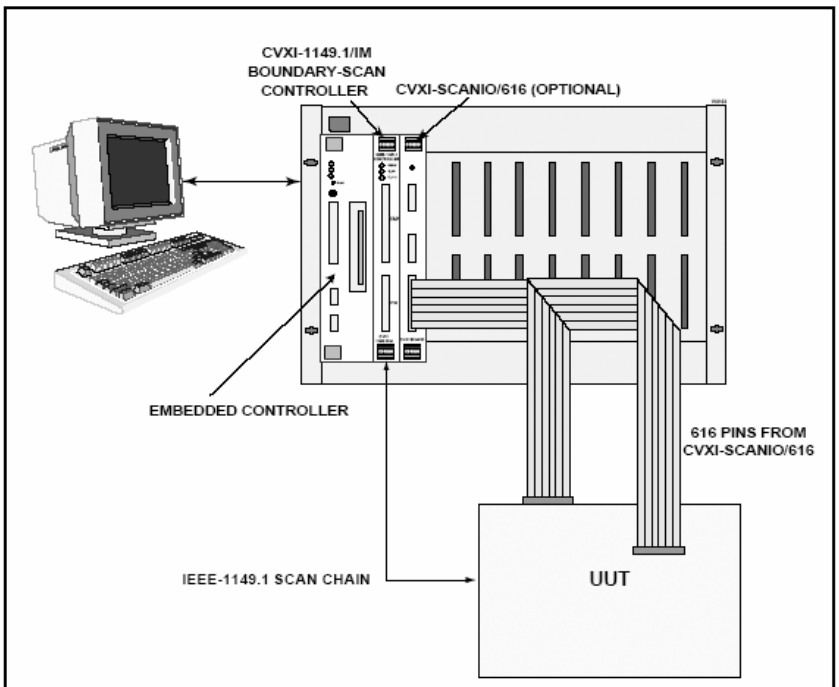



Figure 3. Typical Embedded Controller Configuration

If the number of non-scanable nodes exceeds the capabilities of the CVXI-1149.1/IM's 64 digital I/O lines, the Corelis model CVXI-SCANIO/616 VXI module can be used in combination with the scan controller. The CVXI-SCANIO/616 offers 616 bi-directional digital I/O lines (expandable to several thousand) that can be controlled from one of the CVXI-1149.1/IM's eight TAP's.

### TCK Generation

Two independent programmable TCK generators are used to drive the Test Access Ports at frequencies up to 35 MHz. Each generator is dedicated to one of the two TAP controllers. They operate independently from each other according to the needs of the active port. If different clock rates are required or if synchronization to the unit under test or other testers is required, one or both of the TCK's can be fed from an external clock input. The use of external clock inputs extends the range of the TCK speed down to DC due to the fully static design of the CVXI-1149.1/IM controller.

### Self-Test Mode

The CVXI-1149.1/IM provides two levels of self-test. Initially, power-up self-test is performed to test the proper operation of the internal hardware without interference with any of the external devices connected at the TAP ports.

The CVXI-1149.1/IM also supports an enhanced self-test loopback mode that provides additional testing including TAP buffers and connectors. This test method requires the installation of an external loopback cable harness, whose presence is automatically detected, enabling this test mode at power-up. In this case the TDO as well as all TMS lines are read back through the TDI input for verification.

### UUT Synchronization Features

Special operational features of the CVXI-1149.1/IM support different needs of certain UUT systems. In particular, there are situations where the UUT and external test equipment must be synchronized with scan activity. This requires the CVXI-1149.1/IM to signal that certain TAP states have been reached (such as one of the Update or Capture states). A related need is for the TAP controller to wait in one of the Pause states until triggered by the UUT system when it is ready to proceed.

### Event Detection

Each TAP controller may be programmed to signal either its entry into one of the Update or to one of the Capture states. The signal may be in the form of a VXIbus TTL trigger, or a modification of output Parallel I/O discretes. This alerts the UUT system to the possible need to respond as required.

### Pause Waiting

The pause waiting feature when programmed, causes the TAP controller to stay in any of the Pause states until triggered by an external signal. This feature, combined with the above event detection causes the controller to alert the UUT system when a response is required, and forces the controller to wait for a "ready" signal before proceeding. Thus 'sync-on-capture' and 'sync-on-update' are fully supported.

### BIST UUT Testing

Certain UUTs require their TAP controller to stay in the Run-Test/Idle state for a minimum time or TCK intervals while BIST is performed internally. This feature is fully supported under embedded processor program control via downloaded programming.

## ScanExpress and ScanPlus Family

Corelis has a complete family of boundary-scan test and in-system-programming tools. Corelis' ScanExpress and ScanPlus tools provide a user with the ability to perform comprehensive boundary-scan interconnect testing and in-system-programming of CPLDs, FPGAs, and flash memory devices.

Software is available for infrastructure and interconnects testing of both boards and systems. Boundary-scan defect testing is particularly useful for finding stuck at, opens, shorts, and bridging faults when using BGA components or other fine pitch, difficult to probe, packages.

The ScanExpress and ScanPlus family of tools include an automatic boundary-scan Test Pattern Generator (ScanExpressTPG™), boundary-scan test execution and in-system-programming software (ScanPlus Runner™), and a boundary-scan interactive debugger.

The ScanExpressTPG automatically generates test patterns that enable testing of boundary-scan chain integrity, PCB interconnects, buswires, and clusters including memories and FIFOs. These test vectors are then applied to the Unit Under Test through one of the Corelis boundary-scan controllers such as the CVXI-1149.1/IM.

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## SPECIFICATIONS

### Processor

- Am29030 32 Bit RISC

### On board memory

- 4 Mbyte (16Mbyte optional), 32 bit wide dual access shared RAM

### Clock source

- Dual internal programmable from 64 KHz to 35 MHz
- External through front-panel connector

### Interrupts

- VXI bus interrupt requester with user programmable priority level

### VXIbus TTL Sync Mode Triggers

- One of 8 lines programmable as input
- One of 8 lines programmable as output

### Front panel indicators

- The RESET red LED indicates that the card is in reset and all on-board logic is disabled. This LED is driven directly from the RESET bit (00) of the VXI control register and is under software control.
- The FAILED red LED indicates that power-up self-test failed.
- The VXI green LED indicates that the card is being accessed via the VXI bus.
- The JTAG green LED indicates that one of the UUT TAP interfaces is in the midst of scan transaction.

### Hardware Reset

- Via front panel hidden push button

### Connectors

- Eight TAP's are available through two 50 pin 3M type connectors
- 64 Digital I/O lines available through two 34 pin 3M type connectors
- External clock input available through a SMB connector
- 2 each external sync* active low edge TTL trigger inputs are available in the above 50 pin 3M type connector

### VXI bus interface

- C size, single slot card module
- Version 1.4 VXI bus specification compliant
- Message based protocol and shared RAM
- A16/A24/A32/D16/D32 compatible

### Power Consumption

- + 5 V @ 5.4 Amps Max

### Ordering information

- Model CVXI-1149.1/IM Intelligent Boundary-Scan Controller

### Includes:

- User manual
- Scan Library C source code on disk

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