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Find the *Corelis CVXI-1149.5* at our website: ***Click HERE***

CORELIS

CVXI-1149.5

MTM Bus Tester Module

Features

- **Full IEEE-1149.5 electrical and protocol compatibility**
- **MTM-Bus Master, Slave, or Monitor**
- **Single Slot, C size VXIbus Rev. 1.4 compatible**
- **Dual MTM-Bus physical interfaces**
- **Compatible with BA-1149.5 Bus analyzer**
- **MTM-Bus Interface options: TTL, BTL, custom**
- **Error injection and detection on a word-by-word basis**
- **On-board RISC CPU**
- **4M byte (8M byte optional) data storage for transmit and receive data**
- **User definable directives**
- **Received data time stamping**
- **Programmable MTM-Bus clock rates up to 12.5 MHz**
- **Internal or external MTM-Bus clock source**
- **Message based device with shared RAM**
- **VXIbus slave A16/A24/A32 D16/D32 and programmable interrupter**



What is IEEE-1149.5?

IEEE-1149.5 standardizes a serial backplane test and maintenance bus which is used to integrate testable modules, which may consist of one or more logic boards, into a testable and maintainable subsystem. The bus protocol standardizes a method for communication of test and maintenance commands and serial data between a subsystem test control module (bus master) and the other modules (bus slaves) on the bus. The MTM-Bus is intended for use in the test, diagnosis, and maintenance of electronic subsystems and modules. It may be used to support module test, subsystem test, subsystem diagnostic, and software/hardware development.

To support these applications, the MTM-Bus is designed as a serial backplane bus with multidrop topology.

As the multidrop bus signals are common between all modules, a board may be removed from the backplane without breaking the communication link between other modules in the backplane. With the appropriate physical-layer design, the protocol supports access between a single master module and up to 250 individually addressable slave modules for a total of 251 MTM-Bus modules. Addressing is defined so that the bus master may communicate with one, some, or all of the slaves at one time.

As the bus may be used to transmit a significant amount of data, such as serial test patterns, the bus protocol has been designed to support full-duplex data transfer operations. To ensure that available IEEE-1149.5 bus interface devices support a reasonable data rate, IEEE-1149.5 bus interface

devices are required to support MTM-Bus operation to at least 6.25 MHz. The upper limit for the bus operation is limited only by the implementation of the physical layer protocol and the bus interface devices used.

Overview

The CVXI-1149.5 is a single-slot, VXIbus "C"size module, designed for control, test, and simulation of systems that utilize the IEEE-1149.5 Standard Backplane Module Test and Maintenance (MTM) bus protocol. The CVXI-1149.5 provides intelligent interfacing between the serial MTM-Bus and the VXIbus. Software controls the CVXI-1149.5 operation as either an MTM-Bus master, slave emulator, or bus monitor. Extensive error injection and detection capabilities are also provided. Its full compliance with the IEEE-P1149.5 MTM-Bus protocol and the VXIbus system specification revision 1.4 makes it an excellent choice for testing, dynamic simulation, and development applications. The CVXI-1149.5 is a message based, VXIbus slave device with shared-RAM.

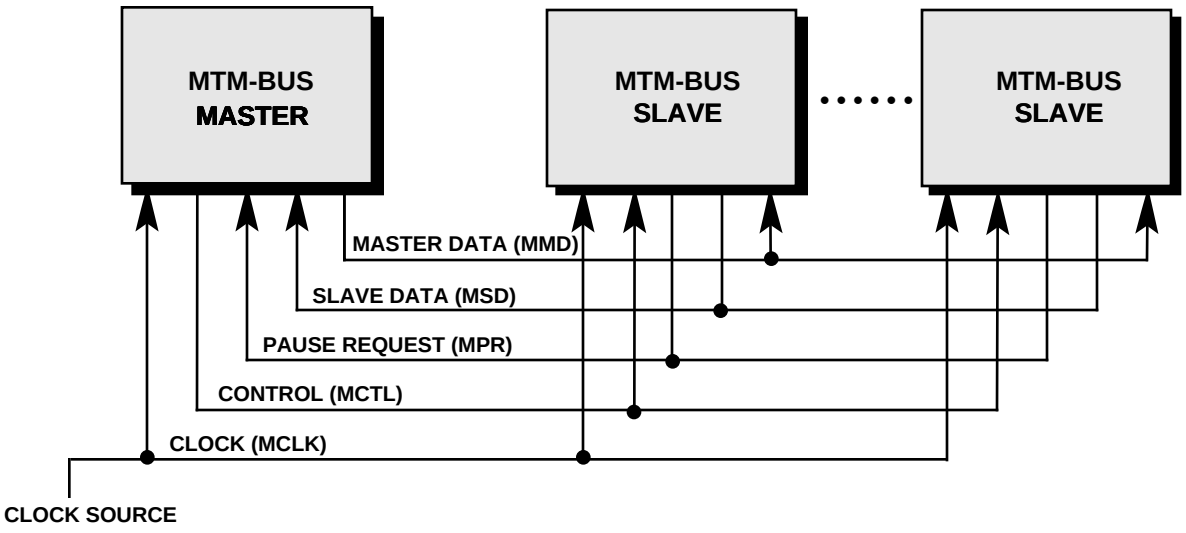
The operating modes of the CVXI-1149.5 are controlled through the use of on-board A16 registers. MTM-Bus message traffic is stored and retrieved using the on-board dual-port (shared) RAM. The CVXI-1149.5 internal registers control and operate the module. For example, the Configuration register defines the operating mode, the Clock Select Register selects the clock source and programs the clock divider circuit, the Interrupt Select register selects one of seven VXIbus interrupt request signals.

The CVXI-1149.5 on-board 4M byte (8M optional) memory is shared by the internal CPU and the VXIbus host with memory arbitration being handled automatically by the hardware. In addition to storing the MTM-Bus message data, the memory contains a directive list that sequences the card through its operational modes. The CVXI-1149.5 recognizes special commands called “directives” that control its operation as an MTM-Bus device. Each directive is a simple 32-bit instruction that describes one of a handful of predetermined operations that the card is required to perform. The directive list method is used in both master and slave modes.

The CVXI-1149.5 may also be used as a passive MTM-Bus monitor. In this mode, all, or filtered messages transferred across the MTM-Bus can be captured and recorded in the dual port memory along with the time-stamping and the status of each serial word received. The status bits that are appended to each of the received words provide an instant, word by word information of parity, short word, long word, header word and slave interrupt.

The MTM-Bus signals are duplicated, creating two MTM-Bus interface circuits: MTM_J and MTM_K. The CVXI-1149.5 card can be physically connected to two bus systems at the same time, while communicating with one bus at a time. This dual bus implementation duplicates the wires and physical layer protocol without replicating the link-layer protocol and allows recovery from an MTM-Bus fault by switching to a backup set of MTM-Bus signal interconnections. This feature is implemented in all three of the CVXI-1149.5 modes of operation.

The CVXI-1149.5 card is available with either open collector TTL or BTL compatible physical MTM-Bus interface. The capability to accommodate custom data interfaces



IEEE P1149.5 MTM-bus backplane signals. Includes the free-running test-bus clock (MCLK), Master and Slave data signals (MMD &MSD), the Master control signal (MCTL), and the optional pause request signal (MPR)

BACKPLANE MTM-BUS SIGNALS

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is accomplished by means of an on-board "daughter board" capability. This feature allows a user (or Corelis/JTAG Technologies) to design a custom physical interface for applications requiring a unique voltage level, output impedance, or a differential drive capability.

Shared Memory

The card is designed to communicate with the MTM-Bus by sending data that is stored in the dual-port memory to the MTM-Bus and at the same time store incoming messages in other locations of the dual port memory. The memory is accessible to the host computer at any time.

The on-board microprocessor updates memory resident pointers that are used to direct the host to the data buffers in memory.

The shared memory VXIbus address is programmed by the VXIbus resource manager by writing the appropriate address offset to the VXIbus Offset register. The on-board memory arbitration circuitry provides the host accessibility to the entire memory at any time. This feature eliminates the overhead of register based communication and enables the host and the on-board microprocessor to exchange larger data blocks at maximum speed with virtually no overhead, handshake protocol or acknowledge mechanism.

MTM-Bus Communication

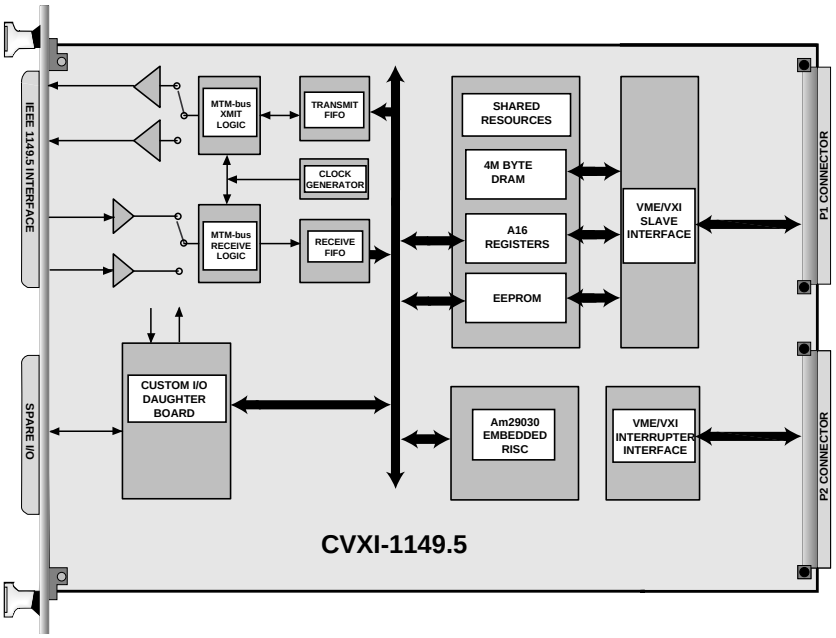
The MTM-Bus interface is configured differently for the three modes of operation. In the Master mode of operation, the CVXI-1149.5 card drives the MCLK, MCTL, and MMD signals and receives the MSD and the MPR signals. The user can command the card to receive MCLK externally and to ignore the slave MPR signal.

In the Slave mode of operation, the card receives the MCLK, MCTL and MMD signals and drives the MSD and the MPR signals. The user can also configure the card to drive MCLK.

In the bus Monitor mode, the card is only receiving the MTM-Bus signals and the data sent by both the external master and slave(s) is recorded in the dual port memory along with the time-stamping of each transfer. The user can program the card to receive all messages or to filter the data and only record messages sent to/ from a particular MTM-Bus slave.

Transfer Rates

The MCLK clock rate is programmable from 156 KHz to 12.5 MHz in steps. The user has the option of configuring the card to generate the clock on-board or to receive it from an external source. The clock source selections include the on-board clock generator, the front panel EXT CLK connector, the VXIbus TTLTRG* lines or the MTM-Bus (external) MCLK signal.



CVXI-1149.5

Error Injection and Detection

The CVXI-1149.5 card is capable of intentionally generating different types of MTM-Bus related errors. By injecting errors, the application programmer is able to test the error handling and recovery of the unit under test (UUT). When configured as an MTM-Bus master, the card can generate parity errors, send words that are either normal length, too short or too long. Also, the card can override the slave MPR signal, thereby causing a data overrun (DOR) error on the slave. The parity and word-length errors can be programmed on or off during each transmitted word, which enables the application program to create arbitrary sequences of errors and monitor the UUT behavior under such conditions. The data sent by the card is controlled directly by the user simply by placing the data in the dual port memory. Arbitrary data that contains MTM-Bus header words and data along with possible errors is read from the memory by the card and is transmitted over the MTM-Bus.

The card is capable of detecting MTM-Bus communication errors, including MCLK collision, MCTL and MMD collision (master mode), MSD collision (slave mode), received data parity errors, word length errors (slave), MPR time-out (master mode), data overrun (slave mode) and missing MCLK.

Programming

Programming the card from the host is performed in two distinct modes of operation, differing mainly in the type of operation required and the speed of executing the command. The first programming mode is the VXIbus word serial protocol which is used primarily for configuration and set-up of the card by the VXIbus resource manager. Note that the word serial protocol is a VXIbus imposed standard that is used by all VXIbus message based devices and for the most part is transparent to the application programmer. The second programming mode is the shared memory directives that enable the

application program to command the card through the various MTM-Bus related transactions in a very efficient manner.

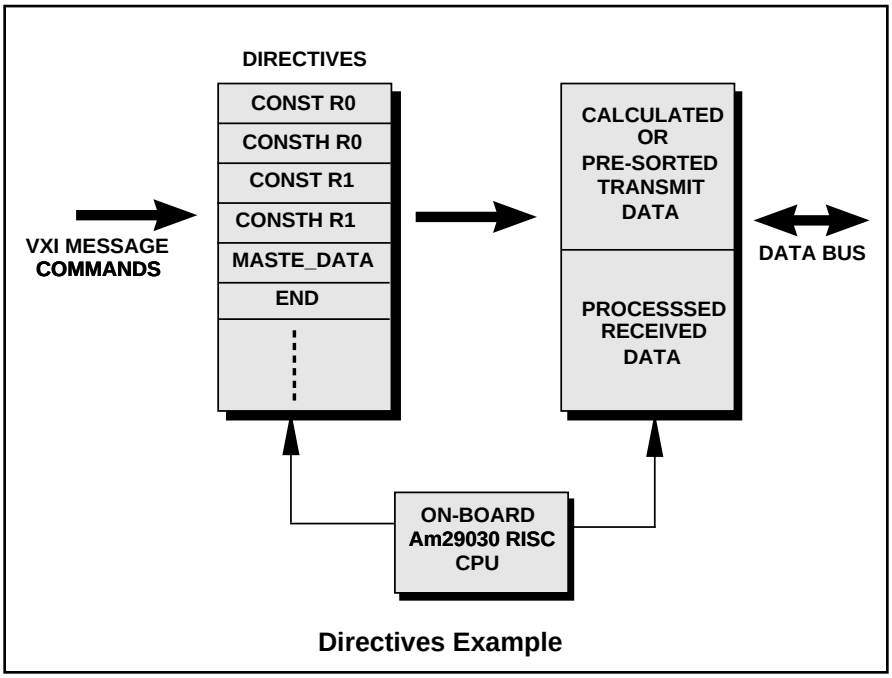
Word Serial Protocol

The card accepts commands using the word serial protocol, utilizing the VXIbus A16 registers to transfer commands and status information to and from the external host(s), also known as commander(s). The operations controlled by the word serial protocol are used by the VXIbus resource manager to identify the card type and to configure the card as a message based device in a global VXIbus test system, containing other VXIbus modules. The command repertoire is similar to the one found in other VXIbus message based instruments. Note that the VXIbus word serial protocol itself is relatively slow, aimed at non real-time critical applications. Upon power-up, the word serial protocol is used by the VXIbus resource manager (typically plugged into slot 0) to configure the card and to assign its memory address and its interrupt request line. When power-up initialization and self-test successfully complete, the communication to and from the host is performed primarily via the dual port memory resident directives.

Directives

Operation of the MTM-Bus interface is controlled by special commands called directives. Unlike word serial commands, directives are memory based commands. The directives reside in a pre-assigned area of the dual-ported memory and are typically written by the host and read by the on-board microprocessor. Interpretation of the directives by the on-board processor is performed very fast so that most directives are interpreted and executed in a few microseconds. In a typical MTM-Bus application, the host configures the card via the word serial protocol and then instructs the Am29030 microprocessor to commence interpreting the directives.

The directives are organized in a sequential list and are read and executed by the on-board microprocessor one after the other.



Directives Example

The directive list resides in the shared memory. The host loads the directives prior to instructing the card to start reading and parsing the directives. The host can prepare data packets required to be sent serially to the MTM-Bus and store it anywhere in the unallocated shared memory. Directives can point to these buffers and instruct the microprocessor to read the data packets and send them to the MTM-Bus. The card does not start executing the directives in the list until it is so commanded by the VXIbus commander (host). The ***run*** word serial command is sent by the host instructing the card to start executing the directives in the list.

The following example of a directive list shows a simple application that instructs the CVXI-1149.5 card to send and receive data to/from the UUT, and to interrupt the host when all done. In this example, it is assumed that the card was previously configured to Master mode of operation and will start executing the directive list as soon as the word serial ***RUN*** command is issued:

CONST R0, $0	set R0 lower half to $0000.
CONSTH R0, $20	set R0 upper half to $0020.
CONST R1, $1000	set R1 lower half to $1000.
CONSTH R1, $20	set R1 upper half to $0020.
MASTER_DATA, R0, R1, 12	Transmit 12 words from address in (R0) and store received words in address in (R1).
END	Halt further directives execution and interrupt the host

Each directive occupies one 32 bit word in the dual port memory. The example above shows how with only 6 simple one-word directives the card can send and receive messages to and from external MTM-Bus slaves.

The directive list can be enhanced by the user to include more directives that are application specific. For example, to handle non-volatile memory programming via the MTM-Bus, the user can add a WRITE_EEPROM directive that calculates all the necessary steps required for programming the memory and prepares the correct raw data and address structures to be sent to the unit under test (UUT). Such a directive would receive minimal data from the host and would greatly expedite memory programming by generating much of the required commands, data and address patterns on-board. The use of the directives concept allows the CVXI-1149.5 to be used as a powerful and flexible intelligent serial data generator and recorder, thereby reducing the VXIbus system host involvement.

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MTM-Bus Operational Modes

The CVXI-1149.5 has three distinctive modes of operation: Bus Master, Bus Slave, and Bus Monitor. The host commands the card to configure itself to the desired mode by issuing the ***Low Level Configuration*** word serial command, after setting the reserved parameters in dual-port memory.

MTM-Bus Master Mode

The CVXI-1149.5, when used as a bus master, communicates with slaves under test using messages which consist of a series of packet transfers. A message consists of a Header packet, an optional Acknowledge packet, and a variable number of Data packets. The messages are written to the dual port memory by the host, which then commands the CVXI-1149.5 card to go execute the directive list that instruct the microprocessor to read the data and to send it over the MTM-Bus.

To start a message, the CVXI-1149.5 master transmits a Header packet which includes the address of the slave(s) who are to participate in the message sequence along with a bus command. If a single slave is addressed and the Header packet includes a request for an acknowledge packet, the addressed slave will respond with the acknowledge packet (which includes the slave status word). The message may then include the transfer of data packets, in either a half-duplex or full-duplex mode, between the CVXI-1149.5 master and slave modules. If multiple slaves are addressed, no acknowledge packet will be sent from any slave, and any transfer of Data packets is from the CVXI-1149.5 master to the slave(s).

All packet transfers occur under the control of the CVXI-1149.5 master module. The CVXI-1149.5 master controls all operations on the MTM-Bus by asserting and releasing the Module Control (MCTL) and Module Master Data (MMD) signals. Data transferred between master and slave modules is done serially with 17-bit packets. All data within packets is serially transferred most-significant bit (MSB) first. Although the transfer of data packets is controlled by the CVXI-1149.5 master, addressed slave modules may request that the CVXI-1149.5 master insert Pause states between data packet transfers by asserting the Pause Request (MPR) signal. This feature may be used to accommodate slow slaves or to simplify data flow control across the interface between zones with asynchronous clocks.

Slave modules may also request the attention of the CVXI-1149.5 master by sending an interrupt, multiplexed on the Slave Data (MSD) signal wire, at any time between packet transfers. As there is only one MSD input to the master module, the master identifies the interrupting module via polling or a contend sequence.

Slave Mode

Each CVXI-1149.5 emulated slave is addressed by a programmable eight-bit address field. This eight-bit field allows for 256 addresses which include 250 single module addresses for both master and slaves (‘0’ through ‘FA’ HEX), one broadcast address (‘FB’ HEX), and four Multicast addresses (‘FC’,’FD’,’FE’, and ‘FF’ HEX).

The slave module responds to one of the software programmable 251 module addresses so that it can be addressed by the master module. An additional address parity bit is provided to ensure that the slave will not improperly respond to another module’s address in the event of a module address fault.

Through the use of the directives feature, a slave module can act as a smart slave or a dumb slave. As a smart slave, the module could, for example generate pre-determined data patterns or perform certain calculations on received or transmitted data in a test system.

Monitor Mode

In this mode, all, or filtered messages transferred across the MTM-Bus, can be captured. This mode is enabled by a host command via the VXIbus.

BA-1149.5 Bus Analyzer

The CVXI-1149.5 card is fully compatible with the BA-1149.5 MTM-Bus analyzer product. The BA-1149.5 unit, together with a Hewlett-Packard HP1650/ HP1660/ HP16500 series logic analyzer, provides real-time MTM-Bus command monitoring and tracing capabilities that are essential for MTM-Bus hardware and software debug and test. The MTM-Bus front panel connector is designed such that a straight through flat cable can be used to connect the CVXI-1149.5 card to the BA-1149.5 bus analyzer unit.

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Specifications

Word Serial Commands

Begin Normal Operation
Abort Normal Operation
End Normal Operation
Read Protocol
Read Protcocol Error
Read Interrupters
Read Interrupter line
Assign Interrupter line
Asynchronous Mode Control
Control Event
Add Directive
Continue Directive Execution
Copy and Execute Firmware
Halt
Clear Interrupt Cycle
Low Level Configuration
Set Interrupt Mask
Run
Selftest
Execute Directive List
Displays MTM-bus State Information in MTM-bus Mnemonics

MTM-bus Commands

The commands supported are:
Core Commands
Data Transfer Commands
Module Initialization and Self-Test Commands
Module I/O Control and Test Commands
User-Defined Commands

A complete description of these commands is available in the MTM-bus specification.

Master Mode

- Single or multiple slave addressing
- 16 (short), 17 (normal), or 18 (long) bit serial packets, MSB first
- End of Message (EOM) indicator bit
- Programmable slave Pause Request (MPR) recognition and time-out
- Slave interrupt recognition on a word by word basis
- Supports all link layer bus states
  - IDLE
  - XFER
  - PAUSE
  - ERROR
- Programmable Parity error insertion on a word-by-word basis
- MPR programmable time-out:
  - Disabled
  - 1 to 16 µsec in 1µsec steps
  - 100 to 1500 µsec in 100 µsec steps

Slave Mode

Addressing

- 8 bit addressing (256 addresses)
- 250 single module addresses (0 through 'FA' HEX)
- 1 broadcast (FB HEX)
- 4 multicast (FC, FD, FE, and FF HEX)

Interrupt and Error Handling

- Parity checker for all incoming data words
- Integrity checker verifies word length for all incoming messages
- MSD line collision detector
- Detection of no clock on MCLK line
- Programmable parity generator (odd / even) on a word by word basis for all MSD data words
- Programmable interrupt generator can be activated or turned off after each word transmitted over the MSD line

Time Stamping

- 24 bit time stamp on all received records the time intervals of incoming data

Monitor Mode

- Recording of MTM-Bus filtered data
- Recording of both master and slave messages with time-stamping
- Monitors MMD, MSD, MCTL, and MPR
- Recording of errors, slave interrupts, and header word indicators
- 24 bit time stamp on all received messages

Directives

Certain directive commands are included with the module. The user can also add any number of application specific directives as desired.

DIRECTIVE	DESCRIPTION
CALL	Call a directive subroutine
CONST	Load a register with a 16-bit constant
CONSTH	Load the upper 16 bits of a register
DELAY	Delay directive execution for the specified duration
END	End directive execution
INTERRUPT	Interrupt the host computer
JUMP	Change the flow of execution to another address
LOOP	Cause directive execution to loop the specified number of times
MASTER_DATA	Send MTM -bus Data in Master mode
READ_A16	Read a 16 bit A16 register
READ_RAM	Read a 32 bit shared RAM memory location
RETURN	Return from a directive subroutine
SLAVE_DATA	Receive/Respond to MTM-bus data in Slave mode
WRITE_A16	Write a 16 bit data value to an A16 register
WRITE_RAM	Write a 16 bit data value to shared RAM

On-Board Memory

4M bytes of dual port RAM (8M optional), 32 bits wide, accessible by both VXIbus host and on-board CPU

Clock Source

- Programmable internal or external clock source.
- External clock from front panel connector
- External clock from any one of eight VXIbus TTLTRG* trigger lines
- Internal clock source programmable from 156 KHz to 12.5 MHz

Processor

Am29030 Embedded 32 bit RISC Microprocessor

Interrupts

VXIbus interrupt requester, priority level is user programmable

MTM-Bus Redundancy

2 interface circuits MTM_J and MTM_K provide direct hook-up to two MTM-Bus interfaces without external switching devices

VXIbus Interface

- C size, single slot
- Version 1.4 compatible
- Message based, with shared RAM
- A16/A24/A32 D16/D32 compatible
- Programmable Interrupter

MTM-Bus Outputs

- BTL open collector, 100 ma sink current
- TTL open collector, 64 ma sink current
- Custom interface with an optional user specified daughter card

Power

+5 V @ 5.4A Max.

Front Panel LED's

RESET	Indicates the on-board Am29030 is reset by the host
FAIL	Indicates failed self-test condition
ACCESS	Indicates card is being accesse by a VXIbus host
MTM - BUS	Indicates data transfer over the MTM-Bus

Reset Switch

Via a front panel hidden push-button momentary switch

Connectors

- SMB connector for external clock input
- 50-pin 3M type connector for MTM-Bus interfaces. Fully compatible with the BA-1149.5 MTM-Bus analyzer
- 34-pin 3M type test connector for optional daughter card.

CORELIS 12607 Hidden Creek Way
Cerritos, California 90703
Tel: (562) 926-6727, Fax: (562) 404-6196
sales@corelis.com
http://www.corelis.com
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