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Find the *Corelis NetUSB-1149.1* at our website: ***Click HERE***

CORELIS

NetUSB-1149.1/E™

High-Performance LAN/USB 2.0 Boundary-Scan Controller

- **Concurrent (gang) testing and in-system programming of CPLDs and Flash devices for up to 4 boards (higher number supported with additional hardware)**
- **User programmable sustained Test Clock (TCK) up to 80 MHz, in <2% increment per TAP, at effective throughput of 320MHz**
- **Supports direct programming of I2C and SPI-based devices**
- **Hardware comparison of expected patterns against observed results is done concurrently for each TAP**
- **Easily connects to PCs and workstations via USB port or 10/100Base-T Ethernet**
- **High-speed (up to 480 Mbit/sec signaling) device compliant with Revision 2.0 of the USB Specification (backward compatible with the Full-speed features of USB 1.1)**
- **Pre-power up test for shorts between power and ground lines on the UUT for each TAP**
- **TAP signals and GPIO discrete signals are individually programmable from 1.3V to 3.3V (5 volt tolerant)**
- **Direct Write signal for expediting Flash programming**
- **Support for monitoring Flash RDY/BSY**
- **USB and Ethernet connection allow extended distance from PC to UUT- no TAP extenders are needed**
- **Automatic signal delay compensation for long cable lengths to the UUT**
- **Plug and play Windows device drivers**
- **Fully compatible with ScanPlus and ScanExpress families of products**



Figure 1. NetUSB-1149.1/E Boundary-Scan Controller

Introduction

In the last few years, the use of boundary-scan has expanded beyond traditional board test applications into in-system programming of CPLDs, FPGAs, and Flash memories. These new applications require much higher performance.

Until now, available products were limited in Test Clock (TCK) frequency and the comparison of the expected patterns with the observed results was done by the host computer. Now that boards include more and denser memories including flash, users are asking for higher throughput boundary-scan tools that will allow faster testing and in-system programming. This includes concurrent (often referred to as gang) testing and in-system programming of more than one board at a time.

In response to this need, major development efforts in Boundary-Scan technology were undertaken at Corelis. The success of this development has produced a quantum leap in scan vector throughput, maintaining Corelis as the clear leader in providing sophisticated yet easy to use Boundary-Scan test equipment.

A key element of this ground breaking technology is the NetUSB-1149.1/E™ controller which dramatically increases the test and in-system programming speed by applying a vast number of innovative and proprietary techniques developed at Corelis.

The result of these new techniques allows for an unsurpassed boundary-scan throughput at TCK frequencies reaching a sustained 80MHz rate and a scan efficiency of 100% at each of up to four concurrently scanning JTAG ports.

Corelis thus presents the NetUSB-1149.1/E High-Performance Boundary-Scan Test and In-System Programming Controller, as the premier solution for users whose applications demand the highest possible scan vector throughput that is currently available on the market.

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General Description

The NetUSB-1149.1/E is an advanced robust controller that can be used in the testing and/or in-system programming (ISP) of devices, boards, or systems compliant with the IEEE-1149.1 standard. The controller connects to the computer either through it's USB interface or LAN interface for easy installation at close or remote locations.

The NetUSB-1149.1/E controller contains several performance enhancing functional sections aimed at increasing test vector and in-system programming throughput. The combination of these functional elements results in a very high data-scanning rate, which is completely decoupled from the USB and Ethernet intefaces. The scanned patterns are distributed to the target device or devices via the TAP interfaces on the controller.

The NetUSB-1149.1/E controller can apply test vectors and/or ISP patterns to boards with a variety of JTAG chain topologies. In the simplest, yet often used case, the controller will provide the interface between the computer and a target system consisting of a single JTAG Test Access Port (TAP). This would be the case where the target system consists of one JTAG chain and its associated TAP.

If the board under test consists of groups that include multiple devices, each with their own respective TAP, then the NetUSB-1149.1/E allows for test vectors to be applied to each of the target TAPs individually, one TAP at a time, or jointly to all of the TAPs. Figure 1 depicts such a configuration.

Figure 2 depicts a case where the NetUSB-1149.1/E is connected to four identical boards. In this case the system can test and program the four boards concurrently. Note that the concept of concurrency here not only applies to the simultaneous application of test vectors and ISP patterns to each board but also applies to the simultaneous verification of each individual board. A failure on any of the individual boards will be properly logged and will not prohibit the continuation of testing on the remaining target devices. The concurrent (often referred to as gang) mode of operation offers great performance increases when testing, in-system programming, and verifying multiple targets.

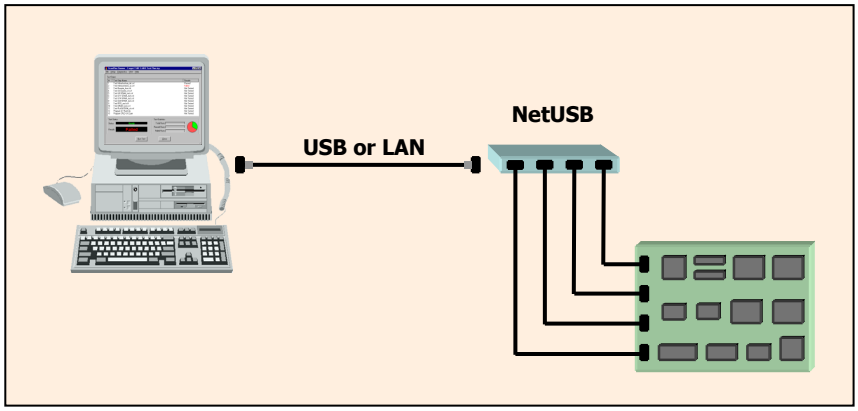


Figure 1. Connection to a single UUT with four TAPs

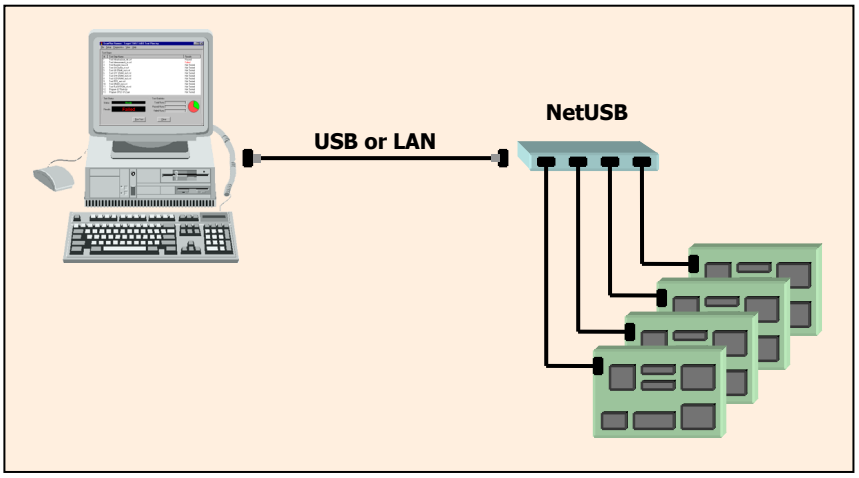


Figure 2. Connection to four UUTs with a single TAP each

Programmable Clock

The system-wide TCK rate for all TAP ports is programmable under software control. A wide range of TCK frequencies can be achieved by using the on-board Phase-Locked-Loop (PLL) generation circuitry. The user is given the ability to select the desired TCK rate from a range of values from 390 KHz to 80MHz at resolution increments of less than 2%.

Adjustable Low Voltage Outputs

The voltage level of each TAP is software programmable and can be set to any voltage between 1.3V and 3.3V in increments of 0.05V. The ports of the NetUSB-1149.1/E can also be slew rate (fast/slow) adjusted.

Scan Input Signal Delay Compensation

Automatic delay compensation is inserted within the signal paths. This feature is used to combat the well-known problems associated with the combination of high TCK rates and remote target locations at extended distances.

Target Voltage Detection System

The NetUSB-1149.1/E includes analog-to-digital converters, which can measure connected power voltages from the target. Such voltages from two distinct target levels can be measured and compared against user-defined limits. This feature can provide detailed signal voltage

checks at any stage of a test plan.

Automatic Detection of Target Power Shorts

With the target powered down, a well-regulated drive current with current limit can be momentarily applied to the target power bus. By measuring this current, the approximate load resistance can be calculated. This provides for the automatic detection of target power shorts, prior to applying power to the target unit.

Target Presence Detection Capabilities

The TAPs on the NetUSB-1149.1/E have a dedicated pin on the JTAG interface connector that can be used to detect the presence of the target board. The state of this signal can be monitored by software to detect both the presence of the target device as well as the proper insertion of the test cable.

Parallel Input/Output Ports

Each TAP connector contains 3 general purpose parallel I/O signals (GPIOs) whose direction and drive (totem-pole or open-collector) is configurable. The input and output ports can be used to control and sense various functions in the target system which cannot be controlled or observed through boundary-scan operations. These ports are useful for the testing of target systems that incorporate components that are not compliant to IEEE Standard 1149.1. Open-collector signals are often needed to drive reset and emulation signals.

Direct Programming of I2C and SPI-based Devices

The NetUSB-1149.1/E includes the capability of directly programming I2C and SPI-based devices. The SPI and I2C interfaces on the NetUSB-1149.1/E are independent of the JTAG test interface; this means that the user can use the NetUSB-1149.1/E controller to perform JTAG-based testing and programming and also to perform direct programming of serial EEPROM and flash memories without removing the JTAG connector or switching to a dedicated SPI and I2C programmer.

Using direct programming port, serial FLASH/EEPROM devices can be programmed at speeds up to the device theoretical programming time. This is significantly faster than programming the devices indirectly using JTAG, typically 10 times faster and often surpassing this, depending on target configuration.

Built-in Self-Test

The NetUSB-1149.1/E has a built-in self-test capability. Logic has been provided at the local TAP connector to loop back data shifted out on TMS and TDO.

USB Interface

The NetUSB-1149.1/E can connect to the host PC computer via its USB interface. The NetUSB-1149.1/E is a high-speed device compliant with Revision 2.0 of the USB Bus Specification (backward compatible with the full-speed features of Revision 1.1).

Ethernet Interface

The NetUSB-1149.1/E can also connect to the host PC computer or workstation via a standard 10/100BaseT LAN interface. The Ethernet interface is IEEE 802.3u 100BASE-FX compatible with automatic speed switching, accessed through an RJ-45 connector.

Pin	Signal Name			I/O	Description
1	TRST*			Input to UUT	Test Reset (optional)
3	TDI			Input to UUT	Test Data Input
5	TDO			Output of UUT	Test Data Output
7	TMS			Input to UUT	Test Mode Select
9	TCK			Input to UUT	Test Clock
11	GPIO1	Write_Strobe*	SPI_CS2*	Input to UUT	General Purpose Output, Flash Programming Write Signal or SPI Chip Select (optional)
13	GPIO2		SPI_SCK	Input to UUT	General Purpose Output or SPI Serial Clock (optional)
15	GPIO3	Ready_Busy*	SPI_SDO (MISO)	Output of UUT	General Purpose Output, Flash Programming Ready Signal or SPI Serial Data Out (optional)
16			SPI_SDI (MOSI)	Input to UUT	SPI Serial Data Input (optional)
17	VCC1			UUT Power Rail	UUT Power Test Point 1 (optional)
18	I2C_SCL			Input to UUT	I2C Serial Clock (optional)
19	VCC2			UUT Power Rail	UUT Power Test Point 2 (optional)
20	I2C_SDA		SPI_CS1*	Input to UUT	I2C Serial Data or SPI Chip Select (optional)

Table 1. NetUSB-1149.1/E 20-pin Connector

Note: Direction specified is relative to the UUT. All other even pins of the connector (2, 4, 6, 8, 10, 12 and 14) should be connected to ground (GND) .

Compatible with ScanPlus and ScanExpress Family of Products

The NetUSB-1149.1/E is both hardware and software compatible with the complete ScanPlus™ and ScanExpress™ family of IEEE-1149.1 test and in-system programming products.

The NetUSB-1149.1/E also contains an expansion port that is compatible with other equipment supplied by Corelis such as the ScanTAP-32™. Using this expansion port, the number of TAPs supported by the controller can be expanded.

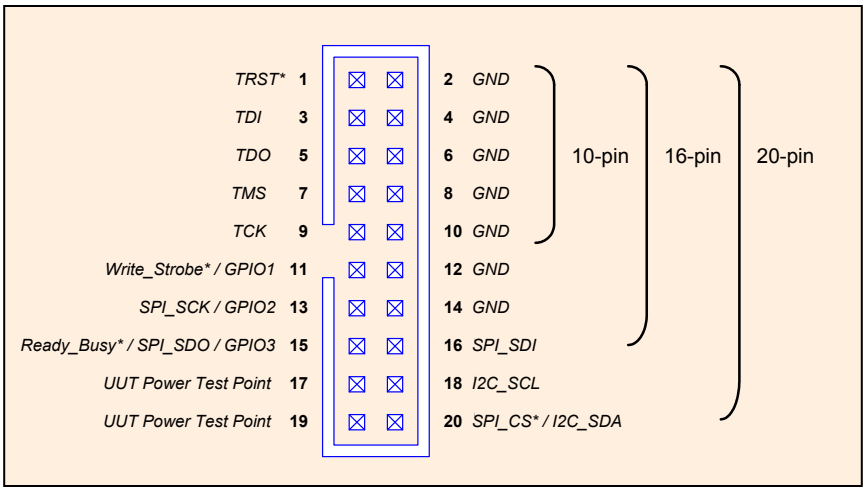


Figure 3. NetUSB-1149.1/E target connector pin assignments for various TAP cables

TAP Connectors

The NetUSB-1149.1/E contains four 20-pin TAP connectors. All four connectors have the same signals and the same pinout. Each connector is a shrouded header (0.100 × 0.100 in. spacing) with long ejectors that are compatible with standard 20-pin IDC flat cable connectors (with strain relief). Note that only the first 10 pins are required for basic boundary-scan operation. For Flash Programming with external write or the Ready Busy signal, use the first 16 pins of the TAP. To build in support for power-to-ground short checking, use all 20 pins of the TAP. Also, to do direct programming of I2C or SPI-based devices in addition to JTAG testing and in-system programming, it is recommended to use the 20-pin TAP.

Pins 17 and 19 of each NetUSB-1149.1/E TAP connector can be used to sense that the target power pin is not shorted to GND. Up to 2 different power pins can be checked on each of the four 20-pin connectors of the NetUSB-1149.1/E controller.

The 3 GPIO signals are general-purpose output signals that are directly controlled by the Parallel I/O menu of ScanPlus Runner. The dual purpose Write_Strobe* (GPIO1) signal is used for Flash programming, and if used will override the Parallel Output (GPIO1) function. The dual purpose Ready/Busy* (GPIO3) signal is used for Flash programming, and if used will override the Parallel Output (GPIO3) function.

For direct programming of I2C-based devices, pins 18 and 20 provide the I2C SCL and SDA lines respectively.

For direct programming of SPI-based devices, pins 11, 13, 15, 16 and 20 provide the CS2*, SCK, SDO, SDI and CS1* lines respectively.

For the target design, it is recommended that an industry-standard 10-pin, 16-pin or 20-pin TAP connector format be used, depending on the specific testing and in-system programming requirements. Refer to Corelis application note 06-118 for additional details on these different connector formats. Corelis offers TAP cables to mate with all of these different formats.

Ordering information

NetUSB-1149.1/E (P/N 10337A) that includes:

- NetUSB-1149.1/E Hardware Controller
- NetUSB-1149.1/E User's Manual
- NetUSB-1149.1/E Software Disk
- Four 20-pin to 10-pin target cables
- Power Supply

Adjustable Voltage	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
3.3	-0.3	0.8	2.0	3.6	0.4	2.9	8	-8
2.5	-0.3	0.7	1.7	3.6	0.4	2.1	8	-8
1.8	-0.3	0.6	1.2	3.6	0.4	1.4	8	-8
1.5	-0.3	0.5	1.0	3.6	0.4	1.1	8	-8
1.25	-0.3	0.4	0.8	3.6	0.4	0.8	6	-6

Table 2. NetUSB-1149.1/E Signal DC Characteristics

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NetUSB-1149.1/E Specifications:

Host Computer	
CPU	Pentium II @ 266 MHz or better
Operating System	Windows 95/98/ME/NT/2000/XP
USB Interface	
Version	Revision 2.0 high-speed device (backward compatible with the full-speed features of Revision 1.1)
Ethernet Interface	
Version	IEEE 802.3u 100BASE-FX
TAP Interface	
Version	IEEE-1149.1
Connectors	Four 20-pin shrouded headers, 0.1 in. × 0.1 in. spacing (3M 3428-6302 or equivalent)
Number of TAPs	4
Maximum TCK frequency	80 MHz
Maximum scanning data length	Unlimited
TCK frequency steps	1.00 MHz increments between 25 and 80 MHz, 0.50 MHz increments between 12.5 and 25 MHz, 0.25 MHz increments (or less) below 12.5 MHz
Programmable Interface Voltage	1.25 to 3.3 V in 0.05 V increments
Programmable TAPs	4, each TAP can have its own programmable voltage settings
Signals DC characteristics	See Table 2
Physical	
Case Outline Dimensions	5.2 in. x 7.1 in. x 1.5 in.
Power Short Test Pins	
Power (Vcc) Sense Pins	Two per TAP (Vcc1, Vcc2), 8 total
Vcc Measurement Type	Short to GND detect; Voltage sensing, Target unpowered
Voltage Sense Resolution	8-bit ADC
Voltage Sense Accuracy	+/- 50 mV
I/O Connectors	
Serial Port	Standard female DB9 socket
USB Connector	Standard USB type B socket
Ethernet Connector	Standard RJ-45 socket
Expansion Connector	68-pin SCSI II type (AMP P/N 787171-7 or equivalent)
Power Requirements	
From external supply (included)	5 Vdc @ 4 A maximum
Operating Environment	
Temperature	0ºC to 55ºC
Relative Humidity	10% to 90%, non-condensing
Storage Environment	
Temperature	-40ºC to 85ºC
Relative Humidity	0% to 100%, non-condensing

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