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Find the *Corelis PCI-1149.1* at our website: *Click HERE*

CORELIS

"We combine exceptional ease of use with advanced technical innovation"

PCI-1149.1/Turbo™

High-Performance Boundary-Scan Test and In-System Programming Controller

- Supports four JTAG, SPI or I2C ports
- Concurrent (gang) testing and in-system programming of CPLDs and Flash devices on 1-4 boards, expandable to 1024
- Supports direct programming of I2C and SPI-based devices
- On-the-fly hardware comparators individually verify scan data against expected results in parallel on all TAPs
- User programmable JTAG TCK speeds up to 80 MHz with effective throughput of 320MHz
- 32-bit PCI bus interface supports high data transfer rates
- Pre-power up test for shorts between power and ground lines on the UUT for each TAP
- TAP signals and GPIO discrete signals are individually programmable from 1.3V to 3.3V (5 volt tolerant)
- Direct Write signal for expediting Flash programming
- Support for monitoring Flash RDY/BSY
- Up to 30 feet of extended distance from the PC to the Pod - no TAP extenders are needed
- Automatic signal delay compensation for long cable lengths to the UUT
- 16 inputs and 16 outputs of programmable parallel I/O
- Analog voltage measurement of +/- 50V
- Plug and Play drivers for Windows 2000/XP
- Fully compatible with ScanPlus™, ScanExpress™, CodeRunner™ and CodeSymphony™ products



Figure 1. PCI-1149.1/Turbo Boundary-Scan Controller

Overview

In the last few years, the use of boundary-scan has expanded beyond traditional board test applications into in-system programming of CPLDs, FPGAs, and Flash memories. These new applications require much higher performance.

Until now, available products were limited in Test Clock (TCK) frequency and the comparison of the expected patterns with the observed results were done by the host computer. Now that boards include more and denser memories including flash, users are asking for higher throughput boundary-scan tools that will allow faster testing and in-system programming. This includes concurrent (often referred to as gang) testing and in-system programming of more than one board at a time.

In response to this need, major development efforts in Boundary-Scan technology were undertaken at Corelis. The success of this development has produced a quantum leap in scan vector throughput, maintaining Corelis as the clear leader in providing sophisticated yet easy to use Boundary-Scan test equipment.

A key element of this ground breaking technology is the PCI-1149.1/Turbo™ controller which dramatically increases the test and in-system programming speed by applying a vast number of innovative and proprietary techniques developed at Corelis.

The result of these new techniques allows for an unsurpassed boundary-scan throughput at TCK frequencies reaching a sustained 80MHz rate and a scan efficiency of 100% at each of up to four concurrently scanning JTAG ports.

Corelis thus presents the PCI-1149.1/Turbo™ High-Performance Boundary-Scan Test and In-System Programming System, as the premier solution for users whose applications demand the highest possible scan vector throughput that is currently available on the market.

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General Description

The PCI-1149.1/Turbo™ is an advanced robust system that can be used in the testing and/or in-system programming (ISP) of devices, boards, or systems compliant with the IEEE-1149.1 standard. It is comprised of two major elements:

- PCI-1149.1/Turbo™ Controller Card (Controller)
- ScanTAP-4 Remote Pod (Pod)

The Controller connects to the Pod with a high performance SCSI ribbon cable available in lengths up to 30 feet for easy installation at remote locations.

The PCI-1149.1/Turbo™ controller card contains several performance enhancing functional sections aimed at increasing test vector and in-system programming throughput. The combination of these functional elements results in a very high data-scanning rate, which is completely decoupled from the PCI bus. The scanned patterns are distributed to the target device or devices via the ScanTAP intelligent pod. In addition, 16 parallel inputs and 16 parallel outputs (including two open collector drivers) are provided to test or control non-Boundary-Scan chains of the target device.

Standard configuration of the PCI-1149.1/Turbo includes the ScanTAP-4 intelligent pod that contains 4 TAPs. The ScanTAP-4 applies test vectors and/or ISP patterns to boards with a variety of JTAG chain topologies. In the simplest, yet often used case, the ScanTAP-4 will provide the interface between the PCI-1149.1/Turbo™ controller and a target system consisting of a single JTAG Test Access Port (TAP). This would be the case where the target system consists of one JTAG chain and its associated TAP.

If the board under test consists of groups that include multiple devices, each with their own respective TAP, then the ScanTAP-4 allows for test vectors to be applied to each of the target TAPs individually, one TAP at a time, or jointly to all of the TAPs. Figure 2 depicts such configuration.

Figure 3 depicts a case where ScanTAP-4 is connected to four identical boards. In this case the system can test and program the four boards concurrently.

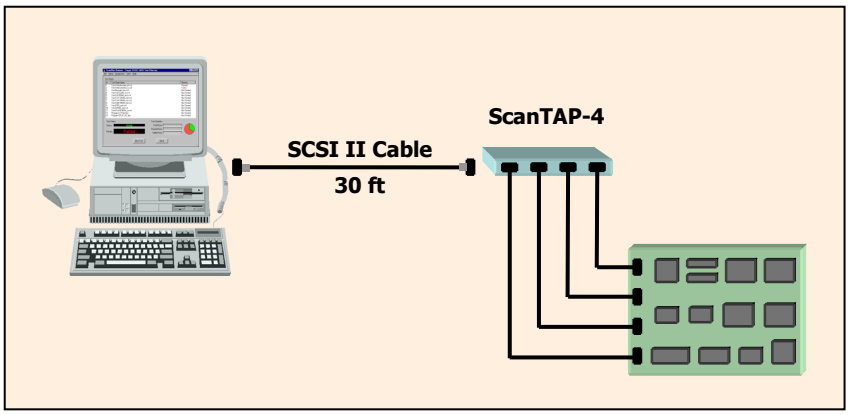


Figure 2. Connection to a Single UUT with Four TAPs

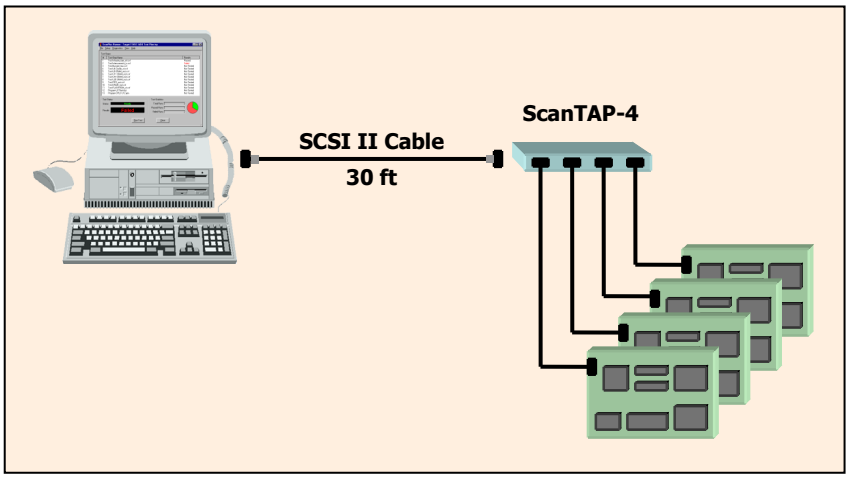


Figure 3. Connection to Four UUTs with a Single TAP Each

Note that the concept of concurrency here not only applies to the simultaneous application of test vectors and ISP patterns to each board but also applies to the simultaneous verification of each individual board. A failure on any of the individual boards will be properly logged and will not prohibit the continuation of testing on the remaining target devices. The concurrent (often referred to as gang) mode of operation offers great performance increases when testing, in-system programming, and verifying multiple targets.

The ScanExpress architecture provides for concurrent testing and programming with practically unlimited scalability. ScanTAP pods are available that support 4, 8 or 32 TAPs. Multiple ScanTAP pods may be combined to support up to 1024 target boards.

Adjustable Low Voltage Outputs

The voltage level of the parallel I/O, the local TAP port, and each Pod TAP is software programmable and can be set to any voltage between 1.3V and 3.3V in increments of 0.05V. The ports of the ScanTAP-4 Pod can also be slew rate (fast/slow) adjusted.

Scan Input Signal Delay Compensation

Automatic delay compensation is inserted within the signal paths. This feature is used to combat the well-known problems associated with the combination of high TCK rates and remote target locations at extended distances.

Programmable Clock

The system-wide TCK rate for all TAP ports is programmable under software control. A wide range of TCK frequencies can be achieved by using the on-board Phase-Locked-Loop (PLL) generation circuitry. The user is given the ability to select the desired TCK rate from a range of values from 390 KHz to 80MHz at resolution increments of less than 2%. Should an external TCK timing reference be required for synchronization, or a user-unique frequency, an external SMB connector is provided.

Target Voltage Detection System

The Controller and its remote Pod include analog-to-digital converters, which can measure connected power voltages from the target. Such voltages from two distinct target levels can be measured and compared against user-defined limits. This feature can provide detailed signal voltage checks at any stage of a test plan.

Automatic Detection of Target Power Shorts

With the target powered down, a well-regulated drive current with current limit can be momentarily applied to the target power bus. By measuring this current, the approximate load resistance can be calculated. This provides for the automatic detection of target power shorts, prior to applying power to the target unit.

Target Presence Detection Capabilities

The TAPs on the remote Pod have a dedicated pin on the JTAG interface connector that can be used to detect the presence of the target board. The state of this signal can be monitored by software to detect both the presence of the target device as well as the proper insertion of the test cable.

Parallel Input/Output Port

The Controller contains 16 parallel input signals and 16 parallel output signals. These input and output signals are organized into two 8 bit parallel ports. The 16 parallel outputs are implemented as tri-state logic that can be set to logical high, low, or high-impedance.

The input and output ports can be used to control and sense various functions in the target system which cannot be controlled or observed through boundary-scan operations. These ports are useful for the testing of target systems that incorporate components that are not compliant to IEEE Standard 1149.1.

In addition, each port of the Pod controls 3 discrete I/O signals whose direction and drive (totem-pole or open-collector) is configurable. Open-collector signals are often needed to drive reset and emulation signals.

Direct Programming of I2C and SPI-based Devices

The PCI-1149.1/Turbo includes the capability of directly programming I2C and SPI-based devices. The SPI and I2C interfaces on the PCI-1149.1/Turbo are independent of the JTAG test interface; this means that the user can use the PCI-1149.1/Turbo controller to perform JTAG-based testing and programming and also to perform direct programming of serial EEPROM and flash memories without removing the JTAG connector or switching to a dedicated SPI and I2C programmer.

Using the direct programming port, serial FLASH/EEPROM devices can be programmed at speeds up to the device theoretical programming

Pin	Signal Name			I/O	Description
1	TRST*			Input to UUT	Test Reset (optional)
3	TDI			Input to UUT	Test Data Input
5	TDO			Output of UUT	Test Data Output
7	TMS			Input to UUT	Test Mode Select
9	TCK			Input to UUT	Test Clock
11	GPIO1	Write_Strobe*	SPI_CS2*	Input to UUT	General Purpose Output, Flash Programming Write Signal or SPI Chip Select (optional)
13	GPIO2		SPI_SCK	Input to UUT	General Purpose Output or SPI Serial Clock (optional)
15	GPIO3	Ready_Busy*	SPI_SDO (MISO)	Output of UUT	General Purpose Output, Flash Programming Ready Signal or SPI Serial Data Out (optional)
16			SPI_SDI (MOSI)	Input to UUT	SPI Serial Data Input (optional)
17	VCC1			UUT Power Rail	UUT Power Test Point 1 (optional)
18	I2C_SCL			Input to UUT	I2C Serial Clock (optional)
19	VCC2			UUT Power Rail	UUT Power Test Point 2 (optional)
20	I2C_SDA		SPI_CS1*	Input to UUT	I2C Serial Data or SPI Chip Select (optional)

Table 1. ScanTAP-4 20-pin Connector

Note: Direction specified is relative to the UUT. All other even pins of the connector (2, 4, 6, 8, 10, 12 and 14) should be connected to ground (GND) .

time. This is significantly faster than programming the devices indirectly using JTAG, typically 10 times faster and often surpassing this, depending on target configuration.

Built-in Self-Test

The PCI-1149.1/Turbo™ has a built-in self-test capability. Logic has been provided at the local TAP connector to loop back data shifted out on TMS and TDO. Cooperative testing between the Controller and the Pod has also been implemented to insure proper interface signal integrity.

PCI Bus Interface

The Controller is a single function universal 32-bit 33MHz PCI device compliant with Revision 2.2 of the PCI Bus Specification. It is operational in either 5V or 3.3V interface signaling platforms. It is mapped to the memory space of the host system determined during system initialization.

Compatible with ScanPlus and ScanExpress Family of Products

The PCI-1149.1/Turbo™ is both hardware and software compatible with the complete ScanPlus and ScanExpress™ family of IEEE-1149.1 test and in-system programming products.

ScanTAP-4 Connector

The ScanTAP-4 contains four 20-pin TAP connectors. All four connectors have the same signals and the same pinout. Each connector is a shrouded header (0.100 × 0.100 in. spacing) with long ejectors that are compatible with standard 20-pin IDC flat cable connectors (with strain relief). Note that only the first 10 pins are required for basic boundary-scan operation. For Flash Programming with external write or the Ready Busy signal, use the first 16 pins of the TAP. To build in support for direct SPI/I2C programming or power-to-ground short checking, use all 20 pins of the TAP.

Pins 17 and 19 of each ScanTAP-4 connector can be used to sense that the target power pin is not shorted to GND. Up to 2 different power pins can be checked on each of the four 20-pin connectors of the ScanTAP-4 unit.

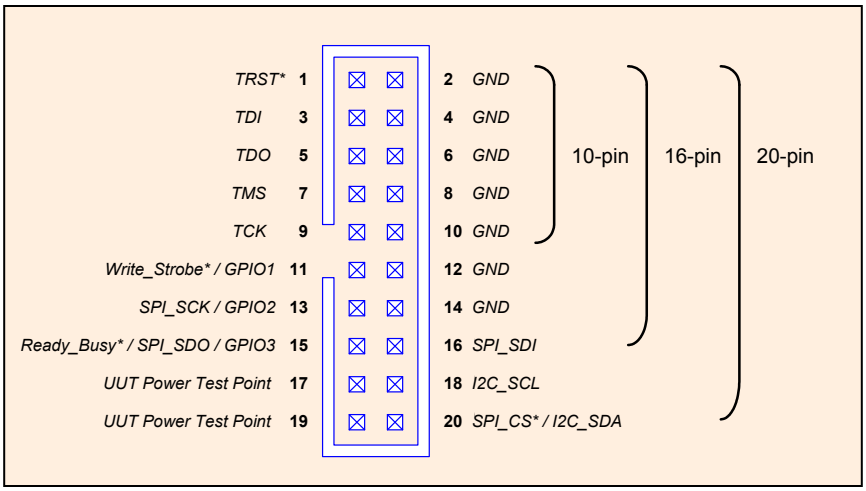


Figure 4. ScanTAP-4 Target Connector Pin Assignments for Various TAP Cables (*see Corelis application note 06-118 for additional details*)

PCI-1149.1/Turbo Hardware Specifications:

PCI Interface	
Bus Width	32-bit
Configuration	Plug and Play
Memory Space	132 Mbytes
Signaling	5v or 3.3v (universal)
ScanTAP Interface	
Maximum TCK frequency	80 MHz
Maximum scanning data length	Unlimited
TCK frequency steps	1.00 MHz increments between 25 and 80 MHz, 0.50 MHz increments between 12.5 and 25 MHz, 0.25 MHz increments (or less) below 12.5 MHz
I/O Connectors	
Boundary-Scan Connector (P4)	68-pin SCSI II type (AMP p/n 787171-7 or equivalent)
Parallel Input Port Connector (P1)	34-pin header (3M p/n 2534-6002UB or equivalent)
Parallel Output Port Connector (P2)	34-pin header (3M p/n 2534-6002UB or equivalent)
Power Requirements	
From host computer	5 Vdc @ 1.5A maximum
Physical	
Board Outline Dimensions	3.875 in. × 6.75 in.
Operating Environment	
Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing
Storage Environment	
Temperature	-40°C to 85°C
Relative Humidity	10% to 90%, non-condensing

Table 2. PCI-1149.1/Turbo Hardware Specifications

ScanTAP-4 Hardware Specifications:

PCI-1149.1/Turbo Interface	
Host Connector	68-pin SCSI (AMP part no. 787171-7 or equivalent)
Host Cable Length	6 foot (standard) - Corelis P/N 15314 15 foot (optional) - Corelis P/N 15328 30 foot (optional) - Corelis P/N 15329
Target Interface	
Connectors	Four 20-pin shrouded headers (0.1 in. × 0.1 in. spacing)
Number of TAPs	4
Programmable Output Voltage	1.25 to 3.3V, in 0.5V steps
Programmable Threshold Voltage	1.25 to 3.3V, in 0.5V steps
Signal DC Characteristics	See Table 4
JTAG Interface	
Compliance	IEEE-1149.1 compliant interface
Maximum TCK Clock Frequency	80 MHz
Maximum scanning data length	unlimited
I2C Interface	
Maximum SCL Clock Frequency	100 kHz
SPI Interface	
Supported Chip Selects	Up to 2 per TAP
Maximum SCK Clock Frequency	1 MHz
Power Requirements	
5.0V	Supplied by the PCI-1149.1/Turbo controller
Physical	
Mechanical Dimensions (enclosure)	4.0 ± 0.25 x 4.6 ± 0.25 x 0.75 ± 0.25 (inches)
Operating Environment	
Temperature	0°C to 55°C
Relative Humidity	10% to 90%, non-condensing
Storage Environment	
Temperature	-40°C to 85°C
Relative Humidity	10% to 90%, non-condensing

Table 3. ScanTAP-4 Hardware Specifications

Adjustable Voltage	V_{IL}		V_{IH}		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} (mA)	I_{OH} (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
3.3	-0.3	0.8	2.0	3.6	0.4	2.9	8	-8
2.5	-0.3	0.7	1.7	3.6	0.4	2.1	8	-8
1.8	-0.3	0.6	1.2	3.6	0.4	1.4	8	-8
1.5	-0.3	0.5	1.0	3.6	0.4	1.1	8	-8
1.25	-0.3	0.4	0.8	3.6	0.4	0.8	6	-6

Table 4. ScanTAP-4 Signal DC Characteristics

For direct programming of I2C-based devices, pins 18 and 20 provide the I2C SCL and SDA lines respectively.

For direct programming of SPI-based devices, pins 11, 13, 15, 16 and 20 provide the CS2*, SCK, SDO, SDI and CS1* lines respectively.

For the target design, it is recommended that an industry-standard 10-pin, 16-pin or 20-pin TAP connector format be used, depending on the specific testing and in-system programming requirements.

Please refer to Corelis application note 06-118 for additional details on these different connector formats. Corelis offers TAP cables to mate with all of these different formats.

System Requirements

- Available PCI Slot
- Microsoft Windows 2000 or XP
- CD-ROM drive
- Pentium 4 processor or higher
- 128 megabytes (MB) of RAM

Ordering information

The PCI-1149.1/Turbo Boundary-Scan Controller Card (P/N 10311A) includes:

- PCI-1149.1/Turbo PCI card
- ScanTAP-4 remote pod
- 6 ft PCI-1149.1/Turbo to ScanTAP cable
- Four 20-pin to 10-pin target cables
- One 20-pin to 16-pin target cable
- One 20-pin to 20-pin target cable
- PCI-1149.1/Turbo user's manual
- PCI-1149.1/Turbo software disk

Optional Configurations

Optional custom configurations are available that support the following:

- ScanTAP-8 pod (8 TAPs)
- ScanTAP-32 pod (32 TAPs)
- 64-1024 TAPs using ScanHUB-16 TAP expanders and multiple ScanTAP-4, ScanTAP-8 or ScanTAP-32 intelligent pods

Please contact Corelis for further configuration and pricing information.

Optional accessories

- 15 ft PCI-1149.1/Turbo Controller Card to ScanTAP cable (P/N 15328)
- 30 ft PCI-1149.1/Turbo Controller Card to ScanTAP cable (P/N 15329)
- Package of 12" 10-pin TAP cables (qty 4) for ScanTAP (P/N 15310-2)
- Package of 12" 16-pin TAP cables (qty 4) for ScanTAP (P/N 15311-2)
- Package of 12" 20-pin TAP cables (qty 4) for ScanTAP (P/N 15312-2)
- Package of 36" 10-pin TAP cables (qty 4) for ScanTAP (P/N 15310-3)
- Package of 36" 16-pin TAP cables (qty 4) for ScanTAP (P/N 15311-3)
- Package of 36" 20-pin TAP cables (qty 4) for ScanTAP (P/N 15312-3)

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