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CORELIS

HP Logic Analyzer Preprocessor for the 64-bit PCI Local Bus

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Preface

This is the documentation for the PI-PCI64 preprocessor based on the Hewlett-Packard Logic Analysis systems. It is intended to explain the operation and capabilities of the preprocessor and the configuration software.

Audience

This document assumes that you are familiar with the Hewlett-Packard Logic Analyzer and the operation of the 64-bit PCI Local Bus.

Organization

This document has the following chapters:

- Chapter 1, **Introduction,** describes the general characteristics and capabilities of the preprocessor and inverse assembler software.
- Chapter 2, **Setting Up the Preprocessor,** describes how the preprocessor is to be connected to the logic analyzer probes. Also contains information about how to load the logic analyzer with the inverse assembler software.
- Chapter 3, **Using the Preprocessor for State Analysis,** provides a description of how to invoke the inverse assembler and interpret the information that it displays.
- Chapter 4, **Using the Preprocessor for Timing Analysis,** provides a description of how to capture timing waveforms using the PI-PCI64.
- Chapter 5, **Using the Preprocessor for JTAG Bus Analysis,** describes how the logic analyzer is to be connected to the preprocessor. Also contains information about loading and using the configuration file.
- Chapter 6, **Using the Preprocessor for Boundary Scan Testing**, describes how a Corelis Boundary-Scan Tester is to be connected to the preprocessor.
- Appendix A, **PI-PCI64 Logic Analyzer Channel Assignments**, lists the PCI Local Bus pins and where they are connected to the preprocessor.
- Appendix B, **PC I/O Mapped Addresses Decoded by PCI64B**, ranges of addresses for specific symbol displayed.
- Appendix C, **PI-PCI64 Specification & Operating Characteristics,** details the specifications and operating characteristics for the PI-PCI64 preprocessor.
- Appendix D, **Troubleshooting**, describes common errors and the solutions to these problems.

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Related Publications

PCI Local Bus Specification
PCI Local Bus System Design Guide
Hewlett Packard, 1660A Logic Analyzer User's Reference
Hewlett Packard, 1670A Logic Analyzer User's Reference
Hewlett Packard, 16500A/B/C Logic Analysis System User's Reference
Hewlett Packard, 16550A 100MHz State/500MHz Timing Logic Analyzer User's Reference
Hewlett Packard, 16554A and 16555A State/Timing Logic Analyzer User's Reference

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Chapter 1: Introduction

The preprocessor and configuration software described in this document provides PCI Local Bus state debug information on a HP 166X/167X/1655X Logic Analyzer's State Listing display.

The PCI-PCI64 preprocessor provides the mechanical and electrical link between your PCI Local Bus system and the HP 166X/167X/1655X Logic Analyzer.

The PI-PCI64 configuration software on the flexible disk sets up the logic analyzer to be compatible with the PCI Local Bus and assigns names to signals found on the bus. One state configuration file sets up the logic analyzer to capture all bus activity on every rising edge of CLK, except *Idle* cycles. Therefore, the logic analyzer's trace buffer contains only relevant bus activity. By changing the logic analyzer's capturing arrangement, you can choose the types of cycles which will be stored in the trace buffer. The other state configuration file sets up the logic analyzer to capture only valid data by using qualifying signals with CLK. The logic analyzer performs the de-multiplexing of the AD bus and C/BE[0...3] signals to provide a single trace entry per PCI bus cycle.

Power Requirements

The PI-PCI64 preprocessor draws a maximum of 0.150 Amperes at +5 volts, 0.020 Amperes at +12, -12, & +3.3 volts from the PCI Local system.

Signal Line Loading

The PI-PCI64 preprocessor adds one CMOS load (22V10) to your PCI Local Bus system's boundary scan signals, TDI, TDO, TMS, TCK, & TRST #. The preprocessor also adds one CMOS load (22V10) to your PCI Local Bus system's interface control signals, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#; the error reporting signals, PERR#, SERR#; and the system clock, CLK. If the additional loads cause problems, simply remove the IC, U4, and store it away as this provides some additional triggering features that are not mandatory for normal operation.

Equipment Supplied

The PI-PCI64 preprocessor consists of the following:

- The PI-PCI64 interface circuit card;
- The configuration software on a 3.5-inch disk; and
- This operating manual.

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Chapter 2 Setting Up the Preprocessor

This chapter explains how to install the preprocessor and configuration software on a logic analysis system. It deals with the physical connection of the logic analyzer pods, preprocessor to the PCI Local Bus system, and the software installation.

Minimum Equipment Required

The minimum equipment for state analysis capabilities for a PCI Local Bus target system comprises:

- An HP Logic Analyzer with at least four 16-channels pods for 32 bit PCI systems or six 16-channel pods for 64 bit PCI systems.
- A PI-PCI64 preprocessor interface card.
- The PCI Local Bus configuration software.

PI-PCI64 LEDs

The PI-PCI64 has four LEDs on its interface board (see **Figure 1**). The LEDs will illuminate when power is applied to the PCI Local Bus.

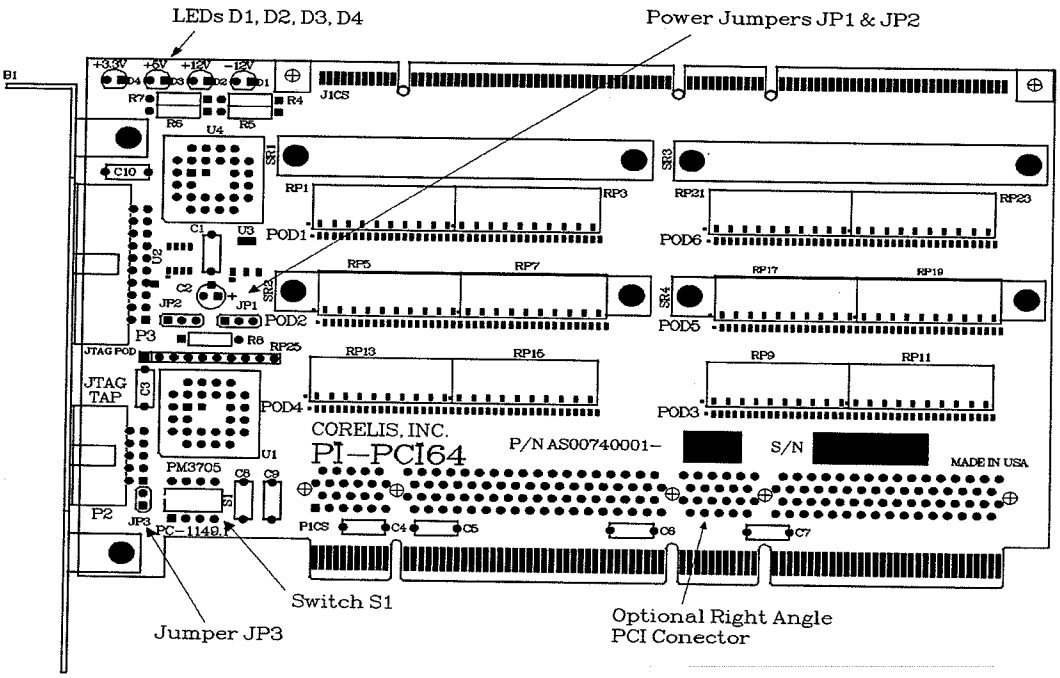


Figure 1
PI-PCI64 Component Locations

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Logic Analyzers Supported

The following logic analyzers are supported by the PI-PCI64:

HP 1660A/AS/C/CS, HP1661A/AS/C/CS
These logic analyzers provide 4K of memory depth with 136 channels (HP 1660A/AS/C/CS) or 102 channels (HP 1661A/AS/C/CS) of 100 MHz state analysis or 250 MHz of timing analysis.

HP 1670A/71A
These logic analyzers provide 64K of memory depth with 136 channels (HP 1670A) or 102 channels (HP 1671A) of 70 MHz state analysis or 125 MHz of timing analysis.

HP 16550A
This logic analyzer provides 4K of memory depth (8K with some configurations), with 102 channels per card of 100 MHz state analysis or 250 MHz of timing analysis. The logic analyzer will also support various combinations of state/timing analysis.

HP 16554A
This logic analyzer provides 512K of memory depth with 68 channels per card of 70 MHz of state analysis or 125 MHz of timing analysis. The logic analyzer will also support various combination of mixed state/timing analysis. At least two HP 16554 cards are required.

HP 16555D
This logic analyzers provide 2M of memory depth with 68 channels per card of 100 MHz state analysis or 200 MHz of timing analysis. At least two HP 16555 cards are required.

HP 16555A/56A
These logic analyzers provide 1M of memory depth with 68 channels per card of 100 MHz (16556A) or 110 MHz (16555A) state analysis or 200 MHz (16556A) or 250 MHz (16555A) of timing analysis. At least two HP16555 or HP16556 cards are required.

Connecting the PI-PCI64 to Your PCI Local Bus System

Integrating software into hardware is very cumbersome when the individual logic analyzer probes are connected to the target system. A preprocessor provides the following capabilities:

- Allows easy access to the PCI Local Bus pins via an adapter.
- Maintains a clean integration environment.

To connect the preprocessor to the target system (computer), follow the steps below:

1. Turn off the logic analyzer and the target system power.
2. Insert your PCI64 card into a 32 or 64 bit PCI slot.
3. Firmly connect the logic analyzer pods into the pods of the PCI64 card according to **Table 1** or **Table 2.**
4. Power on the logic analyzer and then your target system.
5. Verify that the LEDs, D1, D2, D3, D4 have illuminated. Note that D4 will not illuminate if the PCI system does not have a 3.3V power supply.

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Table 1
PI-PCI64 Logic Analyzer Pod Assignment

PI-PCI64 Connector	HP 16550 (one card) Pod*	HP 16554/55/56 (two cards) Pod*	All other logic analyzers
Pod 1	D1 (Master module)	B1 (Master module)	Pod 1
Pod 2	D2 (Master module)	B2 (Master module)	Pod 2
Pod 3	D3 (Master module)	B3 (Master module)	Pod 3
Pod 4	D4 (Master module)	B4 (Master module)	Pod 4
Pod 5	D5 (Master module)	A1 (Expansion module)	Pod 5
Pod 6	D6 (Master module)	A2 (Expansion module)	Pod 6

Table 2
PI-PCI64 Logic Analyzer Pod Assignment for Qualified Clocking

PI-PCI64 Connector	HP 16550 (two cards) Pod*	HP 16554/55/56 (two cards) Pod*	All other logic analyzers
Pod 1	D1 (Master module)	B1 (Master module)	Pod 1
Pod 2	D3 (Master module)	B3 (Master module)	Pod 3
Pod 3	D5 (Master module)	A1 (Expansion module)	Pod 5
Pod 4	C1 (Expansion module)	A3 (Expansion module)	Pod 7
Pod 5	-	-	-
Pod 6	-	-	-

* The letters corresponding to these pods may vary depending on which slots the logic analyzer cards are installed in the HP 16500 mainframe.

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Loading the Logic Analyzer Configuration

Table 3 shows the various configuration files that are available. The logic analyzer can be configured for the preprocessor to capture 64 bit state data by loading the disk file PCI64_ST_A for HP 1660/61 or HP 1670/71 analyzers, PCI64_ST_B for HP 16550 analyzer, and PCI64_ST_C for a dual HP 16554/55/56 analyzer. The logic analyzer can be configured for the preprocessor to capture 64 bit qualified clocking state data by loading disk file PCI64B_ST_A for HP 1660 or HP 1670 analyzers, PCI64B_ST_B for a dual HP 16550 analyzer, and PCI64B_ST_C for a dual HP 16554/55/56 analyzers. The logic analyzer can also be configured for the preprocessor to capture 32 bit state data by loading the disk file PCI32_ST_A for HP 1660/61/62 or HP 1670/71/72 analyzers, PCI32_ST_B for HP 16550 analyzer, and PCI64_ST_C for HP 16554/55/56 analyzer. The load operation:

- Assigns all 16-channel pods to the state analyzer.
- Assigns all labels comprising the Format Specification.
- Assigns the clocking arrangement used by the state analyzer.
- Installs the state symbols into the state analyzer.

Table 3
Configuration Files for the PI-PCI64

Logic Analyzer	Configuration File	Description
All	BA_1149_A	Configuration for JTAG bus monitor
All	JTAG_STA_A	JTAG/IEEE for state monitor.
HP 1660/61, 1670/71	Example1_A	Configuration for trigger condition
HP 1660/61, 1670/71	Example2_A	Configuration for multiple trigger condition
HP 1660/61, 1670/71	PCI32_ST_A	Configuration for 32 bit state analysis.
HP 16550	PCI32_ST_B	Configuration for 32 bit state analysis.
HP 16554/55/56	PCI32_ST_C	Configuration for 32 bit state analysis.
HP 1660/61, 1670/71	PCI64B_A	Configuration for 64 bit qualified clocking state analysis.
HP 16550	PCI64B_B	Configuration for 64 bit qualified clocking state analysis.
HP 16554/55/56	PCI64B_C	Configuration for 64 bit qualified clocking state analysis.
HP 1660/61, 1670/71	PCI64_ST_A	Configuration for 64 bit state analysis
HP 16550	PCI64_ST_B	Configuration for 64 bit state analysis
HP 16554/55/56	PCI64_ST_C	Configuration for 64 bit state analysis
All	PCI64_TM	Configuration for timing analysis

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Figure 2 shows the state configuration for files PCI64_ST_A while **Figure 3** shows the state configuration for PCI64B_ST_A. **Figure 4** shows the state configuration for PCI32_ST_A. **Figure 5** and **Figure 6** show the directory listing for the disk shipped with the PI-PCI64 preprocessor.

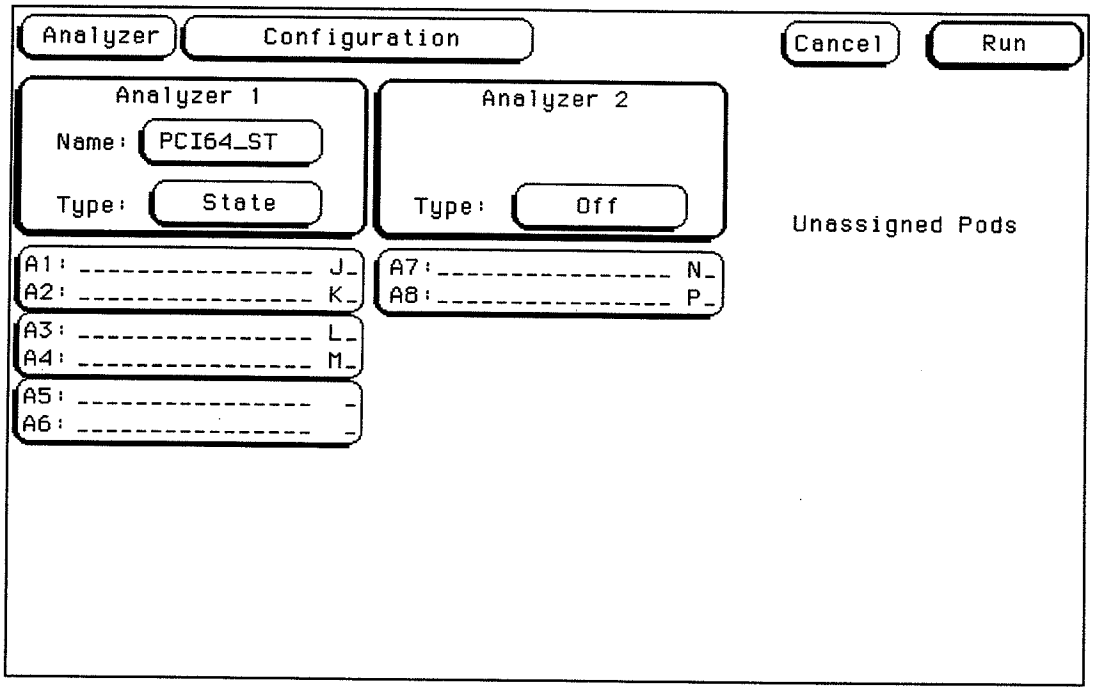


Figure 2
PI-PCI64 Configuration for PCI64_ST_A

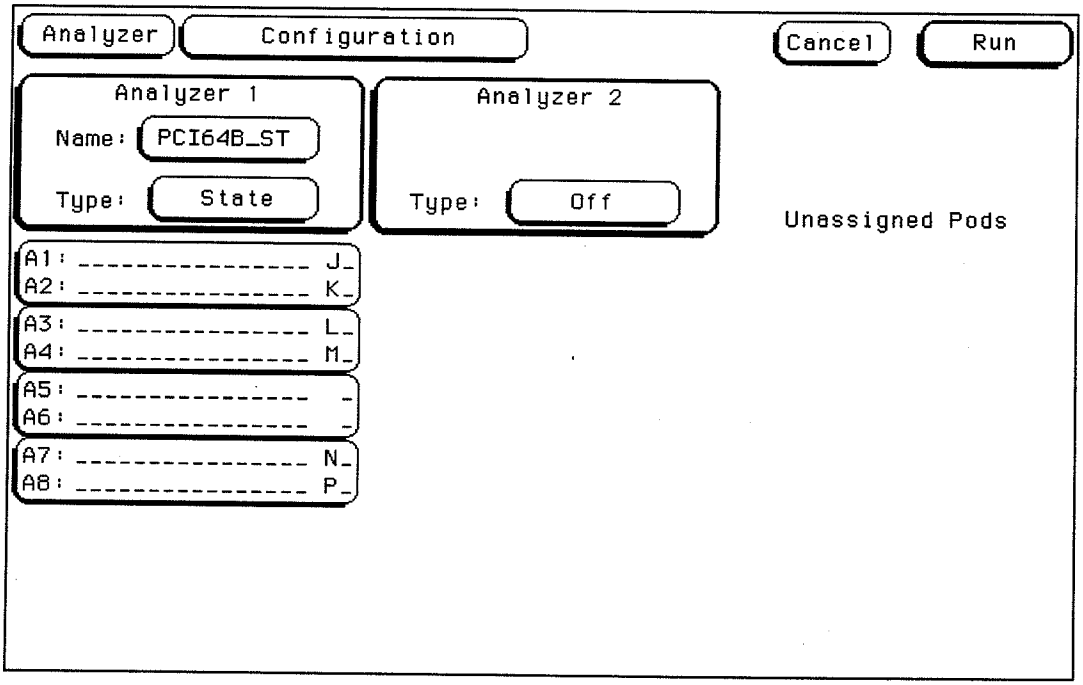


Figure 3
PI-PCI64 Configuration for PCI64B_ST_A

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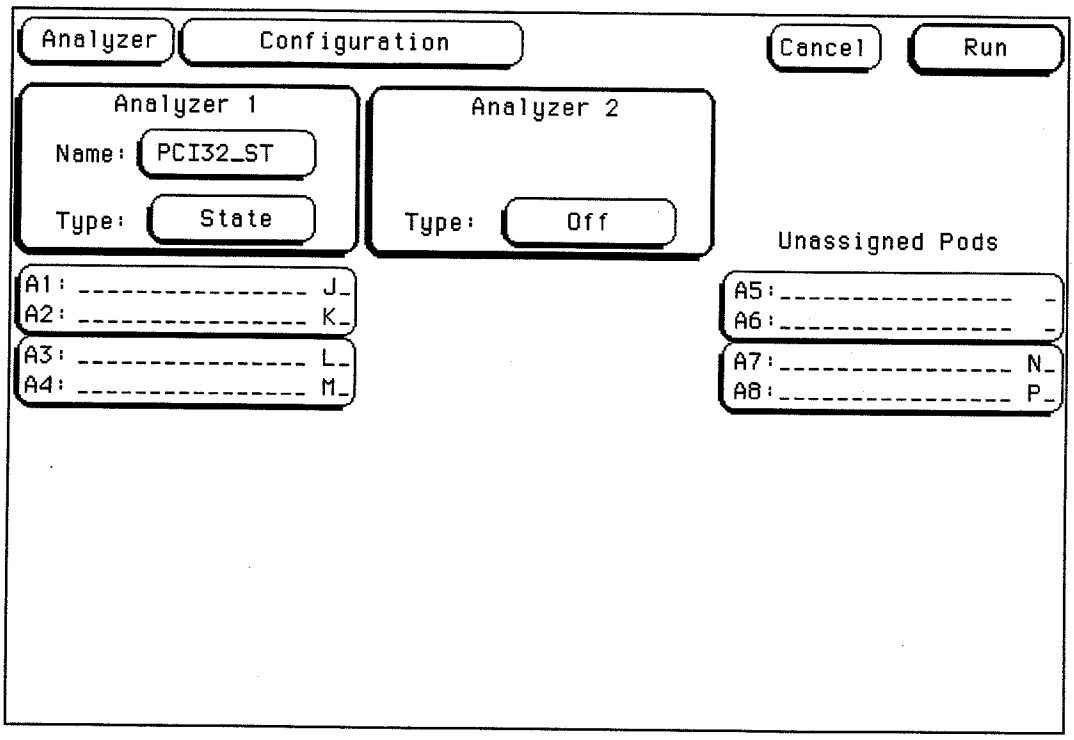


Figure 4
PI-PCI32 Configuration for PCI32_ST_A

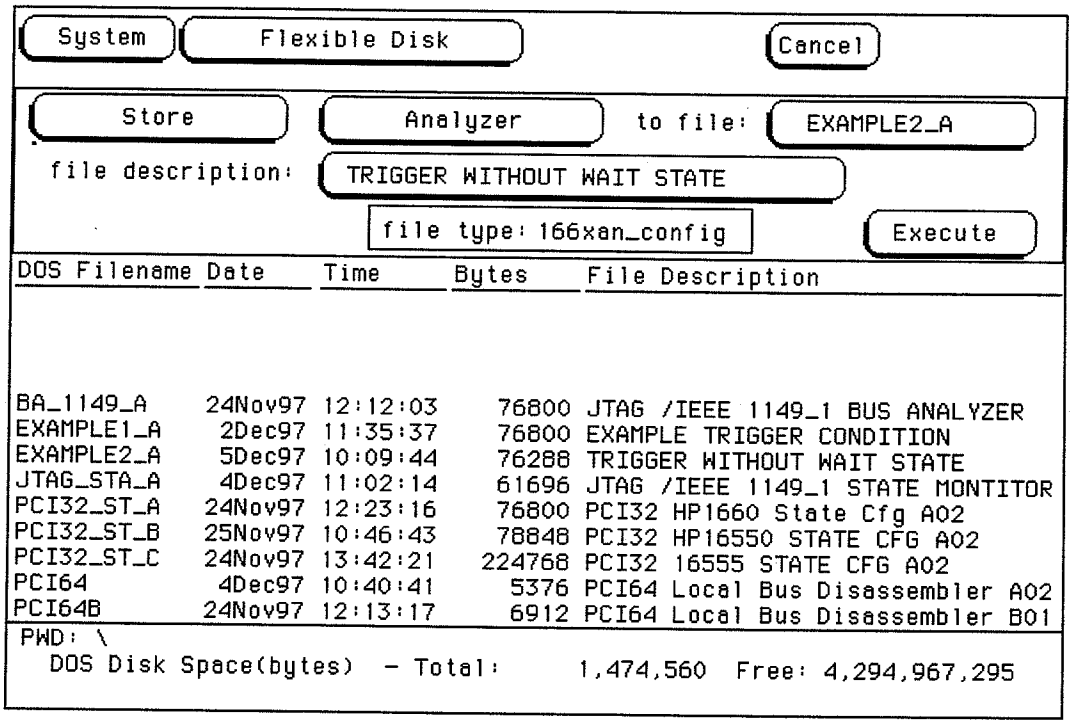


Figure 5
PI-PCI64 Disk Directory

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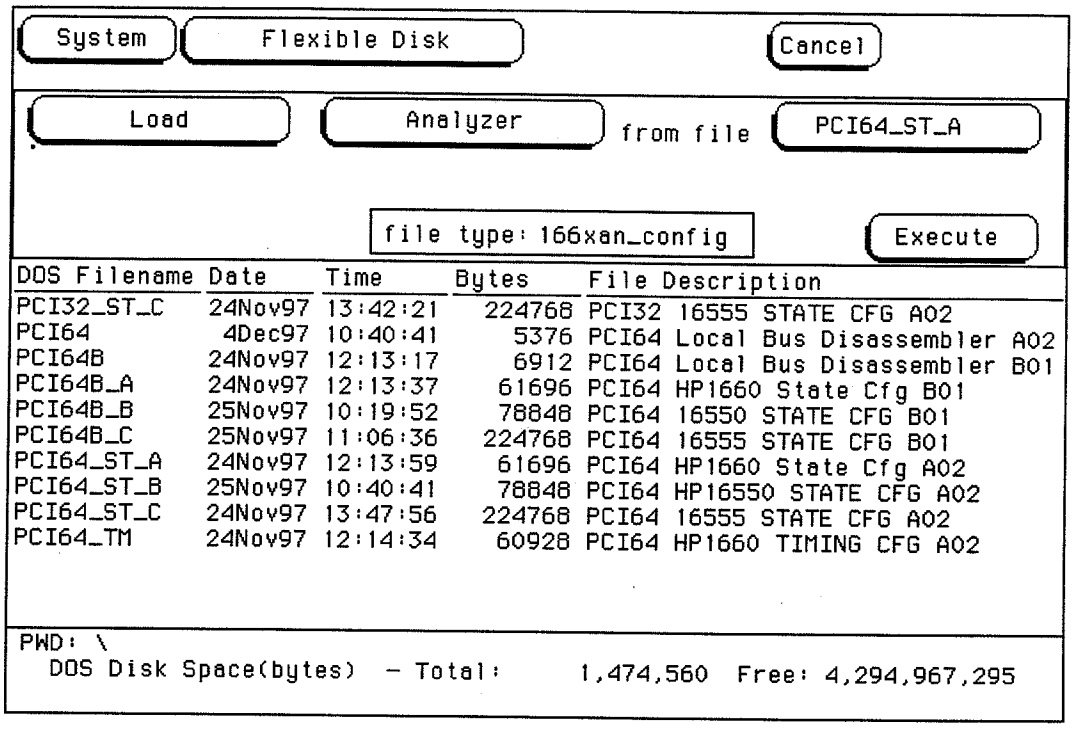


Figure 6
PI-PCI64 Disk Directory

Optional PCI Connector

The PI-PCI64 has been designed to accept a right angle connector, J2. The connector should be soldered on side A, Solder Side. PCI systems designed with riser cards will most likely require the additional connector for mechanical reasons. Refer to **Figure 1** for connector location.

NOTE

Once the connector is installed, the PI-PCI64 will no longer be able to be used in a non-riser PCI system and have another PCI board adjacent to the PI-PCI64. This restriction is due to the spacing requirement of a PCI system. However, if there is no board required to be adjacent to the PI-PCI64, then there is no restriction.

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Chapter 3 Using the Preprocessor for State Analysis

This chapter describes how to capture state data and interpret the information the logic analyzer displays.

Logic Analyzer State Menus

Obtaining the desired state display involves manipulating several key logic analyzer menus. The menu options relevant to operation of the logic analyzer are explained in the following subsections. (Refer to the appropriate HP Logic Analyzer Module manual for additional information concerning menu operation.)

State Format Specification Menu

On loading the file PCI64_ST_X (see Section 2), the labels will be defined according to the signal listing shown in Appendix A. In addition, the following settings should be verified:

- Clock: The rising edge of the J-Clock (CLK).

The format specification screen are displayed in **Figure 7** and **Figure 8**.

On loading the file PCI64B_ST_X, the labels will be defined according to the signal listing shown in Appendix A. In addition, the following settings should be verified:

- Master Clock: The rising edge of J-clock (CLK) and a high on the N-clock (U4).
- Slave Clock: The rising edge of J-clock (CLK) and a high on the L-clock (U4).

The format specification screen is displayed in **Figure 9, Figure 10**, and **Figure 11.**

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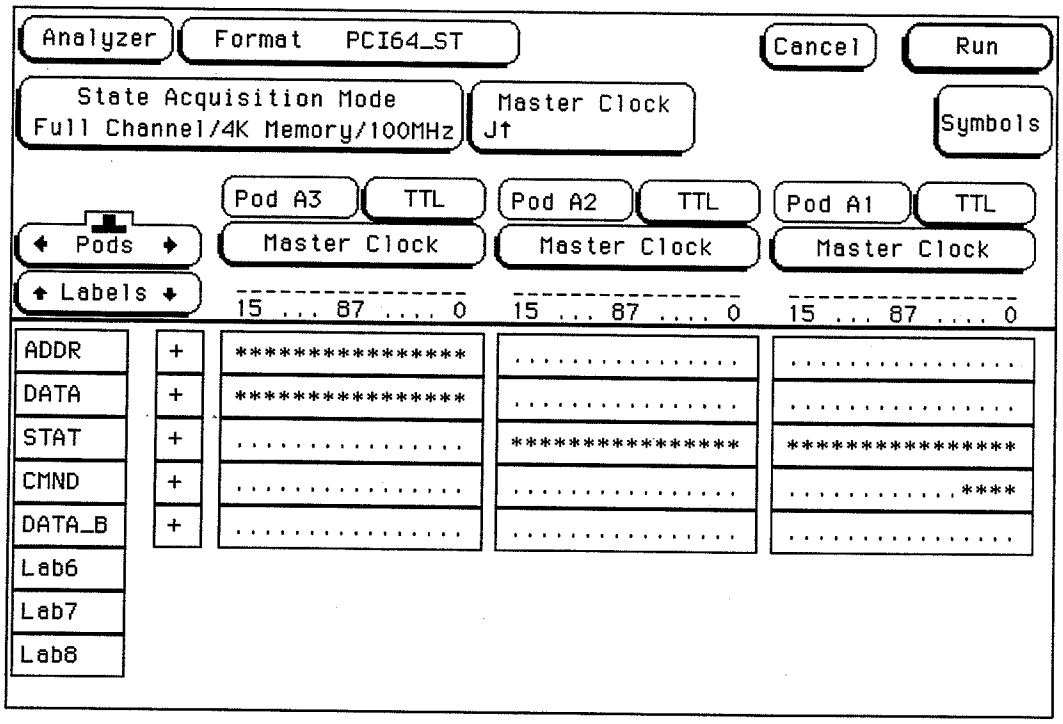


Figure 7
PI-PCI64 State Format Specification: Pods 1-3

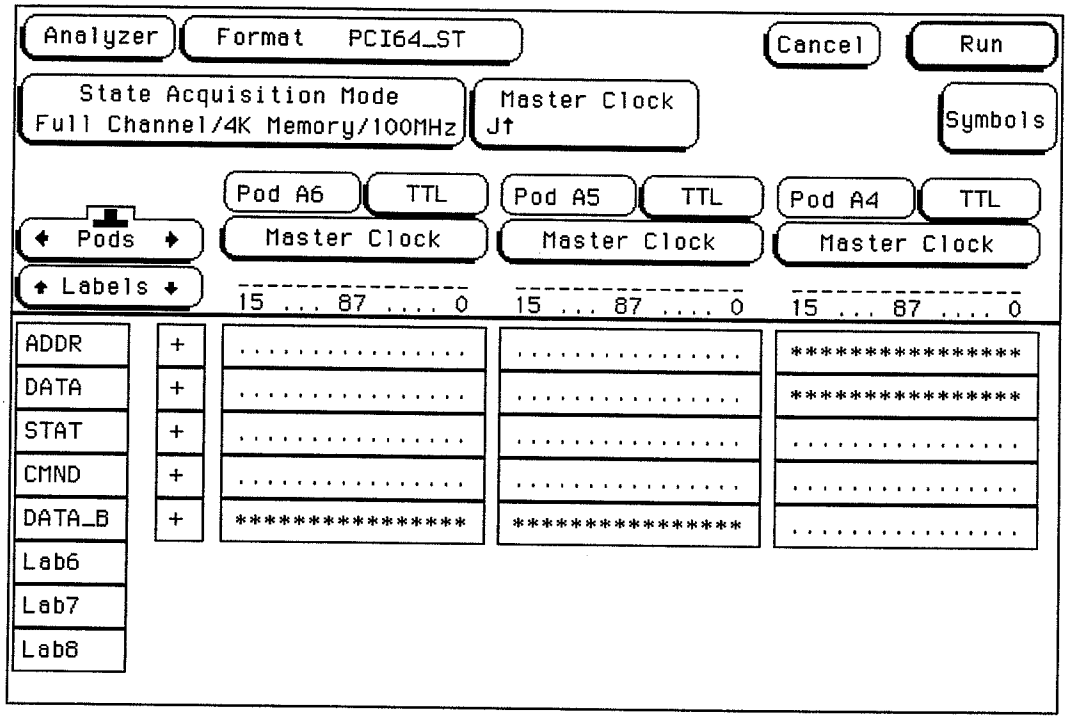


Figure 8
PI-PCI64 State Format Specification: Pods 4-6

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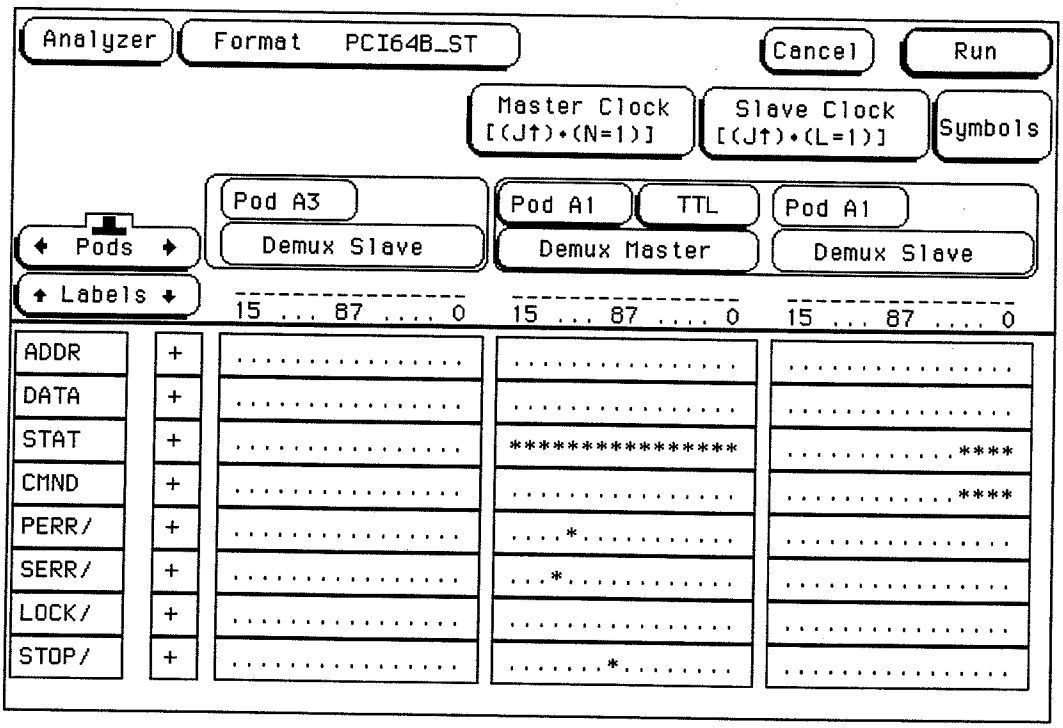


Figure 9
PI-PCI64 State Format Specification: Pods 1-3 for PCI64B_ST

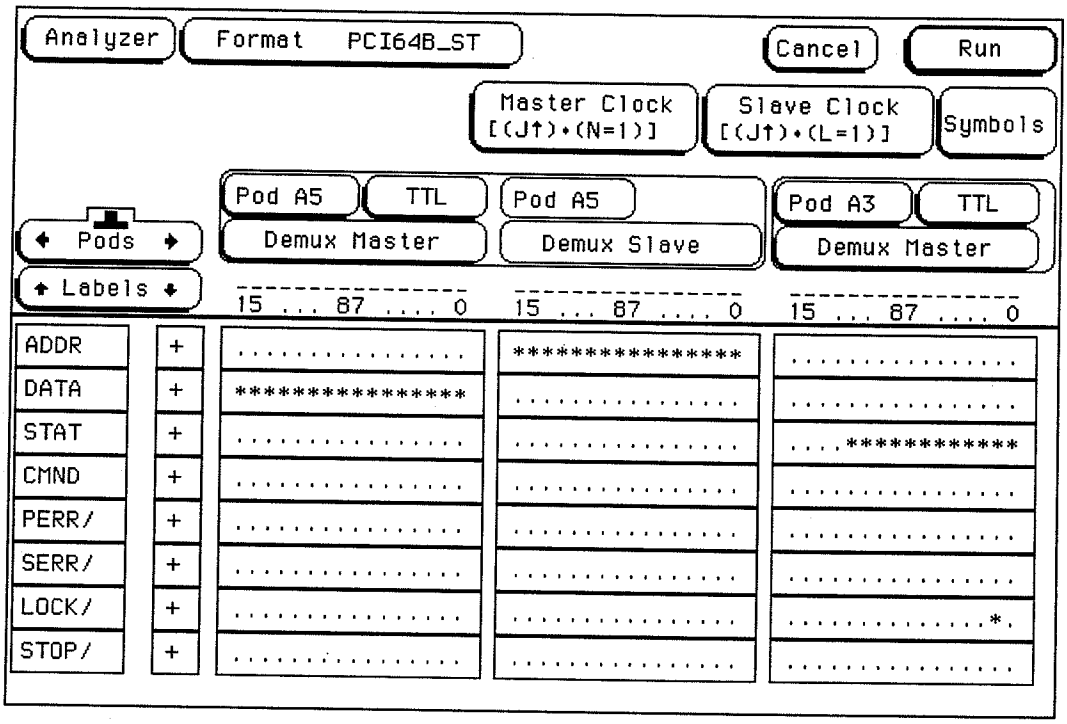


Figure 10
PI-PCI64 State Format Specification: Pods 3-4 for PCI64B_ST

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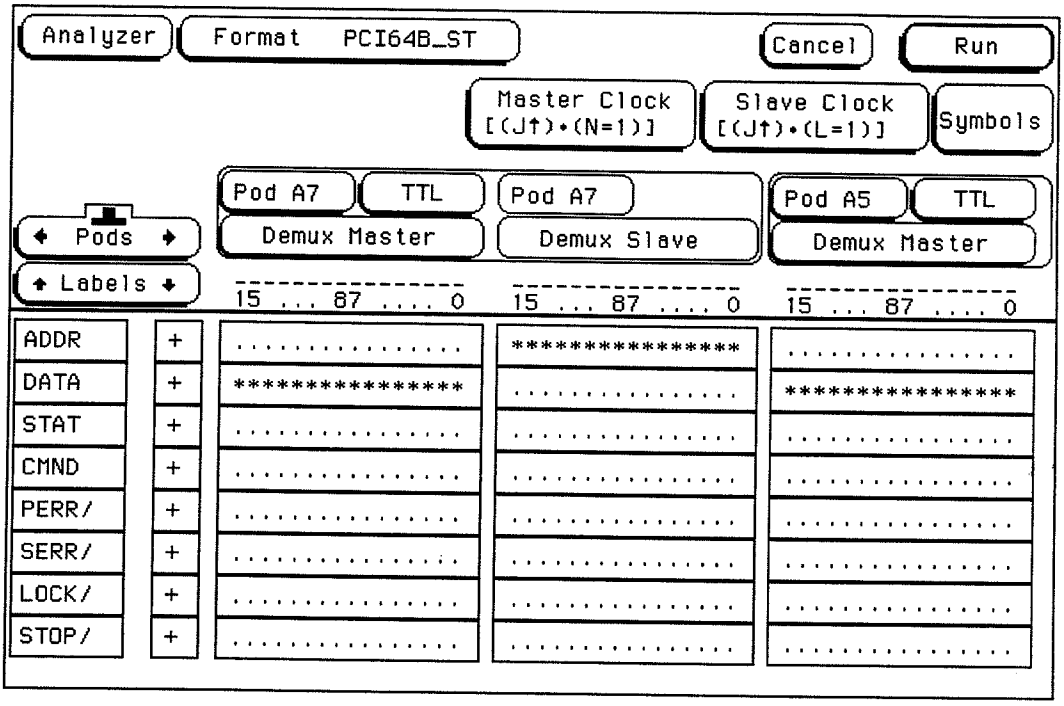


Figure 11
PI-PCI64 State Format Specification: Pods 5-7 for PCI64B_ST

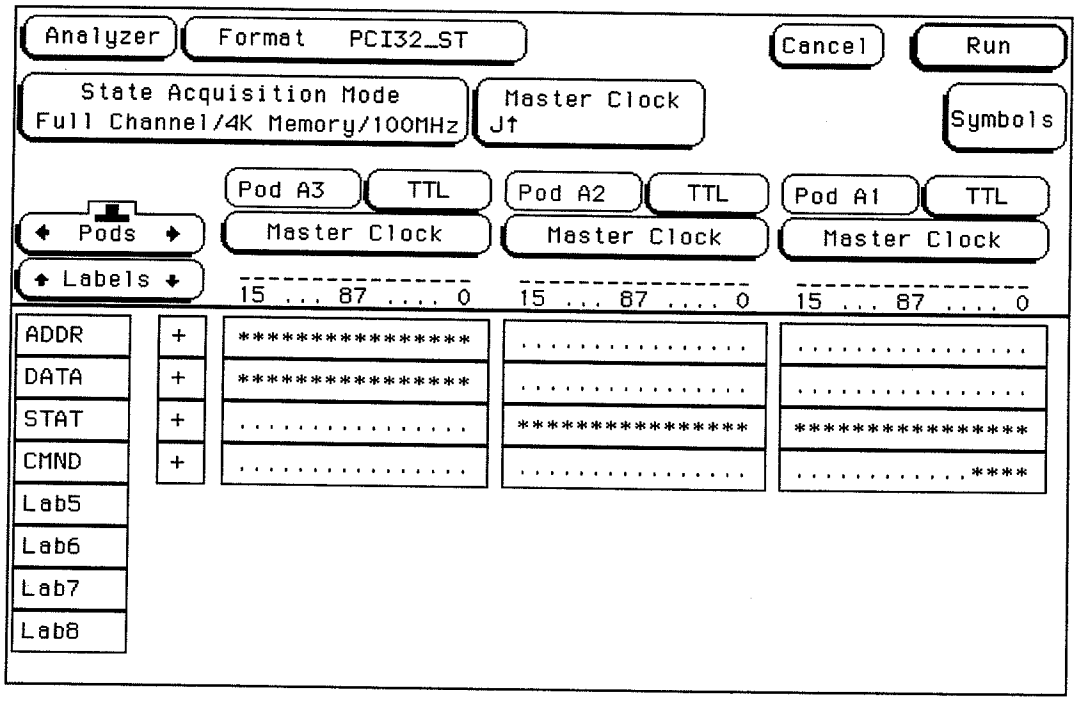


Figure 12
PI_PCI32 State Format Specification: Pods 1-3 for PCI32_ST

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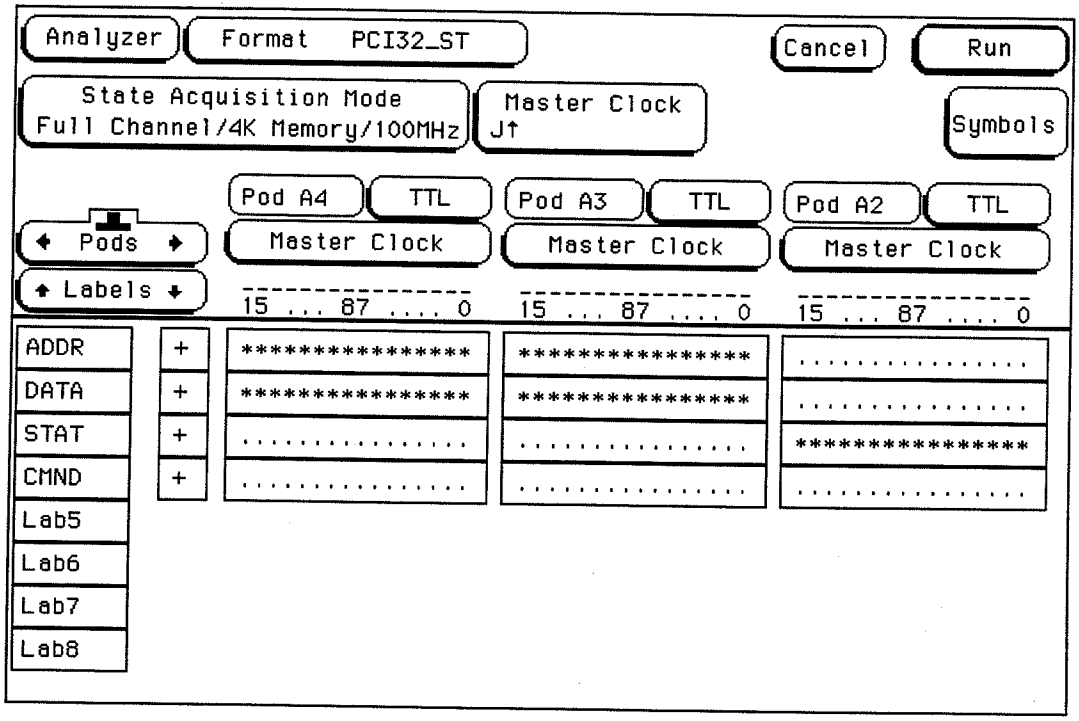


Figure 13
PI-PCI32 State Format Specification: Pods 2-4 for PCI32_ST

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Trigger Menu

The Trigger menu is used to specify a sequence of states required before the logic analyzer triggers. The data stored in the trace memory can also be filtered so as to meet qualification parameters. The Trigger menu for an HP 1660 obtained by loading one of the configuration file , PCI32_ST_A, from **"PI-PCI64 Inverse Assembler Disk"** is shown in **Figure 14**.

To trigger on an address enter the 8 digit hex address in the address field and change the STAT label to ADDR PHASE. **Figure 15** shows the Trigger menu which was used to trigger on address 000001F7. **Figure 16** shows the listing menu which displays activities at the trigger's address. Example1 contains the configuration file used to trigger an address 1F7H.

The Trigger menu can also be used to eliminate waits states from the state listing display. By adding the third level with a loop so that the pattern repeats in this sequence: storing the address phase of a cycle then looking for the data phase and after storing the data phase it looks for the next address phase. Example2 contains the configuration file. This file is not recommended for capturing burst cycles. **Figure 17** shows the Trigger menu which for an HP 1660 obtained by loading PCI64_ST from **"PI-PCI64 Inverse Assembler". Figure 18** shows the listing menu which displays activities of each addresses.

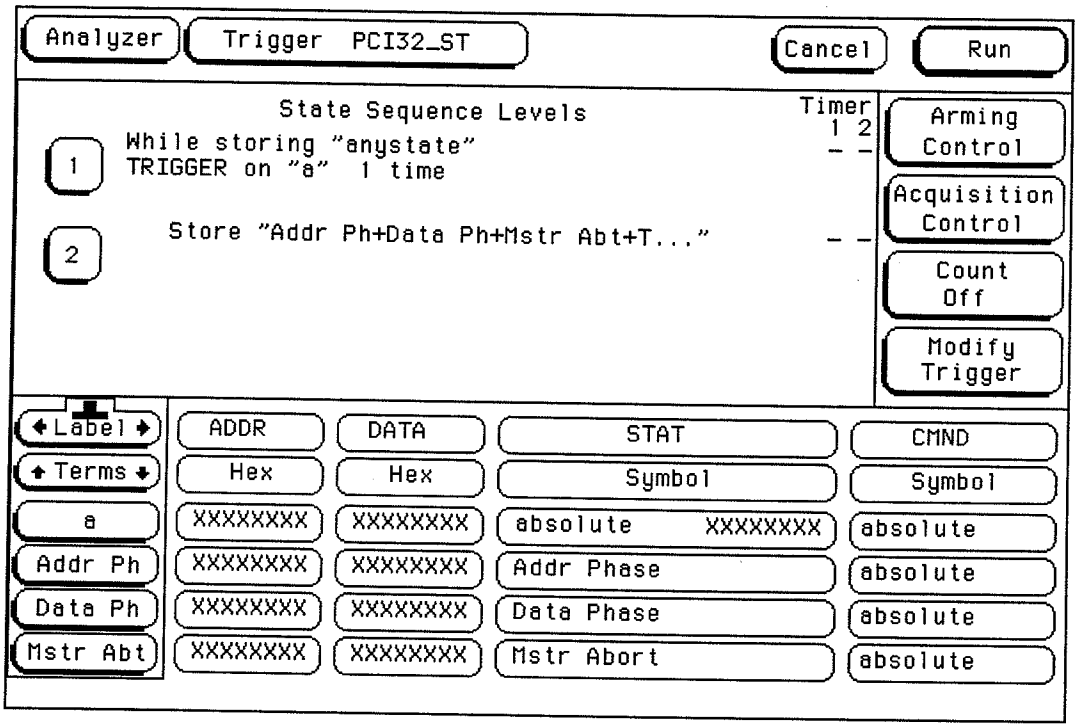


Figure 14
Trigger Menu

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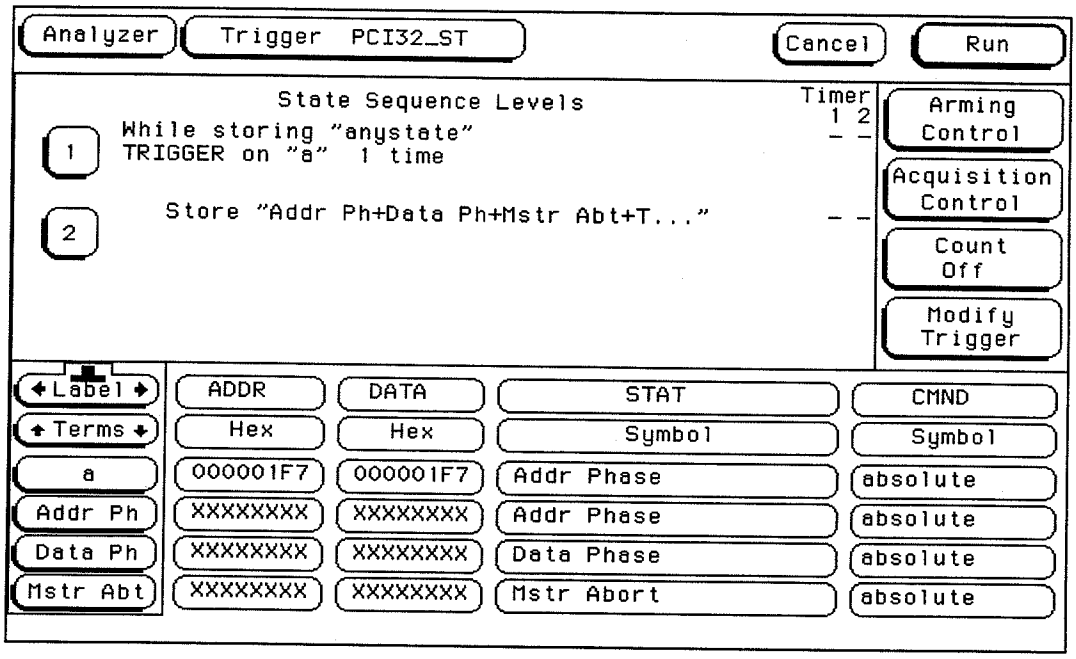


Figure 15
Example Trigger Condition

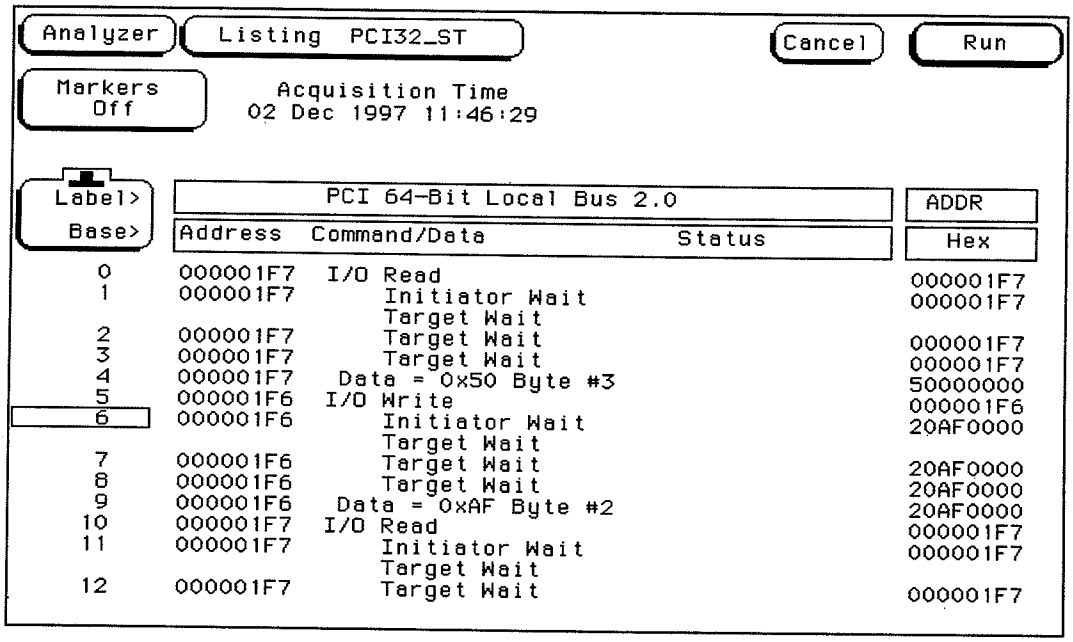


Figure 16
Listing Menu for Trigger Condition

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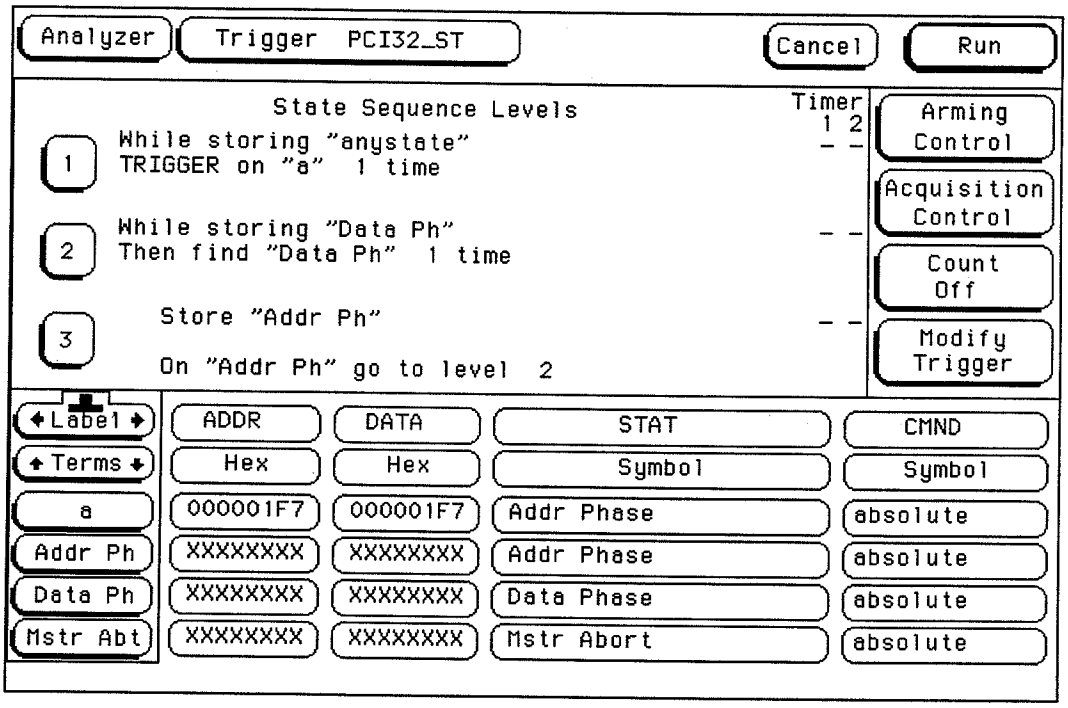


Figure 17
Trigger Conditions for Removal of Wait States

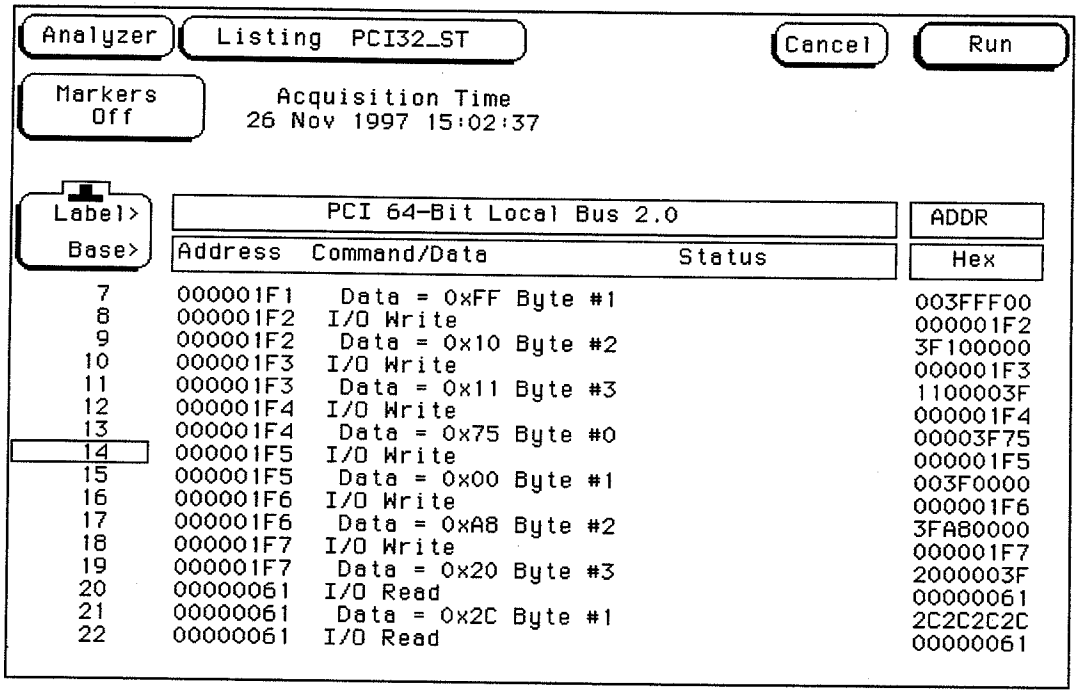


Figure 18
Listing Menu for Removal Wait States

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Interpreting the Display

The PCI Local Bus executes a mixture of bus cycles. The logic analyzer will capture all of the cycles which cause a rising edge of the clock. Some types of cycles which can occur on a PCI Local Bus system are:

- Memory read and write cycles.
- I/O read and write cycles.
- Configuration read and write cycles.
- Special read and write cycles. For example, interrupt acknowledge.

The logic analyzer tracks this activity and synchronously fills the State Listing display with the information explaining each state of the sequence.

PCI Local Bus Transactions

The cycles of the PCI Local Bus are performed as single transactions. The interface circuit establishes what type of cycle is being executed on the PCI Local Bus and captures the PCI Local Bus data. The logic analyzer establishes which type of cycle is currently executing and properly displays the result of the cycle. For example:

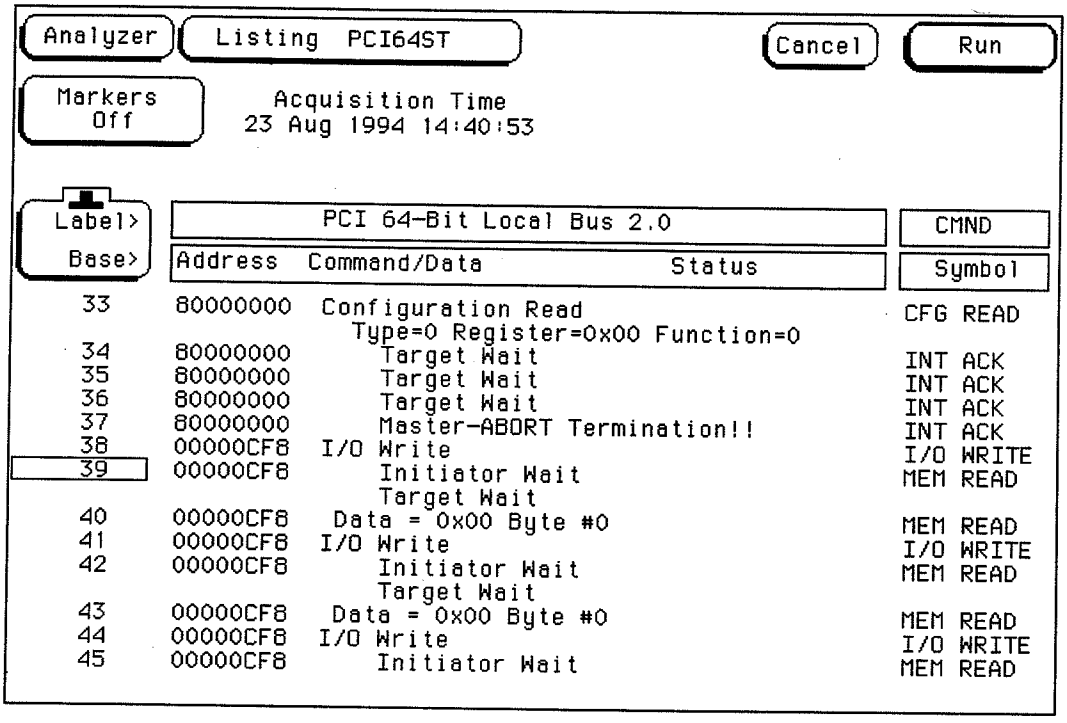


Figure 19
Example Disassembled Trace

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In **Figure 20**, the PCI Local Bus is executing Configuration read and I/O write cycles. The logic analyzer was configured with the configuration file PCI64_ST and to trigger on a Configuration read from address 0x80000 0000. The trace display shows that the no device responded to the read request. This has been detected because DEVSEL# had not been asserted by the seventh clock cycle and therefore the initiator (master) has terminated the cycle. Subsequently, I/O byte writes occur to address 0xCF8.

In **Figure 21**, the configuration file PCI64B_ST has been loaded into the logic analyzer to capture one PCI Local Bus cycle per trace entry. The file configures the logic analyzer to perform the AD bus de-multiplexing. The PCI Local Bus was performing I/O cycles. Notice that at address 0x02FB, the I/O cycle was terminated by the target when it asserted the STOP# signal. Also notice that the PCI64B disassembler decodes all I/O addresses according to standard PC I/O mapped conventions. Reference **Table 13** in Appendix B for a complete listing of the addresses and their symbol.

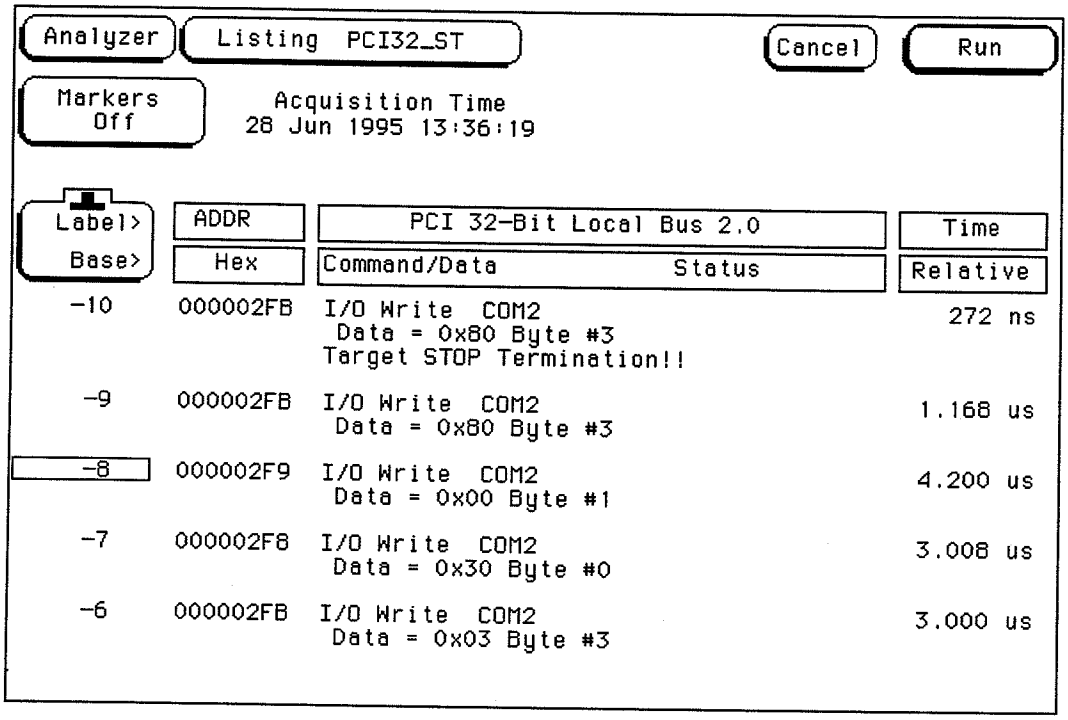


Figure 20
Example Disassembled Trace for PCI64B_ST

The difference between the two configuration files, PCI64_ST and PCI64B_ST, is that PCI64_ST uses the logic analyzer to filter the unwanted Idle and certain wait state cycles with resource terms. The advantages of this configuration is that data is clocked into the logic analyzer on every rising edge of CLK.

This, however, will store more data than may be wanted. The configuration file PCI64B_ST uses qualified clocking and the demultiplexing capabilities of the logic analyzer to store one trace entry per PCI Local Bus cycle. Here, only the specific bus cycles can be captured as displayed in **Figure 20**. Early on in debugging of the PCI Local Bus interface, the PCI64_ST configuration is recommended. When the interface becomes mature, the PCI64B_ST is then recommended.

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