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Time Stamping Data Cycles

In the configuration file, PCI64_ST_A, COUNT:TIME is disabled. However, capturing state trace listings with is useful for timing cycles or routines. Time stamping is enabled from the Trigger menu. **Figure 21** captured program execution when COUNT:TIME has been enabled.

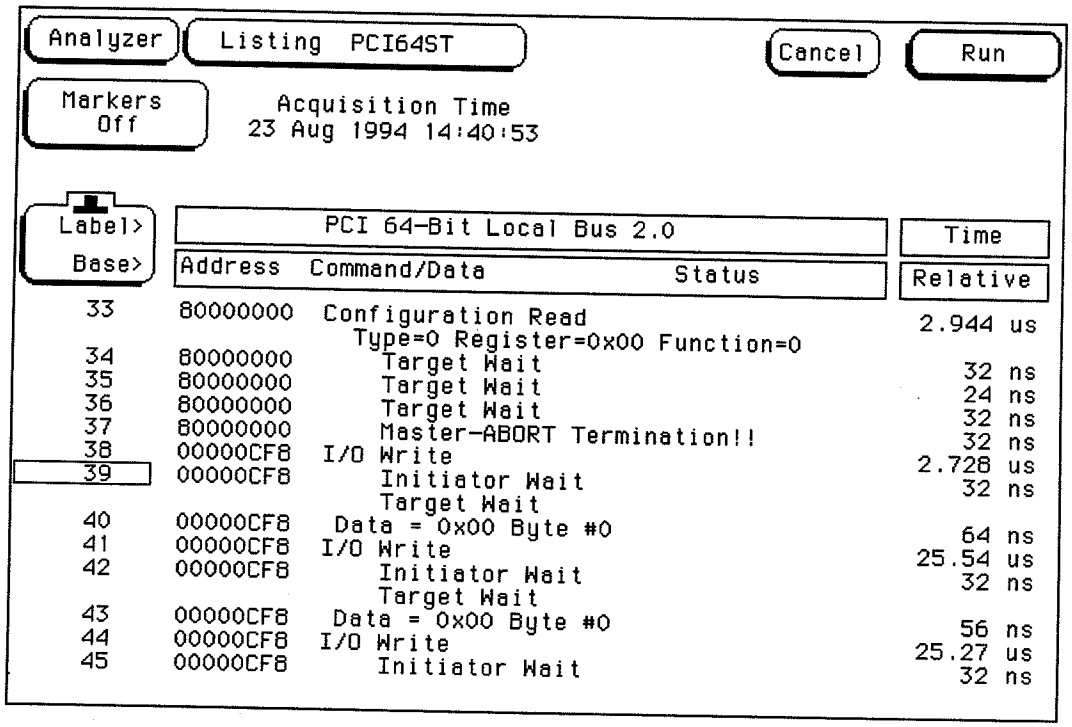


Figure 21
Trace Display with Cycle Timing

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In the configuration file, PCI64_ST_A, are defined symbols for the STATus field. The symbols were defined on the State Format Specification: Specify Symbols menu. **Figure 22** shows the assignments made for the pre-defined symbols. You may add or delete any symbol.

The logic analyzer displays these symbols when the STATUS field has been changed from HEX to SYMBOL on either the State Trace Specification or Display menus. The symbols make specifying a trace specification and interpreting trace display easier.

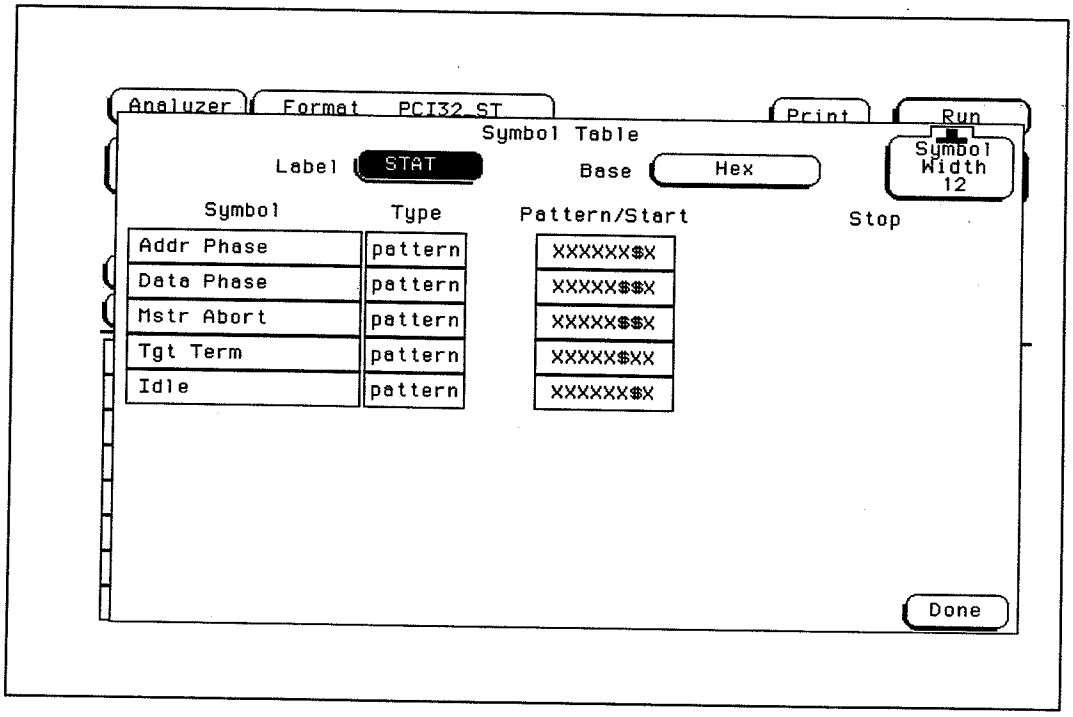


Figure 22
Symbol Definitions Loaded with PCI64_ST_A

The CMND label has symbol definitions which match those for the CBE[3::0]# signals. The definitions are the same as those found in Chapter 3 of the PCI Local Bus Specification Revision 2.1. These symbols are very useful when only certain types of bus cycles need to be monitored.

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Table 4
Resource Terms Definitions of PCI64_ST_A

	Addr Phase	Data Phase	Master Abort	Target Term
FRAME#	0	X	X	X
TRDY#	X	0	X	X
IRDY#	X	0	0	X
DEVSEL#	X	0	1	X
STOP#	X	1	X	0

Loading the PCI64 Inverse Assembler

If your configuration file becomes corrupt or you would like to create a different configuration file, the following procedure describes the necessary steps to obtain disassemble with the new configuration file. Assign the machine you are configuring to STATE. This is changed from the CONFIG menu. Assign all of the pods you are using to this machine. Choose either the state configuration as described in **Figure 2** or state configuration described in **Figure 3** for qualified clocking.

1. Create the three labels, ADDR, DATA, and STAT and assign to these labels the channels that are specified in Appendix A. Only these three labels are required by the inverse assembler. However, you may create as many as you desire.
2. Define the clocks which will be used to clock the data into the logic analyzer. Refer to the section title, **State Format Specification** on page 17 for the clocking arrangements required.
3. Load the disassembler, PCI64 or PCI64B into the current configuration. This is performed in the SYSTEM:DISK menu. Load the disassembler using the LOAD:ANALYZER command.
4. Display the trace list by pressing the LIST key on the logic analyzer. Change the HEX field for the DATA label to INVASM.
5. Store your configuration to disk, so that you may recall this configuration in the future.

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Chapter 4 Using the Preprocessor for Timing Analysis

This chapter describes how to capture timing waveforms with the preprocessor and interpret the information it displays.

Logic Analyzer Timing Menus

Obtaining the desired timing waveform display involves manipulating several key logic analyzer menus. The menu options relevant to capture timing waveforms for the PCI Local Bus processor are explained in the following subsections. (Refer to the appropriate HP Logic Analyzer Module manual for operation.)

System Menu

Loading the configuration file, PCI64_TM_A from the disk will configure the logic analyzer for state and timing analysis. Your system should look like that of **Figure 23.**

Timing Format Specification Menu

Loading the file PCI64_TM_A, the labels will be defined according to the signal listing shown in Appendix A. The format specification screen is displayed in **Figure 24** through **Figure 27.**

Timing Trace Specification Menu

The Timing Trace Specification Menu is used to specify an event required before the logic analyzer triggers. The trigger can be a pattern, edge, glitch or any combination of pattern with an edge/glitch. The Acquisition mode can be either Transitional or glitch.

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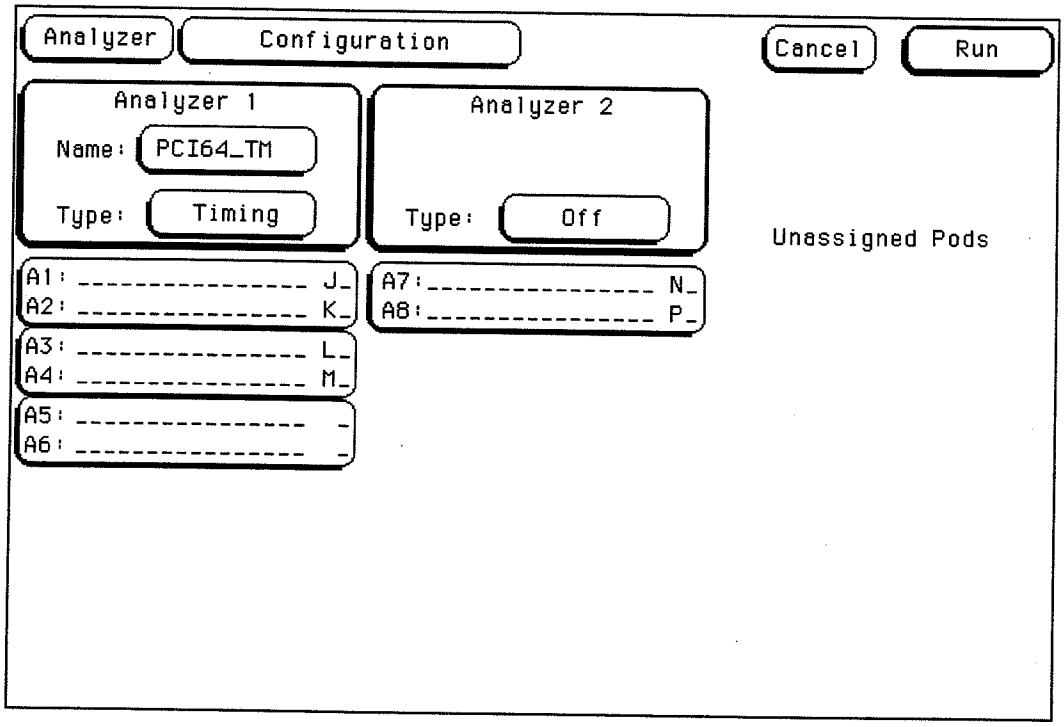


Figure 23
PI-PCI64 SYSTEM Configuration for Timing

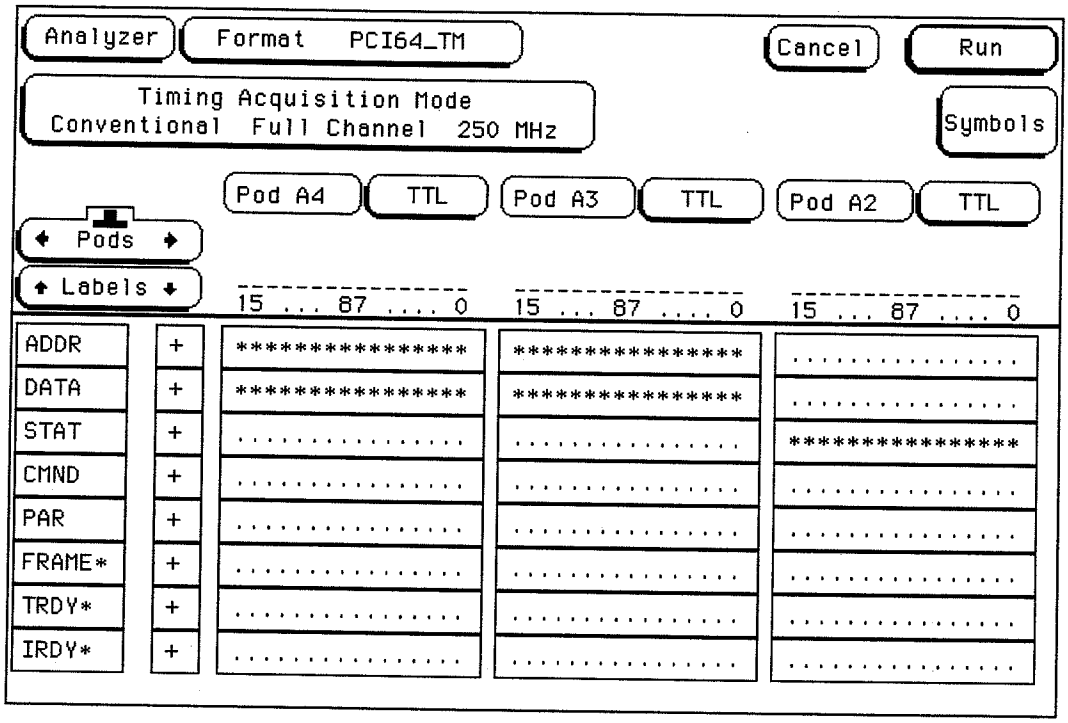


Figure 24
PI-PCI64 Timing Format Specification: Pods 3-4

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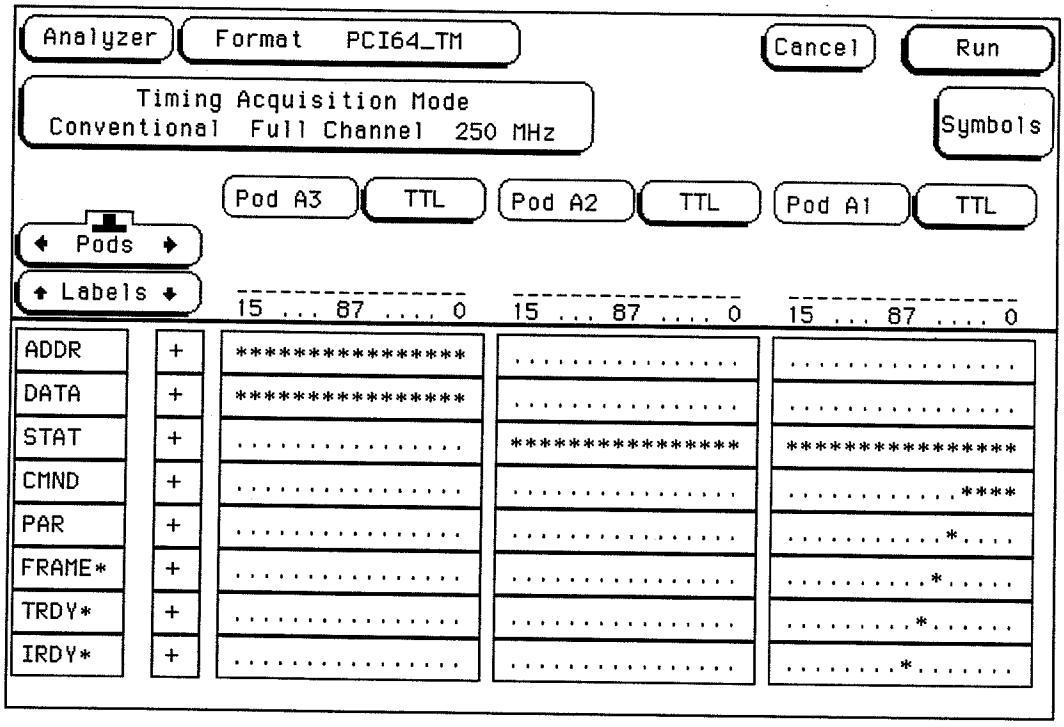


Figure 25
PI-PCI64 Timing Format Specification: Pods 1-3

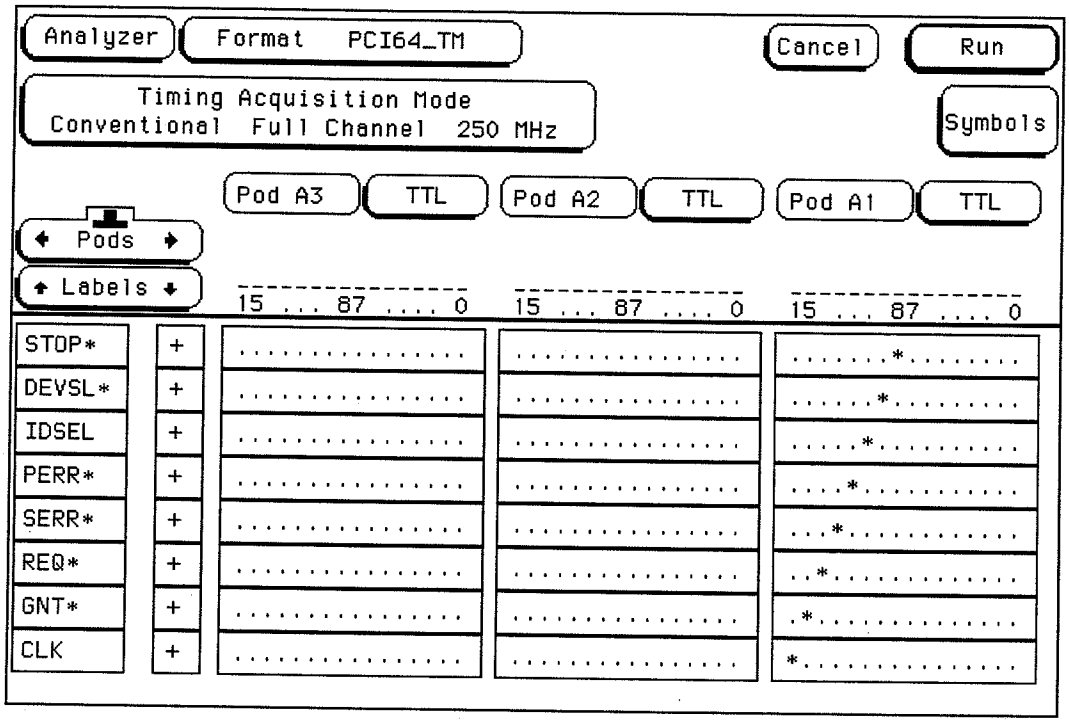


Figure 26
PI-PCI64 Timing Format Specification: Pods 1-3

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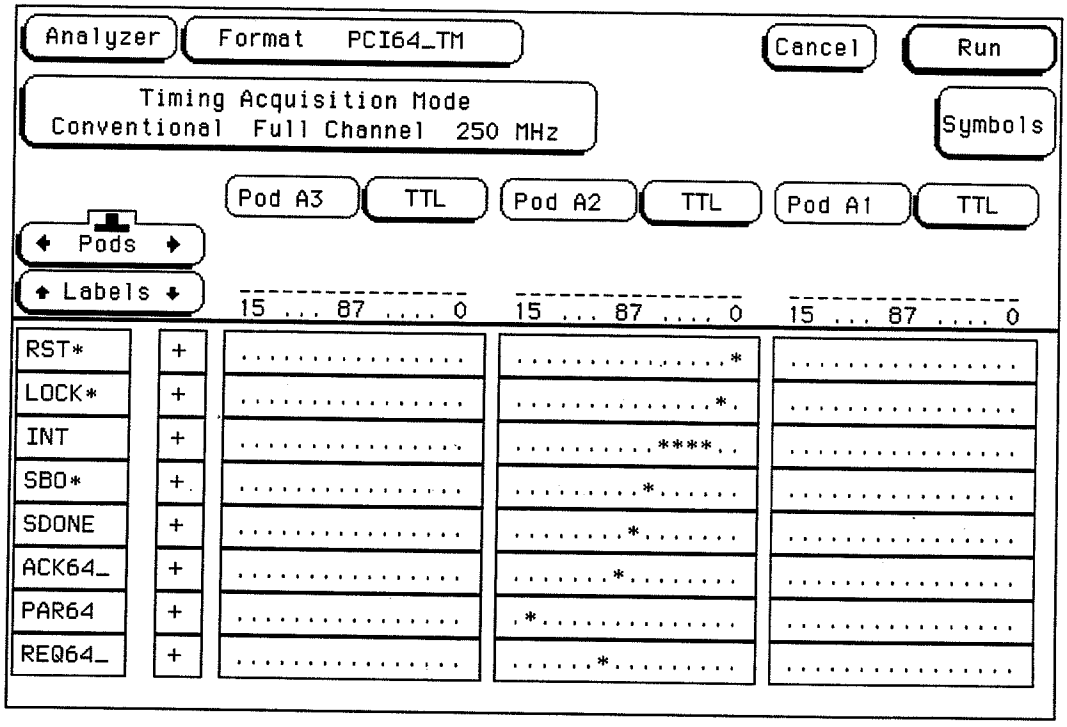


Figure 27
PI-PCI64 Timing Format Specification: Pods 1-3

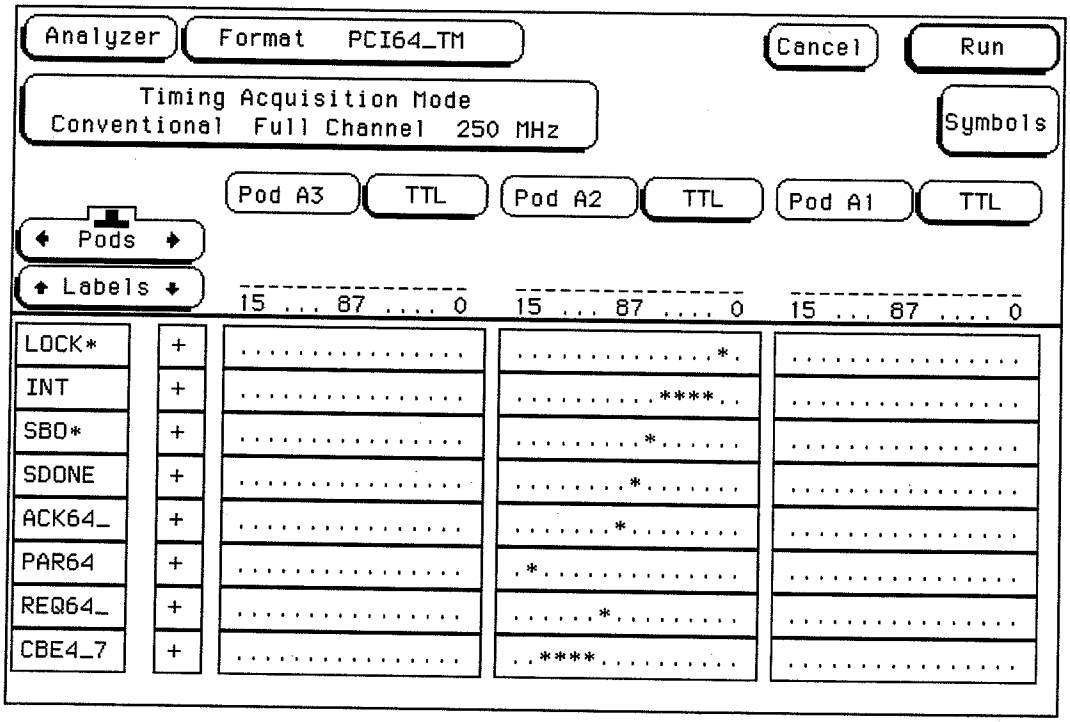


Figure 28
PI-PCI64 Timing Format Specification: Pods 1-3

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Capturing Timing Waveforms

To capture a timing waveform, specify a trigger condition and then press RUN. As soon as the trigger condition is satisfied, the logic analyzer will display the capture waveforms. **Figure 29** shows a waveform display which was captured using the FRAME# = 0 as a trigger condition.

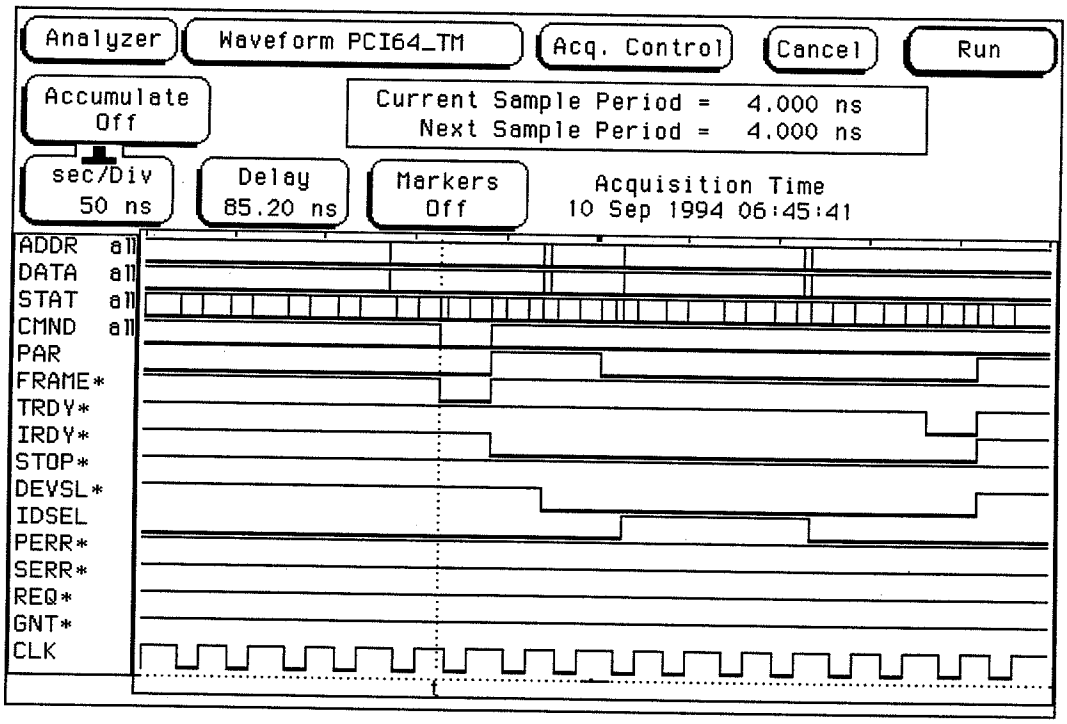


Figure 29
Timing Waveforms Captured with the PI-PCI64 Preprocessor

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Chapter 5 - Using the Preprocessor for JTAG Bus Analysis

This chapter includes information on using the PCI-JTAG bus analyzer with the HP 166X/167X/165XX logic analyzer to analyze the IEEE-1149.1 Serial Test Bus.

The PCI-JTAG Bus Analyzer, when connected to the HP 166X/167X/165XX logic analyzer, provides the mechanical and electrical link between your IEEE-1149.1 bus system and the Hewlett-Packard logic analyzer. The PCI-JTAG bus analyzer connects to the five Test Access Port Signals and routes them to the correct logic analyzer inputs.

The PCI-JTAG configuration software on the flexible disk sets up the logic analyzer to be compatible with the JTAG bus and assigns names to signals found on the bus.

Installation Overview

To analyze your IEEE-1149.1 bus system with the Corelis PI-PCI64:

1. Attach a termination adapter to POD 1 of your logic analyzer.
2. Plug the logic analyzer POD 1 probe into the 20 pin connector on the PI-PCI64, POD 5/7.
3. Load the logic analyzer configuration file "JTAG_STA_A or BA_1149_A" from the disk labeled "**PI-PCI64 Inverse Assembler**".

Connecting the HP Analyzer to the Bus Analyzer

Connect the HP 166X/167X/165XX Logic Analyzer pod to an HP1650-63203 Termination Adapter. Then connect the termination adapter to the mating 20 pin connector, Pod 5/7, on the PI-PCI64 probe adapter.

Setting Up the Analyzer from the Disk

The logic analyzer can be configured for IEEE-1149.1 Bus analysis by loading the configuration file "BA_1149_A" from the flexible disk. To load the configuration file:

1. Install the flexible disk labeled "PI-PCI64" Configuration File for use with HP 166X/167X/165XX in the front disk drive of the logic analyzer.
2. Select one of the following menus:
   - For the HP166X/167X, select SYSTEM:DISK;
   - For the HP165XX, select the System Front Disk menu.
3. Configure the menu to "Load" the analyzer with the configuration file "BA_1149_A". See **Figure 5.**
4. Execute the load operation to load the file into the HP 166X/167X/165XX Logic Analyzer.

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State Format Specification

The configuration file "BA_1149_A" contains pre-defined format specifications for monitoring your JTAG Bus system (see **Figure 30**. The JTAG-STATE configuration file can also be used to trace the data transfers across the JTAG serial bus (see **Figure 31** for the JTAG STATE display format).

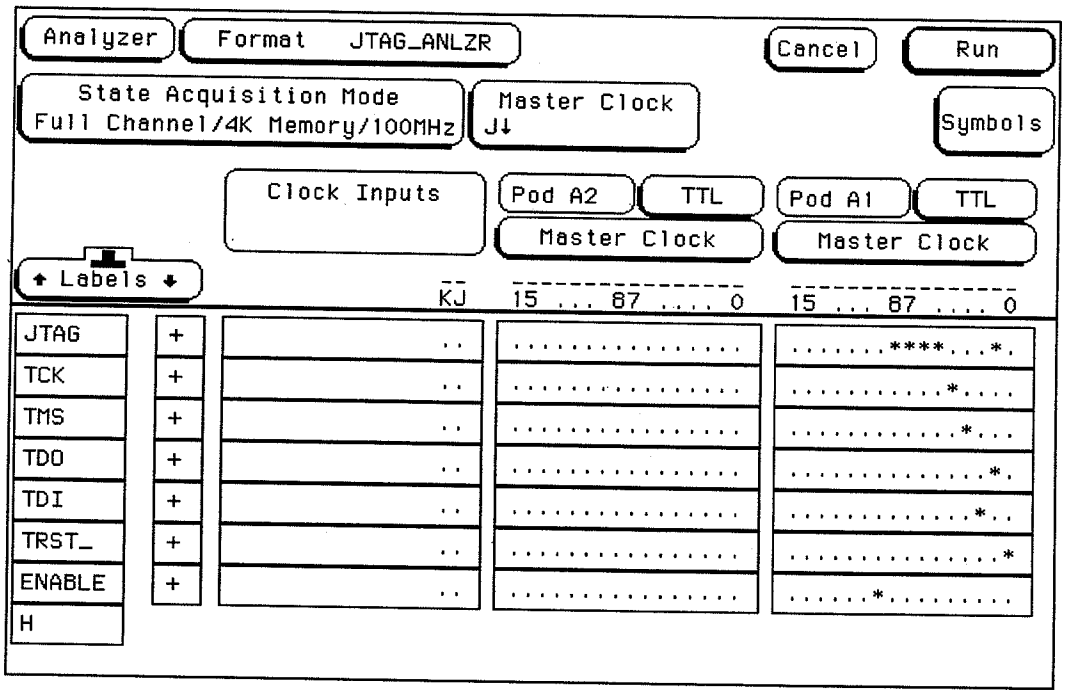


Figure 30
BA_1149 Format Specification

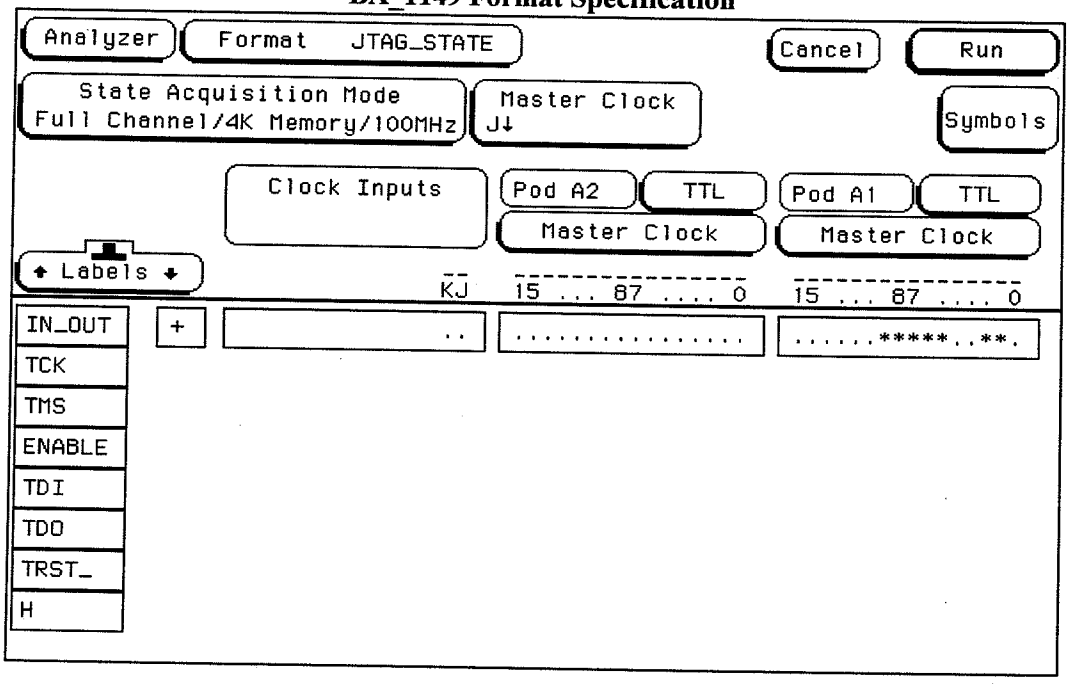


Figure 31
JTAG_STATE Format Specification

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Trace Menu

The Trace menu is configured to allow you to trigger on JTAG state and/or data information such as IEEE 1149.1 states, JTAG Test Access Port signals and data. The trace set-up menu is shown in **Figure 32** and **Figure 33.**

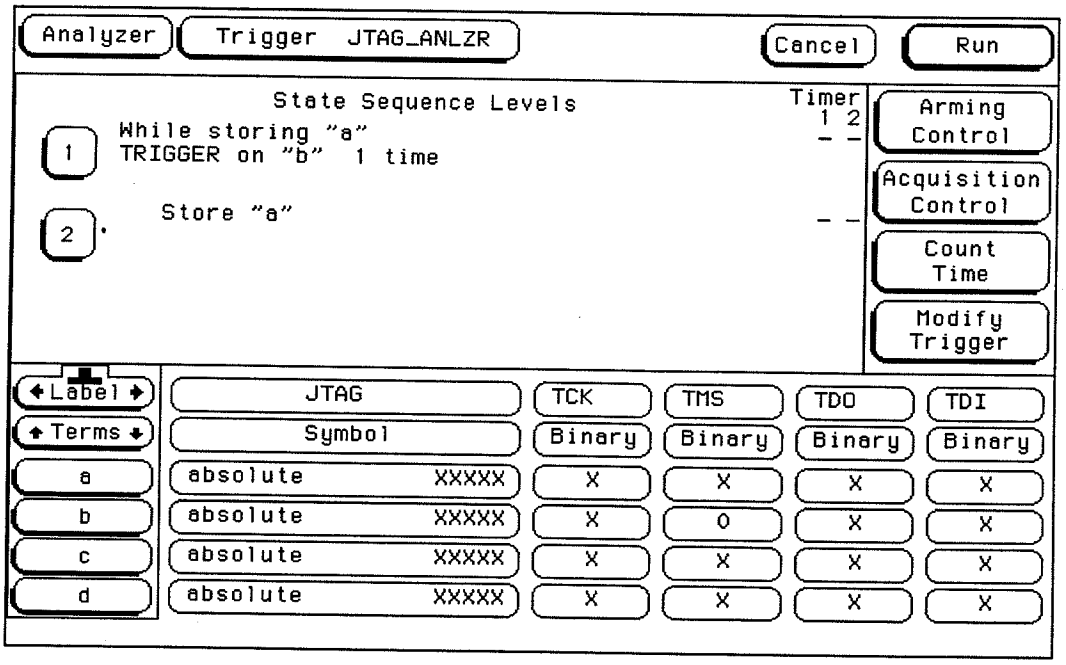


Figure 32
BA_1149 Trace Set-Up Display

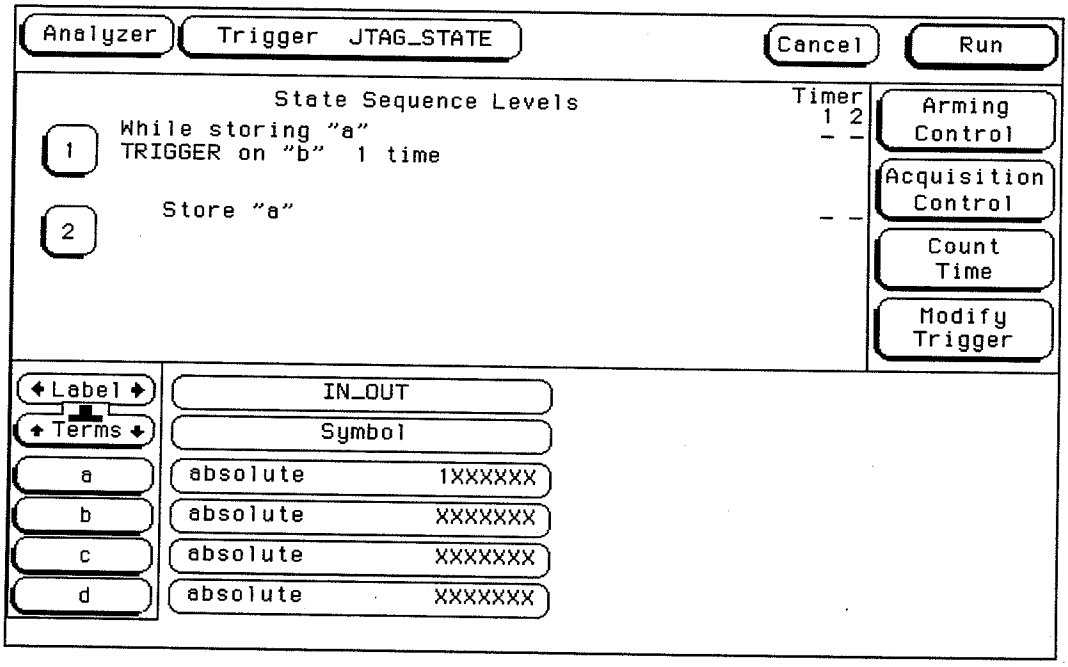


Figure 33
JTAG_STATE Trace Set-Up Display

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Slow Clock

If you have the interface module hooked up and running and observe a slow clock or no activity from the interface board, the +5 supply coming from the PCI bus may not be getting to the programmable logic device, U1, on the PI-PCI64 printed circuit board.

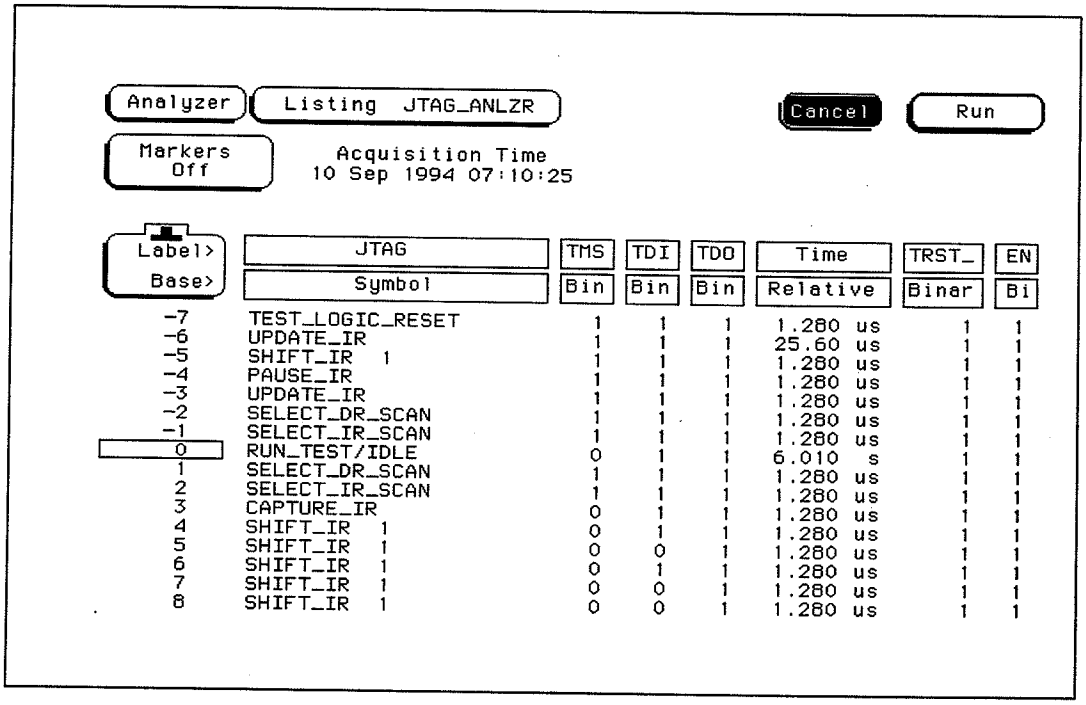
> **Note**
> The logic analyzer will also flash "Warning Slow Clock" when data is no longer being transmitted across the bus. Before checking the +5 volt supply, make sure that data is being transmitted across the bus.

To check the +5V supply coming from the PCI bus, verify that the +5V LED is lit. If not, then verify that +5V is getting to the PCI connector.

- If +5V is observed, then verify that +5V is present on U1 by checking that jumper JP1 is installed between pins 2 and 3. Reference **Figure 1** for component location.
- If +5V is observed and you feel confident that the +5V is getting to U1, then contact your nearest Corelis Sales office for information on servicing the adapter.

Listing Menu

Captured data is displayed as shown in **Figure 34** and **Figure 35** for configuration files BA_1149 and JTAG_STATE respectively. The symbol tables in the analyzer are constructed to allow you to identify the information as JTAG state mnemonics.



Label> / Base>	JTAG Symbol	TMS Bin	TDI Bin	TDO Bin	Time Relative	TRST_ Binar	EN Bi
-7	TEST_LOGIC_RESET	1	1	1	1.280 us	1	1
-6	UPDATE_IR	1	1	1	25.60 us	1	1
-5	SHIFT_IR 1	1	1	1	1.280 us	1	1
-4	PAUSE_IR	1	1	1	1.280 us	1	1
-3	UPDATE_IR	1	1	1	1.280 us	1	1
-2	SELECT_DR_SCAN	1	1	1	1.280 us	1	1
-1	SELECT_IR_SCAN	1	1	1	1.280 us	1	1
0	RUN_TEST/IDLE	0	1	1	6.010 s	1	1
1	SELECT_DR_SCAN	1	1	1	1.280 us	1	1
2	SELECT_IR_SCAN	1	1	1	1.280 us	1	1
3	CAPTURE_IR	0	1	1	1.280 us	1	1
4	SHIFT_IR 1	0	1	1	1.280 us	1	1
5	SHIFT_IR 1	0	0	1	1.280 us	1	1
6	SHIFT_IR 1	0	1	1	1.280 us	1	1
7	SHIFT_IR 1	0	0	1	1.280 us	1	1
8	SHIFT_IR 1	0	0	1	1.280 us	1	1

Figure 34
BA_1149 Captured Data Display

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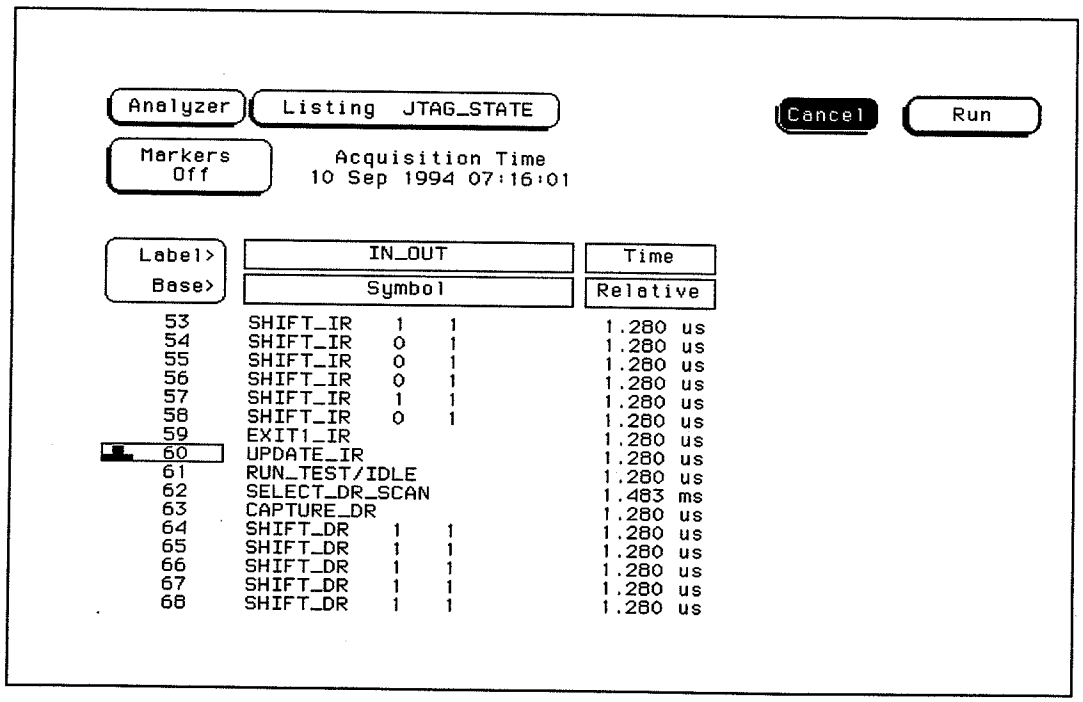


Figure 35
JTAG_STATE Captured Data Display

Timing Analysis

Five timing lines are available for the convenience of the user on POD 5 of the logic analyzer.

- TCK (POD 5, BIT 4)
- TMS (POD 5, BIT 3)
- TDI (POD 5, BIT 2)
- TDO (POD 5, BIT 1)
- TRST# (POD 5, BIT 0)

These lines may be monitored with POD 1 of the HP 165X/166X/167X/165XX logic analyzer. For more information on timing analysis, refer to the reference manual for your specific logic analyzer.

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Chapter 6 - Using the Preprocessor for Boundary Scan Testing

This chapter includes information on using the PI-PCI preprocessor with IEEE-1149.1 Serial Test Bus Testers from Corelis.

The PI-PCI64 supports the PC-1149.1 PC-AT Bus Boundary-Scan Controller and the PM3705 PC-AT Parallel I/O Centronics-based Boundary-Scan Controller. While the PCI card under test is either being developed or is in production test, the PI-PCI64 preprocessor provides a quick and convenient way of connecting to the target.

Selecting the Boundary Scan Tester

Switch S1 selects between the PM3705 tester and the PC-1149.1 tester. In the down position, connect only the PC-1149.1 tester. In the up position, connect only the PM3705 tester.

TDI/TDO Bypass

The scan chain can be closed by installing the jumper, JP3. Refer to **Figure 1** for the location of JP3. When JP3 is installed, the boundary scan signals TDI and TDO are shorted together so as to bypass the slot the PC-PCI64 is installed.

> ***Caution***
> Damage may occur if a Boundary-Scan compatible PCI card is installed in the extended connector of the PI-PCI64 when jumper JP3 is installed. All cards should be removed from the extended connector of the PI-PCI64 when JP3 is installed.

Connecting the Boundary Scan Tester

Connector P3 is provided as the Boundary Scan Tester port. Simply connect, via a cable, the boundary scan tester to connector P3 of the PI-PCI64. Be sure that S1 has been properly set and jumper JP3 has been properly configured before attaching the tester. Refer to **Figure 1** for component location.

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Appendix A PI-PCI64 Logic Analyzer Channel Assignments

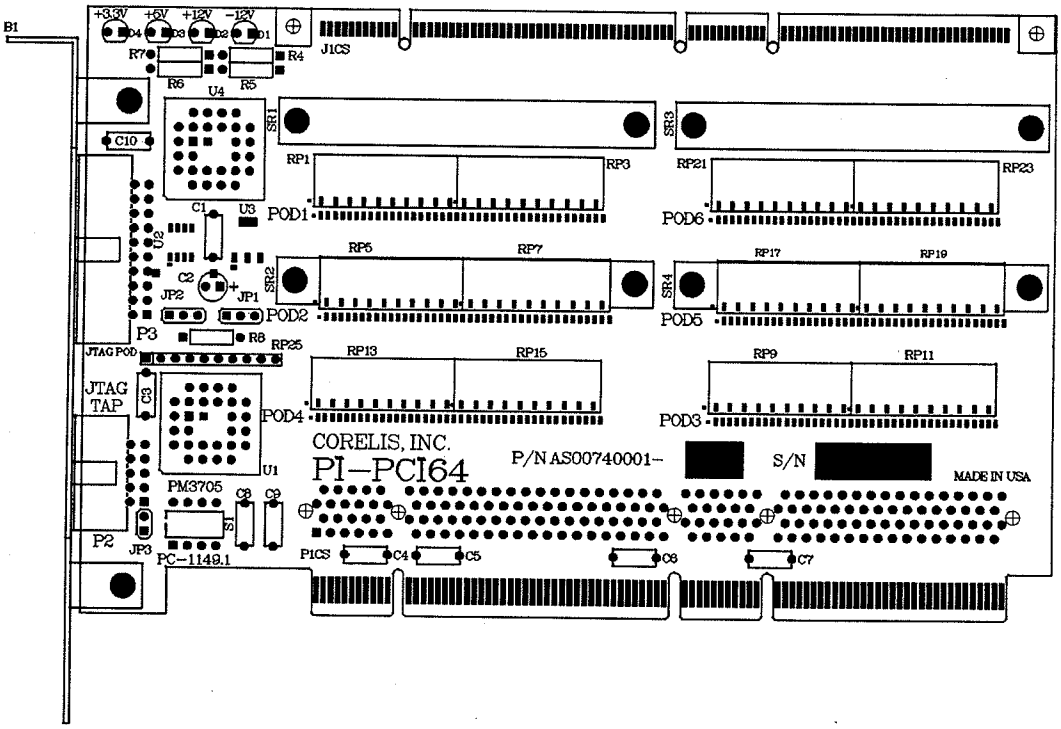


Figure 36
PI-PCI64 Component Layout

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Table 5
PI-PCI64 Logic Analyzer Channel Assignments. Pod 1.

Channel Number [pin #]	Pod 1 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	
0 [37]	CBE#0	A52	STAT, CMND
1 [35]	CBE#1	B44	STAT, CMND
2 [33]	CBE#2	B33	STAT, CMND
3 [31]	CBE#3	B26	STAT, CMND
4 [29]	PAR	A43	STAT
5 [27]	FRAME#	A34	STAT
6 [25]	TRDY#	A36	STAT
7 [23]	IRDY#	B35	STAT
8 [21]	STOP#	A38	STAT
9 [19]	DEVSEL#	B37	STAT
10 [17]	IDSEL	A26	STAT
11 [15]	PERR#	B40	STAT
12 [13]	SERR#	B42	STAT
13 [11]	REQ#	B18	STAT
14 [9]	GNT#	A17	STAT
15 [7]	CLK	B16	STAT
CLK [3]	CLK	B16	

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Table 6
PI-PCI64 Logic Analyzer Channel Assignments. Pod 2.

Channel Number [pin #]	Pod 2 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	
0 [37]	RST#	A15	STAT
1 [35]	LOCK#	B39	STAT
2 [33]	INTA	A6	STAT
3 [31]	INTB	B7	STAT
4 [29]	INTC	A7	STAT
5 [27]	INTD	B8	STAT
6 [25]	SBO#	A41	STAT
7 [23]	SDONE	A40	STAT
8 [21]	ACK64#	B60	STAT
9 [19]	REQ64#	A60	STAT
10 [17]	CBE4	B66	STAT
11 [15]	CBE5	A65	STAT
12 [13]	CBE6	B65	STAT
13 [11]	CBE7	A64	STAT
14 [9]	PAR64	A67	STAT
15 [7]			STAT
CLK [3]			

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Table 7
PI-PCI64 Logic Analyzer Channel Assignments. Pod 3.

Channel Number [pin #]	Pod 3 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	
0 [37]	AD0	A58	ADDR, DATA
1 [35]	AD1	B58	ADDR, DATA
2 [33]	AD2	A57	ADDR, DATA
3 [31]	AD3	B56	ADDR, DATA
4 [29]	AD4	A55	ADDR, DATA
5 [27]	AD5	B55	ADDR, DATA
6 [25]	AD6	A54	ADDR, DATA
7 [23]	AD7	B53	ADDR, DATA
8 [21]	AD8	B52	ADDR, DATA
9 [19]	AD9	A49	ADDR, DATA
10 [17]	AD10	B48	ADDR, DATA
11 [15]	AD11	A47	ADDR, DATA
12 [13]	AD12	B47	ADDR, DATA
13 [11]	AD13	A46	ADDR, DATA
14 [9]	AD14	B45	ADDR, DATA
15 [7]	AD15	A44	ADDR, DATA
CLK [3]			

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Table 8
PI-PCI64 Logic Analyzer Channel Assignments. Pod 4.

Channel Number [pin #]	Pod 4 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	
0 [37]	AD16	A32	ADDR, DATA
1 [35]	AD17	B32	ADDR, DATA
2 [33]	AD18	A31	ADDR, DATA
3 [31]	AD19	B30	ADDR, DATA
4 [29]	AD20	A29	ADDR, DATA
5 [27]	AD21	B29	ADDR, DATA
6 [25]	AD22	A28	ADDR, DATA
7 [23]	AD23	B27	ADDR, DATA
8 [21]	AD24	A25	ADDR, DATA
9 [19]	AD25	B24	ADDR, DATA
10 [17]	AD26	A23	ADDR, DATA
11 [15]	AD27	B23	ADDR, DATA
12 [13]	AD28	A22	ADDR, DATA
13 [11]	AD29	B21	ADDR, DATA
14 [9]	AD30	A20	ADDR, DATA
15 [7]	AD31	B20	ADDR, DATA
CLK [3]			

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Table 9
PI-PCI64 Logic Analyzer Channel Assignments. Pod 5.

Channel Number [pin #]	Pod 5 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	Master Clock
0 [37]	AD32	A91	DATA_B
1 [35]	AD33	B90	DATA_B
2 [33]	AD34	A89	DATA_B
3 [31]	AD35	B89	DATA_B
4 [29]	AD36	A88	DATA_B
5 [27]	AD37	B87	DATA_B
6 [25]	AD38	A86	DATA_B
7 [23]	AD39	B86	DATA_B
8 [21]	AD40	A85	DATA_B
9 [19]	AD41	B84	DATA_B
10 [17]	AD42	A83	DATA_B
11 [15]	AD43	B83	DATA_B
12 [13]	AD44	A42	DATA_B
13 [11]	AD45	B81	DATA_B
14 [9]	AD46	A80	DATA_B
15 [7]	AD47	B80	DATA_B
CLK [3]			

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Table 10
PI-PCI64 Logic Analyzer Channel Assignments. Pod 6.

Channel Number [pin #]	Pod 6 Signal Name	PCI Pin #	Label
GND [even]	GND	Vss	Master Clock
0 [37]	AD48	A79	DATA_B
1 [35]	AD49	B78	DATA_B
2 [33]	AD50	A77	DATA_B
3 [31]	AD51	B77	DATA_B
4 [29]	AD52	A76	DATA_B
5 [27]	AD53	B75	DATA_B
6 [25]	AD54	A74	DATA_B
7 [23]	AD55	B74	DATA_B
8 [21]	AD56	A73	DATA_B
9 [19]	AD57	B72	DATA_B
10 [17]	AD58	A71	DATA_B
11 [15]	AD59	B71	DATA_B
12 [13]	AD60	A70	DATA_B
13 [11]	AD61	B69	DATA_B
14 [9]	AD62	A68	DATA_B
15 [7]	AD63	B68	DATA_B
CLK [3]			

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Table 11
PI-PCI64 Logic Analyzer Channel Assignments. JTAGPod

Channel Number [Pin #]	JTAG Pod P3 Signal Name
GND[20]	GND
0 [19]	TRST#
1 [18]	TDO
2 [17]	TDI
3 [16]	TMS
4 [15]	TCK
5 [14]	ENABLE
6 [13]	STATE 0
7 [12]	STATE 1
8 [11]	STATE 2
9 [10]	STATE 3
10 [9]	unused
11 [8]	unused
12 [7]	unused
13 [6]	unused
14 [5]	unused
15 [4]	unused
CLK [3]	TCK

Table 12
PI-PCI64 Boundary Scan Tester Port: P2.

Pod 2 Pin Number	Signal Name Switch S1 Position Down	Signal Name Switch S1 Position Up
1	TRST	TRST
3	TD0	TD1
5	TD1	TD0
7	TMS	TMS
9	TCK	TCK

The even pin number of Pod 2 in **Table 12** is grounded.

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Appendix B PC I/O Mapped Addresses Decoded by PCI64B

Table 13
PC I/O Mapped Addresses Decoded by PCI64B

I/O Address	Symbol Displayed
000 — 00F	DMA#1 (8237)
020 — 021	PIC#1 (8259)
040 — 043	Timer (8253)
060 — 064	8742 Controller
070 — 071	CMOS RAM
080 — 08F	DMA Page Registers
0A0 — 0A1	PIC#2 (8259)
0C0 — 0DF	DMA#2 (8237)
0F0 — 0FF	80287 Coprocessor
1F0 — 1FF	Hard Disk
200 — 20F	Game/Control
238 — 23B	Bus Mouse
23C — 23F	Alt. Bus Mouse
278 — 27F	LPT3
2B0 — 2BF	EGA
2C0 — 2CF	EGA
2D0 — 2DF	EGA
2E0 — 2E7	GPIB
2E8 — 2EF	COM4
2F8 — 2FF	COM2
300 — 30F	Prototype
310 — 31F	Prototype
378 — 37F	LPT2
380 — 38F	SDLC
3A0 — 3AF	SDLC
3B0 — 3BB	MDA
3BC — 3BF	LPT1
3C0 — 3CF	EGA
3D0 — 3DF	CGA
3E8 — 3EF	COM3
3F0 — 3F7	Floppy Disk
3F8 — 3FF	COM1

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Appendix C - PI-PCI64 Specifications and Operating Characteristics

Timing Mode

Conventional Sample Period: 4ns/2ns minimum, 8.18 ms maximum.
Conventional Maximum Time Covered by Data: 34.3s/68.6s maximum.
Channel to Channel Skew: 2 ns typical.
Minimum Detectable Glitch: 3.5 nanoseconds wide at the threshold.
Maximum Glitch Width: Sample period - 1 ns.

State Mode

Clock Repetition Rate: Single phase is 100 MHz maximum for the HP 1660A
Clock Pulse Width: ≥ 3.5 nanoseconds at threshold.
Setup Time: Data must be present prior to clock transition, 0-3.5 ns.
Hold Time: Data must be present after rising clock transition, 3.5-0 ns.
Acquisition Memory Depth: 8192 states. 4096 states with time or state counting.
Number of Pattern or Range Symbols: 1000 total.

Probes

Input RC: 100 kohm ± 2% shunted by approximately 8 pF at the probe tip.
TTL Threshold Preset: ± 1.6 volts.

Testing and Troubleshooting

There are no automatic tests or adjustments for the PI-PCI64 Preprocessor. If a failure is suspected in the PI-PCI64 Preprocessor, contact Corelis' Office for information on servicing the board.

Replaceable Parts

Since there are no automatic tests which can be used to diagnose a hardware failure on the PI-PCI64, there are no customer replaceable parts for the PC-PCI64 Preprocessor. If a failure is suspected in the PI-PCI64 Preprocessor, contact Corelis' Office for information on servicing the board.

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Table 14
General Requirements and Operating Characteristics

General Requirements:	
Signals Monitored	All signals except POWER and GROUND
Signal Loading	100 Kohm @ 8 pF One CMOS load (22V10) on: FRAME#, IRDY#, TRDY#, DEVSEL, PERR#, SERR#, TDI, TDO, TMS, TCK, TRST#
Accessories Required	None.
Logic Analyzer Supported	PCI: HP166X, 167X, 165XX JTAG: HP166X, 167X, 165XX
Number of Probes Used	Six 16-channel probes for state and/or timing analysis. Refer to Table 1. Only one probe for JTAG analysis.
Power Requirements	Maximum 0.025 amps at +5 Vdc supplied by the PCI Local Bus system.
Maximum Acquisition Speed	250/500 MHz Timing 100 MHz State
Temperature:	
Operating	0 C to +55 C (+32 F to +131 F)
Non-operating	-40 C to +75 C (-40 F to +167 F)
Altitude:	
Operating	Up to 4600 meters (15,000 feet)
Non-operating	Up to 15,300 meters (50,000 feet)
Humidity	90% non-condensing. Avoid sudden extreme temperature changes that could cause condensation within the instrument.
Construction:	
Physical Dimensions	6.730" wide by 4.200" high. Add 0.550" to height for extension connector.
Multi-Layer PCB	8 Layers: 5 Signal, 3 Power
Planes	Ground, +5 V, +3.3 V

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Appendix D Troubleshooting

If you encounter difficulties while making measurements, use this section to guide you through some possible solutions. Each heading lists a problem you may encounter, along with some possible solutions. Error messages which may appear on the logic analyzer are listed below in quotes "". Symptoms are listed without quotes.

Target Board Will Not Bootup

If the target board will not bootup after connecting the preprocessor interface, then check bus and cable interfaces.

"Slow or Missing Clock"

This error might occur if the logic analyzer cards are not firmly seated in the HP 16500 frame. Ensure that the cards are firmly seated.

This error might also occur if the target system is not running properly. Ensure that the target system is on and operating properly.

If the error message persists, check that the logic analyzer pods are connected to the proper connectors, as listed in **Table 1** and **Table 2**.

"No Configuration File Loaded"

Verify that the appropriate module has been selected from the Load {module} from File {filename} in the HP 16500 disk operation menu. Selecting Load {All} will cause incorrect operation when loading most preprocessor interface configuration files.

"...Inverse Assembler Not Found"

This error occurs if you rename or delete the inverse assembler file that is attached to the configuration file. Ensure that the inverse assembler is not renamed or deleted.

No Inverse Assembly

Verify that the inverse assembler has been synchronized by placing an opcode at the top of the display and pressing the Invasm key (see "Using the Invasm Field" Chapter 3).

Incorrect Inverse Assembly

This problem is usually caused by a hardware problem in the target system. A locked status line will often cause incorrect or incomplete inverse assembly.

- Check the activity indicators for status lines locked in a high or low state.
- Verify that the STAT, DATA, DATA_B, and ADDR format labels have not been modified from their default values. These labels must remain as they are configured by the configuration file.

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- Verify that all microprocessor caches and memory managers have been disabled. In most cases, if the microprocessor caches and memory managers remain enabled you should still get inverse assembly, but it may be incorrect since some of the execution trace was not visible to the logic analyzer.
- Verify that storage qualification has not excluded storage of all the needed opcodes and operands.

No Activity on Activity Indicators

If there is no activity, one of the cables, board connections, or preprocessor interface connections is probably loose. Check all connections.

Capacitive Loading

Excessive capacitive loading can cause signals to degrade, resulting in incorrect capture by the preprocessor interface or system lockup in the microprocessor. All preprocessor interfaces add additional capacitive loading. Remove as many pin protector, extenders, and adapters as possible.

Unwanted Triggers

Unwanted triggers can be caused by unexecuted pre-fetches. Add the pre-fetch queue depth to the trigger address to avoid this problem.

Intermittent Data Errors

This problem is usually caused by incorrect signal levels. Adjust the threshold level of the data pod. Use an oscilloscope to check the signal integrity of the data lines, as needed.

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