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MULTI-DROP DATA TRANSPORTERS

PVIC and VIC Family

PCI-to-PCI Vertical Interconnections and VME-to-VME VIC-Based Connections



HIGHLIGHTS

- Fully transparent byte, word, long-word transactions
- Onboard autonomous block mover offering multiple chained DMAs, executed concurrently
- Supports hot disconnection
- Full PCI speed traffic at 132 MBytes/s bandwidth
- Advanced mechanism for real-time interprocessor communication
- Up to fifteen stops per interconnection spanning up to 200 meters, no driver required
- VME, PMC and PCI form factors
- Versatile interrupt dispatching logic for remote and local interrupt handling
- Rich set of broadcast modes

APPLICATIONS

Typical applications include any real-time distributed high-speed data transportation such as robotics, aircraft test equipment, distributed CPU clusters, flight simulators, physics experiments, etc.

GENERAL DESCRIPTION

Combining VME interconnection know-how, which contributed to an ISO standard (VIC Bus - ISO/IEC 26.11458), with in-depth PCI expertise, the PVIC (PCI Vertical InterConnection) concept gives the PCI the right dimension in advanced data acquisition systems: the data backbone between PCI-based VME or CompactPCI processors and workstations.

As in every major CES product, it combines state-of-the-art technology with a system-level approach. This translates into unique features such as atomic cycle support, global semaphores, intelligent broadcasts, etc. in order to build a smooth running scalable multiprocessor architecture.

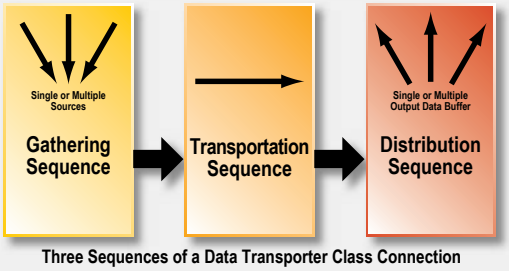
Together with CES deterministic PowerPC computing cores and network interfaces, PVIC provides a totally safe and easy-to-use global solution, which meets demanding data-processing requirements in command and control, distributed telecommunications and signal processing.

PCI bus is widely used as a local bus for both VME and CompactPCI processor boards and desktop workstations. The PVIC concept described here has been developed by CES to allow PCI-based processors to be connected in clusters of up to 15 nodes spanning up to 200 meters. While preserving the full PCI throughput (132 MBytes/s at 32-bit, 33 MHz) for block accesses, the transparent mapping of remote PCI addresses minimizes latencies and drastically reduces the software overhead.

Belonging to the data transporter class, the PVIC architecture features self-hosted data transportation through an onboard block mover engine, multiple DMA channels, as well as efficient signaling services. The PVIC connection also offers linked lists, multi-cast cycles, local and remote interrupt, mailboxes and global semaphores. Broadcast and multicast cycles, interrupt dispatching, mailboxes, a mirrored memory and global semaphores provide the hardware support for efficient inter-processor communication.

For maximum flexibility, each of the PVIC interfaces can be adapted to the users environment and distance requirements due to small piggy-backs called PIBs (Physical Interface Board), which are available for small distances (down to 1 meter), medium distances (up to 30 meters) and long distances (up to 200 meters).

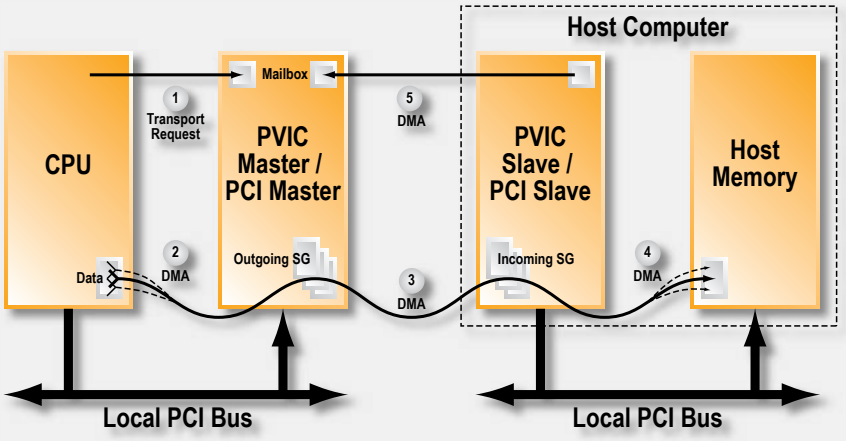
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Three Sequences of a Data Transporter Class Connection

PVIC ARCHITECTURE

The PVIC (PCI Vertical InterConnection) is the PCI equivalent of the VIC (VME InterConnection) with added functionalities, such as an onboard chained DMA engine and intelligent broadcast logic. The PVIC is a 16-bit bus time-multiplexed clocked at 66 MHz, delivering a 132 MBytes/s bandwidth memory mapped.



Transportation Sequences

1 - Local CPU request phase
2 - Local PCI data transport phase
3 - PVIC data transport phase
4 - Remote PCI data transport phase
5 - End of transaction / acknowledgement phase

PVIC TRANSACTIONS

The PVIC provides a transparent PCI bus-to-PCI bus coupler, which supports all byte, word, long word and burst cycles with no latency.

PVIC supports the following transaction types:

> Write single shot
> Broadcast
> Write burst and burst broadcast
> Write mirrored memory
> Read single shot
> Read burst
> Semaphore test and set

The arbitration on the bus is multilevel (standard and high-priority) with a rotating arbiter and support for “fair” mode, so that multiple concurrent transactions can occur.

TRANSPARENT MODE

The PVIC is mapped in the PCI bus through two independent spaces:

> Standard PCI configuration space, which contains all of the required CSRs to set up the connection
> PCI memory space window, which allocates the memory windows for each PVIC-interconnected local PCI bus

The memory allocation uses one in-coming and one out-going scatter / gather with page sizes of 64 KBytes and 4 KBytes respectively.

Once the initialization library has set up the desired working modes and page selection, a fully transparent connection is established between all of the PVIC interconnected systems.

MESSAGE PASSING

For multiprocessor applications an efficient message passing mechanism is required. Therefore the PVIC uses a global semaphore logic and provides a mailbox system for efficient interprocessor communication.

Message signaling occurs with a user-level programmable FIFO-based interprocessor message passing mechanism.

DMA BLOCK MOVER

PVIC nodes may incorporate a DMA sequencer as an option. The DMA sequencer supports elementary DMAs or linked lists of DMA. The DMAs can be controlled either from the local PCI or from a remote PCI through PVIC.

Complete messages can be sent to specific nodes or may be broadcast. DMA sequences operate at full PCI speed with a payload of up to 16 KBytes per elementary DMA.

Multiple DMA chains can be defined per node. Sixteen DMA channels can run concurrently per node.

INTELLIGENT BROADCAST

Data distribution requires high-speed, safe and efficient mechanisms when transporting data to its destination.

The PVIC provides a unique broadcast mechanism, which incorporates an acknowledge check from all slave nodes, to guarantee reception. It also has an address relocation mechanism, where each slave node remaps the data to its own chosen address, so that software data copy is no longer required. The broadcast logic also supports burst transactions.

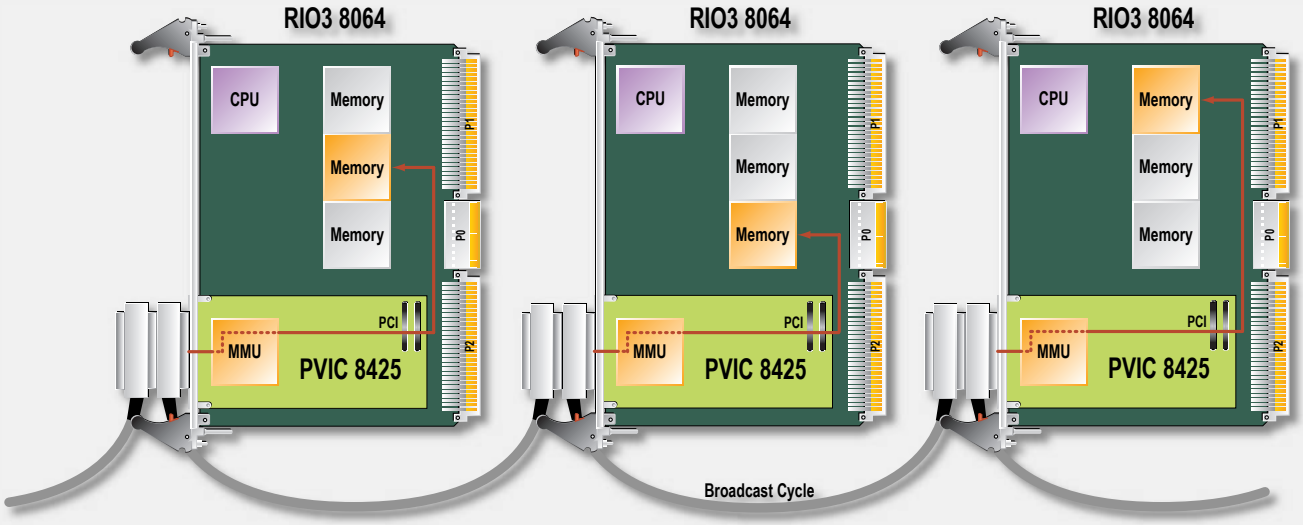
INTERRUPT STRUCTURE

The PVIC incorporates an advanced interrupt dispatching logic, which supports local and remote interrupt handling.

Interrupt sources are the four PCI interrupt lines, the PCI error interrupts, PVIC transaction error interrupts and the DMA controller interrupts (normal ending condition or error condition). All of these sources can be transparently exported to the local PCI bus or to a remote PCI bus.

The interrupt logic incorporates a complete set of CSRs, a programmable priority encoder as well as an enabling / disabling logic.

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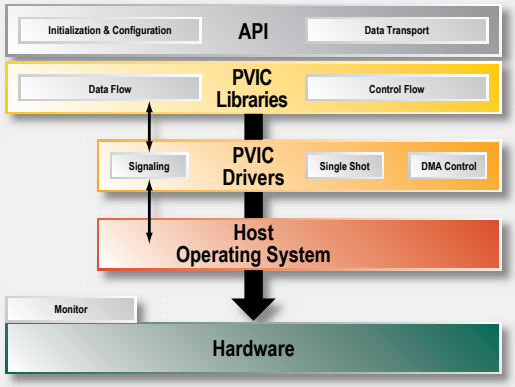
Broadcast Transfer with Multiple Addresses

COMPREHENSIVE SOFTWARE SUPPORT

> Generic Unix library
> Optimized LynxOS® and VxWorks® drivers for real-time applications
> Prepackaged Alpha, Linux®, PC, Silicon Graphics and Sun optimized drivers

SOFTWARE API

The PVIC system is supported by an API consisting of a C library and associated drivers. Since it is memory mapped, the PVIC library software is relatively simple. However to benefit from the self-hosted data transportation mechanism the software to handle the DMAs local and remote support is included in the associated drivers. For all platforms not already covered by existing packages, a generic UNIX library is available in source code (C code).



PVIC LIBRARIES AND DEDICATED DRIVERS

Generic C Library	32250A
Drivers for General Purpose Operating Systems	
Linux PC	31250L
WindowsNT PC	31250D
IRIX	31250I
Alpha OSF	31250J
Solaris	31250K
Drivers for Real-Time Operating Systems	
LynxOS®	31250A
VxWorks®	31250B

COMMAND EXAMPLES

Declaration

pvicNodeXxx: A PVIC node is treated as an object called “pvicNode”. Such an object can represent a local or remote PVIC node. A properly initialized “pvicNode” object allows the user to execute most of the PVIC functions on any node in the system. For example, the user can transparently execute a PVIC DMA on a local or remote node:

> pvicDmaStart (local_node);
> pvicDmaStart (remote_node);

Configuration

pvicSetupXxx: Handles the task of PVIC node setup at boot time or after PVIC system reset. The PVIC monarch (with node-id 1) will interrogate other PVIC slaves, initialize the PVIC timing parameters and then store the system and node configuration parameters in its SSRAM. After initialization, a PVIC node scan function allows the user to get an initialized “pvicNode” object for each node present.

pvicOutpageXxx: Programs the out-going scatter / gather pages of a PVIC node. A simple dynamic outpage allocation mechanism is used.

pvicInpageXxx: Programs the in-coming scatter / gather pages of a PVIC node, which includes matching logic.

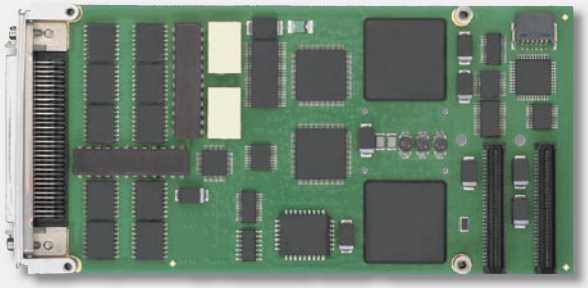
pvicPciXxx: Includes PVIC PCI related functions, such as programming the PCI configuration registers, PCI abort handling and performing PCI configuration type 0 and type 1 cycles over the PVIC bus.

Data Transportation

pvicDmaXxx: Supports the powerful PVIC DMA engine, which allows to write to remote PVIC nodes at (almost) full PCI speed. A remote DMA read is not executed, but can be performed by programming the remote PVIC node accordingly.

> The DMA transfer is defined through DMA descriptor blocks (pvicDmaBlock) located in the local SSRAM
> More than 6000 DMA descriptors can be set up and chained together
> A DMA FIFO allows to post up to sixty-four chains of DMA descriptors
> A DMA FIFO empty, half-full and full status allows to preload the DMA FIFO without overflowing
> The DMA engine can fetch the chain parameters from the DMA FIFO automatically (FIFO mode) or step by step (Single Mode)
> A DMA end, error or suspend interrupt can be generated on a per DMA descriptor base
> A DMA signature allows to run up to sixteen PVIC DMA transfers concurrently with interrupt notification
> The DMA can be suspended and atomically continued allowing higher priority transfers to be executed

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PVIC 8425 - PMC INTERFACE

The PMC member of the PVIC family, the PVIC 8425, can be used with CES VME or CompactPCI-based processor boards for in-chassis processor interconnection (from 1 meter to 30 meters) or long distance inter-chassis connection. It takes advantage of the RIO4, RIO3, RIOC and RIOS technology, which allows simultaneous VME or CompactPCI acquisition, CPU operation and PCI input / output. It supports dedicated GTL or differential onboard physical interfaces.

It features an embedded physical interface, which can be either GTL 8425BA or differential 8425DA, therefore it does not require any PIBs.

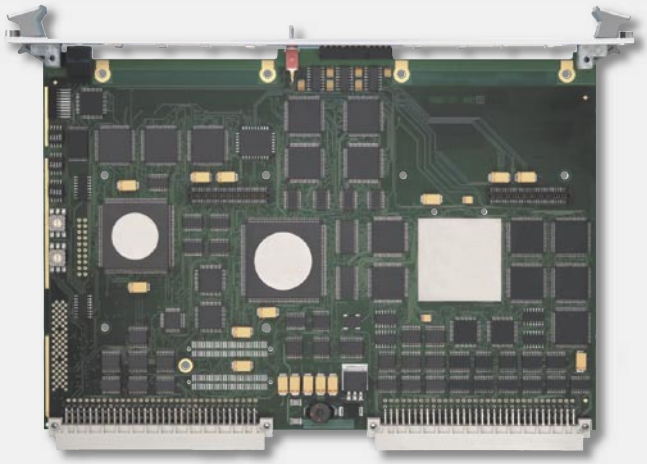


PVIC 7225 - PCI / PCI-X COMPATIBLE HOST COMPUTER

The PVIC 7225 is a PCI ISA form factor board for use in PCI / PCI-X-equipped workstations (Alpha, Macintosh, PC, Silicon Graphics, Sun, etc.). It supports differential, GTL and optical physical interfaces. Drivers are available under the principal operating systems of these workstations.

The combination is available to deliver continuous data transfers at over 50 MBytes/s to 100 MBytes/s into the host without any impact on the host computing capacity.

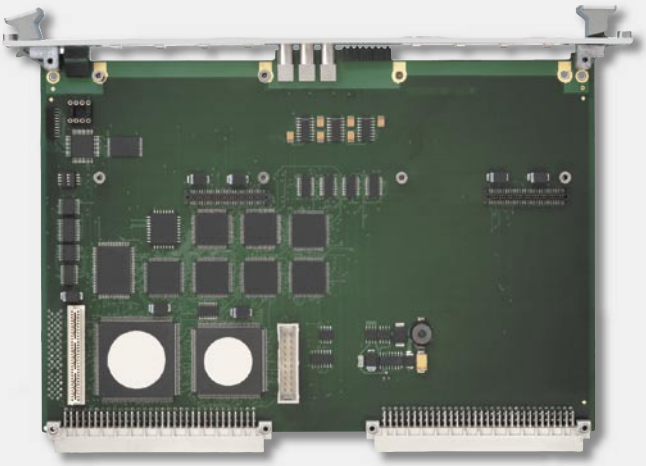
Two versions are available, one for PC's equipped with PCI and one for PC's equipped with PCI-X in PCI emulation.



PVIC 8025 -VME INTERFACE

The PVIC 8025 is the VME interface of the PVIC family. It features the following:

- VME slot-1 and arbiter functions
- VME master / slave D64 interface
- Autonomous VME link list DMA block mover
- Remote or local trigger logic
- Completely transparent VME-to-remote PCI data transporter
- Supports both single shot and DMA transfers between PVIC and VME

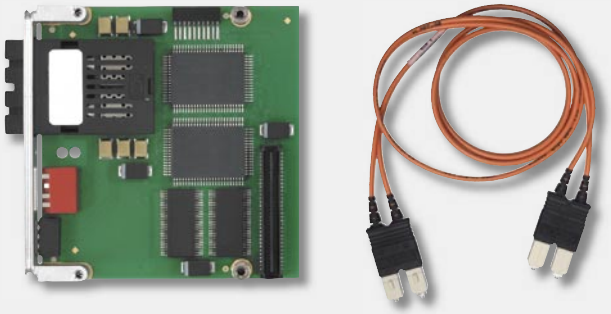


PVIC 8426 - PVIC BRIDGE

The PVIC 8426 is attached to a CES RIO3 through its PCI extension connector, thus leaving free the two PMC slots of the motherboard. It can be equipped with two different PVIC physical interfaces, each of which may be either GTL, differential or optical (maximum one optical PIB), and therefore used as a PVIC bridge. PVIC 8425 mezzanines can be interfaced with a long-distance PVIC link through the PVIC 8426 bridge.

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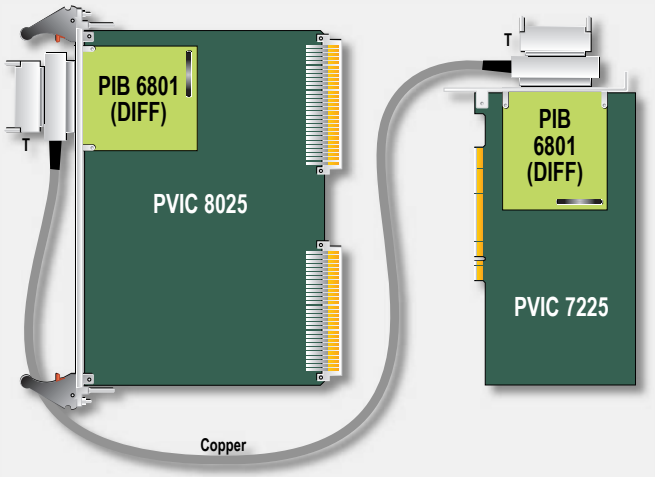


PIB 6801 - DIFFERENTIAL PHYSICAL INTERFACE

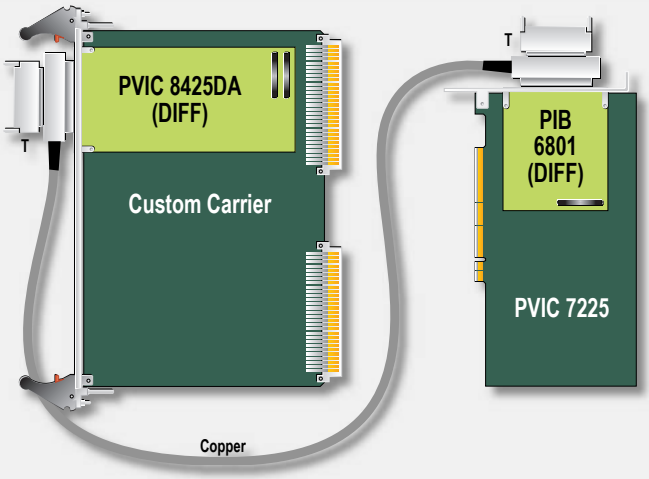
For distances up to 15 meters (132 MBytes/s at 66 MHz) or 30 meters (66 MBytes/s at 33 MHz). Interconnected with a shielded round cable with auto daisy-chaining (VDC 6500), which is equipped with a SCSI II 68-pin connector. A terminator (TER 6225) must be used at both ends of the differential bus.

PIB 6802 - OPTICAL PHYSICAL INTERFACE

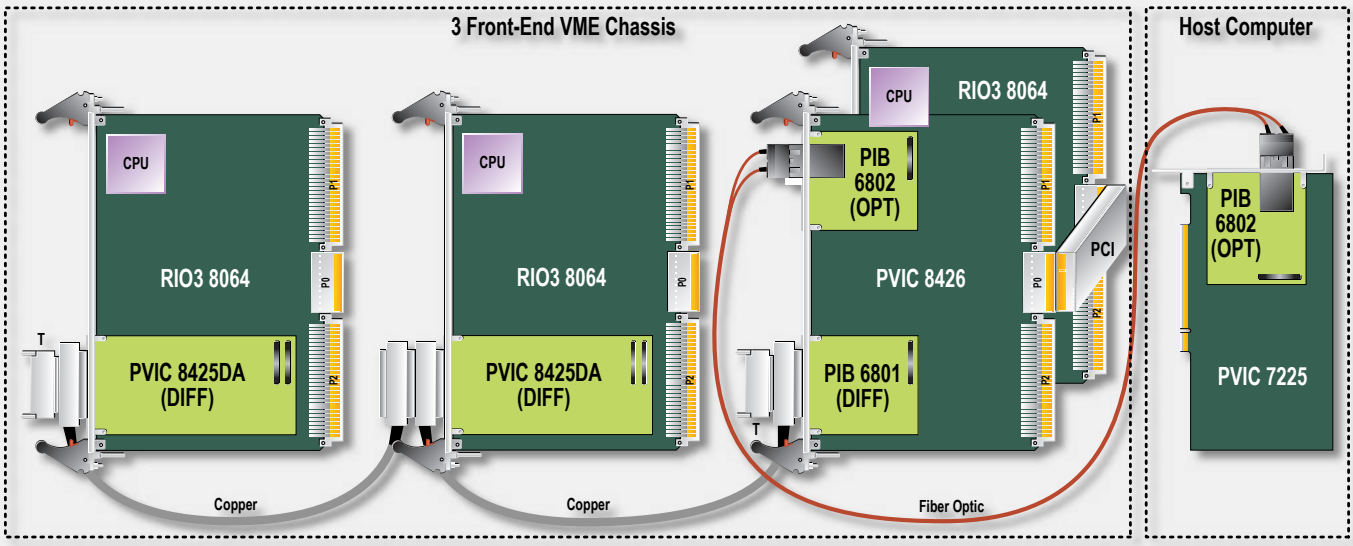
For distances up to 200 meters (1.5 GBits/s). Interconnected with a 850 nm multi-mode fiber, which is equipped with standard SC connectors.



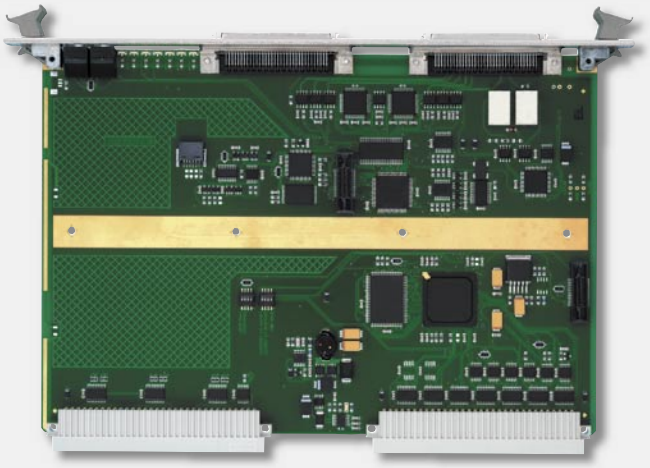
Host PC to VME without processor



Host PC to custom PMC carrier



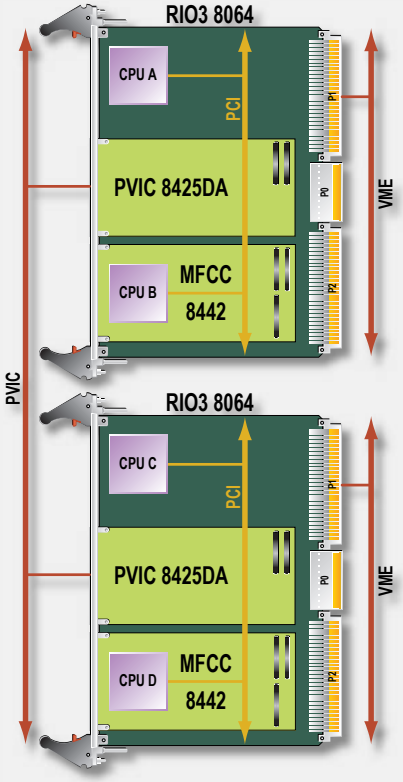
Host to multiple VME chassis with processors in each chassis

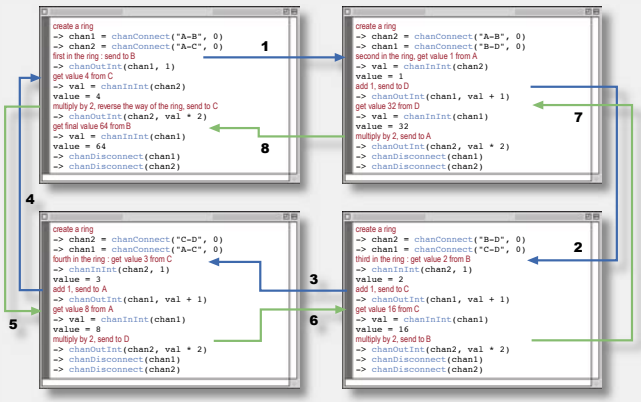


PVIC 8026 - VME-TO-VME VIC-BASED CONNECTION

The PVIC 8026 is a VME board that allows transparent VME-to-VME connections, which are function-compatible with the VICbus family. Although, the PVIC 8026 uses the modern PVIC link technology. It features the following:

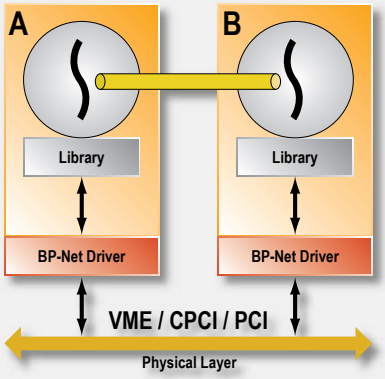
> VME-to-VME transparent link
> VME master / slave interface VME Rev D
> MBLT support in slave mode
> Connects up to fifteen chassis in a multi-drop / multi-master
> Transmission medium on a 68-pin twisted pair cable with LVDS technology
> Simple memory-mapped connections through scatter / gather
> SCSI II cables and connectors





Four processors exchanging messages via CES BP-Net over PCI and VME in a transparent manner:

> **CPU A is a RIO3 board**
> **CPU B is a MFCC plugged on CPU A**
> **CPU C is another RIO3 board**
> **CPU D is another MFCC plugged on CPU C**



CES BP-Net Block Diagram

NETWORK PROTOCOLS

Network services including TCP/IP, which offers services such as NFS, FTP, remote login, etc. and a high-speed connection-oriented protocol, may be used over VME, CompactPCI and PCI using the BP-Net software package.

Using BP-Net to Transfer Data

An application based on several processors linked with a PCI bus can use CES BP-Net to exchange data and synchronize processors at a very high-speed. CES BP-Net furnishes all of the features needed to use the bus, lifting the burden of DMA programming, interrupt management, mapping, alignment and error handling from the user.

It offers three types of services to ensure efficient communication between CES processors:

> **Inter-process communication:** This mechanism allows the processes of any processor to share resources and preserve the integrity of these resources. It covers the functionalities of remote DMA channels, semaphores and message queues.
> **Efficient and straight-forward message passing system (the channel library):** This functionality is very close to the hardware and fully exploits its potential to optimize the performance (high-speed DMAs).
> **Full TCP/IP stack using the VME, CompactPCI, PCI or PVIC bus as a network device:** This permits an easy development of TCP/IP-based applications, which can be distributed over clusters of CES processor boards. In addition, this gives access to the set of tools associated with TCP/IP (NFS, remote login, etc.) at a very high-speed.

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