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PVIC Systems

PCI-to-PCI Link

User's Manual
DOC 3925A/UM
Version 5.0
October 2001

CREATIVE ELECTRONIC SYSTEMS S.A.

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October 25, 2001
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PVIC Systems - PCI-to-PCI Link

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May 2000	Version 4.0	Integration of PVIC 8425 (Differential Nose)
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May 1999	Version 2.0	Integration of the new position of switches (64 and 128 MBytes)
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Chapter 1
Introduction

1.1 General Description

The PVIC is a high bandwidth PCI to PCI transparent connection: remote PCI resources are seen as if they were local (memory mapped).

The PVIC concept has been developed by CES to allow PCI based processors or workstations to be connected into clusters of up to 15 nodes spanning up to 200 meters. While preserving the full PCI throughput (132 MBytes/sec at 32-bit, 33 MHz) for block accesses, the transparent mapping of remote PCI addresses minimizes latencies and drastically reduces the software overhead.

An integrated DMA controller allows performing complex data transactions with minimal CPU load. Broadcast and multicast cycles, interrupt dispatching, mailboxes, a mirrored memory and global semaphores provide the hardware support for efficient interprocessor communication.

PVIC General Features

- Full 32-bit PCI interface (33 MHz)
- Transparent bus-to-bus supporting Byte, Word, Lword and Burst
- Up to 15 PVIC nodes
- PVIC at 132 MBytes/s bandwidth (16-bit bus @ 66 MHz)
- Architecture similar to VIC system
- Mixed transmission technology:

    - GTL
        - Up to 1 meter, low-cost, low-power for in-crate connection
        - Up to 2 meters for point-to-point connection
        - Ribbon flat cable with SCSI II type connector

    - DIFF
        - Differential PECL up to 30 meters at 33 MHz or 15 meters at 66 MHz
        - Shielded SCSI III cable with screwed connectors

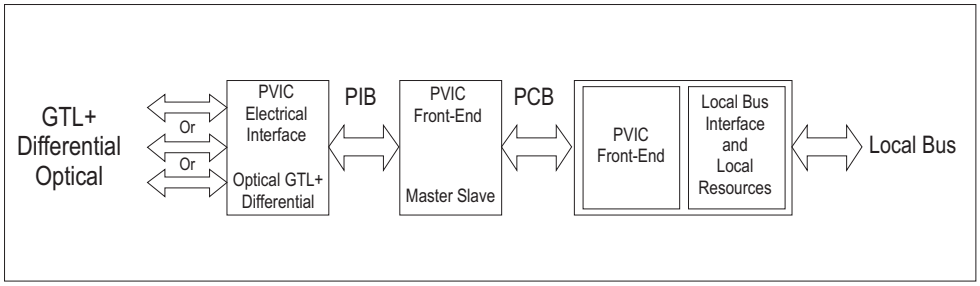
    - ODL
        - 1.5-Gbit/s Optical fiber up to 200 meters
        - Fully transparent

- Three transmission media living together in same system
- Embedded DMA controller for fast data movement
- 64 chaining list entry DMA Request FIFO
- Linked DMA chaining list support
- Full PCI and PVIC bandwidth
- Local bus to PVIC through selectable windows
- Out-going scatter / gather with 64 KBytes pages
- Write posting and read prefetch
- Large and multiple write-buffer & read-buffer
- Interrupt routing and dispatching between the nodes

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- Onboard mirrored memory (MM)
- Global semaphore with reservation
- 512-mailbox for local interrupt on memory modification
- 512-message queue for mailbox modified

Figure 1.1: PVIC Node Block Diagram



The block diagram above shows the functional building blocks of the PVIC. The PVIC interface is connected to the local bus - PCI, VME or CompactPCI - through the local bus interface. The different PVIC electrical interfaces are implemented on piggybacks (PIB) that can be exchanged from case to case to fit the user requirements.

1.2 The PVIC Product Family

The PVIC family is declined in the following interfaces:

PVIC 8025 VME 6U

VME master / slave interface supporting block mode. Allows a PCI device to directly read / write remote VME resources.

PVIC 4025 / 4425 CompactPCI 6U / 3U

CompactPCI initiator / target interface supporting block mode. Allows a PCI device to directly read / write remote CompactPCI resources.

PVIC 7225 PCI short format

Allows user to connect remote VME / CompactPCI / PCI based workstations to a PCI based workstation.

PVIC 8425 PMC

Used as second "backplane" within a VME or CompactPCI crate.

PVIC 8426 VME 6U

PVIC to PVIC gateway allows user to mix different PVIC transmission media within a system.

The different PVIC electrical interfaces are implemented on piggybacks (PIB) which can be exchanged from case to case to fit the user requirements. The exception is the PVIC 8425 which only supports the GTL+ and DIFF technology mounted directly on the PMC board. The main characteristics of all PVIC interfaces are shown below.

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Table 1-1: PVIC Interfaces Characteristics

PVIC Interface	PVIC Busses (Bridge)	Local Bus			PVIC bus technology		
		PCI	VME	CompactPCI	GTL+	DIFF	OPT
PVIC 4025	1			6U	√	√	√
PVIC 4425	1			3U	√	√	√
PVIC 7225	1	Short Format			√	√	√
PVIC 8025	1		6U		√	√	√
PVIC 8425	1	PMC			√	√	
PVIC 8426	2	PCI Extension			√	√	√

Depending on the PVIC technology different PVIC PIBs, cables and terminators are required.

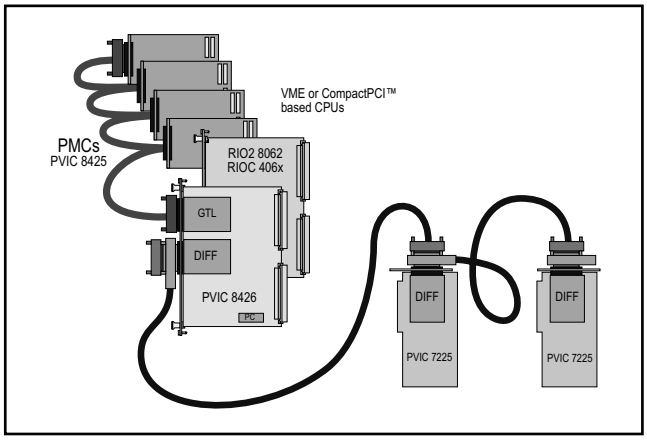
Table 1-2: PVIC Bus Description

PVIC bus technology	PIB	Cable	Terminator	PVIC interfaces supported
GTL+	6800A0	6502x0	6226A0	4025, 4425, 8025, 8426
GTL+	6800B0	6502x0	6226A0	7225
GTL+	onboard	6502x0	6226A0	8425
DIFF	6801A0	6500x0	6225A0	4025, 4425, 8025, 8426
DIFF	6801B0	6500x0	6225A0	7225
DIFF	onboard	6500x0	6225A0	8425D
OPT	6802A0	6727x0		4025, 4425, 8025, 8426
OPT	6802B0	6727x0		7225

1.3 PVIC Implementation Examples

Any type of interface can be mixed in a PVIC system.

Figure 1.2: PVIC System



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1.4 Documentation Organization

This document is common to all PVIC interfaces:

Chapter 2 gives a description of the PVIC resources common to all PVIC interfaces.
Chapter 3 describes the PVIC Master interface common to all PVIC interfaces.
Chapter 4 describes the PVIC Slave interface common to all PVIC interfaces.
Chapter 5 explains the PVIC Mirrored Memory, which is common to all PVIC interfaces.
Chapter 6 gives information about the PVIC DMA controller present on all PVIC interfaces.
Chapter 7 describes the PVIC interrupt dispatching mechanism for all PVIC interfaces.
Chapters 8 to 12 presents PVIC hardware interface specific information like mechanical and technical specifications, motherboard layout and switch settings.
Chapter 13 deals with PVIC PIBs, cables and terminators. It also describes the cabling rules.
Chapter 14 explains how to install a PVIC interface.

The description of all registers in this manual is given mainly for debug purposes or for users who want to write their own PVIC library or to learn more about PVIC transfers mechanisms.

1.5 PVIC Software and Online Documentation

The PVIC software comes with a Generic PVIC Software Library that includes:

- Full featured generic PVIC software library.
- Example programs for PVIC initialization and operation.
- Hyper-linked online documentation for easy navigation.
- More detailed information about PVIC features and operation.



We strongly encourage the user to access all functions of the PVIC system through the CES generic library and invite you to refer to the CES PVIC Library Online Documentation.

Please checkout the README file in the main directory of the Generic PVIC Software Library tree for further instructions.

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Chapter 2. PVIC Resources

2.1 Introduction

The PVIC has control and status registers, SSRAM and mirrored memory. These resources are common to all PVIC interfaces: 4025, 4425, 7225, 8025, 8425, 8426.

The PVIC resources are mapped on the PCI bus through two independent spaces:

- PCI configuration space
- PCI memory space.

These spaces are automatically mapped at power-on by the local CPU firmware. Please refer to the local CPU firmware manual for more information concerning the mapping of PCI resources (PPCMon manual, LynxOS or VxWorks BSP manual in case of CES processors).

2.2 PCI CONFIG Mapping

Table 2-1: PCI Config Mapping

Offset	*31:24*	*23:16*	*15:8*	*7:0*
0x00	Device Id		Vendor Id	
0x04	Status		Command	
0x08	Base_Class	Sub_Class	Programming IF	Rev. ID
0x0C	BIST Reg	Header Type	Latency Timer	Cache Line Size
0x10	PCI MEMORY Base Address			
0x14 - 0x38	Not Implemented			
0x3C	Max LAT Line	Min GNT Reg	Int Pin Reg	Int Line Reg
0x40 - 0x7C	Reserved			
0x80	PVIC CSR3	PVIC CSR2	PVIC CSR1	PVIC CSR0
0x84	Reserved			
0x88	Reserved		PVIC CSR4	
0x8C - 0xBC	Reserved			
0xC0	PVIC DMA S0			
0xC4	PVIC DMA S1			

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Table 2-1: PCI Config Mapping

Offset	*31:24*	*23:16*	*15:8*	*7:0*
0xC8	PVIC DMA S2			
0xCC	Reserved			
0xD0	Reserved	PVIC-RIUS	PVIC-RMI	PVIC-RIR
0xD4 - 0xFC	Reserved			

Accesses to PCI CONFIG registers can only be done in single beat transfers (no burst mode allowed).

2.3 PCI MEMORY Mapping

The size of the PCI MEMORY window can be hardware-selected (32 to 256 MBytes) with two micro-switches located on the PVIC motherboard:

Table 2-2: PCI Memory Window Size Selection

SW1	*SW2*	*Window Size*
OFF	OFF	32 MBytes
ON	OFF	64 MBytes
OFF	ON	128 MBytes
ON	ON	256 MBytes

Accesses to the first sub-window of the PCI MEMORY (0x0000'0000 to 0x0003'FFFF) can only be done in single-beat transfers (no burst mode allowed).

The standard out-going pages (0x0004'0000 to 0x0FFF'FFFF) support PCI burst access.

Table 2-3: PCI Memory Mapping

Offset	*31:24*	*23:16*	*15:8*	*7:0*
0x0000'0000	Device Id		Vendor Id	
0x0000'0004	Status		Command	
0x0000'0008	Base_Class	Sub_Class	Programming IF	Rev. ID
0x0000'000C	BIST Reg	Header Type	Latency Timer	Cache Line
0x0000'0010	PCI MEMORY Base Address			
0x0000'0014 - 0x0000'0038	Not Implemented			
0x0000'003C	Max LAT Reg	Min GNT Reg	Int Pin Reg	Int Line Reg
0x0000'0040 - 0x0000'0076	Reserved			
0x0000'0080	PVIC CSR3	PVIC CSR2	PVIC CSR1	PVIC CSR0
0x0000'0084	Reserved			
0x0000'0088	Reserved		PVIC CSR4	
0x0000'008C - 0x0000'00BC	Reserved			
0x0000'00C0	PVIC DMA S0			
0x0000'00C4	PVIC DMA S1			

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Table 2-3: PCI Memory Mapping

Offset	31:24	23:16	15:8	7:0
0x0000'00C8	PVIC DMA S2			
0x0000'00CC	Reserved			
0x0000'00D0	Reserved	PVIC RIUS	PVIC RMI	PVIC RIR
0x0000'00D4 - 0x0001'FFFC	Reserved			
0x0002'0000 - 0x0003'FFFC	SSRAM			
0x0004'0000 - 0x0004'FFFC	Out-Going Page # 0x4			
0x0005'0000 - 0x0005'FFFC	Out-Going Page # 0x5			
0x0006'0000 - 0x01FF'FFFC	Out-Going Page # 0x6 to 0x1FF			
0x0200'0000 - 0x03FF'FFFC	Out-Going Page # 0x200 to 0x3FF only if PCI MEMORY Window] 32 MBytes			
0x0400'0000 - 0x07FF'FFFC	Out-Going Page # 0x400 to 0x7FF only if PCI MEMORY Window] 64 MBytes			
0x0800'0000 - 0x0FFF'FFFC	Out-Going Page # 0x800 to 0xFFF only if PCI MEMORY Window] 128 MBytes			

2.4 PCI CONFIG Registers

Table 2-4: PCI Vendor ID Register (offset + 0x0)

Bits	Mode	Name	Description
[15:00]	R	Vendor ID	This register contains CES Vendor ID (0x10D9)

Table 2-5: PCI Device ID Register (offset + 0x2)

Bits	Mode	Name	Description
[5:00]	R	Device ID	This register contains the Vendor ID of CES PVIC Interfaces: PVIC 4025: 0x4025 PVIC 7225: 0x7225 PVIC 8425: 0x8425 PVIC 8426: 0x8426

Table 2-6: PCI Command Register (offset + 0x4)

Bits	Mode	Name	Description
[15:10]	R	Reserved	Read as 0x000
[09]	R	FBTB_E	Fast back to back disabled Read as 0

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Table 2-6: PCI Command Register (offset + 0x4)

Bits	Mode	Name	Description
[08]	R / W	SERR_E	SERR Enable. This control bit enables the System Error interrupt. Value at RESET = 0
[07]	R	Reserved	Read as 0
[06]	R	PERR_E	PERR Enable, Read as 0
[05]	R	VGA_Snoop	Not used, Read as 0
[04]	R	MWI_E	Memory Write & Invalidate Enable. Not used, Read as 0
[03]	R	SCYC_E	Special Cycle Enable. Not used, Read as 0
[02]	R / W	BM_E	PCI Bus Master Enable. This bit must be set while the local DMA is used or for PVIC to Local Bus cycle. Value at RESET = 0
[01]	R / W	MEM_E	PCI Memory Space Access Enable. This control bit enable the PCI Slave decoding. This bit must be set only after initialization of PCI Memory Base Register. Value at RESET = 0
[00]	R	IO_E	PCI IO Space Access Enable. Not used, Read as 0
[15:10]	R	Reserved	Read as 0x000

Table 2-7: PCI Status Register (offset + 0x6)

Bits	Mode	Name	Description
[15]	R	PERR	Not used, Read as 0
[14]	R / W	SERR	System Error signaled. This bit is set while the unit is driving SERR. (in case of Direct-Write error detection). This bit is cleared when set to . Value at RESET = 0
[13]	R / W	Rx_MABO	Receive PCI Master Abort. This bit is set when the unit terminates a master cycle with a master abort sequence. This bit is cleared when set to 1. Value at RESET = 0
[12]	R / W	Rx_TABO	Receive PCI Target Abort. This bit is set when a target terminates a master cycle with a target abort sequence. This bit is cleared when set to 1. Value at RESET = 0
[11]	R / W	Tx_TABO	Send Target Abort. This bit is set when the unit terminate a PCI Slave cycle with target abort. This bit is cleared when set to 1. Value at RESET = 0
[10:09]	R	DEVSEL[01:00]	This 2-bit field specify the access time category. Read as “01” (medium).
[08]	R	DPERR	Not implemented, Read as 0
[07]	R	RFBTBC	Fast back to back capable. Not used, Read as 0
[06:00]	R	Reserved	Not used, Read as 0
[15]	R	PERR	Not used, Read as 0

Table 2-8: PCI Revision ID Register (offset + 0x8)

Bits	Mode	Name	Description
[07:00]	R	Rev_ID	Hardware Revision. This 8-bit field indicates current unit hardware revision. (Initial version = 0x01)

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Table 2-9: PCI Programming Interface Register (offset + 0x9)

Bits	Mode	Name	Description
[07:00]	R	Prog_IF	Not used, Read as 0

Table 2-10: PCI Sub-Class Register (offset + 0xA)

Bits	Mode	Name	Description
[07:00]	R	Sub_Class	Not used, Read as 0

Table 2-11: PCI Base-Class Register (offset + 0xB)

Bits	Mode	Name	Description
[07:00]	R	Base_Class	Not used, Read as 0

Table 2-12: PCI Cache Line Size (offset + 0xC)

Bits	Mode	Name	Description
[07:00]	R	Cache Line Size	Not used, Read as 0

Table 2-13: PCI Latency Timer Register (offset + 0xD)

Bits	Mode	Name	Description
[07:04]	R / W	LAT	This 5-bit field determines the latency timer value used in PCI Master transaction. Value at RESET = 00000
[03:00]	R	Not implemented	Read as 0

Table 2-14: PCI Header Type Register (offset + 0xE)

Bits	Mode	Name	Description
[07]	R	FUNCT	Not used, Read as 0
[06:00]	R	LAYOUT	Not used, Read as 0

Table 2-15: PCI BIST Register (offset + 0xF)

Bits	Mode	Name	Description
[07:00]	R	Not implemented	Not used, Read as 0

Table 2-16: PCI MEMORY Base Address Register (offset + 0x10)

Bits	Mode	Name	Description
[31:28]	R / W	BASE	Top Memory Space Base address
[27:26]	R / W		Intermediate field conditioned by external static option defining the window size used. (32 or 64 or 128 or 256 MBytes)

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Table 2-16: PCI MEMORY Base Address Register (offset + 0x10)

Bits	Mode	Name	Description
[25:04]	R		Fixed base for minimum of 32 MBytes
[03]	R	PREFETCH	Prefetchable. This status bit is set to indicate prefetch capability. Read as 1
[02:01]	R	TYPE	This 2-bit field indicates to locate anywhere in 32-bit address space. Read as 00
[00]	R	MEM_Space	Read as 0 indicating that this register specify a PCI Memory base address.

The PCI memory window size can be selected via DIP-Switches (refer to section 8.3 and section 12.3).

Table 2-17: PCI Interrupt Line Register (offset + 0x3C)

Bits	Mode	Name	Description
[07:00]	R / W	INTL	8-bit Read / Write Register reserved for software Value at RESET = 0x00

Table 2-18: PCI Interrupt Pin Register (offset + 0x3D)

Bits	Mode	Name	Description
[07:00]	R	INTP	Read as 0x01 for INTA# signaling

Table 2-19: PCI MIN_GNT Register (offset + 0x3E)

Bits	Mode	Name	Description
[07:00]	R	MIN_GNT	Not used, Read as 0x00

Table 2-20: PCI MAX_LAT Register (offset + 0x3F)

Bits	Mode	Name	Description
[07:00]	R	MAX_LAT	Not used, Read as 0x00

The other PCI Configuration Register 0x40 to 0xFF are allocated as follows:

0x40 : 0x7F: Not implemented
0x80 : 0xBF: Local PVIC CSR Registers
0xC0 : 0xFF: Local PVIC DMA & INTC Registers

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2.5 PVIC Control Status Registers

Table 2-21: PVIC_CSR0 PVIC Static Options (offset + 0x80)

Bits	Mode	Name	Description
[07]	R	PVIC Timing Initialized	PVIC Timing Register loaded. Until this bit is set the PVIC Master interface is disabled. 0: PVIC Timing not initialized 1: PVIC Timing initialized. PVIC Monarch has loaded the global PVIC Timing Register.
[06]	R / W	Long_RESET	This bit allows issuing a PVIC Long_RESET. A software SET-CLEAR sequence must be used. It is enabled only if the node is the monarch. (Node_ID = 0001)
[05]	R	ptiCLOCK66	This bit reflect PVIC front-end PTI register bit. 0: PVIC front-end is running at 1x local PCI clock 1: PVIC front-end is running at 2x local PCI clock
[04]	R	ptiFREQ_NE	This bit reflect PVIC front-end PTI register bit. 0: the PVIC Interfaces run with the same local PCI clock (within 1 %). 1: the PVIC Interfaces run with different local PCI clock (25 to 33 MHz).
[03:00]	R	Node_ID	This 4-bit read-only field gives the status information of the Hex-Rotary switch setting the PVIC Node Number. 0000 value is illegal and 0001 specifies that this node is the PVIC monarch.

Table 2-22: PVIC_CSR1 PVIC Control Register (offset + 0x81)

Bits	Mode	Name	Description
[07]	R	Reserved	Not used
[06]	R	ODL_Status	Status from PVIC ODL Interface
[05:03]	R	MM Size	These bits reflect the MM size implemented 000: 4K x 32 bits 001: 8K x 32 bits 010: 16K x 32 bits 011: 32K x 32 bits 100: 64K x 32 bits 101: 128K x 32 bits 110: 256K x 32 bits 111: 512K x 32 bits
[02]	R / W	PVIC Target Abort Mask	This control bit allows to cancel the READ Target Abort PCI handshake. When set, PCI Read are always acknowledged with Target READY. In case of error, the flag LRERR will be set.
[01]	R / W	PVIC Long RESET detected	This bit is set while a PVIC Long RESET is detected. It remains in this state until is cleared by writing 1 over it.
[00]	R	Reserved	Not used

Table 2-23: PVIC_CSR2 PVIC Int Mask Register (offset + 0x82)

Bits	Mode	Name	Description
[07]	R	Reserved	Not used
[06]	R / W	LRERR_Mask	Local READ Error Interrupt Enable. When set, LRERR flag generates a PCI INTA# interrupt and also a SERR# if the SERR_E control bit is set.
[04:05]	R	Reserved	Not used

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Table 2-23: PVIC_CSR2 PVIC Int Mask Register (offset + 0x82)

Bits	Mode	Name	Description
[03]	R / W	RWERR_Mask	Remote WRITE Error Interrupt Enable. When set, RWERR flag generates a PCI INTA# interrupt and also a SERR# if the SERR_E control bit is set.
[02]	R / W	LWERR_Mask	Local WRITE Error Interrupt Enable. When set, LWERR flag generates a PCI INTA# interrupt and also a SERR# if the SERR_E control bit is set.
[01]	R / W	FIFO_Ena	MM Message FIFO Enable. 0: FIFO disabled (reset) 1: FIFO enabled Value at RESET = 0
[00]	R / W	FIFO_Mask	MM Message FIFO Interrupt enables 0: Interrupt disabled 1: Interrupt enabled Value at RESET = 0

Table 2-24: PVIC_CSR3 PVIC Int Status Register (offset + 0x83)

Bits	Mode	Name	Description
[07]	R	Reserved	Not used
[06]	R / W	LRERR_Intfl	Local READ Error Flag. While set, a local to PVIC Read was aborted. This flag is cleared when set to 1.
[05:04]	R	MEM_Size[1:0]	PCI Memory Windows size. 00: 32 MBytes 01: 64 MBytes 10: 126 MBytes 11: 256 MBytes
[03]	R / W	RWERR_Intfl	Remote WRITE Error Flag. While set, a PVIC to Local Write was aborted. This flag is cleared when set to 1.
[02]	R / W	LWERR_Intfl	Local WRITE Error Flag. While set, a local to PVIC Write was aborted. This flag can be clear by writing 1 over it.
[01]	R	Reserved	Not used
[00]	R / W	FIFO_Int	MM Message FIFO Interrupt status. 0: Interrupt inactive (FIFO empty) 1: Interrupt active (FIFO not empty)

Table 2-25: PVIC_CSR4 PVIC FIFO Register (offset + 0x88)

Bits	Mode	Name	Description
[09:31]	R	Reserved	Not used
[08:00]	R	Top MM Address	Message FIFO. Read to this register access the Message FIFO. This 9-bit field supplies the 9 lower MM's address.

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Other PVIC Registers

PVIC registers dedicated to the PVIC DMA Controller and to the Remote Interrupt Dispatching are described on chapter 6 and 7.

Table 2-26: Other PVIC Registers

Name	*Description*	*Address*
PVIC_DMAS0	DMAC Control & Status	(offset + 0xC0)
PVIC_DMAS1	DMAC Exception Status	(offset + 0xC4)
PVIC_DMAS2	DMAC Request FIFO	(offset + 0xC8)
PVIC_RIR	Remote Interrupt Request	(offset + 0xD0)
PVIC_RMI	Remote Interrupt Mask	(offset + 0xD1)
PVIC_RIUS	Remote Interrupt Under-Service	(offset + 0xD2)

PVIC SSRAM

The PVIC local 128 KBytes Synchronous SSRAM is implemented to store PVIC specific data for the Out-going and incoming scatter / gather, the DMA Chaining Block Lists and the Remote Interrupt Dispatching.

The SSRAM is mapped on the PCI Memory space window for local access and also on the PVIC Slave port for remote PVIC Node access. The SSRAM is organized as listed in the table 2-27.

Table 2-27: PVIC SSRAM

SSRAM Base +	*Function*
0x0'0000 - 0x0'000F	Reserved
0x0'0010 - 0x0'3FFF	Out-going scatter / gather page descriptors
0x0'4000 - 0x0'7FFF	In-going scatter / gather page descriptors
0x0'8000 - 0x1'FDFF	DMA chaining block descriptors
0x1'FE00 - 0x1'FEFF	DMA specific interrupt dispatching control blocks
0x1'FF00 - 0x1'FF7F	Reserved for PVIC system initialization
0x1'FF80 - 0x1'FFFF	PCI specific interrupt dispatching control blocks

The unused space e.g. for the out-going scatter / gather or the DMA chaining block descriptors can also be used as general-purpose user SSRAM area.



The SSRAM must be accessed in Single-Beat mode (PCI burst mode is not allowed).

2.6 PVIC Mirrored Memory

The PVIC local Mirrored Memory (MM) is implemented with a true dual-port SRAM (DPRM) device. Throughout this manual the word Mirrored Memory or MM is used for this device. Reflective Memory is also a frequently used name.

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The Mirrored Memory is organized as follows:

Table 2-28: PVIC Mirrored Memory

MM Base +	*Function*	*Note*
0x0'0000 - 0x0'0FFF	LWB #0-7 Data	8 Local to PVIC Write Buffers
0x0'1000 - 0x0'1FFF	VWB #0-7 Data	8 PVIC to Local Write Buffers
0x0'2000 - 0x0'21FF	RRB Data	Read Request Buffer
0x0'2200 - 0x0'23FF	RAB Data	Read Acknowledge Buffer
0x0'2400 - 0x0'24FF	LWB #0-7 Header	8 Local to PVIC Writes Buffers
0x0'2500 - 0x0'25FF	VWB #0-7 Header	8 PVIC to Local Write Buffers
0x0'2600 - 0x0'261F	RRB Header	READ Request Buffer
0x0'2620 - 0x0'263F	RAB Header	READ Acknowledge Buffer
0x0'2640 - 0x0'26FF	Reserved	Reserved for global configuration
0x0'2700 - 0x0'270F	HLWB	Local to PVIC MM High Priority WB
0x0'2710 - 0x0'27FF	Reserved	Reserved for global configuration
0x0'2800 - 0x0'28FF	RWB #0-15	16 Local to PVIC MM Write Buffers
0x0'2900 - 0x0'7FFF	User Mirrored Memory	Standard Size (32 KBytes)
0x0'8000 - 0xF'7FFF	User Mirrored Memory	Extended Size (up to 2 MBytes)



WARNING

The first part of the PVIC Mirrored Memory is used by the PVIC system to hold the PVIC Write and Read Buffers. Writing to this area is strictly forbidden and is likely to provoke unexpected and delayed malfunctions of the PVIC system.

The remaining Mirrored Memory starting from offset 0x0'2900 is available for the user.

The MM is not mapped directly on the PCI Memory space window. Access to MM must actually be handled through the out-going scatter / gather (refer to section 3.1). It can be mapped anywhere in the PCI Memory space window with three different access methods:

1. Debug Access Local Read & Local Write
2. Normal Access Local Read & Global Write
3. Global Reservation Global Read with Reservation & Global Write



NOTE

The Mirrored Memory must be accessed in Single-Beat mode (PCI burst mode is not allowed).

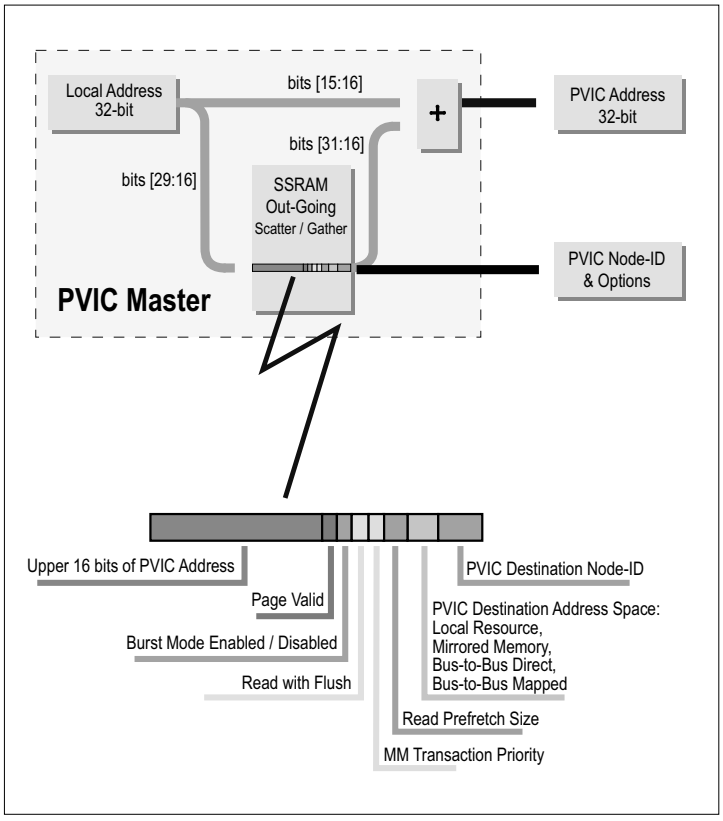
The PVIC Mirrored Memory is described in more detail in chapter 5.

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Chapter 3
PVIC Master Interface

The Local-Bus to PVIC Bridge is controlled through an outgoing scatter / gather. This mechanism, similar to a MMU, allows the complete remapping of the local addressing schema to the PVIC addressing. The PVIC uses a PCI Memory Space window of 32 to 256 MBytes. This window is tailored in 64 KBytes pages (4092 x 64K). Each individual page is associated with a page descriptor supplying the PVIC page parameters.

Figure 3.1: PVIC Master Block Diagram



PVIC out-going page initialization can be done at a software load directly using CES PVIC library instead of at a bit-level as described in this section. Please refer to the PVIC Library Online Documentation.

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3.1 Out-Going Scatter / Gather

The out-going scatter / gather page descriptors are stored in the first 16 KBytes of the SSRAM:

Table 3-1: Out-Going Scatter / Gather

SSRAM Base +	*Function*	*Comments*
0x0'0010	Page-Descriptor for page remapping from 0x004'0000 to 0x004'FFFF	1st user page available.
0x0'0014	Page-Descriptor for page remapping from 0x005'0000 to 0x005'FFFF	2nd user page available.
0x0'3FF8	Page-Descriptor for page remapping from 0xFFE'0000 to 0xFFE'FFFF	...
0x0'3FFC	Page-Descriptor for page remapping from 0xFFF'0000 to 0xFFF'FFFF	Last user page available.



The first 4 pages are used by the PVIC system and the user should not touch or modify them.

A 32-bit page descriptor is encoded as follows:

Table 3-2: Out-Going Scatter / Gather Page Description

Bit#	*Function*	*Comments*
[16:31]	PVIC High Address	PVIC High addresses. This 16-bit field will replace the local bus high address in the PVIC cycle.
[15]	Page VALID	Page entry enable/disable 0 : Invalid page entry (immediate PCI Target Abort) 1 : Valid page entry
[14]	RD-Flush	READ with Flush. This bit allows forcing a flushing of the write-buffer before the READ execution.
[13]	PVIC MM Priority	PVIC Bus Arbitration priority for MM transaction 0 : Low Priority 1 : High Priority
[12]	No_BURST	Disable the local PCI Bus burst capability.
[11:10]	PVIC RPF	PVIC Read Prefetch. This 2-bit field encode the prefetch size in case of local READ burst 00 : 8 words 01 : 16 words 10 : 32 words 11 : 64 words
[09:08]	PVIC-CSpace	This 2-bit field specifies the PVIC destination Space. 00 : PVIC Local resource 01 : PVIC Mirrored Memory 10 : PVIC Bus to Bus DIRECT 11 : PVIC Bus to Bus MAPPED
[07:04]	PVIC-DSpace	PVIC Destination Bus Space. This 4-bit field specifies the destination address space as IO, MEMORY, CONFIG, etc.
[03:00]	PVIC Node_ID Destination	This 4-bit field encodes the PVIC destination node.

The **Node_ID** defines the PVIC destination node. When set to “0000”, PVIC broadcast cycles are generated and therefore reads to this page are rejected on the local PCI Bus (acknowledged with a PCI Target Abort). Moreover broadcast is not authorized with CSpace = "00" (PVIC Local Resources). The self-addressing (Node_ID = local Node_ID) is accepted only for CSpace = "01" (PVIC MM) allowing the local DMA Controller to issue a MM Message FIFO cycle for interrupt generation. When the broadcast is selected with CSpace = "1x" (PVIC Bus to Bus) the PVIC Master Interface issues special Write cycles. These cycles assure that all PVIC nodes are receiving the cycle in their VWB write-buffer (see section 2.6).

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The **CSpace** is encoding the PVIC cycle type. Four types are supported:

Table 3-3: CSpace Encoding

Type	Description
CSpace = 00	Used to access remote PVIC local resources as CSR Register, DMAC Registers, and SSRAM. When selected the bit No_BURST must be set to force single beat transaction.
CSpace = 01	Used to access the Mirrored Memory (MM) on the PVIC port side. When selected the bit No_BURST must be set to force single beat transaction.
CSpace = 10	Used to access resources located on the remote PVIC Node's local bus (Bus to Bus transaction). The destination Bus address is DIRECT, as built locally by the out-going scatter / gather.
CSpace = 11	Used like the previous one except that the destination Bus address is MAPPED. The final address is remapped by the remote in-going scatter / gather. Remapping is allowed in 4 KBytes page size.

DSpace with CSpace = 00

Allows remote access to local resources. During normal runtime always DSpace = 0000, but on start-up, the monarch uses different DSpace values to scan and configure the system.

Table 3-4: DSpace with CSpace = 0 Encoding

DSpace	*Used for*
0000	Normal runtime
0001	GTL+ daughter card installed on port A
0010	DIFF daughter card installed on port A
0011	ODL daughter card installed on port A
0100	Reserved
0101	GTL+ daughter card installed on port B
0110	DIFF daughter card installed on port B
0111	ODL daughter card installed on port B
1000	Capable of 264 MHz PVIC transactions
1001	Capable of 132 MHz PVIC transactions
1010	Capable of 66 MHz PVIC transactions
1011	Capable of 33 MHz PVIC transactions
1100	PVIC Terminator installed on port A
1101	PVIC Terminator installed on port B
1110	PVIC card is present
1111	Accessing PVIC timing register



Remote accesses to local resources have to be done in Single-Beat mode (No_BURST set).

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DSpace with CSpace = 01

Allows remote access to Mirrored Memory (MM).

Table 3-5: DSpace with CSpace = 01 Encoding

DSpace	*Used for*
0000	Normal MM : write global / read local
0001	MM Global Reservation : write global / read local - set global
0010	Debug MM: write local / read local
0011 - 1111	Reserved

A read access to Normal MM (a page with CSpace = 01 and DSpace = 0000) is in practice a read of a local resource accessed through scatter / gather.

A read access to MM Global Reservation (a page with CSpace = 01 and DSpace = 0001) initiates a PVIC Read Request that is treated in a special way by the PVIC front-end logic (see chapter 5).

Write accesses to both spaces are treated identically - a single node or broadcast MM write.

DSpace with CSpace = 10 or 11

The DSpace encodes the destination bus address spaces (PCI Spaces). This information is used in bus to bus transactions (DIRECT or MAPPED). The following table gives the encoding for the PCI target bus.

Table 3-6: DSpace with CSpace = 10 or 11 Encoding

DSpace	*PCI Interface*	
	CBE[03:00]	ADD Space
0000	000x	IACK-Space
0001		Reserved
0010	001x	IO-Space
0011		Reserved
0100	010x	Reserved
0101		Reserved
0110	011x	MEM-Space
0111		Reserved
1000	100x	Reserved
1001		Reserved
1010	101x	CONFIG-Space
1011		Reserved
1100	110x	MEM-MULTIPLE-Space
1101		Reserved
1110	111x	MEM-LINE Space
1111		Reserved

The local PCI interface is using DSpace[03...02] to control the address boundary disconnect.

DSpace[03:02] = 00,01,10 : 256 Bytes address boundary disconnect
DSpace[03:02] = 11 : 1024 Bytes address boundary disconnect

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The **RPF** allows selecting the PVIC prefetch size in case of local PCI burst read. The prefetch improves the PVIC burst read performance. If the prefetch is not recommended (sideband effect) it is possible to disable it by setting the bit No_BURST. The prefetch logic verifies that there is no cross over 256 Bytes address boundary.

The **PRIORITY** defines the PVIC Arbitration request priority. When set the current page will use the high-priority bus request. It is only valid for MM transactions.

The **RD-Flush** allows user-control over Write-Buffer flushing while a read is pending. When set, this bit has the following impact on the local PVIC interface and on the PVIC Slave interface (see also section 2.6):

- Wait until all LWB are flushed
- Refuse any Local Bus Write to the LWB
- Execute the Read Request when the LWB is empty

When it is reset, the Read has priority over the Write Buffer (PVIC Slave and PVIC Master) and should result in shorter Read latency.

3.2 PVIC RESET Control

The PVIC protocol implements two RESET mechanisms (CSR0 registers are listed in section 2.5):

The PVIC Short_RESET (assertion of PVIC signal for less than 500 ns) is used to reattribute the arbiter to the monarch. It cannot be issued under software control.

The PVIC Long_RESET(assertion of PVIC signal for more than 1000 ns) is used to reset the PVIC Interface. Its generation has a strong impact on the PVIC interface as:

- It resets the buffer management
- It resets all PVIC CSR Registers

The PVIC Long_RESET can be issued under software control through PVIC CSR0 Register, only if the PVIC node is the monarch (Node_ID = 0001).

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Chapter 4
PVIC Slave Interface

The PVIC slave interface permits access to the PVIC Local Resources (Registers, SSRAM and MM) and the Local PCI bus. It receives and decodes the PVIC transaction. The decoding is handled only through the Node_ID information. Each PVIC Slave owns a unique Node-ID. PVIC Broadcasts are also decoded with Node_ID = 0000.

4.1 PVIC Slave Port Local Resources

The PVIC Slave interface allows mapping of local PVIC resources like SSRAM, DMA Controller and CSR Space. Access to these local resources MUST be done only in PVIC Single-Beat access. Remote access to MM and to the MM message FIFO is not supported.

Table 4-1: PVIC Slave Port Local Resources Mapping

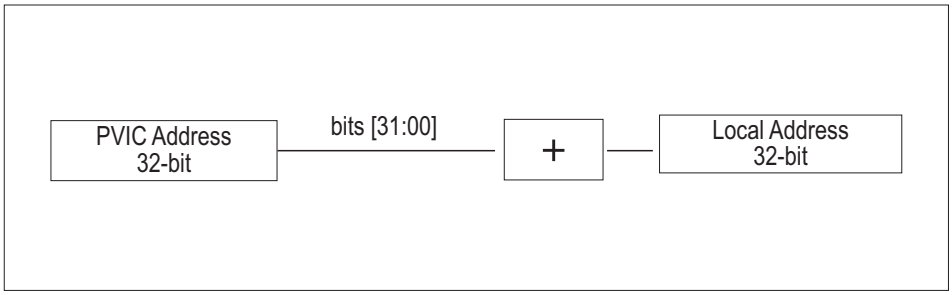
Offset	*31:24*	*23:16*	*15:8*	*7:0*
0x0000'0000 - 0x0000'003C	PCI CONFIG Registers			
0x0000'0040 - 0x0000'007C	Reserved			
0x0000'00080	PVIC CSR3	PVIC CSR2	PVIC CSR1	PVIC CSR0
0x0000'0084	Reserved			
0x0000'0088	Reserved	PVIC CSR4		
0x0000'008C - 0x0000'00BC	Reserved			
0x0000'00C0	PVIC DMA S0			
0x0000'00C4	PVIC DMA S1			
0x0000'00C8	PVIC DMA S2			
0x0000'00CC	Reserved			
0x0000'00D0	Reserved	PVIC RIUS	PVIC RMI	PVIC RIR
0x0000'00D4 - 0x0001'FFFC	Reserved			
0x0002'0000 - 0x0003'FFFC	SSRAM Memory (128 KBytes)			
0x0004'0000 - 0xFFFF'FFFC	CES-reserved			

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4.2 PVIC Slave Bus to Bus DIRECT Addressing

The PVIC Slave Bus to Bus DIRECT uses directly the PVIC address as the Local bus address. The destination bus address must be built by the source out-going scatter / gather.

Figure 4.1: PVIC Slave Bus -to-Bus DIRECT Addressing

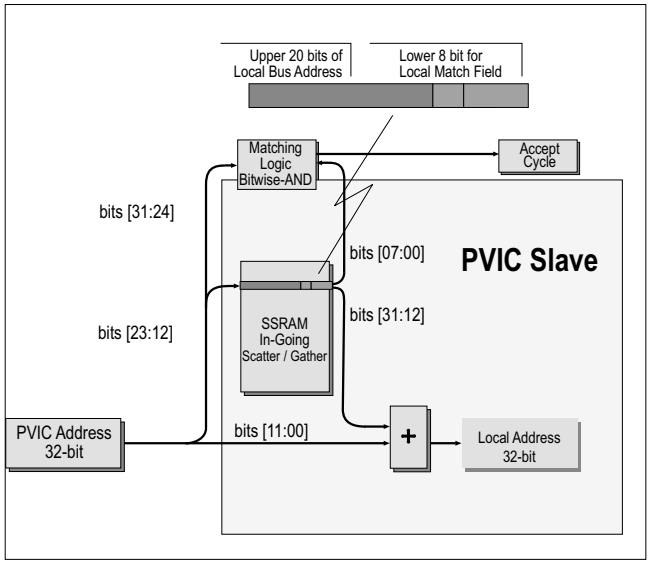


4.3 PVIC Slave Bus to Bus MAPPED Addressing

The PVIC Slave Bus to Bus MAPPED is identical to the previous one except for the local Bus addressing. The PVIC to Local-Bus bridge is controlled through an in-going scatter / gather. This mechanism, similar to a MMU allows the complete remapping of PVIC addressing schema to the local addressing. The PVIC Slave uses a window of 16 MBytes. This window is tailored in 4095 pages, 4 KBytes each. Each individual page is associated to a page descriptor supplying the Local-Bus parameters.

PVIC in-going page initialization can be done at a software load directly using CES PVIC library instead of at a bit-level as described in this section. Please refer to the PVIC library documentation.

Figure 4.2: PVIC Slave for Bus-to-Bus Block Diagram Mapped



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The PVIC Slave Bus to Bus MAPPED logic also incorporates a filtering mechanism to support PVIC Selective Broadcast or Multicast. The PVIC Slave Bus to Bus MAPPED WRITE must have successful MATCH to be processed over the local PCI Bus. In case of no match, the cycle is rejected. The MATCH logic applies only for WRITE.

This filtering mechanism is built with an AND-OR logic match on the following two 8-bit fields.

- Match IN field PVIC Address [31:24]
- Match LOCAL field In-going scatter / gather [07:00]

4.4 In-going Scatter / Gather

The incoming scatter / gather page descriptors are stored in the second 16 KBytes of the SSRAM:

Table 4-2: In-Going Scatter / Gather Pages Mapping

SSRAM Base +	*Function*	*Comments*
0x0'4000	Page Descriptor for page ranging from 0x00'0000 to 0x00'0FFF	1st 4 KBytes page
0x0'4004	Page Descriptor for page ranging from 0x00'1000 to 0x00'1FFF	2nd 4 KBytes page.
0x0'7FF8	Page Descriptor for page ranging from 0xFF'E000 to 0xFF'EFFF	...
0x0'7FFC	Page Descriptor for page ranging from 0xFF'F000 to 0xFF'FFFF	Last 4 KBytes page.

A 32-bit page descriptor is encoded as follows:

Table 4-3: In-Going Scatter / Gather Page Encoding

Bit#	*Function*	*Comments*
[31:12]	Local Bus High Address	Local Bus High address. This 20-bit field will replace the PVIC high address in the Local Bus cycle.
[11:08]	Not used	Low 4 KBytes address.
[07:00]	Match_LOC[07...00]	Local MATCH field.

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Chapter 5
Mirrored Memory

The PVIC Mirrored Memory (MM) allows the building of a shared memory system with Global Write and Local Read. The MM can be mapped with three different access methods by programming the outgoing scatter / gather hardware (refer to section 3.1):

1. Debug Access	Local Read & Local Write
2. Normal Access	Local Read & Global Write
3. Global Reservation	Global Read with Reservation & Global Write

A Local Read or Write will access the MM directly without using the PVIC front-end (bus).

A Global Write to MM is stored temporarily in the MM Write Buffers (RWB). It also writes to local MM. Because the MM write accesses are stored in the RWB write buffers (16 transactions deep), the effective location update occurs a certain time later. This write latency is conditioned by the PVIC occupancy. If required, a software routine should verify with a MM read that the MM write has been completed.

The MM addressing is normally done in broadcast (Node_ID = 0), nevertheless, it is possible to initialize Local to PVIC pages to set-up single cast addressing (Node_ID > 0).

The MM only supports single-beat PCI access, therefore the PCI target interface acknowledges the Initiator with a Target Disconnect in the first data phase.

MM with Global Reservations allows the user to implement atomic operations like semaphore, test-and-set (TAS) function or atomic access to other shared resources. A write to a page setup for MM access with Global Reservation is treated as a Global MM Write. The MM Reservation Read access supplies a status on bit #31 conditioned by the semaphore reservation result:

bit #31 = 0:	Reservation successful. Hardware sets bit #31 set 1 at the addressed MM location.
bit #31 = 1:	Reservation unsuccessful (bit #31 was already set). Hardware leaves the MM addressed location unchanged.

The reservation can be cleared performing a MM write with bit #31 cleared.

5.1 Mirrored Memory Message FIFO

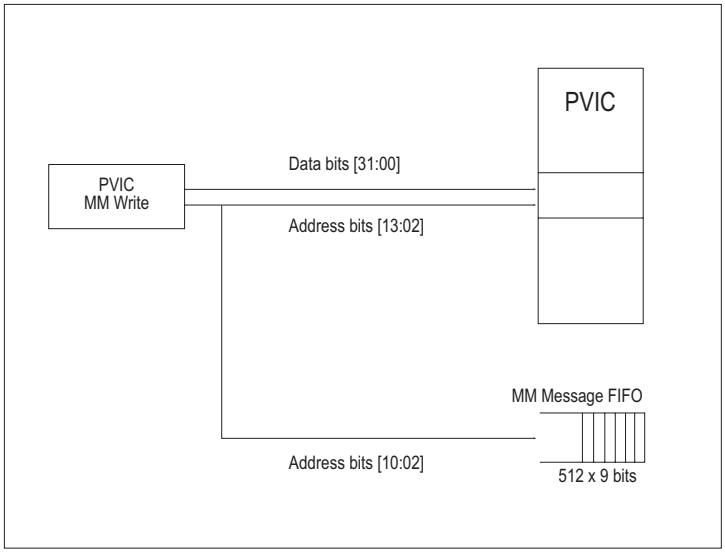
The MM Message FIFO (512 x 9 bits) is implemented in parallel with the Mirrored Memory. When a MM write with PVIC address bit #31 = 1 is issued, the low PVIC address A[10:02] is loaded in the MM Message FIFO while at the same moment the data is written to MM. The MM Message FIFO can hold up to 512 messages.



There is no FIFO watermark. It is the users responsability to avoid the MM Message FIFO to over flow.

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Figure 5.1: Mirrored Memory FIFO Diagram



The FIFO not-empty flag can generate a local interrupt to signal the arrival of messages (Signaled Message Interrupt). The MM Message FIFO interrupt handler must read the MM Message FIFO to get the message location and message content. This mechanism allows simple mailbox-like interrupt dispatching over the PVIC bus. Chapter 7 gives further information about Remote Interrupt Dispatching.

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Chapter 6
DMA Controller

The PVIC interfaces incorporate a DMA controller. This DMA controller provides the following features:

- Local to PVIC DMA
- Support for Read Local, Write PVIC
- DMA Chaining in the SSRAM (128 KBytes)
- 16 byte long chaining-block (4 x 32-bit)
- 32-bit Local address, 32-bit PVIC address
- DMA remotely controllable from the PVIC
- DMA interrupt dispatching over PVIC

The local DMA controller (DMAC) supports local READ and PVIC WRITE. The DMA initialization is controlled by a chaining-block in the local SSRAM. The DMA chaining-block initialization can be done locally (from local PCI Bus) or remotely from the PVIC (from other PVIC controller). Many chaining-block lists can be built in the local SSRAM. The DMA process is started by writing the SSRAM address of the first DMA chaining-block in the DMA Request FIFO and setting the dmaSTART control bit. The DMA Request FIFO allows posting of up to 64 chaining-block start addresses (first chaining-block SSRAM address).

6.1 DMA Overview

The embedded DMA controller is using the SSRAM to hold the DMA chaining-blocks. A DMA sequence is decomposed in two steps.

1. SSRAM chaining block initialization (Write)
2. Trigger the DMA controller by writing DMA_Start register with the address of 1st chaining-block loaded in the DMA_Request FIFO.

These steps can be issued from the local bus or remotely from the PVIC.

As soon as the DMA is started, the DMAC is fetching the first chaining-block and begins its execution. The DMA Controller can work in two modes of operation controlled through the dmaMODE bit.

1. Single START. The DMA is executing a single DMA Request.
2. Continuous START. The DMA is executing DMA Requests as long as the DMA Request FIFO is not empty.

If everything is correct, it triggers the local bus interface to issues the local READ. Data read from the local bus are immediately loaded into a write-buffer. At the end of the current read transaction, the DMAC is loading the header and the PVIC address in the current write buffer. This sequence is interrupted when the word counter reaches 0 or when an error occurs.

When the word counter reaches 0, the DMAC checks if the chaining should continue or stop. If the dmaCONT bit in CAC register is set, the DMAC fetches the next chaining-block and processes it. If it is reset, the DMAC is stopped and if enabled, a DMA interrupt is generated.

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6.2 DMA Registers

Table 6-1: PVIC_DMAS0 DMA Control & Status (offset + 0xC0)

Bits	*Mode*	Name	Description
[31]	R W	dmaSUSPEND dmaSUSPEND	 When written to 1 it clears the dmaSUSPEND status bit. dmaSUSPEND status.
[30]	R/W	dmaABORT	Abort DMA operation.
[29]	R/W	dmaSTART	Start DMA Operation (Conditioned by dmaMODE). If dmaMODE = 0 It is cleared at the end of 1st command.
[28]	R W	dmaRUN dmaFIFOFlush	DMA is executing a chaining-block. DMA_Request FIFO Flush command. When this bit is set, the DMA_Request FIFO is cleared. Act also as DMA general reset.
[27]	R/W	dmaMODE	DMA Mode of Operation: = 0: Single Command = 1: FIFO Command queues
[26]	R W	dmaOVERRUN dmaOVERRUN	This status bit is set if the DMA Controller is detecting any PCI or PVIC 64 KBytes address boundary crossing. When it is set, the DMA is halted with same behavior as “dmaABORT” When written to 1 it clears the dmaOVERUN status bit.
[25]	R	dmaFIFOFull	DMA_Request FIFO flag status.
[24]	R	dmaFIFOEmpty	DMA_Request FIFO flag status.
[23:21]	R	dmaEND[2:0]	=000: DMA is not ended (RUN) = 001: DMA is ended normally (end of chaining) = 010: DMA is ended due to a dmaSUSPEND (end of chaining) = 011: Reserved = 100: Error from DMA_Abort set = 101: Error on PCI or PVIC Address overrun = 110: Error Local PCI Target ABORT = 111: Error Local PCI Master ABORT
[20:17]	R W	Signature Reserved	This 4-bit field contains the dmaSIGNATURE of last command. This field is not updated by the chaining-block fetch. Not used
[16:04]	R	Chaining Block Address	This 14-bit field contains the CAR of last fetched chaining-block. It is updated at every chaining block fetch and therefore contains last chaining block CAP.
[01]	R/W	dmaFIFOHalfFull	DMA_Request FIFO flag status.
[00]	R/W	dmaTEST (CES-reserved)	This control bit is reserved for CES test. When positioned to 1, the DMAC is started normally by fetching CAR, PAP, LAP and CAC, but the DMA chaining-block is not executed.

Table 6-2: PVIC_DMAS1 DMA Exception Status (offset + 0xC4)

Bits	*Mode*	Name	Description
[31:20]	R	dmaWCNT	This 12-bit field holds the current DMA Word counter. It is also provided for software error recovery.
[19:17]	R	Not used	Reserved
[16:2]	R	Saved_CAR	This 14-bit field holds the CAR address of current DMA execution. It is provided for software error recovery.
[01:00]	R	Not used	Reserved

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Table 6-3: PVIC_DMAS2 DMA Request FIFO (offset + 0xC8)

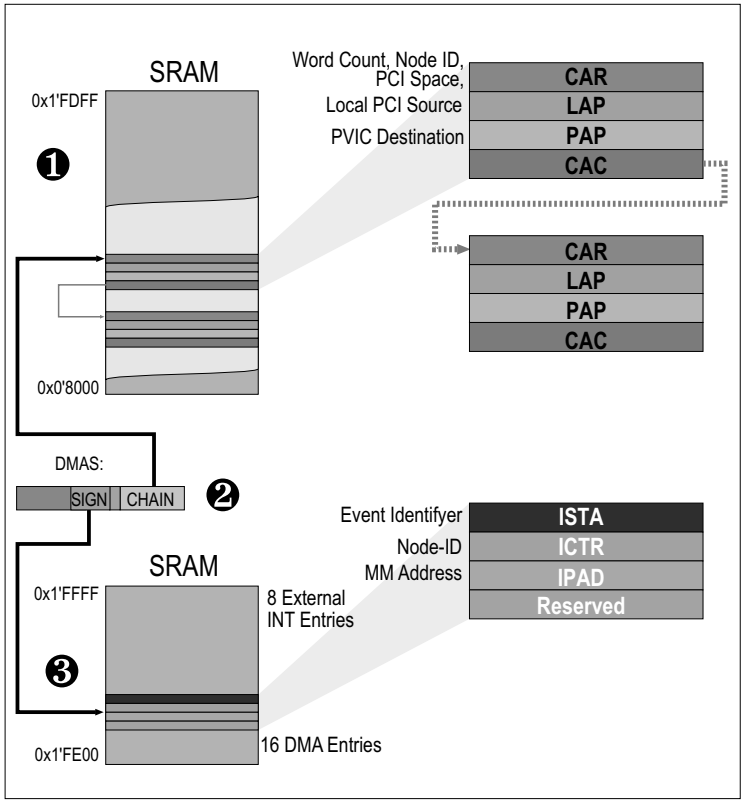
Bits	*Mode*	Name	Description
[31]	R W	dmaSUSPEND Reserved	Reservation dmaSUSPEND set if dmaSUSPEND = 0 Reserved
[30:21]	R	Reserved	Reserved
[20:17]	R W	Reserved Signature	Reserved This 4-bit field are supplied to sign the DMA_Request. It is not updated by the following chaining-block CAR.
[16:02]	R W	Reserved Chaining Block Address	Reserved This 14-bit field specifies the SSRAM address holding the 1st chaining block.
[01:00]	R/W	Not used	Reserved

This register is supplying DMA status information in case of error.

6.3 DMA Chaining Block

The DMA chaining-block is built with four 32-bit long words in the local SSRAM aligned on a 16 Byte boundary. The CAC location points to the next chaining-block.

Figure 6.1: General DMA Sequence



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Table 6-4: CAR Control Address Register (offset + 0x0)

Bits	*Mode*	Name	Description
[31:28]	R/W	L-DSpace	Local Bus Space. This 4-bit field specifies the local PCI address space. 000x: CONFIG Space 000x: IO Space 001x: MEM Space 001x: MEM LINE Space 111x: IACK Space other: Reserved
[27:26]	R/W	P-Disc[1:0]	This 2 bit field specify the PVIC address boundary disconnect. 00: 65536 bytes 01: 1024 bytes 10: 256 bytes
[25]	R/W	P-CType	This bit specifies the PVIC Cycle type. 0: Write with direct acknowledge 1: Write Broadcast
[24]	R/W	P-CSpace	This bit specifies the PVIC destination Space. 0: PVIC Bus to Bus DIRECT 1: PVIC Bus to Bus MAPPED
[23:20]	R/W	P-DSpace	PVIC Destination Bus Space. This 4-bit field specifies the destination Address space as IO, MEMORY, CONFIG, etc.
[19:16]	R/W	PVIC Node_ID	PVIC Destination Node. This 4-bit field specifies the PVIC node address 0000: Broadcast 0001: PVIC Node #1 ... : etc.
[15:14]	R	Not used	Reserved
[13:02]	R/W	WCNT	This 12-bit field specify the DMA word counter in 32-bit word. Size from 1 to 4095 words is supported
[01:00]	R/W	Not used	Reserved

Table 6-5: LAP Local (PCI) Address Pointer (offset + 0x4)

Bits	*Mode*	Name	Description
[31:02]	R/W	Local Address	This field holds the local PCI base address for the current DMA process. WARNING: No support for 64 KBytes boundary crossing
[01:00]	R/W	Not used	Reserved

Table 6-6: PAP PVIC Address Pointer (offset + 0x8)

Bits	*Mode*	Name	Description
[31:02]	R/W	PVIC Address	This field holds the local PVIC base address for the current DMA process. WARNING: No support for 64 KBytes boundary crossing
[01:00]	R/W	Not used	Reserved

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Table 6-7: CAC Chaining Address Control (offset + 0xC)

Bits	*Mode*	Name	Description
[31]	R/W	dmaCONT	This bit allows controlling the chaining process = 0: Stop the chaining after this chaining-block = 1: Continue the chaining if no error occurs
[30:22]	R/W	Reserved	Not used (Reserved for future implementation)
[21]	R/W	SUSPEND_IE	Control Interrupt Enable. When set, if a dmaSUSPEND occurs, a DMA Interrupt is issued over the PVIC at the end of current chaining-block.
[20]	R/W	END_IE	End Interrupt Enable. When set, if no error occurs a DMA Interrupt is issued over the PVIC at the end of current chaining-block.
[19]	R/W	ERROR_IE	Error Interrupt Enable. When set, if an error occurs a DMA Interrupt is issued over the PVIC.
[18]	R/W	dmaNoLINC	Local Address increment control 0: Local Address incremented 1: Local Address holds constant
[17]	R/W	Reserved	Not used (Reserved for future implementation)
[16:04]	R/W	Chaining Block Address	This 14-bit field specifies the SSRAM address holding the next chaining block. It must contain valid information associated with dmaCONT bit #31.
[03:00]	R/W	Not used	Reserved

6.4 DMA Process

The following state diagram shows the DMA process in a more formal way:

Figure 6.2: DMA Process State Diagram

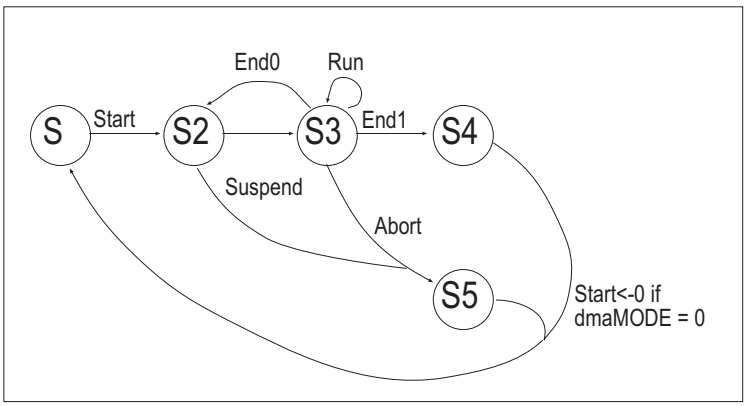


Table 6-8: DMA Process State Description

State	*Description*
State_S1	Idle.
State_S2	Fetch Chaining-Block.
State_S3	Execute DMA Transfer, PCI Cycle...

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Table 6-8: DMA Process State Description

State	*Description*
State_S4	DMA Chain End.
State_S5	DMA Chain Abort (ERROR).
“Start”	= Write PVIC_DMAS0 with DMA_Start = 1 and dmaMODE = 0. = DMA_Request FIFO not empty & DMA_Start =1 and dmaMODE =1.
“End0”	= End current chaining block with CAP DMA_Cont = 1.
“End1”	= End current chaining block with CAP DMA_Cont = 0.
“Abort”	= Local Bus error detected during transfer or dmaABORT set or dmaADDOVERUN set or PCI Error detected.
“Suspend”	= dmaSUSPEND set.
“Run”	= Execute current chaining-block.

6.4.1 DMA Start

The DMA Start command is conditioned by the “dmaMODE” control bit. Two modes of operation are provided:

- Single Command
- FIFO Command

In the two modes of operation, the CAP and the SIGNATURE must be written in the DMAS2 register.

In “Single Command” mode, writing "dmaSTART" control bit to 1 starts the DMA. When started the DMAC reads the DMA_Request FIFO (if it is not empty) to get the 1st chaining-block’s address, fetch the pointed chaining-block and executes it. At the end of this current command (end of the chaining-list or error occurred during the processing), the “dmaSTART” control bit is cleared by hardware. Even if multiple commands are stored in the DMA_Request FIFO, only one is executed at every “dmaSTART” set. If the DMA_Request FIFO is empty when “dmaSTART” control bit is set, the controller is waiting for a command stored in the DMA_Request FIFO to process it.

In “FIFO Command” mode, setting "dmaSTART" control bit to 1 also starts the DMA. The controllers will continuously process DMA commands until the DMA_Request FIFO is not empty. Clearing "dmaSTART" can stop the DMA controller.

In the two modes of operation, the commands are not processed if “dmaSUSPEND” or “dmaABORT” or “dmaADDOVERUN” control bits are set.

6.4.2 DMA Chaining Block RUN

While the DMA is started, the DMA is controlling the data transfer; the data-flow is controlled in real-time by the following parameters, until the end of the current chaining-block:

- LAP low address
- PAP low address
- Word counter value
- Local-PVIC Write-Buffer available (Maxi 4 LWBs used by the DMA at the time)
- Local PCI Latency Timer
- PCI Target Acknowledge (RETRY, DISCONNECT)
- “dmaABORT” control bit

When the current chaining-block execution is terminated (WCNT=0), The DMA controller analyses the CAC Register bit #31. If “dmaCONT” is reset, the DMA command is stopped; otherwise the controller fetches the chaining-block pointed by the current CAP value and executes it.

If the “dmaSUSPEND” control bit has been set, the chaining is halted with DMA_End[2:0] = 010 and the DMA process is suspended.

6.4.3 DMA End

The DMA is ended on multiple conditions, listed in the following table:

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Table 6-9: DMA End

Conditions	*Consequence*	*PVIC Interrupt signaling*
Local PCI Error (Target Abort or Master Abort)	The current chaining-block execution is immediately stopped, the chaining list is stopped and the “dmaSTART” control bit is clear. dmaEND[02:00] = 110 for PCI Target Abort. dmaEND[02:00] = 111 for PCI Master Abort.	If “ERROR_IE” = 1
Abort DMA (dmaABORT=1)	The current chaining-block execution is immediately stopped, the chaining list is stopped and the “dmaSTART” control bit is clear.dmaEND[02:00] = 100	If “ERROR_IE” = 1
Abort DMA (dmaADDOVERRUN=1)	The current chaining-block execution is immediately stopped, the chaining list is stopped and the “dmaSTART” control bit is clear.dmaEND[02:00] = 101	If “ERROR_IE” = 1
Suspend DMA(dmaSUSPEND=1)	The current chaining-block is executed, the chaining list is stopped and the “dmaSTART” control bit is clear.dmaEND[02:00] = 010	If “SUSPEND_IE” = 1
End of Chaining (dmaCONT = 0)	If “dmaMODE” = 0, “dmaSTART” control bit is clear.dmaEND[02:00] = 001	If “END_IE” = 1

6.4.4 DMA Suspend

The DMA chaining process can be suspended by setting “dmaSUSPEND” to 1. To achieve it, the DMAS2_Register must be read. If “dmaSUSPEND” is already set, the bit 31 will be read at 1 and “dmaSUSPEND” will remains set. If “dmaSUSPEND” is clear, the bit 31 will be read at 0 and “dmaSUSPEND” will be automatically positioned to 1. This algorithm allows protecting the “dmaSUSPEND” from multiple sources. The “dmaSUSPEND” can be reset by writing DMAS0 Register with bit #31 set.

6.4.5 DMA Abort

The DMA chaining process can be aborted by writing “dmaABORT” to 1.

6.4.6 DMA Interrupts

The DMA controller can issue multiple PVIC interrupts on a per chaining-block base (refer to chapter 7). The DMA interrupt generation is controlled by the DMA chaining-block bits ERROR_IE, SUSPEND_IE and END_IE and the DMA signature specified when the DMA Request FIFO is loaded.

Each DMA signature has an associated Interrupt Control Block located in SSRAM (refer to chapter 7). The Interrupt Control Block defines the PVIC destination parameters used on event occurrence. It is the user’s responsibility to initialize these blocks correctly.

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Chapter 7
Remote Interrupt Dispatching

The PVIC provides a mechanism to export transparently local interrupts or events to external PVIC nodes. On an event detection (if unmasked), the local controller issues a Mirrored Memory High Priority (MMH) PVIC Write transaction. This PVIC MM Write transaction can directly target the Mirrored Memory Message FIFO and is reserved for remote interrupt signaling of:

- Local PCI INTA#
- Local PCI INTB#
- Local PCI INTC#
- Local PCI INTD#
- Local PCI PERR#
- Local PCI SERR#
- RWERR (Remote Write Error)
- DMA Controller

7.1 Remote Interrupt Control & Status

The remote interrupts are controlled with the following registers.

Table 7-1: PVIC_RICS PVIC Remote Interrupt Control & Status (offset + 0xD0)

Bits	*Mode*	*Name*	*Description*
[31:24]	Reserved		
[23:16]	R/W	RINT-IUS	Interrupt Under Service. These status bits signal the interrupts whose are under service. They are positioned to 1 while the associated interrupt chaining-block is executed. The status bit remains active until it is cleared by writing over the selected bit (from PVIC or local PCI) = 0: IR not under service = 1: IR under service [00] PCI INTA# [01] PCI INTB# [02] PCI INTC# [03] PCI INTD# [04] DMAC [05] RWERR [06] PCI PERR# [07] PCI SERR#

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Table 7-1: PVIC_RICS PVIC Remote Interrupt Control & Status (offset + 0xD0)

Bits	*Mode*	*Name*	*Description*
[15:08]	R/W	RINT-MI	Interrupt Mask. This control bits enable/disable the interrupt request sources (at RESET = 0): = 0 IR Disabled. = 1 IR Enabled. [00] PCI INTA# [01] PCI INTB# [02] PCI INTC# [03] PCI INTD# [04] DMAC [05] RWERR [06] PCI PERR# [07] PCI SERR#
[07:00]	R	RINT-IR	Interrupt Request (IR). These bits reflect the state of the interrupt signals before the masking: = 0: IR Inactive. = 1: IR Active. The PVIC interfaces map the following event sources: [00] PCI INTA# [01] PCI INTB# [02] PCI INTC# [03] PCI INTD# [04] DMAC [05] RWERR [06] PCI PERR# [07] PCI SERR#

While the IUS flag is set, the source is temporary masked. This masking allows the interrupt handler to process it (get the vector with an IACK, analyze it, clear the source, etc.) The DMAC Interrupt IUS is automatically cleared while the event is send over the PVIC.

7.2 Specific Control-Block

The specific Interrupt Control Blocks associated with the sources are mapped as follows in the SSRAM:

Table 7-2: Interrupt Control Blocks Mapping

SSRAM Base +	*Function*
0x1'FF80 - 0x1FF8F	INTA#
0x1'FF90 - 0x1FF9F	INTB#
0x1'FFA0 - 0x1FFAF	INTC#
0x1'FFB0 - 0x1FFBF	INTD#
0x1'FFC0 - 0x1FFCF	Reserved
0x1'FFD0 - 0x1FFDF	RWERR
0x1'FFE0 - 0x1FFEF	PERR#
0x1'FFF0 - 0x1FFFF	SERR#

The DMA Interrupt signaling uses the same mechanism with associated control-blocks indexed by the 4-bit DMA signature located in the DMAS2 Register (DMA Request FIFO):

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Table 7-3: DMA Interrupt Control Blocks Mapping

SSRAM Base +	*Function*
0x1'FE10 - 0x1FE1F	DMA Signature = 0000
0x1'FE20 - 0x1FE2F	DMA Signature = 0001
0x1'FE30 - 0x1FE3F	DMA Signature = 0010
...	...
0x1'FEF0 - 0x1FEFF	DMA Signature = 1111:

The Interrupt Control Blocks are formatted to be similar to the MMH Write-Buffer. During PVIC initialization, these chaining-blocks must be programmed properly.

Table 7-4: ISTA Interrupt Event Identification (offset + 0x0)

Bits	*Mode*	*Name*	*Description*
[31:08]	R/W	SW Event Identification	This 24-bit field contains the software event identification.
[07:00]	R/W	Not used	This 8-bit field will be replaced by hardware event identification.(Refer to next chapter)

Table 7-5: ICTR Interrupt Header (offset + 0x4)

Bits	*Mode*	*Name*	*Description*
[31:28]	R/W	Not used	Reserved
[27:24]	R/W	Wcnt[03:00]	Must be fixed to 1111 for BE[03:00]
[23]	R/W	Burst	Must be fixed to 0 for Single BEAT
[22]	R/W	ASpace	Must be fixed to 0.
[21:20]	R/W	Not used	Reserved
[19:16]	R/W	Src[03:00]	PVIC Source (my local Node Number)
[15]	R/W	Not used	Reserved
[14:12]	R/W	CSpace[02:00]	PVIC Destination Spaces 100 = Mirrored Memory
[11:08]	R/W	CType[03:00]	Encoded PVIC transactions types 0100= Write to High Priority MM Mirrored Memory (Broadcast or not)
[07:04]	R/W	DSpace[03:00]	Encoded Destination Space (Bus to Bus). Must be fixed to 0000.
[03:00]	R/W	Dest[03:00]	Destination Node-ID Number (0000 for Broadcast)

Table 7-6: IPAD Interrupt PVIC MM Address (offset + 0x8)

Bits	*Mode*	*Name*	*Description*
[31]	R/W	PVIC MM Address	Must be fixed to 1 to enable the Mirrored Memory Message FIFO
[30:21]	R/W	Reserved	Must be fixed to 0
[20:02]	R/W	PVIC MM Address	MM Address (up to 1 Mbyte)
[01:00]	R/W	Not used	Reserved

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7.3 PVIC Interrupt Status

The MMH data is supplying the Interrupt source. This event identification is encoded as follows:

Table 7-7: Interrupt Event Identification Encoding

Bits	*Mode*	*Name*	*Description*
[31:08]	R/W	SW Event Identification	This 24-bit field contains the SW event identification
[07:04]	R/W	Node Identification	This 4-bit field contains the local Node-ID identification
[03:00]	R/W	Local Identification	This 4-bit field defines the interrupt sub-sources: **If Not DMA Source**: 0000 = INTA# asserted 0001 = INTB# asserted 0010 = INTC# asserted 0011 = INTD# asserted 0101 = RWERR asserted 0110 = PERR# asserted 0111 = SERR# asserted **If DMA Source**: 1000 = DMA is not ended 1001 = DMA is ended normally (end of chaining) 1010 = DMA is ended due to a DMA_Suspend 1100 = DMA is ended due to a DMA_Abort 1101 = DMA is ended due to PVIC Error 1110 = DMA is ended due to PCI Rx Target ABORT 1111 = DMA is ended due to PCI Tx Master ABORT

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Chapter 8
PVIC 4025, 4425 Interface

8.1 Technical specifications

Table 8-1: 4025 / 4425 Technical Specifications

PIB Slots		
PIB A	Standard PVIC PIB Slot	
PIB B	Not available	
I/O Resources		
Mirrored Memory (DPRM)	32KB (up to 2MB)	
SSRAM	128 KB	
Power Requirement		
+ 3.3 V	1 A typical without PIB daughter card	
+ 5 V	2.5 A typical without PIB daughter card	
± 12 V	Not used	
Top side Power dissipation	12 W	
Bottom side Power dissipation	None	
Environmental Specifications		
Operating Temperature	0° C to 50° C with forced air cooling	
Storage Temperature	- 40° C to 85° C	
Relative Humidity	5% to 95% non condensing	
Mechanical Specifications		
CompactPCI board	PVIC 4025	PVIC 4425
Physical dimensions	Double-height Single Slot (6U)	Single-height Single Slot (3U)
Height	233 mm	100 mm
Depth	160 mm	160 mm
Front panel height	262 mm	128 mm
Front panel depth	2.5 mm	2.5 mm
Front panel width	20 mm	20 mm
Regulatory Compliance		
Immunity	EN 50082-2	
Emission	EN 55022-A	
Safety	EN 60950	

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The PVIC 4025/425 is designed to work within the following environmental specifications:

- Operating temperature 0° C to 50° C
- Forced Air cooling
- Anti-static environment



WARNING

CES accepts no responsibility for failure should these conditions not be respected.

8.2 Motherboard

Figure 8.1: PVIC 4025 Motherboard

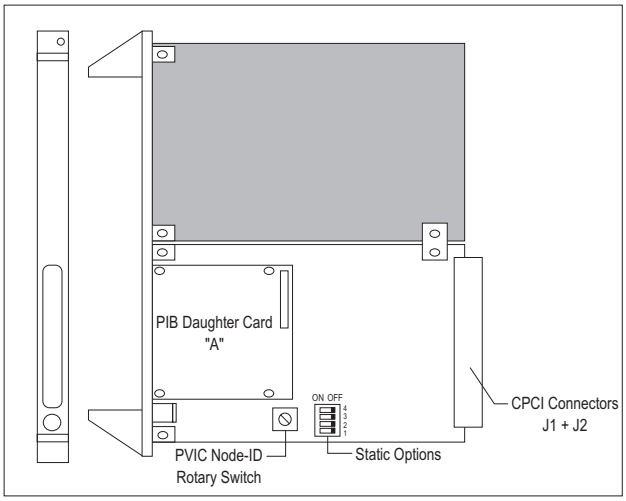
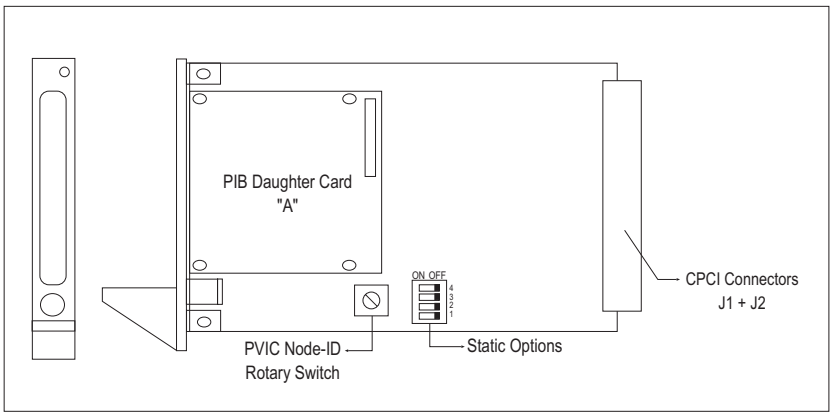


Figure 8.2: PVIC 4425 Motherboard



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8.3 Switches and Jumpers

The PVIC 4025/4425 incorporates two sets of options:

- Node-ID selection: 16-position hex rotary switch allows user to select the PVIC Node Number. The selected value can be read in the PVIC_CSR0 Register. This rotary encoder is located on the motherboard.
- Static Options: 4 micro-switches select the following options:

Table 8-2: 4025 / 4425 Static Options

SW1	*SW2*	*PCI Memory Window Size*
OFF	OFF	32 MBytes
ON	OFF	64 MBytes
OFF	ON	128 MBytes
ON	ON	256 MBytes

SW3	*SW4*	*PVIC Node Speed (Clock)*
ON	ON	33 MHZ
OFF	ON	66 MHZ
ON	OFF	132 MHZ (CES-reserved)
OFF	OFF	264 MHZ

8.4 LED Indicators

The PVIC 4025 / 4425 is not providing LED Indicators.

8.5 CompactPCI Functions

- System Clock driver
- Central Arbiter
- System RESET
- PCI control signal pull-up

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Chapter 9
PVIC 7225 Interface

9.1 Technical specifications

Table 9-1: PVIC 7225 Technical Specifications

PIB Slots	
PIB A	Standard PVIC PIB Slot
PIB B	Not available
I/O Resources	
Mirrored Memory (DPRM)	32 KB (up to 2MB)
SSRAM	128 KB
Power Requirement	
+3.3 V	1 A typical without PIB daughter card
+5 V	2.5 A typical without PIB daughter card
±12 V	Not used
Top side Power dissipation	12W
Bottom side Power dissipation	None
Environmental Specifications	
Operating Temperature	0ºC to 50ºC with forced air cooling
Storage Temperature	0ºC to 50ºC with forced air cooling
Relative Humidity	5% to 95% non condensing
Mechanical Specifications	
Physical dimensions Height Depth Front-panel height Front-panel depth Front-panel width	PCI short card 106 mm 175 mm 121 mm 1.0 mm 18 mm
Regulatory compliance	
Immunity	EN 50082-2
Emission	EN 55022-A
Safety	EN 60950

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The PVIC 7225 is designed to work within the following environmental specifications:

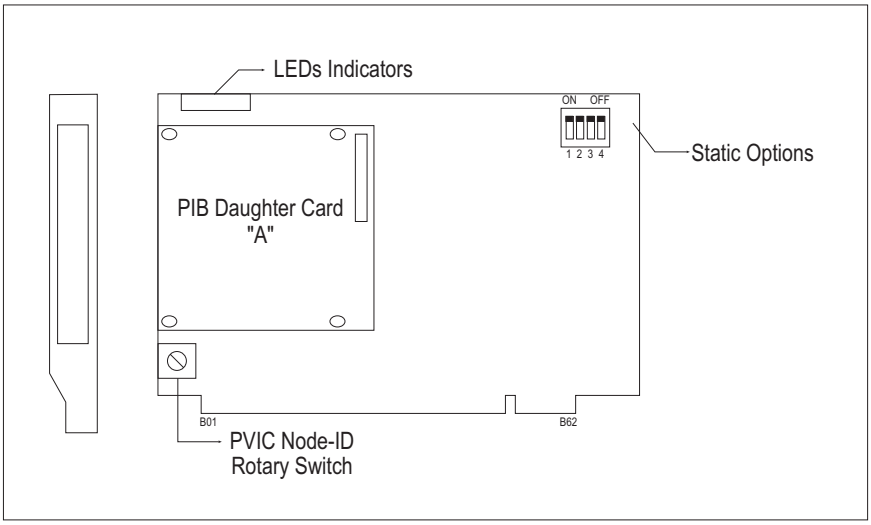
- Operating temperature 0° C to 50° C
- Forced Air cooling
- Anti-static environment

WARNING

CES accepts no responsibility for failure should these conditions not be respected.

9.2 Motherboard

Figure 9.1: PVIC 7225 Motherboard



9.3 Switches and Jumpers

The PVIC 7225 incorporates two sets of static options:

- 16-position Hex rotary switches allow the selection for the PVIC Node Number. The selected value can be read in the PVIC_CSR0 Register. This rotary encoder is directly available from the front panel.
- Static Options: 4 micro-switches determine the following options:

Table 9-2: PVIC 7225 Static Options

SW1	*SW2*	*PCI Memory Window Size*
OFF	OFF	32 MBytes
ON	OFF	64 MBytes

SW3	*SW4*	*PVIC Node Speed (Clock)*
ON	ON	33 MHz
OFF	ON	66 MHz

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Table 9-2: PVIC 7225 Static Options

SW1	*SW2*	*PCI Memory Window Size*
OFF	ON	128 MBytes
ON	ON	256 MBytes

SW3	*SW4*	*PVIC Node Speed (Clock)*
ON	OFF	132 MHz (CES-reserved)
OFF	OFF	264 MHz (CES-reserved)

9.4 LED Indicators

The PVIC 7225 provides 8 LED Indicators (back of PCI board).

Table 9-3: PVIC 7225 LED Description

LED Label	*Function*
PVICMAS	PVIC Master, active when the node is currently the PVIC Master (Arbitration).
PVICTx	PVIC Transmit, active when the node is currently the transmitting PVIC transaction.
PVICRx	PVIC Receive, active when the node is currently receiving decoded PVIC transaction.
PVICFE	PVIC Programmable led indicator
PCISLV	PCI Slave, active when the node is currently decoding a PCI transaction.
PCIMAS	PCI Master, active when the node is currently issuing a PCI transaction.
PCIDMA	DMAC PCI Master, active when the local DMA controller is issuing a PCI transaction.
INTP	PCI Interrupt pending / active when PCI interrupt INTA is activated by the PVIC.


NOTE

The first 6 leds are stretched with monostable (RC = 0.3 s).

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Chapter 10
PVIC 8025 Interface

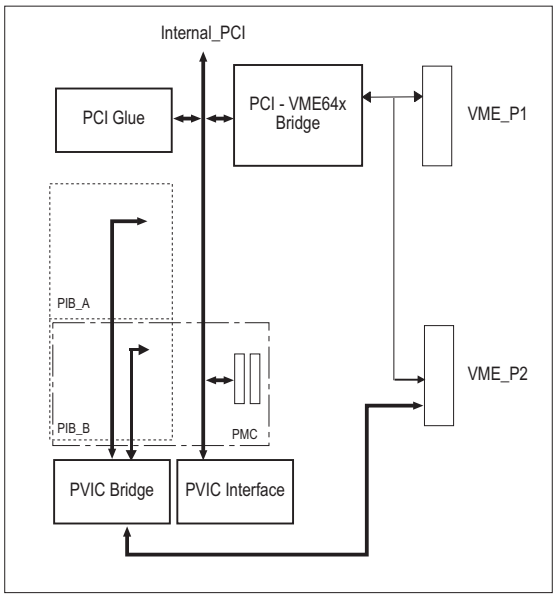
10.1 Introduction

The PVIC 8025 permits to access VME resources via PVIC bus.

It supports:

- VME64x CR / CSR
- VME64x Live Insertion
- Local registers accessible from the VME slave port
- Rerouting of a PIB port on the VME P2 connector
- VME interrupt controller to:
  - Issue a VME Interrupt in case of PCI INTx generated + VME IACK logic
  - Issue a local PCI interrupt (INTB, C, D) on VME interrupt detection
- Local PCI central arbiter and configuration-IDSEL selection
- Full PVIC-VME initialization from the PVIC side and from the VME64 side
  - The PCI-VME bridge is accessible from PCI immediately after power-up
  - The PCI-VME bridge is accessible from VME immediately after power-up

Figure 10.1: PVIC 8025 General Block Diagram



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10.2 Technical specifications

Table 10-1: PVIC 8025 Technical Specifications

PIB Slots	
PIB A	Standard PVIC PIB slot
PIB B	Standard PVIC PIB slot
I/O Resources	
Miirrored Memory (DPRM)	32 KB (up to 2 MB)
SSRAM	128 KB
Power Requirement	
+ 3.3 V	1 A typical without PIB daughter card
+ 5 V	2.5 A typical without PIB daughter card
± 12 V	Not used
Top side power dissipation	12 W
Bottom side power dissipation	None
Environmental Specifications	
Operating Temperature	0° C to 50° C with forced air cooling
Storage Temperature	- 40° C to 85° C
Relative Humidity	5% to 95% non condensing
Mechanical Specifications	
Physical dimensions	Double-height Single Slot VME (6U)
Height	233 mm
Depth	160 mm
Front panel height	262 mm
Front panel depth	2.5 mm
Front panel width	20 mm
Regulatory Compliance	
Immunity	EN 50082-2
Emission	EN 55022-A
Safety	EN 60950

The PVIC 8025 is designed to work within the following environmental specifications:

- Operating temperature 0° C to 50° C
- Forced Air cooling
- Anti-static environment



WARNING

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10.3 PCI / VME64x Bridge

VME64x Bridge Registers Mapping

The VME64x internal registers are mapped on:

- PCI I/O Space at PCIIO 0x0000'0000-0x0000'FFFF (64 KBytes).
- VME64x CR / CSR with geographical addressing, for system supporting the VME64x CR / CSR (1-Mbyte). Configuration CSR: AM code = 0x2F offset: A[23:19] = GA[04:00]
- VME64 A24 with static switches for old VME64 with 3-row connectors (64 KBytes). User / Sup A24 Data Space: AM code = 0x3D and 0x39, A[23:15] = microswitch ID[07:00]

The VME64x CR / CSR or VME64 A24 mapping can be selected with a micro-switch.

The VME64x bridge registers are tailored in four groups:

- VME64x / CR registers. These registers are defined by the VME64x specification. They hold read-only information such as the board manufacturer, device ID, etc.
- VME64x / CSR. These registers hold the VME64x Control & Status Registers.
- VME64x CRAM. VME64x Configuration Memory.
- Internal bridge CSR registers.

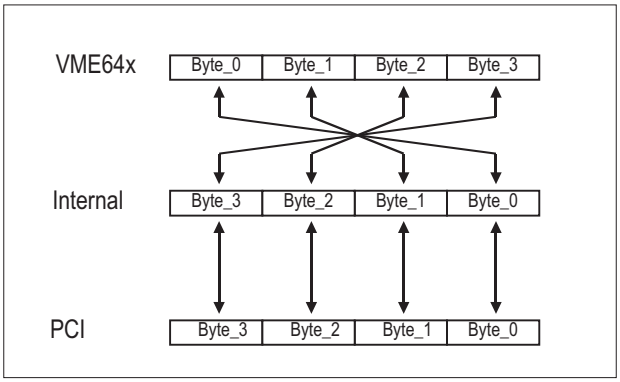
Table 10-2: VME 64x Bridge Registers Mapping

Register section	*VME64x-CR / CSR*	*VME64 static A24*	*PCI I/O Space*
VME64x CR	0x'0000 - 0x'0FFF	0x0000 - 0x0FFF	0x0000 - 0x00FF
VME64x CSR	0x'FF00 - 0x'FFFF	0xFF00 - 0xFFFF	0xFF00 - 0xFFFF
VME64x CRAM	0x'2000 - 0x'20FF	0x2000 - 0x20FF	0x2000 - 0x20FF
Internal CSR	0x'4000 - 0x'40FF	0x4000 - 0x40FF	0x4000 - 0x40FF
PCI Config	0x'8000 - 0x'9FFF	0x8000 - 0x9FFF	Not applicable

VME64x Bridge Registers Description

The PVIC 8025's resources are implemented in little-endian (same as PCI). The VME interface is using a natural byte swapper (local byte number routed to VME byte number). Access to internal 32-bit PVIC 8025 registers in 32-bit mode requires a byte swapping which must be handled by software.

Figure 10.2: PCI / VME 64x Bridge Byte Swapping



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10.3.1 VME64x CR Registers

The PVIC 8025 implements the following VME64x CR Registers. The content of these registers is stored in the CISP serial FlashPROM.

Table 10-3: VME64x CR Registers Mapping

Offset from base	*Resource*	*Value*
0x0003	Checksum	
0x0007		
0x000B	Lenght of ROM_2	
0x000F	Lenght of ROM_3	
0x0013	CSR Data Access Width	
0x001B	CR / CSR Space Specification ID	
0x001F	0x43	ASCII “C”
0x0023	0x52	ASCII “R”
0x0027	CES’s ID_1 (IEEE OUI)	0xA2
0x002B	CES’s ID_2 (IEEE OUI)	0x80
0x002F	CES’s ID_3 (IEEE OUI)	0x00
0x0033	Board’s ID_1	ASCII “5”
0x0037	Board’s ID_2	ASCII “2”
0x003B	Board’s ID_3	ASCII “0”
0x003F	Board’s ID_4	ASCII “8”
0x0043	Rev’s ID_1	ASCII “1”
0x0047	Rev’s ID_2	ASCII “0”
0x004B	Rev’s ID_3	ASCII “0”
0x004F	Rev’s ID_4	ASCII “0”
0x0053 to 0x007B	Reserved	0x00
0x007F	Program ID code	



For a complete description of the CR registers, refer to VME64x specification.

10.3.2 VME64x CSR Registers

The PVIC 8025 implements the following VME64x CSR Registers.

Table 10-4: VME64x CSR Registers

Offset from base	*Size*	*Resource*
0xFFFF	8-bit	CR / CSR BAR
0xFFFB	8-bit	CR / CSR Bit Set Register
0xFFF7	8-bit	CR / CSR Bit Clear Register
0xFFF3	8-bit	CRAM_OWNER Register

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Table 10-4: VME64x CSR Registers

Offset from base	*Size*	*Resource*
0xFFEF - 0xFF7F	Reserved	Not Implemented in PVIC 8025
0xFF63	8-bit	Function_0 ADER_LLB
0xFF67	8-bit	Function_0 ADER_LMB
0xFF6B	8-bit	Function_0 ADER_MLB
0xFF6F	8-bit	Function_0 ADER_MMB
0xFF5F - 0xFC00	Reserved	Not Implemented in PVIC 8025

Table 10-5: CSR BAR Register base + 0xFFFF

Bits	*Name*	*Mode*	*Description*
[07:03]	BAR[04:00]	(R)	This 5-bit field allows reading back the CR / CSR Base address. If the microswitch “vmeCSR_64x” is OFF: BAR[04:00] = micro-switch vmeOPT_CSR[04:00] If the microswitch “vmeCSR_64x” is ON: BAR[04:00] = VME64x Geographical Address GA[04:00] BAR[04:00] = 0x1E if GAP is wrong
[02:00]	Reserved	(R)	Read at 000

Table 10-6: CSR Bit Set Register base + 0xFFFB

Bits	*Name*	*Mode*	*Description*
[07]	VME64x_RESET	(R) (W)	The PVIC 8025 is in VME64x Reset Mode Forces the PVIC 8025 in VME64x Reset Mode
[06]	SYSF_DRV_ena	(R) (W)	The SYSFAIL driver is enabled Enables the SYSFAIL driver
[05]	SYSF_driven	(R) (W)	The PVIC 8025 is driving the SYSFAIL Forces the PVIC 8025 to drive the SYSFAIL (Test Mode only)
[04]	VME64x-enable	(R) (W)	PVIC 8025 VME64x Enabled Enables PVIC 8025
[03]	VME64x-BERR_FF	(R) (W)	The PVIC 8025 has issued a BERR# Sets the VME64x-BERR_FF Flag (Test Mode only)
[02]	CRAM_OWNER	(R) (W)	The CRAM is owned Sets the CRAM_OWNER (Test Mode only)
[01:00]		(R)	Read as 00

Table 10-7: CSR Bit Clear Register base + 0xFFF7

Bits	*Name*	*Mode*	*Description*
[07]	VME64x_RESET	(R) (W)	The PVIC 8025 is in VME64x Reset Mode Forces the PVIC 8025 in VME64x not Reset Mode
[06]	SYSF_DRV_ena	(R) (W)	The SYSFAIL driver is enabled Disables the SYSFAIL driver
[05]	SYSF_driven	(R) (W)	The PVIC 8025 is driving the SYSFAIL Forces the PVIC 8025 not to drive the SYSFAIL (Test Mode only)

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Table 10-7: CSR Bit Clear Register base + 0xFFF7

Bits	Name	Mode	Description
[04]	VME64x-enable	(R) (W)	PVIC 8025 VME64x Enabled Disables PVIC 8025
[03]	VME64x-BERR_FF	(R) (W)	The PVIC 8025 has issued a BERR# Clears the VME64x-BERR_FF Flag (Test Mode only)
[02]	CRAM_OWNER	(R) (W)	The CRAM is owned Clears the CRAM_OWNER (Test Mode only)
[01:00]		(R)	Read as 00

Table 10-8: CRAM_OWNER Register base + 0xFFF3

Bits	Name	Mode	Description
[07:00]	CRAM_OWNER[07:00]	(R/W)	Special VME64x semaphore register. Its value is updated only if the current CRAM_OWNER = 0x00. Otherwise it is not updated with new data. Refer to theVME64x specification.


NOTE

After RESET, CRAM_OWNER is reset to 0x00.

Table 10-9: Function_0 ADER_LLB Register base + 0xFF63

Bits	Name	Mode	Description
[07:02]	ADD_AM[05:00]	(R/W)	VME64x AM code for the mapping of the PVIC 8025 window. The following AM codes are supported: If A32_SUP_MBLT Code A32_SUP_BLT, A32_SUP_DATA, A32_SUP_MBLT, A32_USR_BLT, A32_USR_DATA, A32_USR_MBLT If A32_USR_MBLT Code A32_USR_BLT, A32_USR_DATA, A32_USR_MBLT If A32_SUP_BLT Code A32_SUP_BLT, A32_SUP_DATA, A32_USR_BLT, A32_USR_DATA If A32_USR_BLT Code A32_USR_BLT, A32_USR_DATA If A32_SUP_DATA Code A32_SUP_DATA, A32_USR_DATA If A32_USR_DATA CodeA32_USR_DATA
[01]	DFSR	(R/W)	Dynamic Function Size read. While set, the Function_0_ADER+MMB register is supplying ADEM value. Refer to the VME64x specification.
[00]	XAM	(R)	Not used in the PVIC 8025. Read as 0x0.


NOTE

The ADD_AM[05:00] implementation is the CES interpretation of the VME64x specification. Requires a clarification from VITA.

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Table 10-10: Function_0 ADER_LMB Register base + 0xFF67

Bits	Name	Mode	Description
[07:00]	ADD_C[15:08]	(R/W)	Not used in the PVIC 8025

Table 10-11: Function_0 ADER_MLB Register base + 0xFF6B

Bits	Name	Mode	Description
[07:00]	ADD_C[23:16]	(R/W)	Not used in PVIC 8025

Table 10-12: Function_0 ADER_MMB Register base + 0xFF6F

Bits	Name	Mode	Description
[07:04]	ADD_C[31:29]	(R/W)	PVIC 8025 VME64x high address mapping.
[03:01]	ADD_C[28:24]	(R/W)	PVIC 8025 VME64x middle address mapping. This 3-bit field is conditioned by the selected microswitches vme_WSIZ[02:00]
[00]		(R)	Reserved

10.3.3 VME64x CRAM Memory

The PVIC 8025 is implementing the VME64x Configuration RAM (CRAM Area). It is built with a specific 256 x 8 SRAM accessible in D08(O) every fourth bytes. As defined by the VME64x specification, this memory area is associated with the CRAM_OWNER Register and the CRAM_OWNER_FLAG. As other PVIC 8025 registers, CRAM can also be controlled from the PCI Slave Port.

CRAM_Memory base + 0x2000 ... 0x23FF256 bytes SRAM

10.3.4 Internal CSR Registers

The PVIC 8025 implements the following VME64x CSR Registers:

Table 10-13: Internal CSR Registers Mapping

Offset from Base	Size	Resource
0x4000	32-bit	PCI_CTL0
0x4004	32-bit	PCI_CTL1
0x4008	32-bit	PCI_CTL2
0x400C	32-bit	PCI_CTL3
0x4040	32-bit	VME_CTL0
0x4044	32-bit	VME_CTL1
0x4048	32-bit	VME_CTL2
0x404C	32-bit	VME_CTL3
0x4050	32-bit	VME_CTL4
0x4054	32-bit	VME_CTL5
0x4080	32-bit	BMA_VAP
0x4084	32-bit	BMA_PAP
0x4088	32-bit	BMA_CAP

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Table 10-13: Internal CSR Registers Mapping

Offset from Base	*Size*	*Resource*
0x408C	32-bit	BMA_CTR
0x409C	32-bit	BMA_ICR

Table 10-14: PCI_CTL0 base + 0x4000

Bits	*Name*	*Mode*	*Description*
[31:05]	Reserved	(R)	Not implemented
[04]	Reserved	(R/W)	Not implemented
[03]	Rx_Ini_Abo	(R/W)	Set when a VME-PCI transaction is terminated with a Master Abort
[02]	Rx_Tar_Abo	(R/W)	Set when a VME-PCI transaction is terminated with a Target Abort
[01]	Tx_Tar_Abo	(R/W)	Set when a PCI-VME transaction is terminated with a Target Abort
[00]	Reserved	(R)	Read as 1

Table 10-15: PCI_CTL1 base + 0x4004

Bits	*Name*	*Mode*	*Description*
[31:08]	Reserved	(R)	Not implemented
[07:03]	PCI_Latency_Timer	(R/W)	PCI latency timer, in 250 ns increment
[02:00]	Reserved	(R/W)	Not implemented

Table 10-16: PCI_CTL2 base + 0x4008

Bits	*Name*	*Mode*	*Description*
[31:15]	Reserved	(R)	Not implemented
[14:00]	vmeSG_ADD	(R/W)	Scatter Gather Address pointer. Used to initialize the scatter / gather SRAM

Table 10-17: PCI_CTL3 base + 0x400C

Bits	*Name*	*Mode*	*Description*
[31:00]	vmeSG_DATA	(R/W)	Scatter Gather Data register. Used to initialize the scatter / gather SRAM

Table 10-18: VME_CTL0 base + 0x4040

Bits	*Name*	*Mode*	*Description*
[31:16]	Reserved	(R)	Not implemented,
[15:13]	vme_WSIZ[02:00]	(R)	VME64-PCI window size. Reflects the status of associated microswitches. 000 = 16 MBytes 001 = 32 MBytes 010 = 14 MBytes 011 = 128 MBytes 100 = 256 MBytes 101 = 512 MBytes 110 = 1024 MBytes

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Table 10-18: VME_CTL0 base + 0x4040

Bits	Name	Mode	Description
[12:11]	Reserved	(R)	Not implemented
[10]	vmeARB_RRS	(R/W)	Arbiter mode: = 0: Priority = 1: Round Robin
[09:08]	vmeARB_LEV[01:00]	(R/W)	Bus request level (0, 1, 2 or 3)
[07]	vmeARB_RWD	(R/W)	Arbitration release mode: = 0: Release on request = 1: Release when done
[06]	vmeARB_FAIR	(R/W)	If set, the arbitration is in FAIR mode
[05]	vmeARB_HIDD	(R/W)	If set, the arbitration is in Hidden mode
[04]	vmeLTO_MAX	(R/W)	While set, the PCI transaction is terminated with a Target Abort after 64 retries on the VME64x Bus
[03:02]	vmeLTO_SEL[01:00]	(R/W)	LTO selection (8, 16, 32 or 64)
[01:00]	vmeBTO_SEL[01:00]	(R/W)	VME BTO selection (16, 64, 256 or disabled)

Table 10-19: VME_CTL1 base + 0x4044

Bits	Name	Mode	Description	
[31:16]	Reserved	(R)	Not implemented	
[15]	pmc_12_TCLK	(W)	PMC 1 & 2	JTAG Port control
[14]	pmc_12_TRST	(W)	PMC 1 & 2	JTAG Port control
[13]	pmc_1_TDI	(W)	PMC 1	JTAG Port control
[12]	pmc_2_TDI	(W)	PMC 2	JTAG Port control
[11]	pmc_1_TDO	(R)	PMC 1	JTAG Port control
[10]	pmc_2_TDO	(R)	PMC 2	JTAG Port control
[09]	pmc_1_TMS	(R)	PMC 2	JTAG Port control
[08]	pmc_2_TMS	(R)	PMC 2	JTAG Port control
[07:05]	Reserved	(R)	Not implemented	
[04]	vmeWPERR	(R/W)	Status bit set if a PCI-VME Write-posting error has occurred	
[03]	vmeATO_FF	(R/W)	Status bit set if an ATO time-out has occurred	
[02]	vmeLTO_FF	(R/W)	Status bit set if a LTO time-out has occurred	
[01]	vmeBTO_FF	(R/W)	Status bit set if a BTO time-out has occurred	
[00]	VME_Slot1	(R)	This status bit reflects the state of the VME Slot 1 function. = 0: Slot 1 is disabled = 1: Slot 1 is enabled	

Table 10-20: VME_CTL2 base + 0x4048

Bits	Name	Mode	Description
[31:08]	Reserved	(R)	Not implemented
[15]	pmc_12_BMOD[3]	(W)	PMC 1 & 2 Bus_Mode Port control
[14]	pmc_12_BMOD[2]	(W)	PMC 1 & 2 Bus_Mode Port control
[13]	pmc_12_BMOD[1]	(W)	PMC 1 & 2 Bus_Mode Port control

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Table 10-20: VME_CTL2 base + 0x4048

Bits	Name	Mode	Description
[12]	pmc_1_BMOD[4]	(W)	PMC 1 Bus_Mode Port status
[11]	pmc_2_BMOD[4]	(W)	PMC 2 Bus_Mode Port status
[09:08]	Reserved	(R)	Not implemented
[07]	vmeINTP	(R)	This status bit is active when the unit is driving the VME IRQn
[06]	vmePGM_INT	(W)	This write-only control bit allows the setting of the VME IRQ specified by vmeILEV[02:00]. It is active only while vmeSLEV[02:00] = 000.
[05:03]	vmeSLEV[02:00]	(R/W)	VME Interrupt source level. This 3-bit field allows the selection of the local source activating the VME IRQn specified by vmeILEV[02:00]. = 001: Programmed = 010: Embedded DMA controller = 100: PCI INTA# = 110: PCI INTC# = 111: PCI INTD#
[02:00]	vmeILEV[02:00]	(R/W)	VME Interrupt level (7 to 1)

Table 10-21: VME_CTL3 base + 0x4048

Bits	Name	Mode	Description
[31:08]	Reserved	(R)	Not implemented
[07:00]	vmeVEC[07:00]	(R/W)	VME 8-bit vector

Table 10-22: VME_CTL4 base + 0x4050

Bits	Name	Mode	Description
[31:16]	Reserved	(R)	Not implemented
[15:12]	pciINTD_SRC[03:00]	(R/W)	PCI INTD Source selection
[11:08]	pciINTC_SRC[03:00]	(R/W)	PCI INTC Source selection
[07:04]	pciINTB_SRC[03:00]	(R/W)	PCI INTB Source selection
[03:00]	pciINTA_SRC[03:00]	(R/W)	PCI INTA Source selection = 0000: disabled = 0001: VME IRQ#1 ... = 0111: VME IRQ#7 = 1000: VME Direct Error = 1001: VME BMA Interrupt = 1010: PEB EXT#0 Interrupt = 1011: PEB EXT#1 Interrupt

Table 10-23: VME_CTL5 base + 0x4054

Bits	Name	Mode	Description
[31:12]	Reserved	(R)	Not implemented
[15]	pciINTD	(R)	Interrupt Source
[14]	pciINTC	(R)	Interrupt Source
[13]	pciINTB	(R)	Interrupt Source
[12]	pciINTA	(R)	Interrupt Source

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Table 10-23: VME_CTL5 base + 0x4054

Bits	Name	Mode	Description
[11]	pebEXT1	(R)	Interrupt Source
[10]	pebEXT0	(R)	Interrupt Source
[09]	vmeBMAIRQ	(R)	Interrupt Source
[08]	vmeDIRERR	(R)	Interrupt Source
[07]	vmeIRQ#7	(R)	Interrupt Source
[06]	vmeIRQ#6	(R)	Interrupt Source
[05]	vmeIRQ#5	(R)	Interrupt Source
[04]	vmeIRQ#4	(R)	Interrupt Source
[03]	vmeIRQ#3	(R)	Interrupt Source
[02]	vmeIRQ#2	(R)	Interrupt Source
[01]	vmeIRQ#1	(R)	Interrupt Source
[00]	Reserved	(R)	Not implemented
[31:12]	Reserved	(R)	Not implemented

Table 10-24: BMA_VAP base + 0x4080

Bits	Name	Mode	Description
[31:16]	bmaVADD[31:16]	(R/W)	VME address pointer (fixed)
[15:02]	bmaVADD[15:02]	(R/W)	VME address pointer (14-bit binary counter)
[01:00]	bmaVSW[01:00]	(R/W)	VME Swapping policy: = 00: No swapping = 01: Byte swapping = 10: Word swapping = 11: Byte & Word swapping



The Embedded DMA is not able to issue VME D08 and D16.

Table 10-25: BMA_PAP base + 0x4084

Bits	Name	Mode	Description
[31:16]	bmaPADD[31:16]	(R/W)	PCI address pointer (fixed)
[15:02]	bmaPADD[15:02]	(R/W)	PCI address pointer (14-bit binary counter)
[01:00]	bmaPSP[01:00]	(R/W)	PCI Spaces: = 00: PCI I/O = 01: PCI MEMORY = 10: PCI MEMORY Multiple = 11: PCI MEMORY with no address increment

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Table 10-26: BBMA_VAP base + 0x4088

Bits	Name	Mode	Description
[31:05]	bmaCADD[31:05]	(R/W)	PCI chaining address pointer
[04]	bmaCMPA	(R/W)	Chaining Mode PCI Address control. When set, allows the rejection of new PAP value when the BMA is fetching the next block descriptor. It allows building contiguous PCI data with distributed VME data
[03]	bmaCMIBE	(R/W)	When set, enables the capability to issue an interrupt at the end of the current chaining block
[02]	bmaCMIEE	(R/W)	When set, enables the capability to issue an interrupt in case of error in the current chaining block
[01:00]	bmaCM[01:00]	(R/W)	Chaining control = 00: Stops the BMA chaining = 01: Stops the BMA chaining and writes back the status to PCI = 10: Continues the BMA chaining if no error occurred = 11: Continues the BMA chaining even if an error occurred. In case of error, the BMA status is written back to PCI

Table 10-27: BMA_CTR base + 0x408C

Bits	Name	Mode	Description
[31]	bmaERROR	(R/W)	BMA Error status
[30]	bmaEND	(R/W)	BMA End status
[29]	bmaFFLUSH	(W)	BMA BiFIFO flush command
[28]	bmaABORT	(W)	BMA Abort command. Must be set with bmaVST and/or bmaPST
[27]	bmaVST	(R/W)	BMA VME Start
[26]	bmaPST	(R/W)	BMA PCI Start
[25:24]	bmaBECOD[01:00]	(R)	BMA Error status = 00: PCI Target Abort = 01: VME BERR = 10: VME RETRY = 11: VME BTO time-out
[23]	bmaVANINC	(R/W)	BMA VME Address pointer not incremented
[22]	bmaBDIR	(R/W)	BMA Direction = 0: VME Read - PCI Write = 1: VME Write - PCI Read
[21]	bmaVD64R/W	(R/W)	BMA VME D64 transfer
[20]	bmaFOPS	(R/W)	BMA VME fixed operand size
[19:18]	bmaPOPS[01:00]	(R/W)	PCI flow control = 00: PCI latency timer = 01: 4 word burst = 10: 8 word burst = 11: 16 word burst
[17:15]	bmaVOPS[02:00]	(R/W)	VME flow control = 000: disabled (reserved) = 001: 1 word burst = 010: 2 word burst = 011: 4 word burst = 100: 8 word burst = 101: 16 word burst = 110: 32 word burst = 111: Maximum VME performance

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Table 10-27: BMA_CTR base + 0x408C

Bits	Name	Mode	Description
[14:12]	bmaVAC[02:00]	(R/W)	VME AM address encoding
[11:00]	bmaWCNT[11:00]	(R/W)	VME BMA word counter (32-bit word)

Table 10-28: BMA_ICR base + 0x409C

Bits	Name	Mode	Description
[31:08]	Reserved	(R)	Not implemented
[07]	bmaCEND_Mask	(R/W)	BMA chaining end interrupt mask
[06]	bmaERR_Mask	(R/W)	BMA error interrupt mask
[05]	bmaEND_Mask	(R/W)	BMA end interrupt mask
[04]	bmaCSBEND	(R/W)	BMA chaining sub-block interrupt source
[03]	bmaCERR	(R/W)	BMA chaining error interrupt source
[02]	bmaCEND	(R/W)	BMA chaining end interrupt source
[01]	bmaCHAIN_ERR	(R/W)	BMA chaining chain-err interrupt source
[00]	Reserved	(R)	Not implemented

10.3.5 PCI Configuration

This field is used to access the PCI configuration space of local PCI devices. While the PCI-VME64x bridge is detecting access to this field, the cycle is reported on the PCI bus with configuration space as:

Table 10-29: Local PCI Devices Configuration Space Mapping

PCI bus device	Configuration Spaces
PMC (bottom)	base + 0x9000 - 0x90FF
PEB Extension	base + 0x9400 - 0x94FF
PVIC Device	base + 0x9800 - 0x98FF

10.4 VME64x Slot_1 function

The PVIC 8025 features the VME Slot-1 function. While vmeCSR_64x switch is ON, the Slot 1 function is automatically enabled if GA = 0b00001. If vmeCSR_64x switch is OFF, the Slot 1 function is enabled with the vme_SLOT1 micro-switch.

The PVIC 8025 Slot 1 function provides:

- 4-level VME Arbiter with PRI or RRS mode selected through the VME_CTL0 register
- VME 16 MHz SYSCLK driver
- VME IACK daisy-chain driver
- VME BTO controller with time-out value selected through bits BTOSEL[01:00] located in VME_CTL0 register

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10.5 VME64x PCI-VME Transactions

The PVIC 8025 PCI-VME64 Bridge incorporates an out-going scatter / gather for PCI to VME transaction. The transactions targetting VME64 from PCI must use the fixed window (1- Gbyte):

PCI_{MEM} 0x8000'0000 - 0xBFFF'FFFF: PCI-VME window

This 1-Gbyte window is divided in 16384 pages of 64 KBytes. Each page holds an associated page-descriptor providing various additional information to execute the VME cycle properly.

The PCI-VME pathway is isolated with a 64 word deep FIFO allowing to support write-posting and read ahead buffer.

The scatter / gather SSRAM must be initialized before any PCI-VME transactions. The initialization must be done through the PCI_CTL2 and the PCI_CTL3 registers.



The PCI_CTL2 & PCI_CTL3 are also accessible from the VME Slave port.

PCI-VME Scatter / Gather Page Descriptor

The scatter / gather SSRAM is organized in 32-bit words. Each page entry owns a set of page descriptions (PD) and PDL registers. For the PCI to VME transactions up to 0x4000 sets of PD registers are stored in the scatter / gather SSRAM.

Table 10-30: PCI-VME Scatter / Gather Page Descriptors Mapping

SG SSRAM Offset	*CR / CSR BAR*
0x0000	PD for 1st page (0 to 64 K)
0x0001	PD for 2nd page (64 K to 128 K)
...	...
0x3FFF	PD for last page (1024 M - 64 K to 1024 M)

Table 10-31: PDH + PDL Outgoing Scatter / Gather Page Descriptor

Bits	*Name*	*Mode*	*Description*
[31:16]	vmeVHA[31:16]	(W/R)	VME high address remapping
[15]	vmesgVALID	(W/R)	Page entry valid (page enable)
[14:13]	Reserved	(W/R)	
[12:11]	vmesgSW[1:0]	(W/R)	VME swapping policy: = 00: No swapping = 01: Auto swapping = 10: Word swapping = 11: Byte &Word swapping
[10]	Reserved	(W/R)	
[09]	vmesgRPRF	(W/R)	Read prefetch enable
[08]	Reserved	(W/R)	
[07]	vmesgWPOST	(W/R)	Write Posting enable

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Table 10-31: PDH + PDL Outgoing Scatter / Gather Page Descriptor

Bits	*Name*	*Mode*	*Description*
[06]	vmesgVIACK	(W/R)	VME IACK. When set, the page will issue a VME IACK cycle. The level must be encoded on VME low address bits [03:01].
[05:00]	vmesgVAM[05:00]	(W/R)	VME AM code

10.6 VME64x VME-PCI Transactions

The PVIC 8025 PCI-VME64 bridge incorporates an in-going scatter / gather for VME to PCI transactions. The transaction targetting PCI from VME64 must use the programmable window VMEA32 (16-Mbyte to 1-Gbyte).

The window offset is programmable through the VME64x/CSR registers while the window size is determined by the micro-switches vme_WSIZ[02:00]

This programmable window is divided into pages of 64 KBytes. Each page holds an associated page-descriptor providing various information to execute the PCI cycle properly.

The scatter / gather SSRAM must be initialized before any PCI-VME transactions. This initialization must be done through the PCI_CTL2 and the PCI_CTL3 registers.


NOTE

The PCI_CTL2 & PCI_CTL3 are also accessible from the VME Slave port.

10.6.1 VME-PCI Scatter / Gather Page Descriptor

The scatter / gather SSRAM is organized in 32-bit word. Each page entry owns a set of PDH and PDL. For the VME to PCI up to 0x2000 sets of PDH / PDL registers are stored in the scatter / gather SSRAM.

Table 10-32: VME-PCI Scatter / Gather Page Descriptors Mapping

SG SSRAM Offset	*CR / CSR BAR*
0x4000	PD for 1st page (0 to 64K)
0x4001	PD for 2nd page (64 K to 128 K)
...	...
0x7FFF	PD for last page (1024 M - 64 K to 1024 M)

Table 10-33: PDH + PDL Ingoing Scatter / Gather Page Descriptor

Bits	*Name*	*Mode*	*Description*
[31:16]	vmePHA[31:16]	(W/R)	PCI high address remapping
[15]	vmesgVALID	(W/R)	Page entry valid (page enable)
[14:13]	RESERVED	(W/R)	
[12:11]	vmesgSW[01:00]	(W/R)	Swapping policy = 00: No swapping = 01: Auto swapping = 10: Word swapping = 11: Byte&Word swapping

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Table 10-33: PDH + PDL Ingoing Scatter / Gather Page Descriptor

Bits	*Name*	*Mode*	*Description*
[10:09]	vmesgRPRF[01:00]	(W/R)	Read prefetch policy = 00: Disabled = 01: 4 words = 10: 8 words = 11: 16 words
[08]	vmesgWRPROT	(W/R)	Write protect
[07]	vmesgWPOST	(W/R)	Write Posting enable
[06:02]	RESERVED	(W/R)	
[01:00]	vmesgPSP[1:0]	(W/R)	PCI Space = 00: I/O Space = 01: MEMORY Space = 10: MEMORY multiple Space = 11: Reserved

10.6.2 Special VME64x Slave transactions

The PVIC 8025 PCI-VME bridge also supports some special VME Slave transaction to:

- Access PCI-VME Bridge internal registers
- Access VME64x CR / CSR registers
- Issue PCI configuration cycle from VME (for local PCI initialization directly from VME)

10.7 VME64x Embedded DMA Controller

The PCI-VME64 bridge implements the same DMA controller as the CES RIO2 806x family with the following modifications / improvements:

- The BMA registers are accessible from the VME Slave port.
- The BMA interrupt can be issued on VME or on PCI side.
- The BMA chaining must run on PCI memory resources present on the local PCI side.

10.8 VME64x Interrupt Generator

The PVIC 8025 PCI-VME64x bridge incorporates a VME Interrupt Generator. This logic allows activating a VME IRQ on events such as:

- PCI Interrupt (INTA, INTB, INTC or INTD)
- BMA Interrupt
- Mailbox register

A 3-bit field vmeILEV[02:00] allows the selection the VME IRQ level and another 3-bit field vmeSLEV[02:00] allows selecting the source. Only one source can be selected.


NOTE

Refer to VME_CTL2 and VME_CTL3 register description.

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10.9 VME64x & Local Interrupt Handler

The PCI-VME bridge is incorporating the logic for the PCI interrupt generation. Each PCI INTx (A to D) can be activated on local interrupt sources:

Table 10-34: Interrupt Source Selection

pciINTx_SRC[03:00]	*Source selection*
0000	Disabled
0001	VME IRQ#1
0010	VME IRQ#2
0011	VME IRQ#3
0100	VME IRQ#4
0101	VME IRQ#5
0110	VME IRQ#6
0111	VME IRQ#7
1000	VME DIRECT Error
1001	VME BMA Interrupt
1010	PEB EXT#0
1011	PEB EXT#1

10.10 VME64x Live Insertion

The PVIC 8025 is integrating the VME64x/LI logic:

- LI/I - LI/O control
- LTC1421 acting as power-supply ramp-up controller
- Front-panel switch for connection / disconnection control.

The PVIC Live-Insertion Procedure

Card Plug-In:

- Push the PVIC 8025 front-panel LI-switch to the left into position OFF
- Plug-in the PVIC 8025 into the powered-on VME crate
- Power-on the PVIC 8025 by pushing the front-panel LI-switch the middle to position ON.

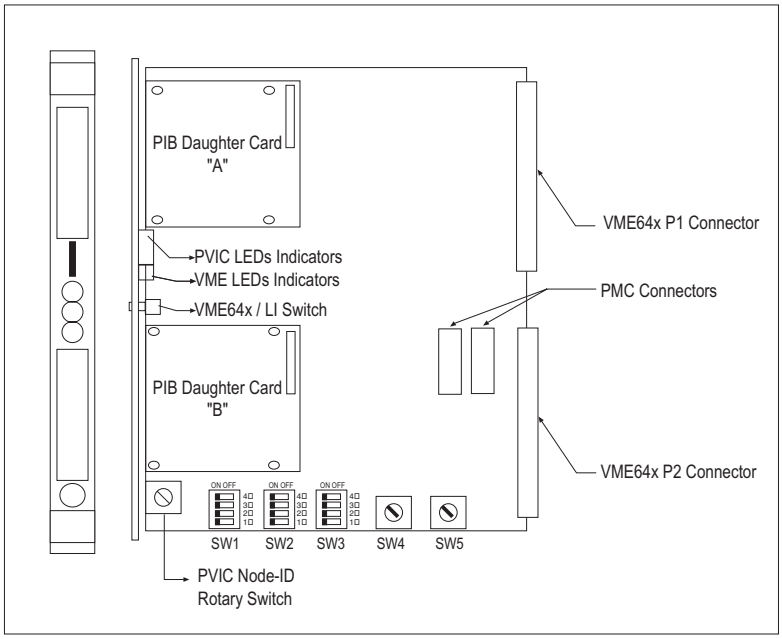
Card Plug-Out:

- Power-off the PVIC 8025 by pushing the front-panel LI-switch to the left into position OFF
- Plug-Out the PVIC 8025 from the powered-on VME crate.

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10.11 PVIC 8025 Static options

Figure 10.3: PVIC 8025 Motherboard



10.11.1 Front Panel Switches

The PVIC 8025 has two switches accessible from the front panel.

One 16-position hex rotary switch allows the selection of the PVIC Node Number. The selected value can be read in the PVIC_CSR0 Register.

One 3-position controlling the VME64X/LI:

MIDDLE	Connected, the PVIC 8025 is powered-on
LEFT	Disconnected, the PVIC 8025 is powered-off
RIGHT_MOM	Local RESET, reported over VME if Slot 1 (system controller)

10.11.2 Front Panel Indicator

The PVIC 8025 provides 12 LED indicators (from top to bottom).

Table 10-35: PVIC 8025 LED Functions

LED Label	*Function*
VME_SLOT1	VME Slot 1, active when the PVIC 8025 is VME system controller
VME_Mast	VME Master, active when the PVIC 8025 owns the VME mastership
VME_Slave	VME Slave, active when the PVIC 8025 is decoding VME cycle
VME_BMA	VMA BMA, active when the embedded BMA controller is running
PCI_SLV	PCI Slave, active when the node is currently decoding a PCI transaction
PCI_MAS	PCI Master, active when the node is currently issuing a PCI transaction

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Table 10-35: PVIC 8025 LED Functions

LED Label	*Function*
PCI_Dmac	DMAC PCI Master, active when the local DMA controller is issuing a PCI transaction
PCI_INTP	PCI Interrupt pending, active when PCI interrupt INTA is activated by the PVIC 8025
PVIC_MAS	PVIC Master, active when the node is currently the PVIC Master (Arbitration)
PVIC_Tx	PVIC Transmit, active when the node is currently the transmitting PVIC transaction
PVIC_Rx	PVIC Receive, active when the node is currently receiving decoded PVIC transaction
PVIC_FE	PVIC Programmable led indicator

10.11.3 Onboard Switches

The PVIC 8025 incorporates four sets of static options. These options are implemented with micro DIP switches, labeled SW1 to SW5.

Table 10-36: 8025 Static Options

Position	*Description*
SW1(2-1)	Define the PCI memory window size used by the PVIC interface. ON - ON: 256 MBytes ON - OFF: 128 MBytes OFF - ON: 64 MBytes OFF - OFF: 32 MBytes
SW1(4-3)	Define the PVIC node speed ON - ON: 33 MHz ON - OFF: 66 MHz OFF - ON: 133 MHz. (Reserved) OFF- OFF: 266 MHz. (Reserved)
SW2(3-1)	vme_WSIZ[02:00], defines the VME A32 Slave window size OFF - OFF - OFF 16 MBytes OFF - OFF - ON 32 MBytes OFF - ON - OFF 64 MBytes OFF - ON - ON 128 MBytes ON - OFF - OFF 256 MBytes ON - OFF - ON 512 MBytes ON - ON - OFF 1024 MBytes
SW2(4)	PVIC_PIB on P2 ON: VME P2 used for PVIC PIB over P2 OFF: VME P2 not used
SW3(1)	VME slot_1, active only if vmeCSR_64x = OFF ON: VME System Controller enabled
SW3(2)	vmeCSR_64x ON: VME64x protocol enabled. The CR / CSR Space is mapped with the GA[04:00] VME pin, following the VME64x specification OFF: VME64X protocol disabled. The local CSR is mapped in A24 with base address specified by SW4 & SW5
SW3(3)	VME_Tx_RESET ON: The PVIC 8025 is able to issue a VME SYSRESET
SW3(4)	VME_Rx_RESET ON: The PVIC 8025 is reset on detection of VME SYSRESET
SW4(4-1)	vme_ID[03:00] VME A24 base address when vmeCSR_64x is OFF
SW5(4-1)	vme_ID[07:04] VME A24 base address when vmeCSR_64x is OFF

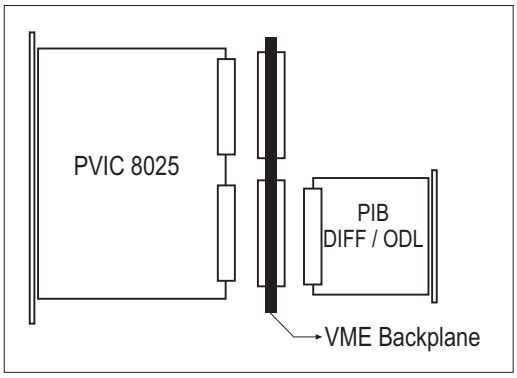
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10.12 PVIC P2 Extension

The PVIC 8025 allows exporting the PVIC PIB physical connection over the VME P2 user's pin. This allows building PVIC systems without using any front-panel connection.

The PIB Bus is physically connected only when SW2(4) "PVIC_PIB on P2" is ON.

Figure 10.4: PIB Bus



NOTE

The PIB Bus is isolated to P2 with CMOS quick-switch. Therefore, the PVIC 8025 must not be plugged in a VME slot where any voltage over 5 V are present on P2 row A & C.

Table 10-37: VME P2 User Pin Assignment

Row A	*Pin*	*Row C*
pibDATA0	1	GND
pibDATA1	2	GND
pibDATA2	3	GND
pibDATA3	4	GND
pibDATA4	5	GND
pibDATA5	6	GND
pibDATA6	7	GND
pibDATA7	8	GND
pibDATA8	9	GND
pibDATA9	10	GND
pibDATA10	11	GND
pibDATA11	12	GND
pibDATA12	13	GND
pibDATA13	14	GND
pibDATA14	15	GND
pibDATA15	16	GND

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Table 10-37: VME P2 User Pin Assignment

Row A	*Pin*	*Row C*
pibCMD0	17	Node_ID3
picCMD1	18	Node_ID2
GND	19	Node_ID1
pinRxCLK	20	Node_ID0
GND	21	3V3
pibTxDATA_EN	22	5V
pibRxDATA_EN	23	pibID2
pibRxSTA0	24	pibID1
pibRxSTA1	25	pibID0
pibTxSTA0	26	pibTERM
pibTxSTA1	27	pibPOWER
pibBGOUT	28	pibTxHREQ
pibBGIN	29	pibTxREQ
pibTxRESET	30	pibRxHREQ
pibRxRESET	31	pinRxREQ
pibODLSTA	32	pibCLK

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Chapter 11
PVIC 8425 Interface

11.1 Technical specifications

Table 11-1: PVIC 8425 Technical Specifications

PIB Slots	
PIB A	Onboard GTL+ or DIFF Interface
PIB B	Not available
I/O Resources	
Mirrored Memory (DPRM)	32KB (up to 2MB)
SSRAM	128 KB
Power Requirement	
+ 3.3 V	1 A typical without PIB daughter card
+ 5 V	2.5 A typical without PIB daughter card
± 12 V	Not used
Top side Power dissipation	12 W
Bottom side Power dissipation	None
Environmental Specifications	
Operating Temperature	0° C to 50° C with forced air cooling
Storage Temperature	- 40° C to 85° C
Relative Humidity	5% to 95% non condensing
Mechanical Specifications	
Physical dimensions	Standard PMC Mezzanine
Height	75 mm
Depth	150 mm
Front panel height	70 mm
Front panel depth	2.5 mm
Front panel width	12 mm
Regulatory Compliance	
Immunity	EN 50082-2
Emission	EN 55022-A
Safety	EN 60950

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The PVIC 8425 is designed to work within the following environmental specifications:

- Operating temperature 0° C to 50° C
- Forced Air cooling
- Anti-static environment

WARNING

CES accepts no responsibility for failure should these conditions not be respected.

11.2 Motherboard

Figure 11.1: PVIC 8425 GTL+ Motherboard (solder side)

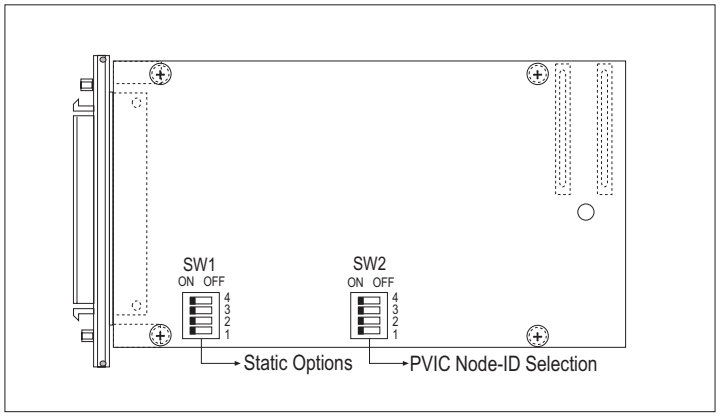
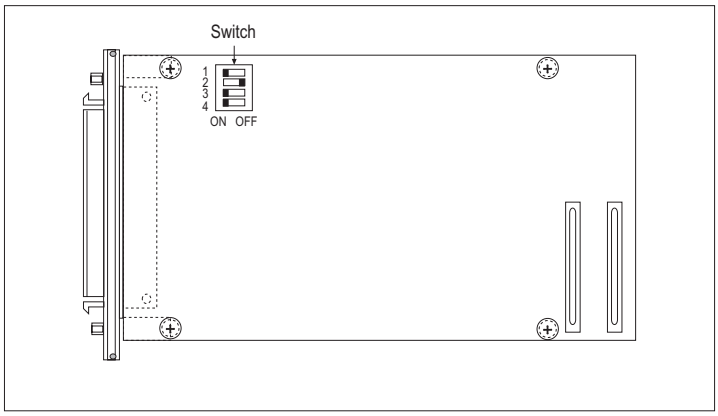
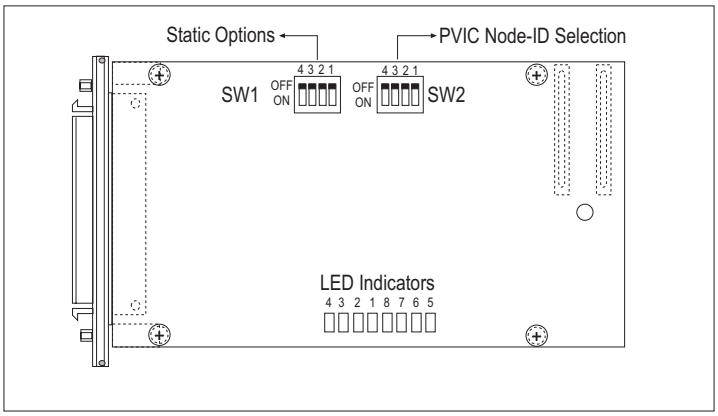


Figure 11.2: PVIC 8425 GTL+ Motherboard (component side)



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Figure 11.3: PVIC 8425 DIFF Motherboard (solder side)



11.3 Switches and Jumpers

PVIC Node Selection: 4 micro-switches allow to select the PVIC Node number according to the following formula:

- PVIC Node-ID = ON(SW2-4) * 8 + ON(SW2-3) * 4 + ON(SW2-2) * 2 + ON(SW2-1) ON(SW2-x) should be replaced with 1 if the corresponding switch is ON. The selected value can be read in the PVIC_CSR0 Register.

- Static Options: 4 micro-switches allow the selection of the following options:

Table 11-2: PVIC 8425 Static Options

SW1-1	*SW1-2*	*PCI Memory Window Size*	*SW1-3*	*SW1-4*	*PVIC Node Speed (Clock)*
OFF	OFF	32 MBytes	ON	ON	33 MHz
OFF	ON	64 MBytes	OFF	ON	66 MHz
ON	OFF	128 MBytes	ON	OFF	132 MHz (CES-reserved)
ON	ON	256 MBytes	OFF	OFF	264 MHz (CES-reserved)

11.4 LED Indicators

The PVIC 8425 (GTL+) is not providing any LED Indicator.
The PVIC 8425D (DIFF) provides 8 LED Indicators (see figure 11.3).

Table 11-3: PVIC 8425 LED Functions

#	*LED Name*	*Function*
1	PVICMAS	PVIC Master, active when the node is currently the PVIC Master (Arbitration).
2	PVICTx	PVIC Transmit, active when the node is currently the transmitting PVIC transaction.
3	PVICRx	PVIC Receive, active when the node is currently receiving decoded PVIC transaction.
4	PVICFE	To be defined
5	PCISLV	PCI Slave, active when the node is currently decoding a PCI transaction.
6	PCIMAS	PCI Master, active when the node is currently issuing a PCI transaction.
7	PCIDMA	DMAC PCI Master, active when the local DMA controller is issuing a PCI transaction.
8	INTP	PCI Interrupt pending / active when PCI interrupt INTA is activated by the PVIC.

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Chapter 12
PVIC 8426 Interface

12.1 Technical specifications

Table 12-1: PVIC 8426 Technical Specifications

PIB Slots	
PIB A	Standard PVIC PIB Slot
PIB B	Standard PVIC PIB Slot
I/O Resources	
Mirrored Memory (DPRM)	32KB (up to 2MB)
SSRAM	128 KB
Power Requirement	
+ 3.3 V	1 A typical without PIB daughter card
+ 5 V	2.5 A typical without PIB daughter card
± 12 V	Not used
Top side Power dissipation	12 W
Bottom side Power dissipation	None
Environmental Specifications	
Operating Temperature	0° C to 50° C with forced air cooling
Storage Temperature	- 40° C to 85° C
Relative Humidity	5% to 95% non condensing
Mechanical Specifications	
Physical dimensions	Double-height Single Slot VME (6U)
Height	233 mm
Depth	160 mm
Front panel height	262 mm
Front panel depth	2.5 mm
Front panel width	20 mm
Regulatory Compliance	
Immunity	EN 50082-2
Emission	EN 55022-A
Safety	EN 60950

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The PVIC 8426 is designed to work within the following environmental specifications:

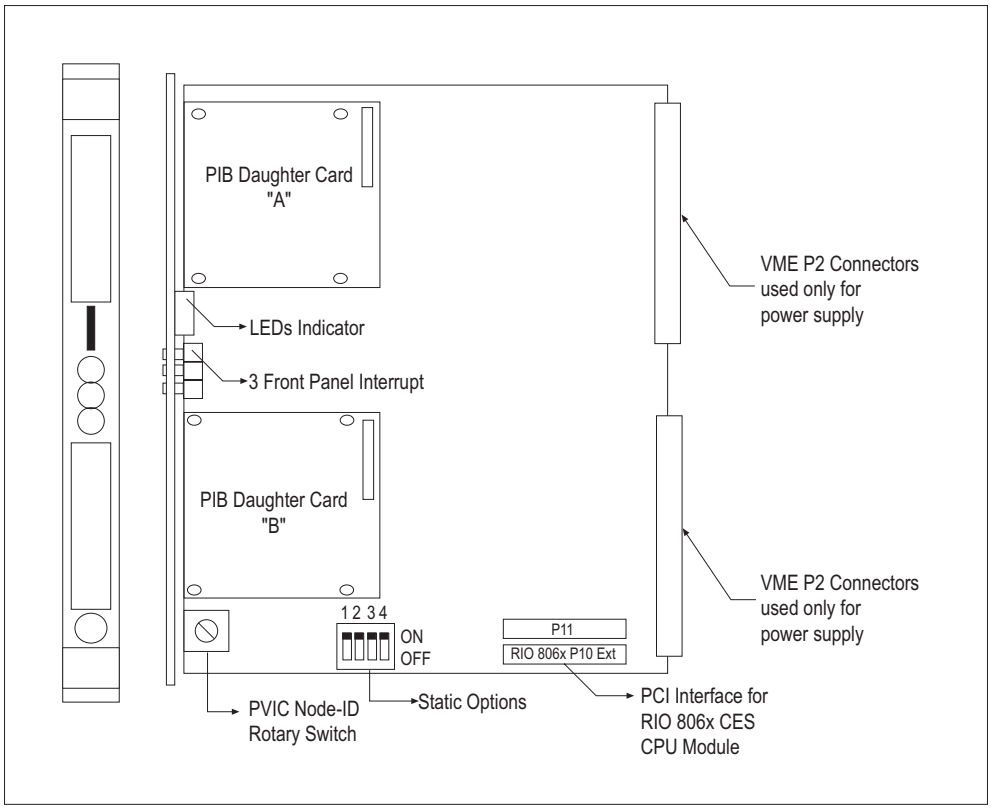
- Operating temperature 0° C to 50° C
- Forced Air cooling
- Anti-static environment

WARNING

CES accepts no responsibility for failure should these conditions not be respected.

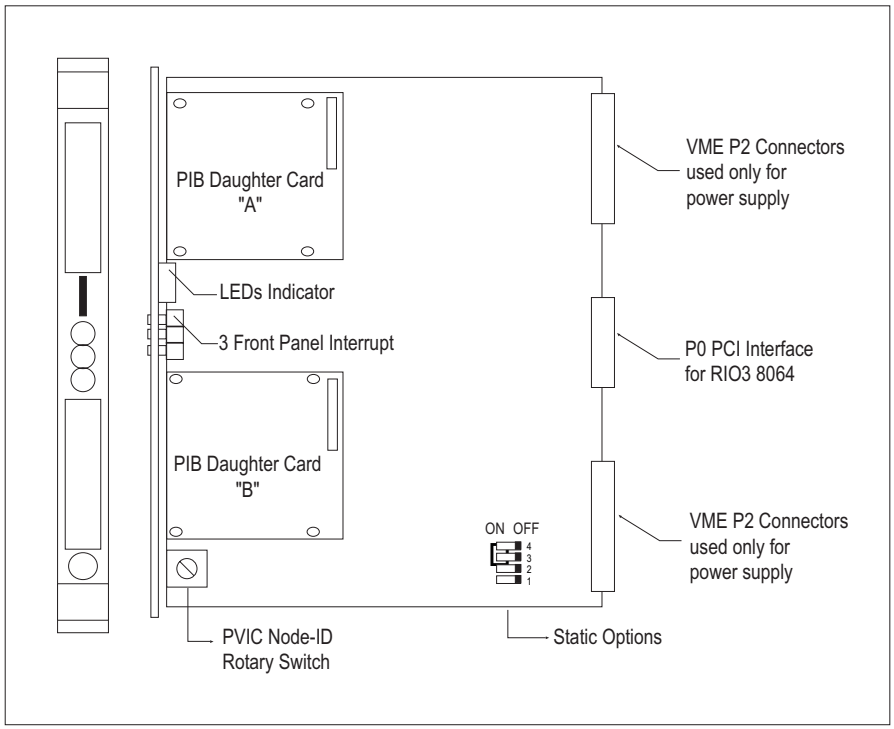
12.2 Motherboards

Figure 12.1: PVIC 8426B Motherboard



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Figure 12.2: PVIC 8426D Motherboard



12.3 Switches and Jumpers

The PVIC 8426 incorporates two sets of static options:

- Node-ID: 16-position Hex rotary switch allows the selection of the PVIC Node Number. The selected value can be read in the PVIC_CSR0 Register. This rotary encoder is directly available on the front panel.
- Static Options: 4 micro-switches allow the selection of the following options:

Table 12-2: PVIC 8426 Static Options

SW1	*SW2*	*PCI Memory Window Size*
OFF	OFF	32 MBytes
ON	OFF	64 MBytes
OFF	ON	128 MBytes
ON	ON	256 MBytes

SW3	*SW4*	*PVIC Node Speed (Clock)*
ON	ON	33 MHZ
OFF	ON	66 MHZ
ON	OFF	132 MHZ (CES-reserved)
OFF	OFF	264 MHZ (CES-reserved)

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12.4 LED Indicators

The PVIC 8426 provides 8 LED Indicators (top to bottom).

Table 12-3: PVIC 8026 LED Functions

LED Label	*Function*
PVICMAS	PVIC Master, active when the node is currently the PVIC Master (Arbitration).
PVICTx	PVIC Transmit, active when the node is currently the transmitting PVIC transaction.
PVICRx	PVIC Receive, active when the node is currently receiving decoded PVIC transaction.
PVICFE	To be defined
PCISLV	PCI Slave, active when the node is currently decoding a PCI transaction.
PCIMAS	PCI Master, active when the node is currently issuing a PCI transaction.
PCIDMA	DMAC PCI Master, active when the local DMA controller is issuing a PCI transaction.
INTP	PCI Interrupt pending/active when PCI interrupt INTA is activated by the PVIC.


NOTE

The first 6 LEDs are stretched with mono-stable (RC = 0.3 s).

12.5 Front Panel Interrupts

The PVIC 8426 provides 3 front panel interrupt inputs. These three interrupt sources can trigger PVIC interrupt dispatching. They are connected in place of PCI Interrupt INTB, INTC and INTD. The 3 front panel interrupts are active low and hold on-board 470 Ω pull up resistors.

INTB	top one
INTC	middle one
INTD	bottom one


NOTE

The 3 front panel interrupts are direct emulation of PCI interrupts and therefore are level sensitive only.

12.6 PVIC Bridging Capability

The PVIC 8426 implements PVIC bridging capability. This allows interconnecting different PVIC electrical interface like GTL+, DIFF or Optical (ODL). The PVIC Bridge is introducing 4 PVIC clock cycles latency on a PVIC transaction.

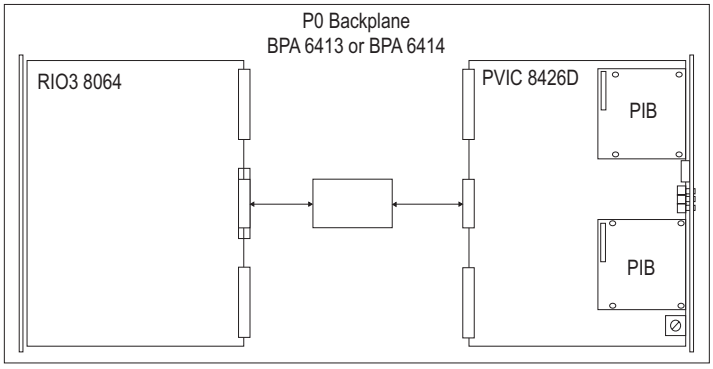

WARNING

When used as bride with two PIBs the PIB on Port A must point towards the PVIC Monarch (Node-ID = 1). Furthermore a PVIC bridge can not be used as Monarch.

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12.7 PVIC 8426D P0 Extension

Figure 12.3: PVIC 8426D Connection with RIO3 8064



12.8 P0 Backplane

To connect the PVIC 8426D and the RIO3 8064 together, a rear-mounted backplane must be used and mounted on the P0 connector on the rear side of the backplane.

2-slot (BPA 6413) and 3-slot (BPA 6414) P0 rear-mounted backplane versions are available.

Table 12-4: P0 Pin Assignement

Pin	*Row A*	*Row B*	*Row C*	*Row D*	*Row E*	*Row F*
1	CLK_SRC	VCC3	SERIN	SEROUT	PRESENT#	GND
2	PAR	CLK_IN	SYNC	RESET#	SPARE	GND
3	AD31	CBE0	CBE1	CBE2	CBE3	GND
4	AD26	AD27	AD28	AD29	AD30	GND
5	AD21	AD22	AD23	AD24	AD25	GND
6	AD16	AD17	AD18	AD19	AD20	GND
7	AD11	AD12	AD13	AD14	AD15	GND
8	AD6	AD7	AD8	AD9	AD10	GND
9	AD1	AD2	AD3	AD4	AD5	GND
10	AD62	AD63	IRDY#	TRDY#	AD0	GND
11	AD57	AD58	AD59	AD60	AD61	GND
12	AD52	AD53	AD54	AD55	AD56	GND
13	AD47	AD48	AD49	AD50	AD51	GND
14	AD42	AD43	AD44	AD45	AD46	GND
15	AD37	AD38	AD39	AD40	AD41	GND
16	AD32	AD33	AD34	AD35	AD36	GND
17	CBE4	CBE5	CBE6	CBE7	PAR64	GND
18	DEVSEL#	ACK64#	RST#	LOCK#	GNT#	GND
19	FRAME#	STOP#	REQ64#	IDSEL	REQ#	GND

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Chapter 13
PIBs, Cables and Terminators

The PVIC interface can be operated with three different electrical interfaces (PIBs): GTL+, Differential (DIFF) and Optical (ODL). While the optical link can only be used for point-to-point connections the GTL+ and DIFF cable can interconnect up to 15 PVIC interfaces. The following table lists the maximum total cable length for the different interface technologies:

Table 13-1: Maximum Cable Length and Node Number for the Different Technologies

PIB Type	*Maximum Node#*	*Maximum Cable Length*
GTL+	15 (multi-point) 2 (point-to-point)	1 m 2 m
DIFF	15 (multi-point)	15 m at 66MHz 30 m at 33MHz
ODL	2 (point-to-point)	200 m

Both, the GTL+ and DIFF electrical interfaces use a 68pin SCSI type connector that is often used to connect SCSI devices as well. The GTL+ and DIFF cable chain must be terminated on both ends with an appropriate terminator.



Do not plug the SCSI type connector of the PVIC cable or terminator into a wrong electrical PVIC interface or a SCSI port. This might damage the PVIC and the SCSI interface card.

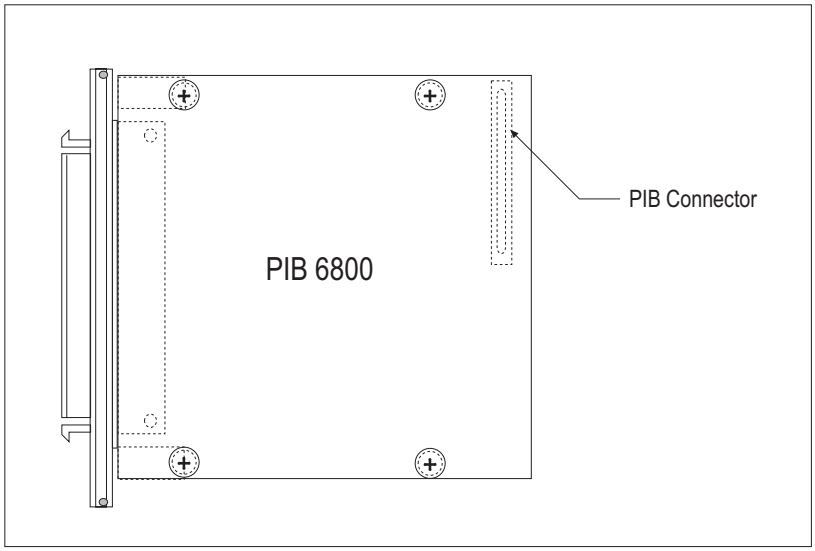
13.1 Mounting and Exchanging PIBs

The PVIC interfaces 4025, 4425, 7225, 8025 and 8426 can be equipped with various electrical interface boards (PIBs). The PIB is plugged onto the PIB socket on the PVIC mother-board and fixed with 4 screws. It can easily be mounted or exchanged. Do not forget to use electrostatic discharge (ESD) protection.

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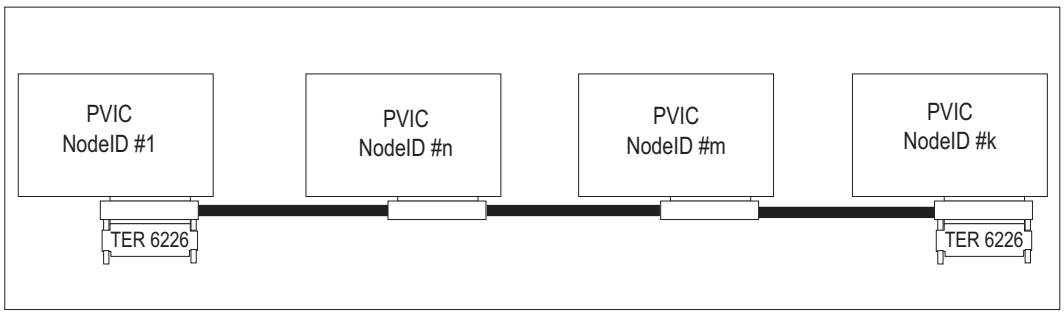
13.2 GTL+ PIB and Cabling Rules

Figure 13.1: PIB 6800 Board



The PVIC GTL + ribbon flat cable allows the interconnection of up to 15 PVIC nodes. At each PVIC bus end a PVIC GTL + terminator (TER 6226) must be plugged onto the male as shown in the figure below:

Figure 13.2: GTL+ Cabling Example



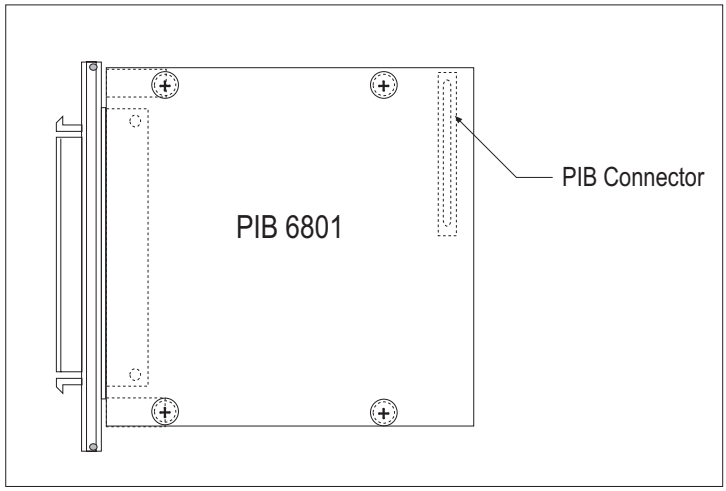
NOTE

The GTL+ cable is symmetric.

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13.3 DIFF PIB and Cabling Rules

Figure 13.3: PIB 6801 Board

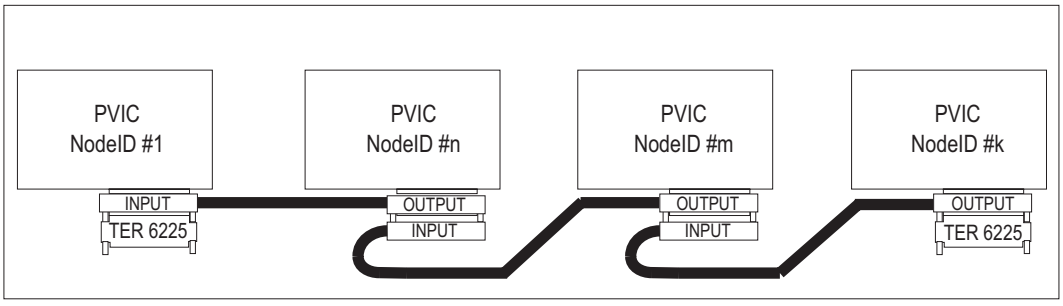


The PVIC DIFF cable is equipped with screwable male-female connectors. This allows to build a daisy-chain interconnecting the PVIC nodes as shown below. At each end of the PVIC daisy-chain a PVIC bus terminator (TER 6225) must be plugged onto the remaining male connector. To transport the PVIC arbitration daisy-chain, the PVIC cable VDC 6500 must be mounted in the proper direction.

NOTE

This means the DIFF cable is not symmetric. The two connectors at each end of the DIFF cable are labeled INPUT and OUTPUT, respectively. The connector labeled INPUT must always point towards the PVIC monarch (Node-ID = 1) as shown in the following figure.

Figure 13.4: DIFF Cabling Example

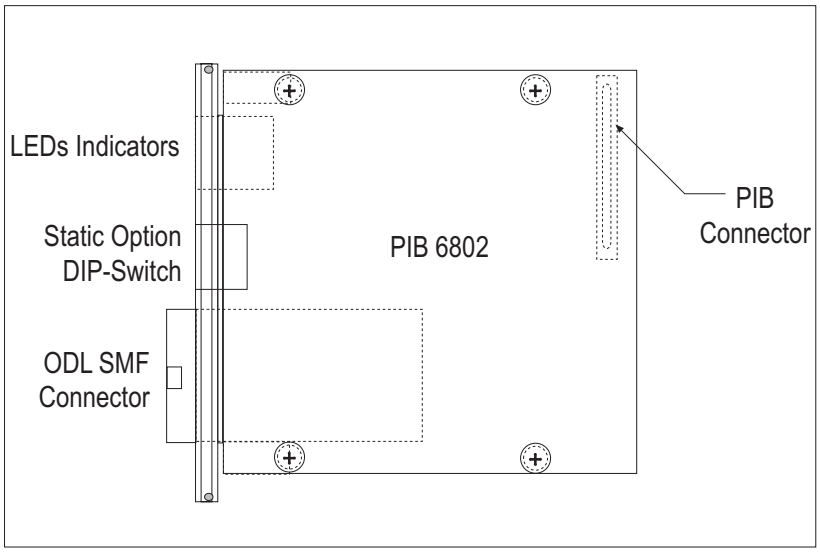


It does not matter which connector is connected first. The INPUT connector can be plugged onto the OUTPUT connector or vise-versa.

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13.4 Optical PIB (ODL) and Cabling Rules

Figure 13.5: PIB 6802 Board



The PIB 6802 front panel is holding the ODL SMF connector, the LED indicators and a block with four micro-switches:

Table 13-2: LED Indicators (from top to bottom)

LED	*Function*
LED #1	LED is on when the remote side has lost the PVIC clock (error condition)
LED #2	LED is on when the ODL 6802 is PIB master
LED #3	LED is on when the GLINK device has their internal PLL locked
LED #4	LED is on when the GLINK device has detected a transmission error (error condition)

Table 13-3: Static Options (micro-switch)

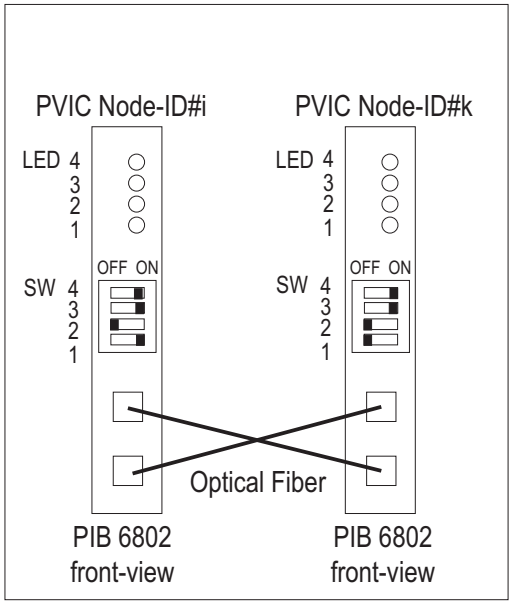
Switch	*Function*
SW 1	Defines PVIC Monarch (Node-ID = 1) side OFF Monarch is on other side ON Monarch is on this side.
SW 2	Selects the GLINK PLL pre-scaler OFF For PVIC at 33 MHz ON For PVIC at 66 MHz
SW 3	Disables the optical link (only valid on the PIB 6802 with SW1 ON) OFF ODL is disabled. The optical fiber can be disconnected ON ODL is enabled. The optical fiber must be connected
SW 4	Not used

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NOTE

SW1 must be selected according to the side on which the PVIC Monarch node is located within the PVIC cable chain.
SW3 permits to disable the ODL while no optical fiber is connected without unmounting the PIB 6802 from its motherboard.
In the figure 13.6, the PVIC Monarch (node ID = 1) is located on the left side of the PVIC cable daisy-chain.

Figure 13.6: ODL Cabling Example



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Chapter 14
Installing the PVIC

The PVIC is designed to work within the following environmental specifications:

- Operating temperature 0° C to 50° C
- Forced air cooling
- Anti-static environment



CES accepts no responsibility for failure should these conditions not be respected.

14.1 Unpacking the PVIC

The PVIC is shipped in a box with protection from electrostatic discharges. A CES sticker is listing the name of the board, the reference number and the serial number.

The PVIC itself is wrapped in a special plastic bag closed by a sticker. When removing the board from its protection be careful not to touch the printed circuits with the fingers and use electrostatic discharge (ESD) protection.

For the part numbers of the PVIC interfaces, PIBs, cables and terminator refer to section 1.2.

14.2 Installing the PVIC

- Set the PVIC switches according to your needs. The first PVIC node must have Node-ID 1 and each further a unique Node-ID] 1 ≥ 15 (see also sections 8.3, 9.3, 12.3).
- In case the PIB is not already mounted on the PVIC interface card plug the PIB in its foreseen socket on the motherboard and fix it carefully with four screws (see also section 13.1).
- In case you use a PVIC bridge interface (8426) be aware that the PIB on Port A must point towards the PVIC monarch (Node-ID = 1) and that the monarch can not be a PVIC bridge (see also section 12.6)
- Power-off the VME, CompactPCI crate, PC or Workstation.
- Mount or insert the PVIC interface card:
  - 4025/4425 into the CompactPCI crate.
  - 7225 into the PCI Bus of your PC or Workstation.
  - 8025 into the VME crate.
  - 8425 onto a PMC socket of the CES RIO2 806x or 406x PowerPC board and insert it into the VME or CompactPCI crate. Fix the PMC carefully.
  - 8426B onto the CES RIO2 8062 PowerPC board and insert it into the VME crate.

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- 8426D onto the VME64x crate, into the slot at right of the CES RIO3 8064 board. Then plug the rear-mounted backplane BPA 6413 or BPA 6414 to connect the PVIC 8426D P0 connector and the RIO3 8064 P0 connector together.

- Connect the PVIC cable(s). Remember that the DIFF cable is not symmetric (see section 13.3).
- In case you use an optical PIB 6802 (ODL) set the dip-switches according the location of the PVIC Monarch (Node-ID = 1) and the PVIC Clock to be used (see section 13.4).
- In case you use GTL+ or DIFF mount a PVIC cable terminator at each physical end of the PVIC cable chain (see sections 13.2 and 13.3).
- Fix the DIFF connectors carefully.
- Before you power-on check that you have not accidentally mixed GTL+ and DIFF cables, connectors and terminators (they all look quite similar) and that you have not plugged a PVIC connector onto a SCSI socket. Be aware that this might damage the PVIC or SCSI interface.
- Power-on the VME, CompactPCI crate, PC or Workstation.
- Install the PVIC software and follow the instructions in the Generic PVIC Online Library Documentation to initialize, test and use the PVIC system (see section 1.5).

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