Fast Cluster

2000 SERIES

Rugged
High Performance Scalable
Embedded Clusters



CSPI
MultiComputer Division

GASS improves real-time target, ocean & sensor modeling capabilities of Navy ASW trainers.

Hydra Sonar Systems are incorporated into the Swedish Navy's Visby class ships

SAPPS will be used by the Royal Swedish Navy to analyze active and passive sonar records

Innovative Solutions from CSPI

Cluster computing is rapidly becoming the preferred technology for Embedded High Performance Computing (HPC). Early adopters are now turning to proven commercial turnkey solutions to capitalize upon the open source Linux environment and MPI as the preferred message passing paradigm making it possible to go from research to deployment without any software changes accelerating the development cycles.

A large class of DOD applications require HPC systems to run simulations based upon complex models demanding the processing power of 100's to 1000's of processing nodes. Memory requirements also increase proportionally with the complexity of these problems.

Complex real-time signal processing and analysis applications require scalable platforms to meet the requirements of large radar and sonar systems, trainers and simulators. Meeting the challenge of the future, clustering solutions using standard COTS technologies and open source software are the best path to offer hardware and software technology insertion, support and affordable development costs.

Rugged Platforms

The FastCluster 2000 SERIES features the compute processing density, rugged packaging, low power, high availability, outstanding performance, scalable open architecture and clustering technology required to support sonar, radar, Command, Control, Communications, Computers, Intelligence, Surveillance and Reconnaissance (C4ISR) applications intended for deployment in the harsh and confined environments of shipboard, airborne, and land-mobile platforms.

FastCluster 2000 SERIES:
The Ultimate Benchmark is Success in the Field

Variants of Mk92 fire control systems are installed on FFG-7 frigates worldwide

Experience

CSPI was founded in 1968 and has over 30 years of experience specifying, designing, and manufacturing commercial and rugged COTS products that deliver architectural peak performance in compliance with standards.

CSPI hardware expertise includes ASIC design for memory controllers and I/O for RISC and DSP architectures ranging from the early i860 and SHARC to the more current PowerPC and AltiVec. In addition, most CSPI product designs involve the integration of the Myrinet chipset switches and network processors. With a focus on delivering ultra dense COTS systems CSPI has extensive experience with multi-layer PC boards, backplanes, systems packaging, ASIC and FPGA designs.

CSPI software expertise includes optimizing signal processing libraries and O/S support for Linux, VxWorks, SuperKit, and PSOS.

CSPI has been selected for a wide variety of DOD programs because our product offerings include several options to afford the customer flexibility in selecting the best modules to configure a system that meets their application specific needs. A partnership with CSPI provides the customer access to Single Board Computers, Blades, MultiComputers, I/O components, disk drives, cabling and enclosures designed with adherence to standards, integrated and supported by a single vendor.

CSPI has always provided product solutions that are complete systems, integrating both hardware and software. CSPI provides all of the tools and support necessary for the user to develop, deploy and maintain the product that they themselves have created.

Some CSPI Program Wins:

Sonar Signal Processing

The Hydra Program

Computing Devices Canada Ltd.

Stimulation / AWS Trainers
Generic Acoustic Stimulation System (GASS) Program
Northrop Grumman Norden Systems, Inc.

DSP COTS technology upgrade
Mk92 Fire Control System

Lockheed Martin / Indra Sistemas S.A.

Surveillance Radar
Advanced Hawkeye Program (E2-C)

Lockheed Martin

Test and Evaluation
RSG Program (Aegis Combat System)
Lockheed Martin for the U.S. Navy's Combat System Engineering Development Site (CSEDS)

Sonar
Sonar Acoustic Post Processing System (SAPPS)
Array Systems Computing / Royal Swedish Navy

Rugged 2000 SERIES MultiComputers are used in the next generation radar for the E--2C Hawkeye

Open Standards

All FastCluster hardware and software is based on open technology, commodity components and industry standards. This makes it easy for engineers to develop and maintain their applications. The result is reduced costs and increased customer satisfaction. It also means that the user, if need be, can draw upon other tools developed to the same standards to aide in their application development.

Fault Tolerant Features

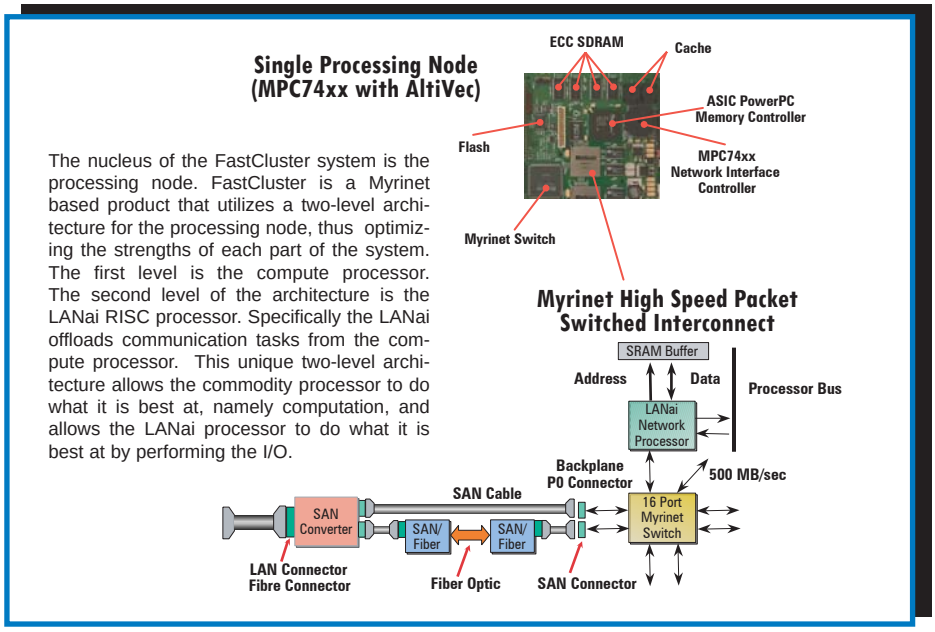
Each FastCluster embedded blade has built-in self-test features and safeguards to monitor and protect against power and thermal events that would interrupt normal system operation.

Live Insertion

All modules support live insertion.

Modularity

Small Line Replaceable Units (LRUs) are used to implement the system reducing the cost of spares and facilitating quick maintenance and deployment.



The nucleus of the FastCluster system is the processing node. FastCluster is a Myrinet based product that utilizes a two-level architecture for the processing node, thus optimizing the strengths of each part of the system. The first level is the compute processor. The second level of the architecture is the LANai RISC processor. Specifically the LANai offloads communication tasks from the compute processor. This unique two-level architecture allows the commodity processor to do what it is best at, namely computation, and allows the LANai processor to do what it is best at by performing the I/O.

Commodity Processor

The first level is the compute processor, which is a commodity processor that has its strengths in its ability to perform multiple gigaflops as well as being a very good general processor. The current processor is the Motorola 7457 at 1 GHz with 2MB of L3 cache.

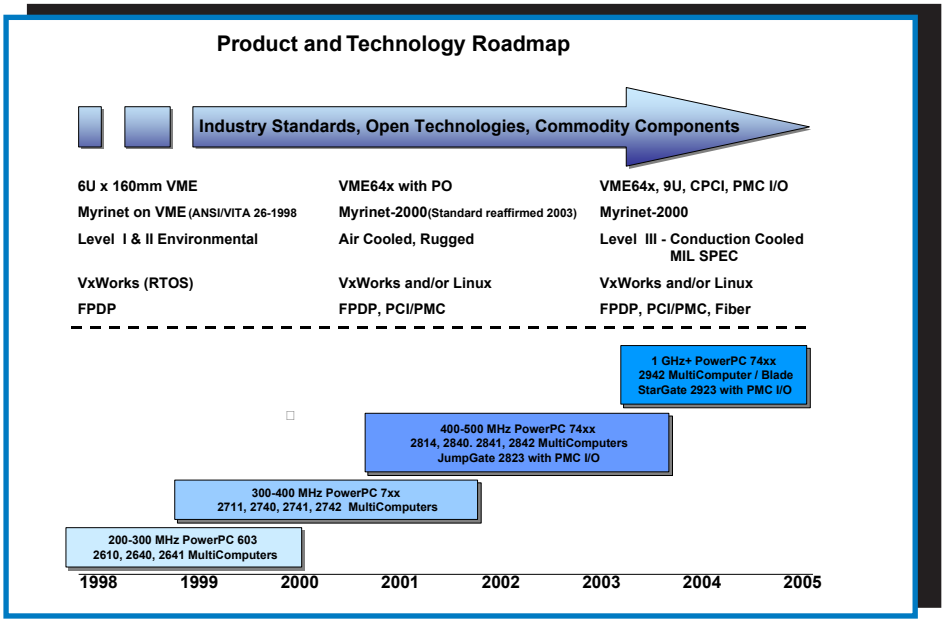
LANai

The current LANai, Myrinet-2000 LANai 9, is capable of transferring data between processors at full duplex speeds up to 250 MB per second in each direction for a total of 500 MB per second per port.The LANai is used in conjunction with a 16 port Myrinet switch to interconnect every processor to every other processor within the system.

FLASH

Every processing node in the system has a large flash memory [32MB] where the operating system resides. This means that each processor can boot from flash greatly increasing the speed of the system booting. Each node can boot stand-alone instead of having to compete with other nodes for a single I/O resource and/or disk resource to boot from.

The user also has access to the FLASH on each node, such that the user application can reside in flash as well. This translates to a fast cold start to run-time mode.



ECC SDRAM

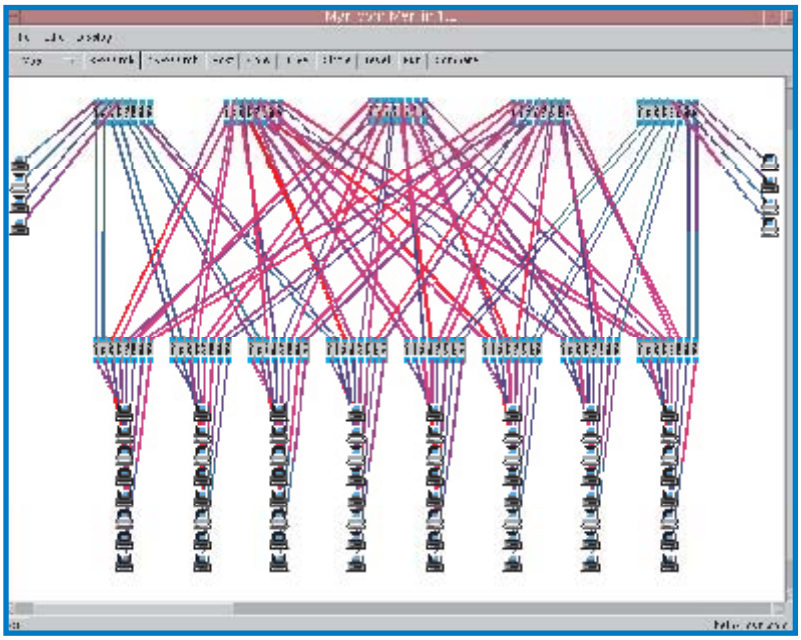
Each node has up to 1 GByte of error-correcting SDRAM.

Switched Fabric Network

CSPI was an early adopter of Myrinet, a high-speed packet-communication and switching technology, and has over seven years of experience integrating this interconnect into multiprocessing systems targeted at defense applications. The continued use of the low power consumption Myrinet components for the interconnect interface on FastCluster products contributes to the viability of the product for defense applications such as C4ISR programs. The benefits of this switched fabric architecture are many: reliability (robustness), scalability (performance increases in a linear manner as the network grows), modularity, interoperability and seamless operation regardless of whether the packet contains voice, video or a data transmission.

Myrinet-2000

Myrinet-2000 is a third generation product based on the American National Standard, ANSI/VITA 26-1998. All components are implemented with full-custom-VLSI CMOS chips. These CMOS-based Myrinet components are extremely reliable. The MTBF of current-production Myrinet switches and interfaces exceeds 5 million hours per port. Myrinet exhibits a very low bit-error rate, and is highly robust with respect to host, switch, and cable faultTransmitting information in data packets routed as point to point communications between sender and receiver Myrinet attains a maximum bandwidth of full-duplex 2+2 Gigabit/second data rate on each link to converge with industry-standard 2.5GBaud 8b/10b-encoded serial links. This protocol permits standard services across heterogeneous processors. Myrinet host interfaces execute a control program to interact directly with host processes for low-latency communication, and directly with the network to send, receive, and buffer packets. The hardware computes and checks a CRC for each packet on each link. The interfaces provide parity checking both in memory and on the PCI bus. Moreover, Myrinet continuously maps itself to find alternate routes, creating a dynamic topology to circumvent faults. This approach enhances data integrity and security by creating a high availability network. The network itself remains available because it can detect and isolate points of failure and will re-route information to other hosts to maintain an operational state.

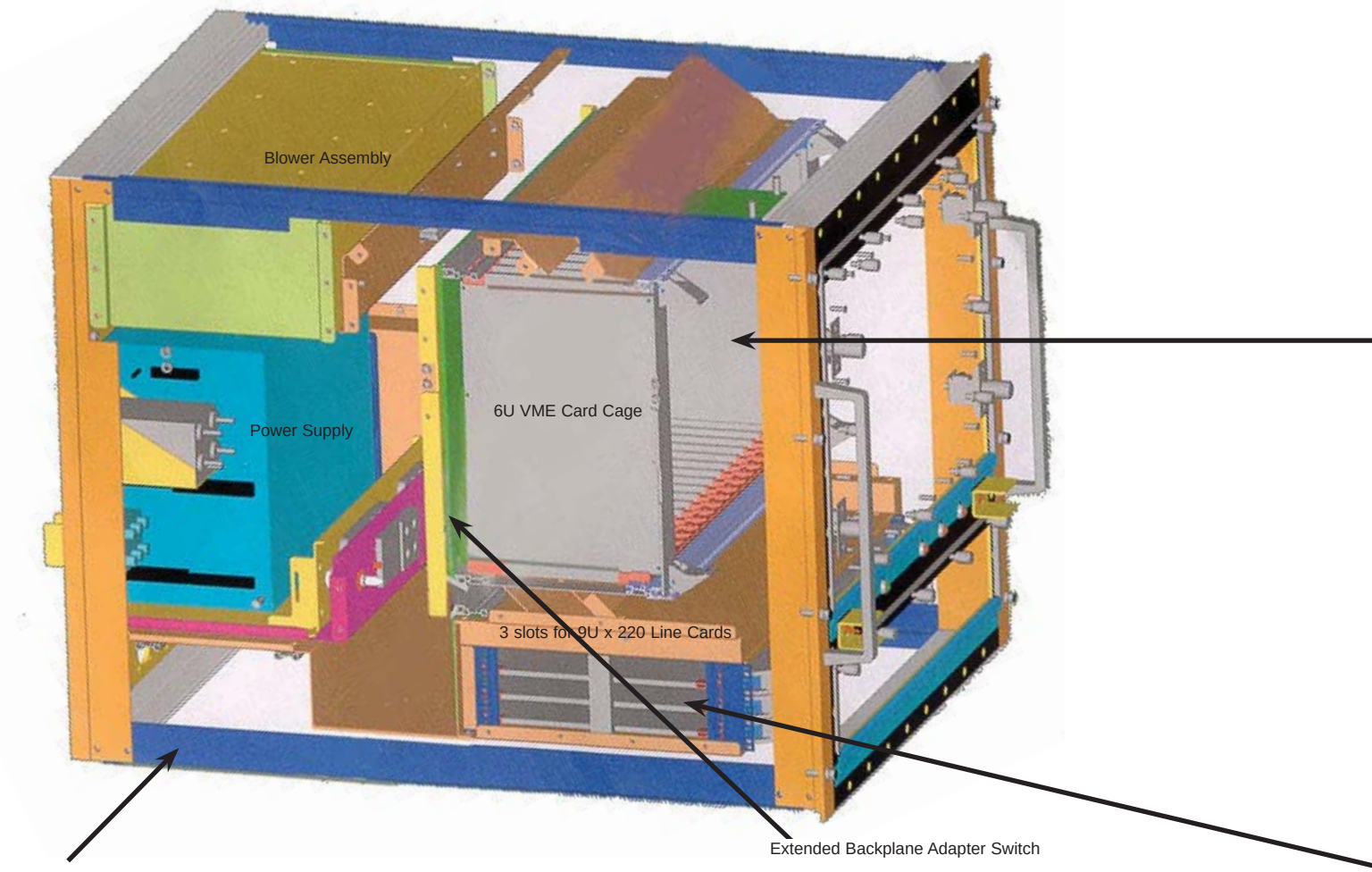


The Myrinet environment provides the capability to monitor, analyze, and simulate network activity. The Merlin 1.2 tool creates a visualization of the current network topology showing all nodes, switches, and the interconnect paths between them. This graphical representation employs a color-coding scheme to display network traffic intensity, offering a quick overview of the communication patterns and data volume transferred between nodes and systems.

Leading Technology

Myrinet is now the market leader in HPC Clusters with 187 systems in the Jun-04 TOP500 (500 fastest clusters) utilizing Myrinet technology. Some of these systems are implemented with 1000's of nodes. CSPI's scalable FastCluster systems leverage the Myrinet clustering technology, the chipset (network processor and switch) and the Myrinet well proven software stack (MPI, GM) for DOD embedded systems. Every compute node is interconnected to every other compute node with the same interconnect (Myrinet-2000) so the user can predict I/O performance as well.

A Clos network architecture is implemented to ensure the best bisection bandwidth for the system. In addition to high-speed transmission Myrinet delivers flexibility with a clustering technology that can switch many different protocols, including Gigabit Ethernet, providing a seamless migration path for the future.



20 Slot Rugged Chassis

Partnering with Elma, CSPI is able to offer a 20 Slot Rugged Chassis designed to meet the harsh environment of shipboard and airborne applications. The chassis has been successfully tested numerous times to environment levels of MIL-STD-810E and MIL-STD-167 and to the EMC requirements of MIL-STD-461E.

The system, packaged in a standard 19" rack configuration has a height of 35" and a depth of 25". The front of the unit contains power and reset switches and voltage indicators along with fan fail and overtemp indicators.

All plug-in circuit boards are removable from the front. All fiber optic signals are connected to the front of the cards and are cabled to the rear interface panel such that all connections to external equipment are available in the rear of the unit. The system power supply is mounted on a shock isolated platform near the rear of the chassis and all cooling air is pulled through an EMI filtered rear panel.

Extended Backplane Adapter Switch (EBAS)

The latest CSPI ruggeded chassis utilizes an acitve backplane switch module to interface between the VME 6U backplane and the 9U line cards.

Other CSPI chassis employ Backplane Overlay Switch Modules or Adapters to provide cut-through routing that is used to implement the network interconnect. Message packets flow through switches which automatically select link data rates according to the type of cabling used. These switches are physically small, low-power, self-initializing devices that can be placed in any location for convenient cabling of the network. Several types of switch modules are available to accommodate configuration differences.

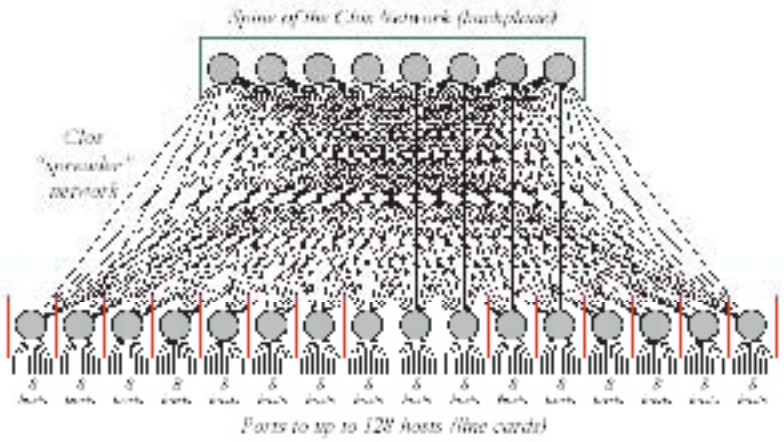
Backplane Overlay Switch Module

FastCluster 2942 Blade

6U Board

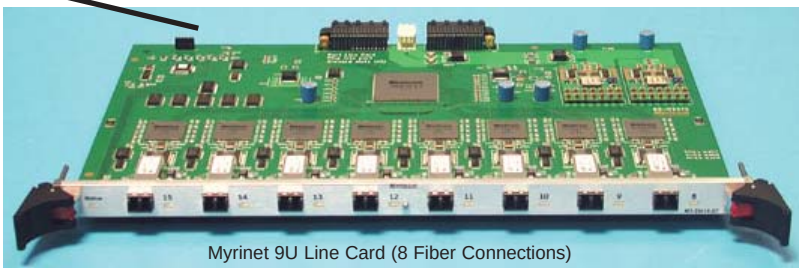
The 6U card cage is designed for processor or I/O boards. It might feature the new FastCluster 2942 blade incorporating a host processor that provides increased performance and efficient power consumption to satisfy the most stringent demands of our defense customers.

Designed with four 1 GHz Motorola 7457 high performance, low power, 32-bit PowerPC microprocessors directly on the motherboard, the FastCluster 2942 6U VME blade eliminates the use of mezzanines to optimize compute density, airflow and cooling



Clos Network

The Clos network, first described by Charles Clos in a paper published in 1954, has several properties that make it an ideal topology for a cluster network: the ability to scale to a large size, modularity, multiple redundant paths, and full bisection bandwidth.



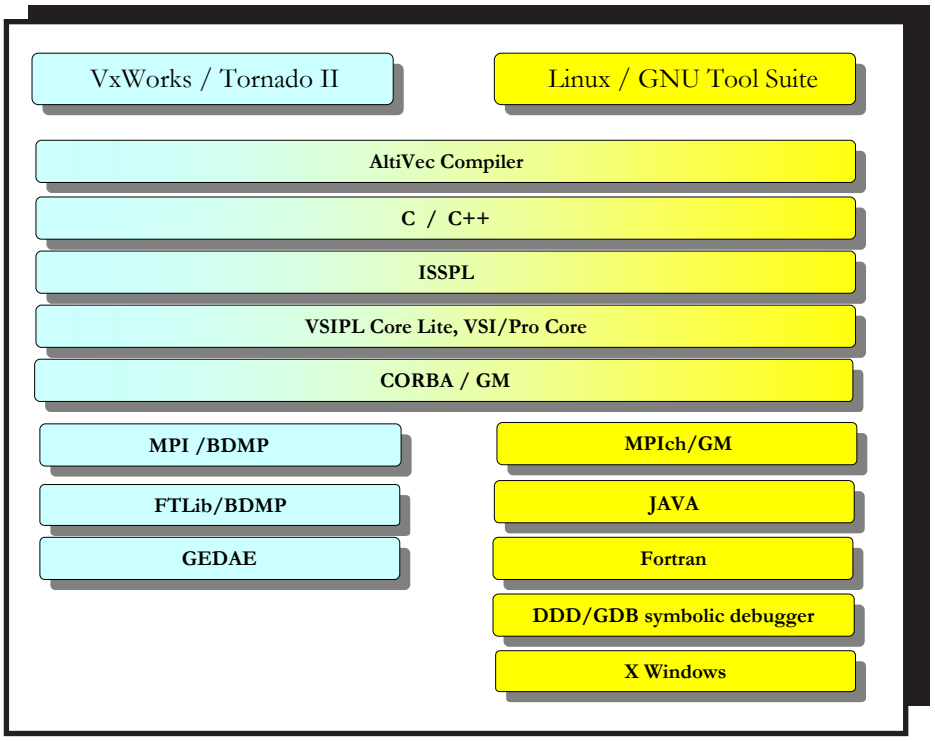
Myrinet 9U Line Card (8 Fiber Connections)

Clos networks require a lot of switches, and a lot of switch-to-switch communication links. The basic building block of the Myrinet Clos Network is a 16-port crossbar switch implemented on a single chip. This crossbar switch is used to create communication links between hosts. This topology creates so many paths between hosts that the minimum bisection of this network -- its traffic handling capacity -- is as large as possible.

The Clos topology providing multiple routes between hosts ensures all the shortest routes are deadlock-free. Each host interface can send successive packets to another host along multiple routes, thus the traffic is dispersed in a way that statistically avoids high utilization of specific network links that can result from single-route mappings.. This same dispersive routing technique provides fault tolerance as it creates redundant paths between hosts allowing for a message to be resend along another route if a failure is encountered.

Myrinet 9U Line Card

The 9U Line Card is designed with a VME PO backplane connector on the rear of the card, a 16-port crossbar switch and eight external connectors on the front panel.



VxWorks / Tornado II

VxWorks, including the WIND Microkernel, is a POSIX compliant real-time operating system environment providing fast multi-tasking, interrupt support, and both preemptive and round robin scheduling for deterministic response to external events.

This efficient RTOS incorporates such features as a scalable run-time kernel to conserve code space and support for many different Application Programming Interfaces (API's). Inter task communication can be accomplished using shared memory, message queues, semaphores, events and pipes, sockets and remote procedure calls, and signals allowing the developer design flexibility to best meet the needs of an application. The integrated networking offers data transmission over the Myrinet fabric. Industry-standard protocols such as TCP/IP, UDP, NFS, FTP, SLIP, BOOTP and Berkley sockets are supported throughout the network as well. This protocol permits interoperability between heterogeneous processors.

CSPI is currently shipping systems with VxWorks 5.4 and Tornado II supporting an application layer that uses C, C++, ISSPL or VSIPL, and MPI to facilitate portability and software reuse

Message Passing Interface (MPI)

This parallel programming library provides multiprocessor control and interprocessor communication. This library provides a simplified way for the programmer to associate specific data with specific processes. The MPI library provides the functions necessary to create dynamically scalable applications. An application may be written on a few processing nodes for simplicity, and then easily expanded to invoke additional nodes for faster execution. MPI is the preferred multiprocessing API for high-performance computing.

MPI, ISSPL and VSIPL are designed to enhance the portability of embedded applications, allowing development on a workstation and ease of migration for implementation in an embedded environment.

Compilers and Debugging Tools

The FastCluster development environment supports the C and C++ compilers optimized for a PowerPC target. Other compilers are available from third party vendors and are easily integrated into the open source, standards based FastCluster platform.

Simple debugging on FastCluster systems can be accomplished using standard “C” assertions to confirm assumptions, by instrumenting applications with print statements dumping the contents of variables or buffers to the screen or a file for later analysis, and by symbolic debugging.

More sophisticated debugging and development tools are available from CSPI and our partners upon request.

Linux / GNU Tool Suite

The CSPI Linux software environment consists of the kernel, libraries, utilities, and development tools. It is based on a POSIX implementation including true multitasking, virtual memory, shared libraries, demand loading, work load balancing, and support for TCP/IP networking. The Linux operating system is easily integrated with clustering software such as MPI and includes a full suite of GNU compiler tools to facilitate development.

Applications developed with Linux and MPI are processor independent and vendor independent. Using standard API's and an open source approach

built on a layered architecture enables collaborative development whereby engineers may work concurrently without destroying each other's contributions. Linux also provides a common software environment permitting the same technology to exist on both the developers desktop (host system) and the deployment platform (target). Available on most processor architectures, Linux promotes the creation of an integrated hardware and software solution. Application code developed on a PC or cluster of workstations is binary compatible with the embedded platform. Linux is of general interest to the modern developer due to these advantages.

Two well-known patches (the preemptive kernel patch and the latency patch) supplement the Linux operating system to drastically improve the real-time characteristics of the kernel. CSPI is shipping these patches with its FastCluster Linux 2.4 release to address the "hard" real-requirements of embedded applications.

Industry Standard Signal Processing Library (ISSPL)

The ISSPL-ALT is a highly optimized library of over 250 functions for 32-bit signal and image processing programs for the PowerPC™ 745x series.

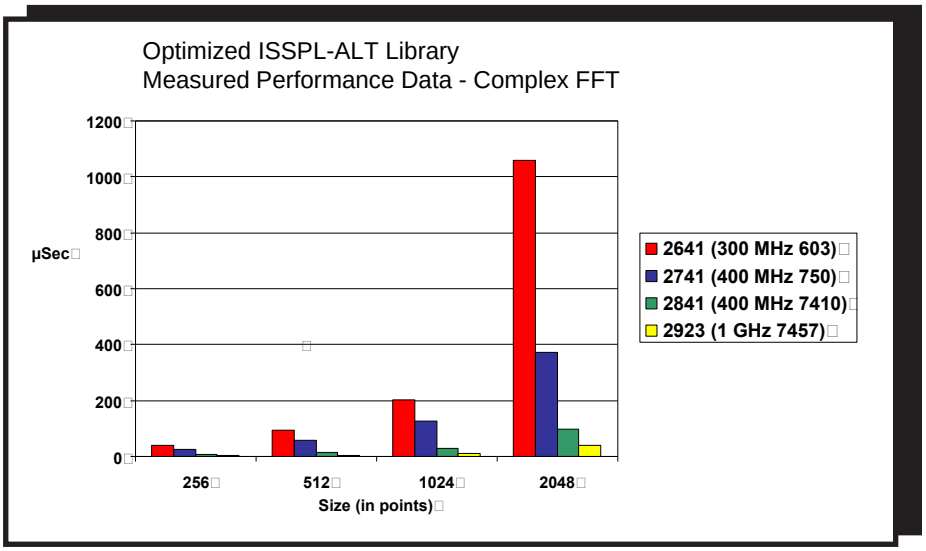
The ISSPL-ALT reduces programming complexity by providing a single calling function for complex mathematical and signal processing routines. Both development and execution times are significantly improved. The ISSPL-ALT provides a full compliment of routines to take advantage of both the AltiVec™ and Floating-Point units of the PowerPC 745x series. All routines are callable from C and C++ compiled programs to achieve rapid and efficient program development. The C emulations of all standard ISSPL-ALT functions are available for initial development work.

As a convenience, there are functions included in the library to provide backward compatibility with earlier versions of ISSPL. These functions assist in converting older programs and help protect the user's software investment. The ISSPL-ALT includes routines from the Floating Point System, Inc. FPS Math™ Library, Quantitative Technology Corporation's Math Advantage™ and the Society of Exploration Geophysicists standard.

Vector Signal and Image Processing Library (VSIPL)

The VSIPL is the result of a DARPA sponsored effort to define an open, industry standard API for vector, signal, and image processing primitives targeted at embedded real-time signal processing systems.
Implemented according to the "Core Lite" profile, VSIPL is a library of 125 functions for vector-based signal processing applications. The function calls are organized into four primary categories: support functions, basic scalar operations, basic vector operations and signal processing. Support functions facilitate object creation and interaction as well as memory management. The scalar and vector operations allow the programmer to perform numerical computation on dense rectangular arrays. Signal processing functions include FFT operations, filtering, correlation and convolution.

The object-oriented design of the VSIPL API employs the concept of blocks and views to provide a level of abstraction from the memory and processor architecture of the underlying machine. A block is a contiguous area of memory used for data storage. Views are a method for classifying the data as vectors or matrices. Blocks and views are created, accessed and destroyed via library functions. Manipulating blocks and views via library functions assists the application programmer in writing code that is truly portable and compatible.



A typical CSPI FastCluster 6U blade incorporates:

1. The latest processor, currently the AltiVec PowerPC, offering the best available general purpose GLOPS/Watt microprocessor.

2. The latest memory technology, error-correcting, 64-bit 100 MHz ECC SDRAM that performs reads at 640 MB/s and writes at 800 MB/s, in configurations at up to 1 GB per processor

3. High-speed interconnect technology, Myrinet-2000, delivering interoperability with previous generation products, low power consumption, and a large endorsement from the HPC community with clusters of 1,000's of nodes already implemented.

4. High Availability features including fast booting from a cold start, hot-swappable hardware and power on self test.

Power On Self Test (POST)

Each Fastcluster node has firmware, residing in the node's flash memory, that consists of a bootloader, a Power On Self Test (POST), a compressed kernel, and a ROM file system (ROMFS). The ROMFS contains the libraries, kernel modules, and executable programs that allow the node to get hooked into the network fabric and to begin executing applications.

Upon power-up or following a hard reset, the bootloader is the first piece of code to execute, followed by POST, if the system is configured to run this test. POST must run in less than five seconds. If a failure is detected, POST saves a diagnostic code in non-volatile memory, then reads two parameters from non-volatile memory. If either OVERRIDE or POST_OVERRIDE is set, POST transfers control back to the product's boot procedure. Otherwise, POST reports a failure code.

POST begins with verification of the CRC-32 checksum of the POST itself. This confirms that the POST program itself is not corrupted. POST then proceeds to verify the correct operation of a small region of low memory. This region is used for stack, interrupt vectors, and global variables.This is followed by tests to verify correct operation of data and address signals for the DRAM, CACHE, and LANai SRAM. POST concludes with tests to verify the correct operation of DMA to and from main memory and the LANai memory as well as checking the operation of all external interrupt signals.

In the unlikely event that a problem is encountered once a system is up and running, all CSPI systems support live insertion for replacement of 6U Blades and line cards.

I/O Solutions

CSPI I/O processing solutions are based on PMC modular designs. This approach of a node having a PCI interface and a Myrinet network interface allows flexible I/O operations.

Several mass storage options are also possible using the PCI/PMC interface: PMC FLASH, PMC Fiber Channel, a PMC RAID Disk, and/or PMC SCSI disk drives. PMC FLASH memory of 2 GBytes per PMC provides a significant RAM disk capability supported under Linux. This is ideal to configure and download the Linux OS, applications and system tests, and to support the complete stand alone operation of a FastCluster system. This FLASH disk capability is independent of the dedicated FLASH memory available on each processing node (32 MB).

The StarGate 2923 delivers an open and scalable system solution for applications, such as signal processing, that are compute intensive and require high speed data streaming (supported by 2 PMC slots).

The StarGate 2923 utilizes the Motorola 7457 microprocessor with AltiVec™ at 1 GHz and has 1 GByte of ECC SDRAM per processing node and a network interface based on the 250/250 MB/s Myrinet-2000 network fabric.

Environmental Specifications

All CSPI boards are designed to meet the severe environmental specifications encountered in airborne and shipboard programs. During the board design phase, care is taken in the physical layout to optimize airflow paths. A detailed thermal analysis is also performed using the Harvard Thermal Inc. TAS Temperature Modeling System. Several iterations of thermal modeling result in an improved board layout and heat sink design and an optimized thermal profile. From this analysis, along with actual test data, the airflow requirements and operating temperature range is defined.

CSPI uses a rigorous worst-case design approach, which results in wide voltage, temperature and clock frequency margins.

Shock and Vibration

Another important goal in designing circuit boards for an extreme structural environment is to increase the natural frequency of vibration above or between the frequencies at which large forces occur in an airborne environment. CSPI uses printed circuit boards designed with a thermal/stiffener rib to increase structural integrity for shock and vibration. The weight of the board is reduced wherever possible, such as in the choice of heat sink material, to benefit airborne systems where weight is at a premium.

In the hardware design effort, CSPI had a finite element model developed where simulated shock and vibration forces were applied to determine the FastCluster blade design's ability to survive various levels of stress.

Conformal Coating

CSPI provides conformal coating on some board products to meet aggressive humidity and salt spray specifications. CSPI has studied various types of coatings including Parylene, acrylic, and urethane to determine both their ability to protect components from moisture and the ease in which the coatings can be removed to facilitate board repair. In addition, tests were performed to analyze the effect various conformal coatings would have in the case-to-air thermal resistance, and hence the cooling ability, of board components. Analysis of the ability of coatings to protect SMT devices was also done, as those devices are more difficult to protect.

Environmental Parameters	Level I Commercial Industrial	Level II Extended Temperature	Level III Rugged
Ambient Air Temperature Range	0° C to 40° C @ 12 cfm	0° C to 55° C @ 12 cfm	-10° C to 55° C @ 12 cfm
Ambient Air Relative Humidity	up to 95% non-condensing	up to 95% non-condensing	up to 95%* 10 cycles @ 240 hrs.
Maximum Altitude	10,000 ft. **	10,000 ft. **	10,000 ft. **
Shock	15gs @ 11 ms half sine	15 gs @ 11 ms half sine	20 gs @ 11 ms half sine
Vibration (random)	0.002 g^2/Hz 10 - 2000 Hz	0.002 g^2/Hz 10 - 2000 Hz	0.04 g^2/Hz 10 - 2000 Hz
Storage Temperature	-40° C to 85° C	-40° C to 85° C	-40° C to 85° C

* Requires Conformal Coating.
**Ambient Temperature, Airflow and Altitude parameters can be traded off among each other .

FastCluster 2000 SERIES: Chassis Configurations

CSPI Chassis

All CSPI chassis products are designed with the customer in mind. Adherence to standard connections and rack-mountable dimensions make it easy to integrate components in our chassis.

CSPI chassis products are intended to operate in a variety of environments while maintaining form, fit and function compatibility across the product line. These environments can range from trucks exposed to the desert heat to shipboard installations, from a developers desktop to a helicopter or fixed wing aircraft. Each environment has unique characteristics with distinct requirements.

To address these diverse operating and storage environments at the lowest cost to the customer, CSPI offers its products in three classes:

Level 1: Commercial/Industrial
used for development, installation in benign environments

Level II: Extended Temperature
used for systems that operate in an extended temperature environment

Level III: Rugged
used in environments with high levels of shock, vibration, humidity, and extended temperature.

5 Slot Chassis

The CSPI 5 Slot Chassis is an ideal choice for systems requiring a small footprint and Level I and Level II compliance. Removable front panels, rear I/O interface panels, and optional slides facilitate the servicing of components. The chassis is designed to optimize system airflow. Cabling wireways, and peripheral device mounting capability make the most efficient use of the compact space available in the chassis.

The CSPI 5 Slot Chassis uses temperature controlled high output axial fans. Since this chassis may be used in an office environment, the speed of the fans is temperature controlled, keeping audible noise to a minimum.

The CSPI 5 Slot Chassis has been designed to endure the shock and vibration encountered in normal trans portation.

21 Slot Chassis

The CSPI 21 Slot Chassis provides a 9U high, front loaded chassis designed to accommodate a variety of 2000 SERIES boards and transition modules to achieve the scalable processing and I/O performance required by a broad class of High Performance Computing applications.

The CSPI 21 Slot Chassis is another alternative for systems requiring Level I and Level II compliance.

The CSPI 21 Slot Chassis uses a thermal management scheme that optimizes forced air cooling to house a full compliment of 21 multiprocessor boards. Maintaining a high value of air flow allows CSPI's Level I and Level II 21 slot chassis products to operate at elevated attitudes for non-pressurized airborne requirements.

Judicious placement of structural and support members in the CSPI 21 Slot Chassis enhances the ability of the chassis to endure the shock and vibration encountered in normal transportation and exceed those levels for use in many airborne applications.

Additionally, all cables, in both the 5 Slot and 21 Slot Chassis, are routed and restrained to prevent failure and all connectors contain lockdowns to prevent signal interruption.

Environmental Parameters	Level I Commercial Industrial	Level II Extended Temperature	Level III Rugged
Inlet Air Temperature Range	0° C to 40° C	0° C to 55° C	-10° C to 60° C
Ambient Air Relative Humidity	up to 95%* non-condensing	up to 95%* non-condensing	up to 95%* non-condensing
Maximum Altitude	10,000 ft. **	10,000 ft. **	10,000 ft. **
Shock	10 G's 11 ms half sine	10 G's 11 ms half sine	20 G's 11 ms half sine
Vibration	0.002 G2/Hz 10 to 2000 Hz	0.002 G2/Hz 10 to 2000 Hz	0.04 G2/Hz 10 to 2000 Hz
Storage Temperature	-50° C to 100° C	-50° C to 100° C	-50° C to 100° C

* Conformal Coating is available as an option for 100% humidity.
**Ambient Temperature, Airflow and Altitude parameters can be traded off among each other
.

20 Slot Rugged Chassis

The CSPI 20 Slot Rugged Chassis uses a thermal management scheme that maximizes forced air cooling to house a full compliment of 20 6U VME boards. Special card guides that stabilize the circuit boards to withstand higher levels of shock and vibration have been selected to provide the widest possible openings and to ensure all available inlet air is productively used to cool component and heatsink surfaces.

For structural integrity the CSPI 20 Slot Rugged Chassis uses 3mm thick aluminum side plates with spot wielded front, rear, top and bottom extruded aluminum profiles to endure the shock and vibration conditions encountered in tactical airborne and shipboard equipment.

All aluminum parts are enhanced with a protective chemical conversion coating per MIL-C-5541E, Class C for corrosion resistance.

From the initial design phase through to final qualification testing the CSPI 20 Slot Rugged Chassis product maintains a focus on delivering a system package that will perform under the most stringent conditions required by your defense application.

The power supplies in all CSPI chassis products have the highest possible efficiency, consistent with the voltage and current specifications, to reduce internal power supply heat dissipation.

Each chassis product is further equipped with a temperature warning system and shutdown feature in the event that overheating were to occur because of a board, fan or power supply failure.

Additionally, CSPI employs development and production techniques that reduce conducted and radiated emanations and that limit suspectibility to outside electrical and magnetic fields.

The CSPI 20 Slot Rugged Chassis is an ideal choice to meet the needs of military applications and was manufactured to comply with the following MIL specs:

MIL-STD-167	Sinusoidal Vibration
MIL-STD-810E	Shock, Acceleration & Random Vibration
MIL-STD-461D	EMC/EMI

CSP Inc. was founded in 1968 and is based in Billerica, Massachusetts. To meet the diverse requirements of its industrial, commercial, scientific and defense customers worldwide, CSPI and its subsidiaries develop and market cutting edge integration solutions for complex IT environments and high-performance cluster computer systems for military applications. The Company's wholly owned subsidiaries include MODCOMP, Inc. ("MODCOMP"), and CSPI MultiComputer Division ("MultiComputer Division").

The Company's **MODCOMP, Inc.** subsidiary, founded in 1970 which includes the 2003 acquisition of Technisource, is a leading provider of IT solutions and systems integration services. MODCOMP works with third parties to develop customized solutions in the global IT markets and has offices in the U.S., U.K. and Germany.

The **MultiComputer Division** designs and builds high-performance cluster computing systems for the defense market. These systems are dense and rugged with powerful real-time I/O and require minimum physical space or power. These systems are used on land, airborne and shipboard platforms for high speed digital signal processing in radar, sonar and surveillance applications.

Among Our Customers

Alliant Tech Systems - AP Labs – Applied Physics Lab, John Hopkins University
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CSP Inc. 43 Manning Road Billerica, MA 01821-3901

Tel: 978-663-7598 Fax: 978-663-0150 www.cspi.com