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Find the *Curtiss-Wright / VMETRO PBT-615DX* at our website: ***Click HERE***

PCI-X & PCI Analyzer,

Exerciser and Protocol Checker

PBT-615



PCI LOCAL BUS

PCI-X

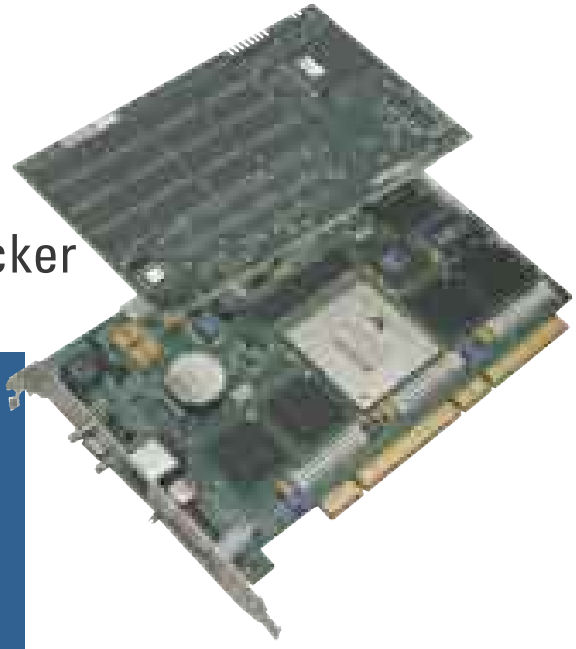
VMETRO

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PBT-615

PCI-X & PCI Analyzer,

Exerciser and Protocol Checker



Features:

State Analyzer:

- 100 MHz State Analyzer for 64-bit and 32-bit systems
- 128K or 256K Trace Buffer with 128-bit wide samples
- Extensive Trace Decoding with Mnemonics and Time Tag and Latency Tag per sample
- Time Tag and Latency Tag per sample
- Protocol sensitive Clock, Transfer or Transaction sampling modes for optimum trace usage and readability
- Demultiplexed Address & Attribute/Data for max trigger and store flexibility
- Search and Extract feature to identify corresponding Split Request and Completion transactions
- Triggering and Trace Decoding of the PCI-X Attribute phase, partitioned in Requester ID, Completer ID, Tag and Byte Count fields.
- PCI-X / PCI mode and frequency detection at power up/reset
- 4 Trigger/Store/Count events including true Range Qualifiers on 32-bit Address and Data (e.g. Address = ABCD1234 - DCBA4321 and/or Data = 01234567 - 87654321)
- 32-levels Trigger Sequencer with Programming Language-like user interface
- Extensive Statistics functions: Bus Utilization, Bus Transfer Rate, Event Occurrence, Command and Burst Distribution.

Built-in Exerciser (CX and DX models):

- 100MHz PCI-X Exerciser (DX only) and 66.7MHz PCI Exerciser (CX and DX)
- Provides true Master and Target for 64-bits and 32-bits systems
- Ease of use with choice of dialog boxes or command line user interface
- Built-in script Recording and Playback engine
- Supports Dual Address Cycles (DAC) and Split Transactions for PCI-X
- Programmable burst lengths and commands
- 8MB Target Memory, available at all times
- Memory Test & Compare functions
- Independent DMA controllers allow insertion of background traffic
- Generates Interrupts
- Exerciser is controlled independently of analyzer

Built-in Protocol Checker (CX and DX models):

- Automatically detects 71 PCI-X and 45 PCI protocol errors
- Trigger output to State Analyzer or optional high-speed Timing Analyzer

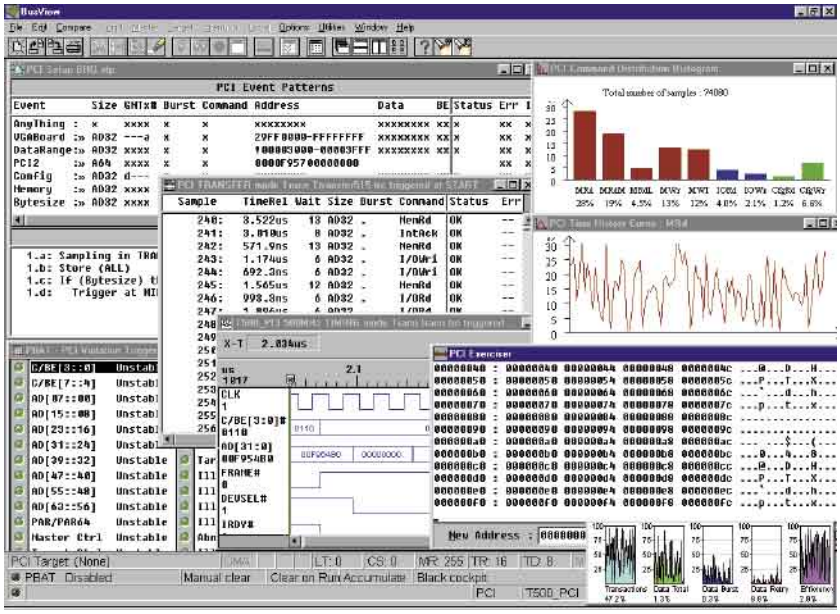
STATE-OF-THE-ART IN PCI-X AND PCI DEBUGGING

As the flagship in VMETRO's range of bus analyzers, the PBT-615 is a PCI-X and PCI Bus Analyzer, Exerciser & Protocol Checker, that is designed for debugging, testing and validation of next-generation PCI-X/PCI boards and systems. The analyzer is able to capture and display all bus activity in PCI-X / PCI bus motherboards up to 100 MHz with powerful trigger and store qualifiers, and offers extensive statistics functions to measure system performance. At the same time, the built-in exerciser unit may act as a PCI-X or PCI master or target controlled through the user-interface or with a built-in script capability, for generation of bus traffic and emulation of not yet available devices. Furthermore, the built-in Protocol Checker automatically detects 71 PCI-X or 45 PCI protocol errors, and can operate concurrently with the state analyzer and the optional piggyback module (PTIMBAT500-PB) for 500 MHz Timing Analysis and Timing Violation detection. The unit is operated through USB or RS232 from a PC running Windows and VMETRO's BusView™ graphical user interface, or via RS232 from an ASCII terminal or terminal emulator. As with all VMETRO analyzers, the unit may be powered from the target system or from an external power supply, and extensive on-line help is available.

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EXPANDABLE WITH PIGGYBACK MODULE

Although the PBT-615 offers a full-featured logic state analyzer with extensive statistics functions as well as a powerful exerciser, the unit can be expanded with a piggyback module (daughtercard) for detailed hardware analysis applications. The PTIMBAT500-PB module offers a 64-channel 500 MHz Timing Analyzer with an ultra-deep 16 MSamples trace buffer. In addition to offering a detailed 2ns resolution view with waveform diagrams of the bus timing, this unit also provides automatic detection of 84 PCI protocol and timing violations, including 50 pico-seconds timing resolution on setup/hold time measurements. The Timing Violation Checker also supports PCI-X control signals up to 66.7 MHz.



ADVANCED TRIGGER AND STORE CAPABILITIES

The PBT-615 uses VMETRO's unique programming language-like trigger sequencer to specify triggers, store and count and delay qualifiers in an "If-then-else…" fashion. Together with the intuitive demultiplexed sampling method (which puts Command, Address, Data and Status as separate items also in the trigger event specifiers) and true inside/outside range specifiers on address and data fields, the user can easily create sophisticated triggers and store qualifiers without having to use multiple events to define trigger attributes of a single transfer. The user can store trigger setups, either in non-volatile memory on the analyzer or on files on the host PC. The analyzer also automatically maintains the current trigger and sequencer setting after power off/on cycling. In sum, all these features allow the user to solve problems quickly, instead of spending hours trying to figure out how to set up and understand the analyzer.

INDEPENDENT SUBFUNCTIONS FOR CONCURRENT OPERATION

As can be seen from the block diagram below, the PBT-615 PCI-X/PCI Bus Analyzer and the PTIMBAT500-PB piggyback module embody a comprehensive set of independent functional units. In essence, this means that there are separate hardware resources for the various functions so that the user, for example, can operate the exerciser while running the state analyzer concurrently. This allows for the monitoring of bus traffic results generated by the PBT-615 and other bus agents simultaneously. Furthermore, with the PTIMBAT500-PB installed, even the 500 MHz timing analyzer and anomaly checker can be run concurrently with the state analyzer and exerciser. This confers maximum debugging efficiency, only made possible by the generous use of hardware resources, an approach in stark contrast with competing products where one common hardware resource (typically an FPGA) is shared for each subfunction, thus allowing only one function to be used at a time.

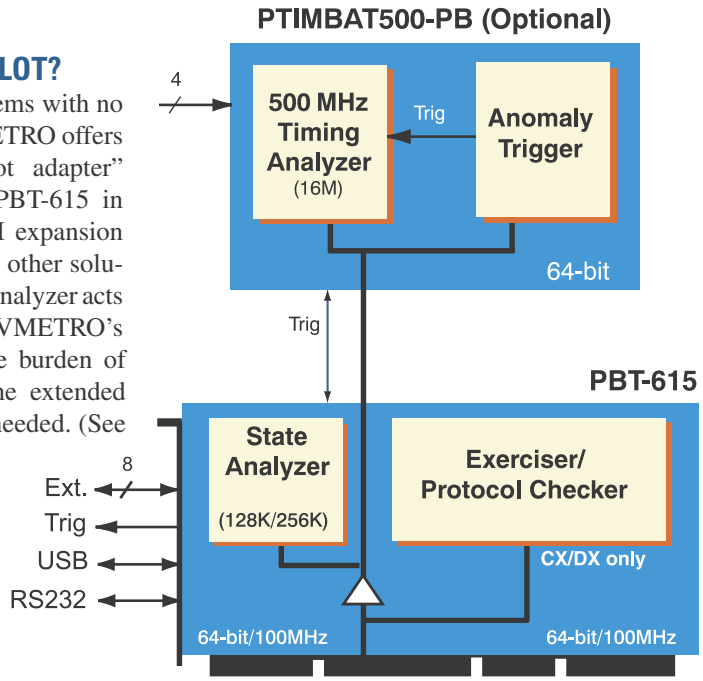
NO SPARE PCI SLOT?

For analysis in systems with no spare PCI slot, VMETRO offers a special "zero-slot adapter" which carries the PBT-615 in addition to one PCI expansion board. Compared to other solutions where the bus analyzer acts as an extender card, VMETRO's approach avoids the burden of an extra load of the extended PCI signals unless needed. (See page 17.)

USB

In addition to a traditional RS232 serial port, the PBT-615 is equipped with a USB (Universal Serial Bus) port. This allows fast and convenient connection between the host PC and the analyzer/exerciser.





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EXTERNAL POWER SUPPLY PROVISION

The PBT-615 has a provision for an external power supply. This makes it possible to use the analyzer in systems with a marginal power supply.

Applications:

- **Software developers involved in I/O-drivers, operating systems, etc.**
- **System integrators putting together equipment from various vendors.**
- **Hardware designers of interface chip motherboards and expansion boards.**

STATE ANALYZER

WITH VARIOUS SAMPLING MODES

The State Analyzer of the PBT-615 captures and displays 64- or 32-bit PCI-X/PCI bus activity up to 100 MHz with highly advanced (yet simple to use) triggering, filtering and counting capabilities. To provide optimum bus analysis for a given problem, the state analyzer offers a choice of three sampling modes. (A fourth sampling mode being offered by the optional 500 MHz Timing Analyzer).

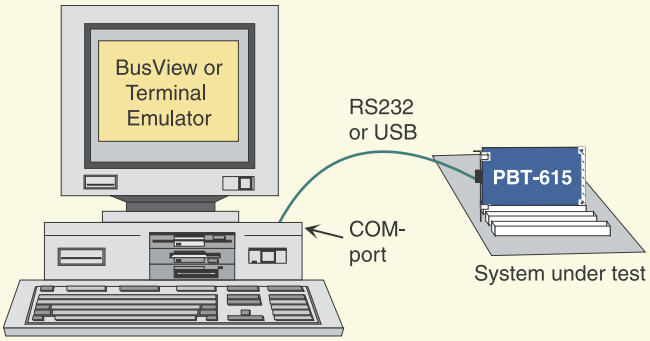
The **Clock** sampling mode is a plain "clock-by-clock" sampling mode as found in any state analyzer. Augmented by address phase highlighting and command mnemonics, this is highly suitable for low-level hardware oriented analysis of the bus protocol.

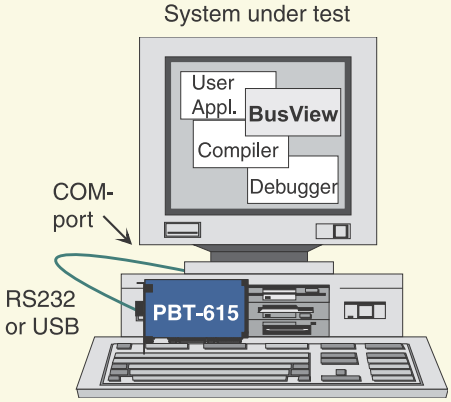
HIGH-LEVEL BUS SAMPLING

For software and system integration issues, debugging the PCI bus on a clock-by-clock basis is not productive, the user would have to spend time on understanding the bus protocol rather than investigating the actual problem. For this reason, analysis on a higher level is required, with focus on bus traffic rather than the bus protocol. Therefore, VMETRO offers two additional unique higher level sampling modes, aimed at producing a more meaningful trace for software and system engineers. One such mode is **Transfer Mode**, in which the analyzer hides details about the bus protocol for the user, and avoids sampling during idle or wait states. This is done by means of protocol-sensitive bus sampling, de-multiplexing of address/data (for 32-bit data transfers), internally generated utility signals for burst detection etc., and extensive use of mnemonics. This allows the user to focus explicitly on the essential Command, Address, Data and Status values, both in the trigger event specifiers and in the trace display. In addition, the user is given information about time from trigger, time between transactions and transfers, the latency or number of wait states per transaction and whether a transfer is part of a burst or at the start of a burst. The other higher level sampling mode is **Transaction Mode**. This is similar to Transfer Mode except that instead of displaying Data, it displays the total Burst Length for each transaction. In this mode, a vast number of PCI transactions are stored in the trace buffer, producing trace that is optimal for system behavior analysis, validation and performance tuning.

TRACE BUFFER OPTIONS

The PBT-615 state analyzer is offered with 128K or 256K samples trace buffer, where each entry represents either a clock cycle, an address or data transfer (for 32-bit data complete with command, address and status values) or a transaction, depending on the chosen sampling mode as described above.





Typical Configurations:

1. EXTERNAL SYSTEM UNDER TEST

- PC running Windows™* and VMETRO's BusView™, or
- ASCII Terminal (VT100 compatible) or
- PC/Workstation with VT100 Terminal Emulator

2. SELF HOSTED

PC running Windows™* and VMETRO's BusView™ together with User's Application and other development tools.

RUN FROM WINDOWS OR TERMINAL (EMULATOR)

Typically, the PBT-615 is operated from a WINDOWS PC, with VMETRO's graphical user interface BusView™. However the product may also be used in a non-Windows environment (e.g. UNIX) thanks to the built-in Terminal user-interface, compatible with ASCII terminals (or emulators thereof) such as VT100 and many others.

* Supported Windows™ versions are: Windows 98, NT 4.0, ME and 2000.

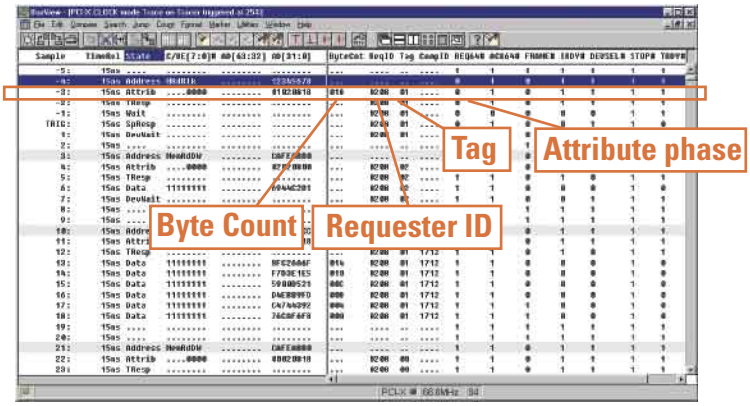
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PCI-X SPECIFIC FEATURES

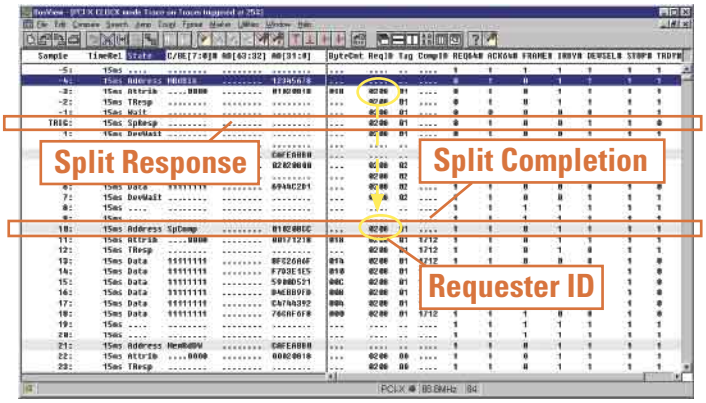
The PCI-X bus protocol includes a number of advanced features such as

- **Attribute phase**
- **Split transactions**
- **Relaxed ordering**
- **Non-cache-coherent transactions**
- **Optimized wait states**
- **Standard block size movements**

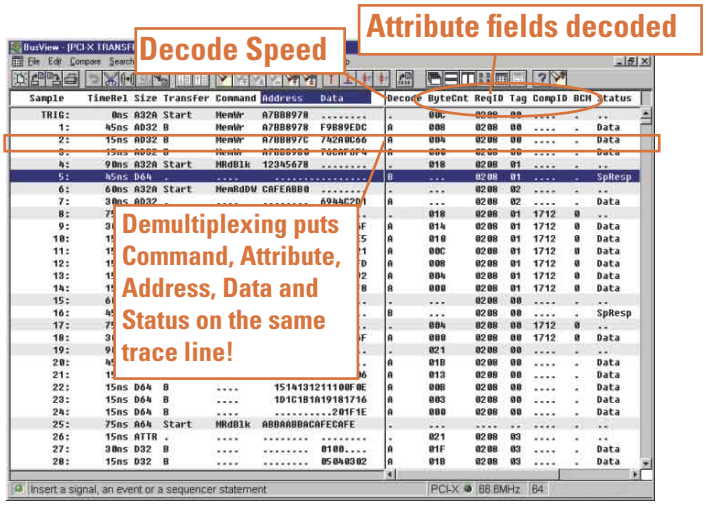
These new features complicate the task of analyzing the bus considerably, unless sophisticated sampling techniques and trace decoding is employed such as in the PBT-615. As an example, the Attribute Phase is presented with separate trace columns for each of the subfields (Byte Count, Requester ID, Tag and Completer ID), dramatically simplifying the process of understanding the captured trace.

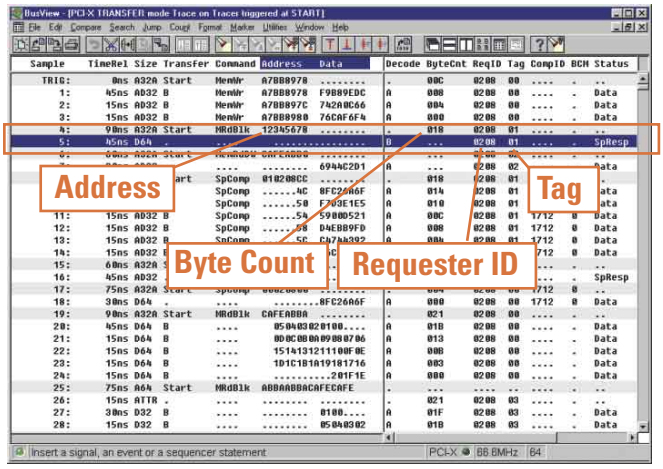


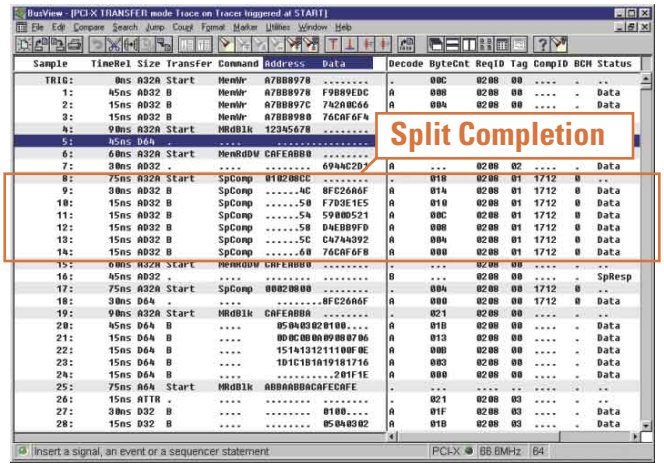
The high degree of decoding, even in Clock Mode sampling, also allows a Split Transaction to be easily spotted, as in the following figure:



For an even more compact presentation, Transfer Mode Sampling is very useful. The sequence screens shown below illustrates some of the decoding capabilities of the PBT-615 and how easy it is for the user to "digest" the trace information.



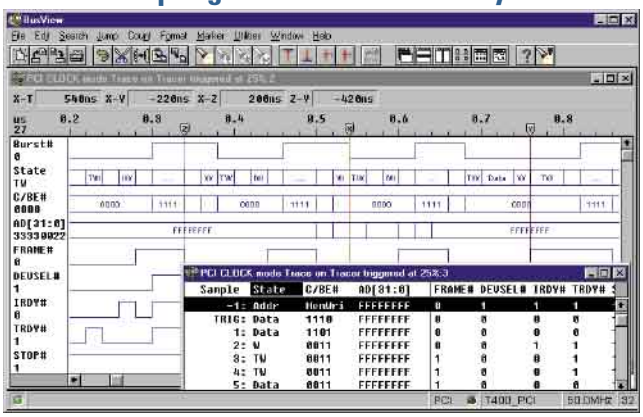


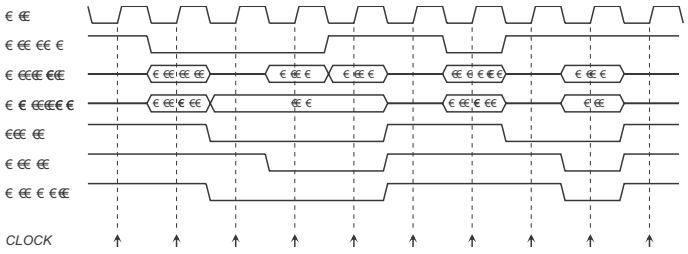


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When sampling the PCI-X/PCI bus, the PBT-615 captures 91 bus signals, 8 external signals plus internally generated time tags and utility bits (128 bits total) into a 128K Trace Memory, optionally 256K. This is a vast amount of information, so in order to give the user the most suitable display for different applications, the PBT-615 offers three different ways to capture the bus activity:

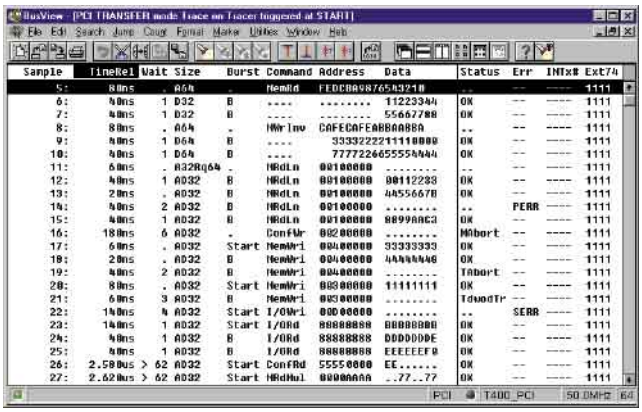
CLOCK sampling - For Hardware Analysis:

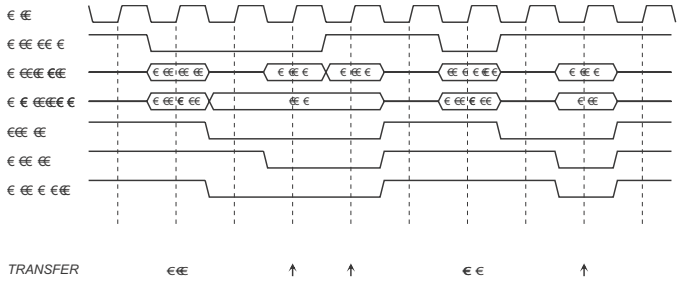




Stores one sample per PCI-X/PCI clock cycle. This captures all the details of how the PCI bus is exercised, clock-cycle by clock-cycle. This is useful to verify the behavior of hardware, such as bus interface state machines. In this mode, no demultiplexing takes place, all signals are captured straight from the bus and displayed as a list and/or as waveforms.

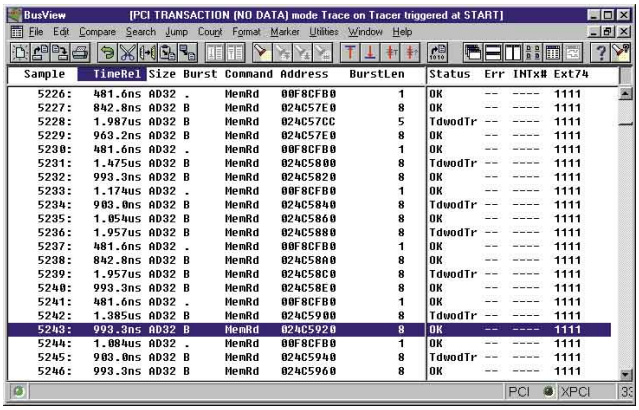
TRANSFER sampling - For Software Analysis:

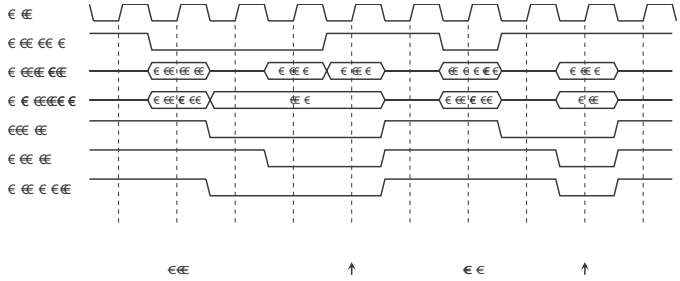




Stores one sample per valid Data Phase. For 32-bit transfers, each sample also includes the Address and Bus Command which is latched from the address phase (demultiplexing). Signals are grouped for easy interpretation of the bus activity. This is the optimum way to analyze bus transactions during Software development.

TRANSACTION sampling- For System Analysis:





Similar to Transfer Mode except that instead of displaying Data it displays the total Burst Length for each transaction. In this mode, a vast number of PCI transactions are stored in the trace buffer, producing trace that is optimal for system behavior analysis, validation and performance tuning.

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DEMULTIPLEXED ADDRESS / DATA

The PCI-X/PCI bus multiplexes Address and Data into a common 32-bit or 64-bit bus. In a similar way, the bus COMMAND signals are multiplexed with the data byte enables (BEx#). This saves system cost, since the number of pins on chips and connectors is reduced. However, multiplexing makes it more difficult to analyze the bus using a regular logic analyzer, since a given sample does not contain all information about a bus transfer. To overcome this, the PBT-615 has the capability to demultiplex Address/Data and COMMAND/BEx# into separate trace channels. This is possible since the PBT-615 has as many as 128 trace channels (for 32-bit transfers), a luxury found only on the most expensive logic analyzers. This important feature not only simplifies readability of the trace, but allows powerful triggers and store qualifiers involving both address and data to be defined easily.

SLOT-SPECIFIC OR USER-DEFINED SIGNALS

The PCI bus has certain slot-specific signals, such as the Request (REQx#) and Grant (GNTx#) signals used for arbitration. These signals can be brought in through eight external inputs on the pin headers on the back panel. The external inputs, fully available in the trigger words, can also be used for any user-specific signals.

GRANT LATCHING

When the slot-specific GNTx# signals are connected as described above, a special latch may be activated to hold the value of the active grant during all data phases. The latched GNTx# value is available in the trace, triggers, store conditions and statistics.

TIME & WAIT STATES TAGS

The PBT-615 provides a high-resolution Time Tag for each sample in the trace list. The time tag may either show relative time between each sample or absolute time from the trigger point.

A second tag in the trace display shows the latency for each PCI transfer, which is defined as the number of wait states from FRAME# asserted to TRDY# asserted.

PBT-615 MODELS

The PBT-615 PCI-X and PCI Bus Analyzer, Exerciser & Protocol Checker is available in three different models to meet various customer needs.

The PBT-615B is an entry-level model, offering a powerful 100 MHz PCI-X and PCI state analyzer with a 128K samples deep trace buffer and a full set of statistics functions.

The PBT-615CX has, in addition to the PBT-615B a 256K trace buffer, a built-in PCI-X and PCI Protocol Checker, and a 66.7 MHz PCI Exerciser with complete master (initiator) and target functions, that also includes a fully user-accessible 8 MB target memory with user-defined BARs.

Both the PBT-615B and PBT-615CX are universal cards in that they are capable of operating in both 5V and 3.3V signaling systems.

The PBT-615DX is a top-of-the-line model with all the features of the PBT-615CX, plus a 100 MHz PCI-X capable Exerciser with complete master (initiator) and target functions, that also includes a fully user-accessible 8 MB target memory with user-defined BARs. As a consequence of acting as a PCI-X master and target at clock frequencies up to 100 MHz, the PBT-615DX is a 3.3V signaling card, while still offering full PCI and PCI-X support.

All PBT-615 models support both PCI-X and PCI, and provide automatic detection of bus type and clock frequency at power-up.

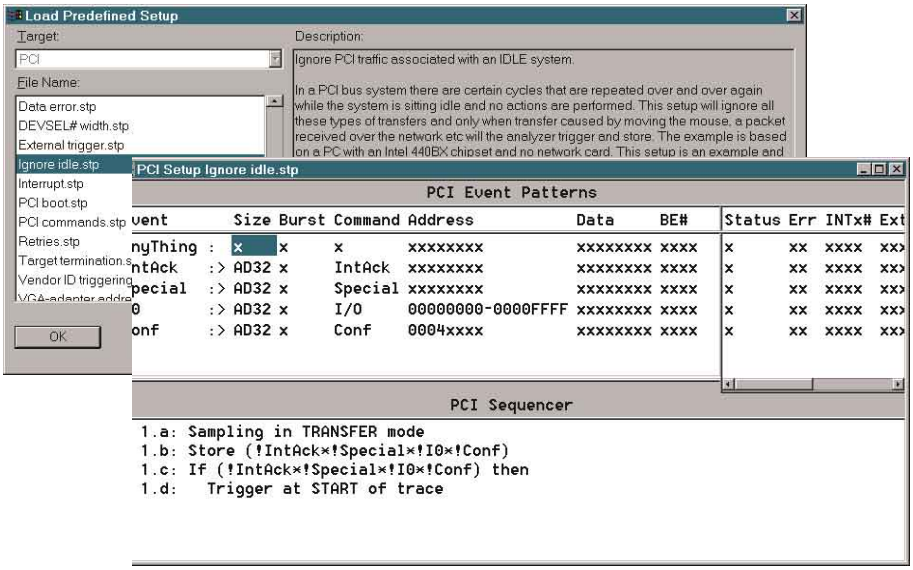
The table below summarizes the various options available in all three PBT-615 models:

	PBT-615B	PBT-615CX	PBT-615DX
Trace Memory	128K	256K	256K
5V Signaling Compliance	✔	✔	–
Protocol Checker on Baseboard	–	✔	✔
PCI Exerciser & Target Memory	–	✔	✔
PCI-X Exerciser & Target Memory	–	–	✔
Applications	Software test and debug of PCI-X & PCI, including all legacy systems (5V).	Software and Hardware test and debug of PCI-X & PCI, including all legacy systems (5V).	Software and Hardware test and debug of 3.3V PCI-X & PCI systems.

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Powerful Trigger & Store Qualifiers

To narrow in on the cycles of interest, the PBT-615 is equipped with powerful triggers and store qualifiers, based on four full-width word recognizers and a flexible sequencer. Each of the word recognizers offers powerful operators like RANGE, NOT and BINARY for address and data fields etc., and the user may specify signal values as hex, binary or mnemonics like "MemRd", "IOWri", etc. This eliminates the need for the user to remember the actual signal values for the different cycle types.



BINARY DETAILS

Values for multi-bit fields like Address and Data are typically entered in hexadecimal format. But occasionally one may want to specify values of individual bits only, like setting bit 15 to 0 and/or bit 0 to 1, and so on. Called "Binary Details", this is another unique feature of VMETRO's bus analyzers.

ADDRESS/DATA RANGE

Each of the four word recognizers allows precise address and data ranges to be defined, with both 'inside' and 'outside' possibilities. This allows the user to trigger, store or count on accesses to a specific area, e.g. a particular data structure or a HW device. Note that the range can be specified with any arbitrary value down to the last digit, while most other analyzers only allow 2^n size ranges to be defined (by setting don't care in the LSBs).

32-LEVEL SEQUENCER

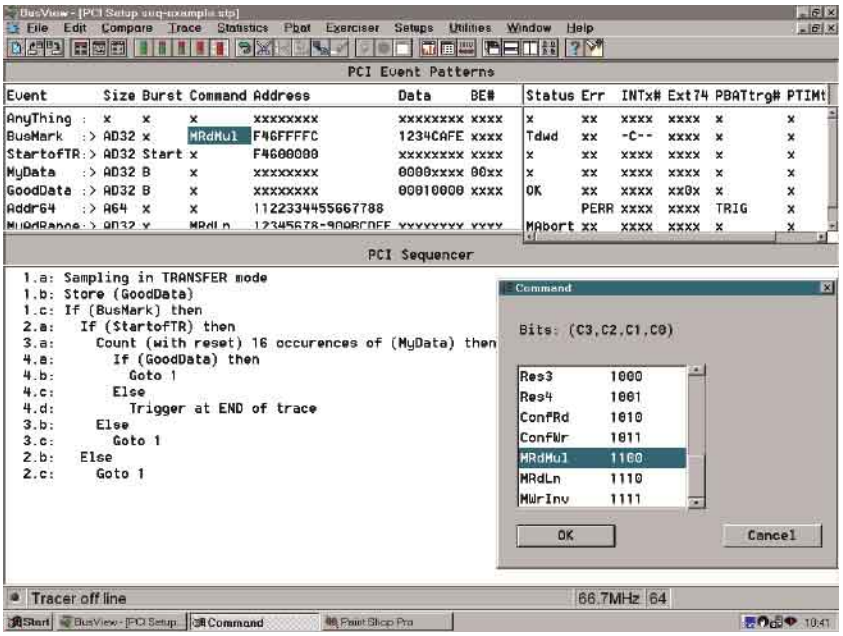
The PBT-615 provides an advanced 32-level Trigger Sequencer with powerful operators like IF, ELSIF, ELSE, STORE, COUNT, DELAY and GOTO. The sequencer is shown in a separate window on the main status screen, and may be used to define nested trigger conditions, define store qualifiers, count and delays statements.

SINGLE EVENT MODE

In many cases a simple trigger like "If Event X then Trigger" is sufficient. For this purpose, there is a default "Single Event Mode" which simply provides a trigger on the event pointed to in the Event Patterns window. When a more complex trigger is required, or a store or count qualifier is needed, the user may switch to the "Sequencer Mode".

PREDEFINED SETUPS

To assist the novice user in defining trigger setups, and to provide a "short-cut" to a number of typical trigger scenarios. BusView offers a function called "Predefined Setups". This function programs the event patterns and sequencer with the appropriate values and commands for the selected task (see dialog box above).



FIVE TRIGGER POSITIONS

For maximum flexibility, the trigger can be placed at five different positions in the trace buffer: Start, 25%, Middle, 75% and End of Trace.

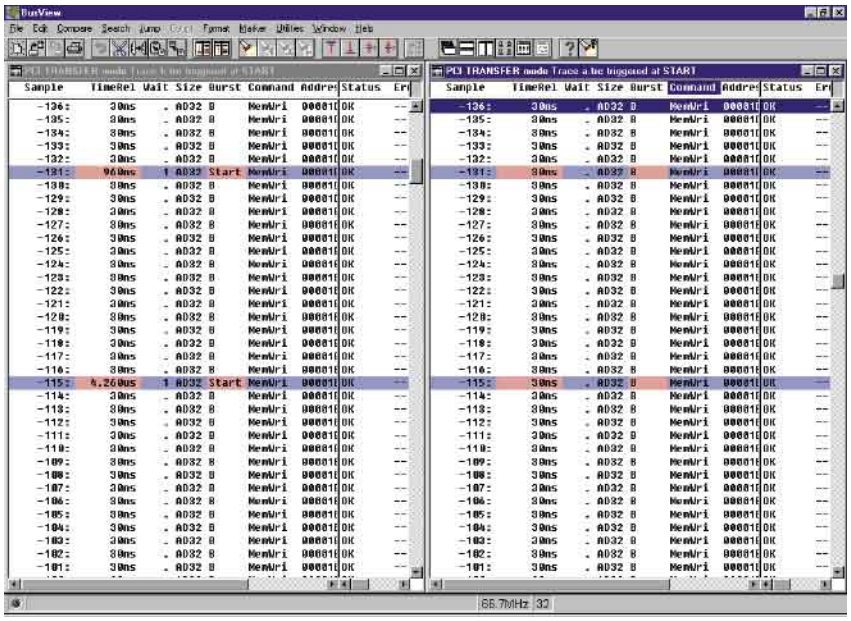
TRIGGER OUTPUT

A Trigger Output signal is available on a pin header on the back panel. The TTL compatible signal has selectable polarity and mode, i.e. the signal may simply change logic level on trigger, or it may be selected to pulse when a trigger or a valid store condition occurs. The Trigger Output signal is useful for triggering external instruments like high speed oscilloscopes, counters, etc.

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TRACE COMPARE

A powerful feature of BusView is the ability to compare the contents of the trace buffer with a trace stored on file on the host PC. This greatly simplifies error location, for example in cases where a system works fine under some circumstances but not under others. Or when one out of several presumably identical systems fails, one may use the Trace Compare function to rapidly spot differences between the failing and functioning systems (see figure at right).



DUMP TRACE TO FILE

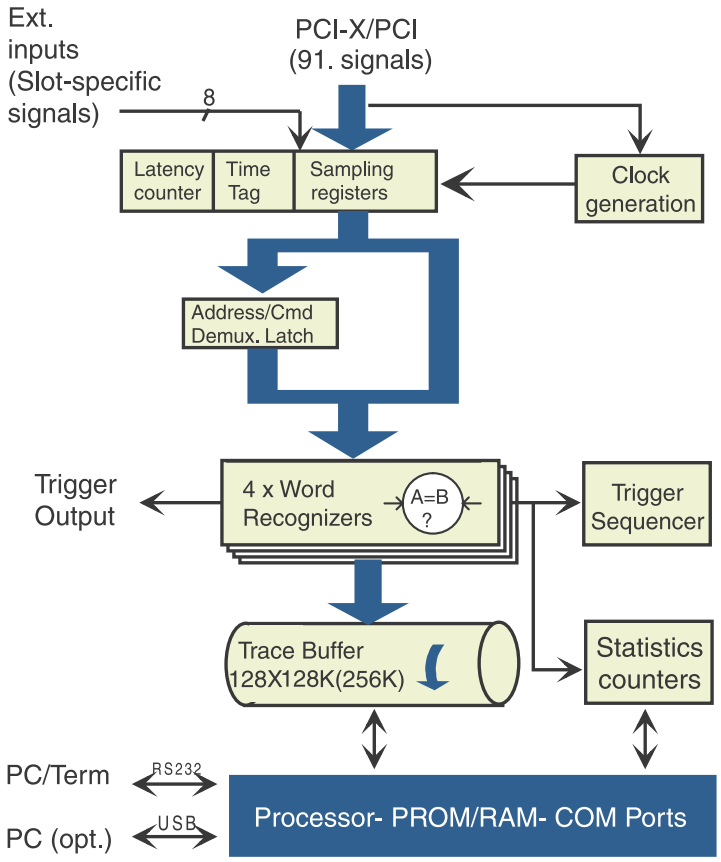
Captured trace data may easily be dumped to a binary or ASCII file on a PC and then loaded back later by means of Dump/Load commands. Partial traces may be loaded, and a packing algorithm reduces transfer time. Trace files may also be reviewed locally on the PC using BusView for Windows, or a DOS Simulator of the Terminal User-Interface.

SEARCH & EXTRACT TRACE DATA

Powerful Search and Extract functions are provided for easy location of particular samples in the trace memory. After a trace is collected, any combination of signals can be searched for in the trace buffer. It is also possible to qualify the displayed data with the search pattern, providing an extracted trace listing, with recalculated time tags, for rapid identification of data of interest.

VERSATILE WAVEFORM DIAGRAMS

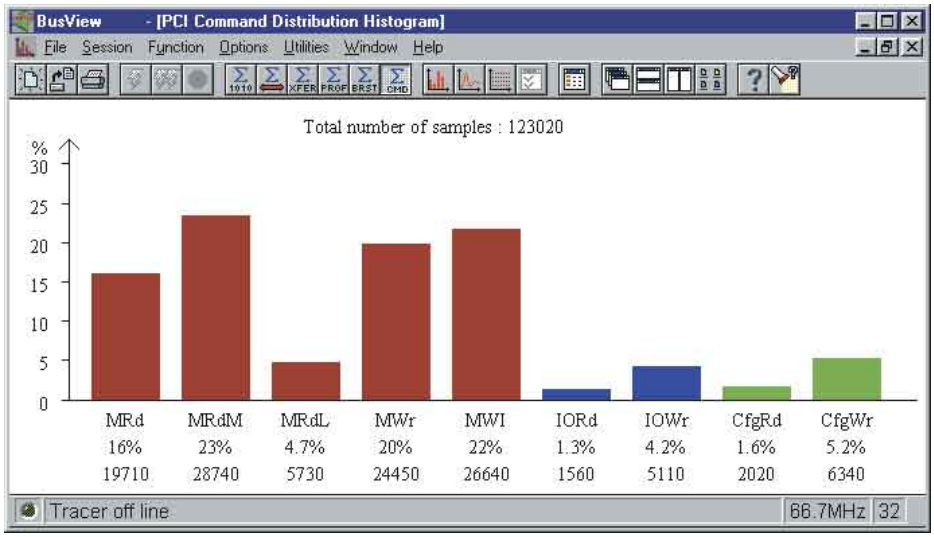
When sampling in CLOCK mode or when using the optional 500MHz Timing Analyzer of the PTIMBAT500-PB Piggyback module, the easy-to-read waveform diagrams provide powerful zooming, cursors and navigation tools. To ease the search for cycles of interest, one may use an “edge-to-edge” scroll mode on a selected signal, as well as explicit jumps to given line numbers or to cursors.



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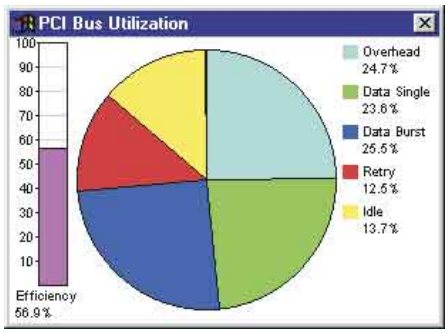
CONCURRENT STATISTICS

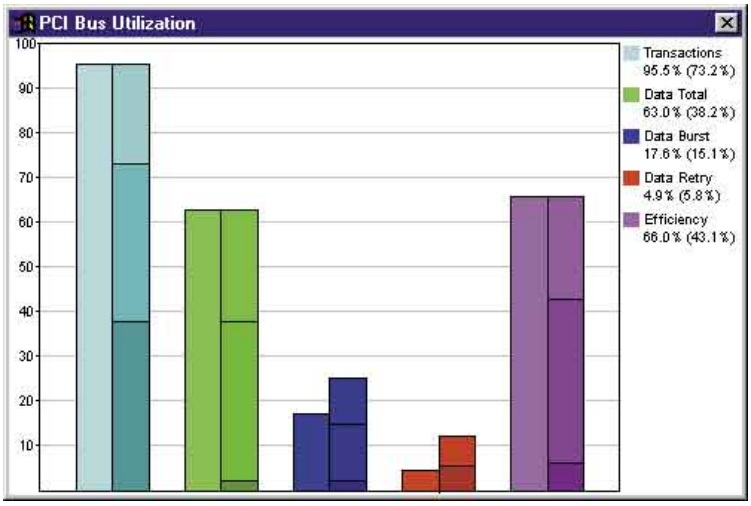
The PBT-615 comes with an extensive set of PCI-X/PCI bus statistics and performance measurement functions. Based on dedicated hardware counters, the analyzer offers real-time Bus Utilization and Efficiency statistics that can run at all times as an active window on the screen, in parallel with bus tracing or exercising. There are also real-time Event Occurrence statistics based on user-defined values in the trigger event recognizers. In addition, measurements of Bus Transfer Rate, Command Distribution and Burst Distribution are done by preprogrammed post-capture analysis of the data in the trace buffer. The user may save the displayed statistics data to an ASCII file, for later data importation into applications such as EXCEL for post processing and display.



BUS UTILIZATION

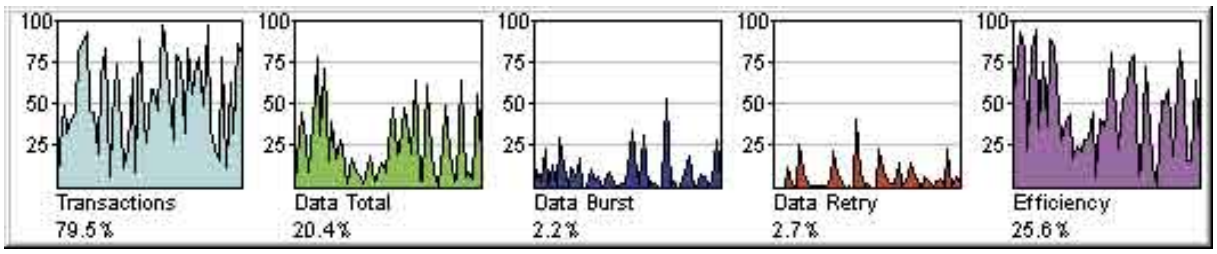
The Bus Utilization function provides a direct readout of the percentage of time the bus is occupied. This is ideal for determining whether the system bus has spare capacity to support another I/O-device or processor etc. This function, which is based on hardware counters and a pre-programmed usage of the word recognizers, provides an immediate response readout of how the bus is being used at any time.



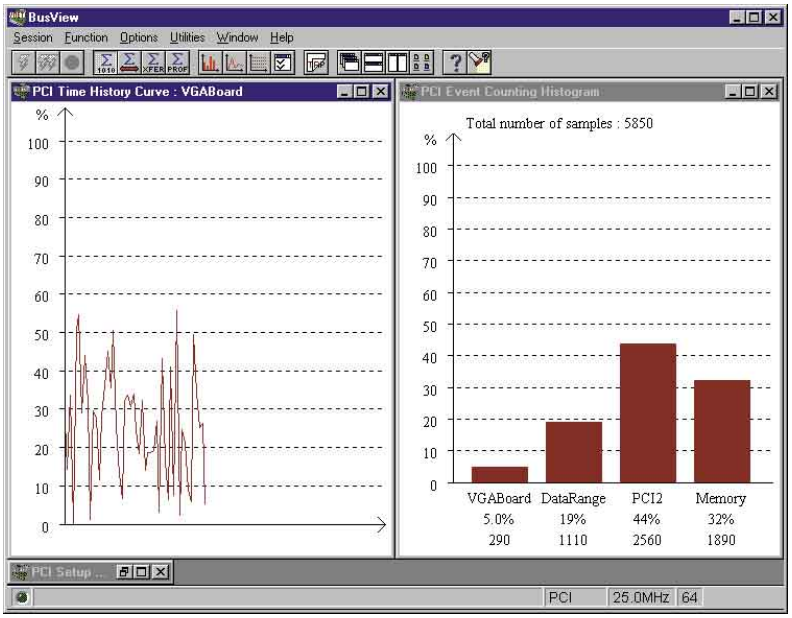


EVENT COUNTING

The Event Counting function, which is based on hardware counters, provides a real-time count of the occurrence of four user-defined events. This very powerful function may, for example, be used to count the number of IACK cycles per second displayed as a function of time, to count the number of Write or Read cycles, or to investigate access patterns to the bus in multi-processor systems, etc.



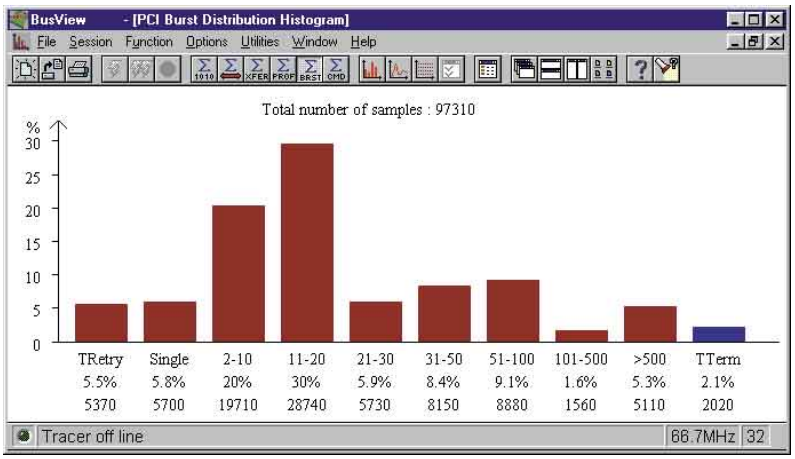
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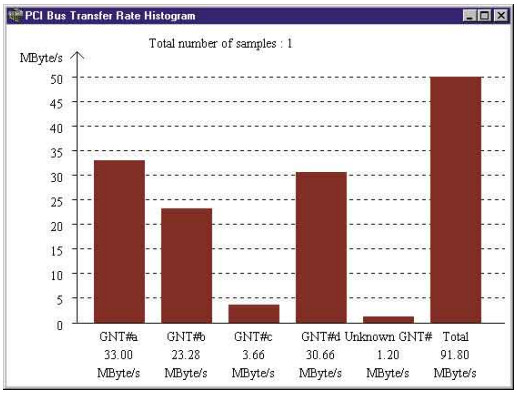


BUS TRANSFER RATE

The Bus Transfer Rate function presents how much data is transferred over the bus, shown in MBytes/s or in MTransfers/s. This can either be shown between selected lines directly in the trace buffer, to measure burst transfer rate, or as histograms that show the average transfer rate over a certain period of time.

This function can be used to verify if system performance specifications have been fulfilled and to assist in system tuning.

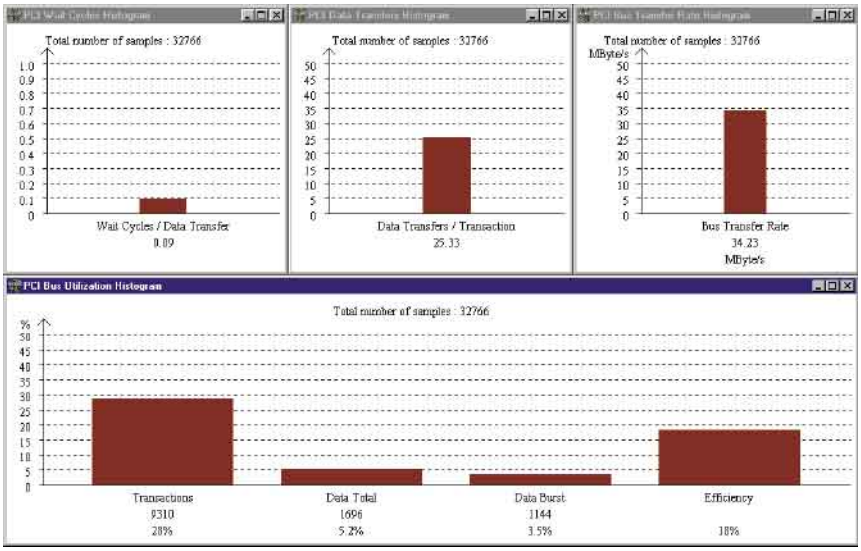




BUS PROFILE

The bus profile function contains a number of different measurements, for characterization of a number of important parameters. These are:

- **Number of Wait States per Data Transfer**
- **Number of Data Transfers per Transaction**
- **Bus Transfer Rate**
- **Bus Utilization, including Bus Rate and Bus Efficiency**



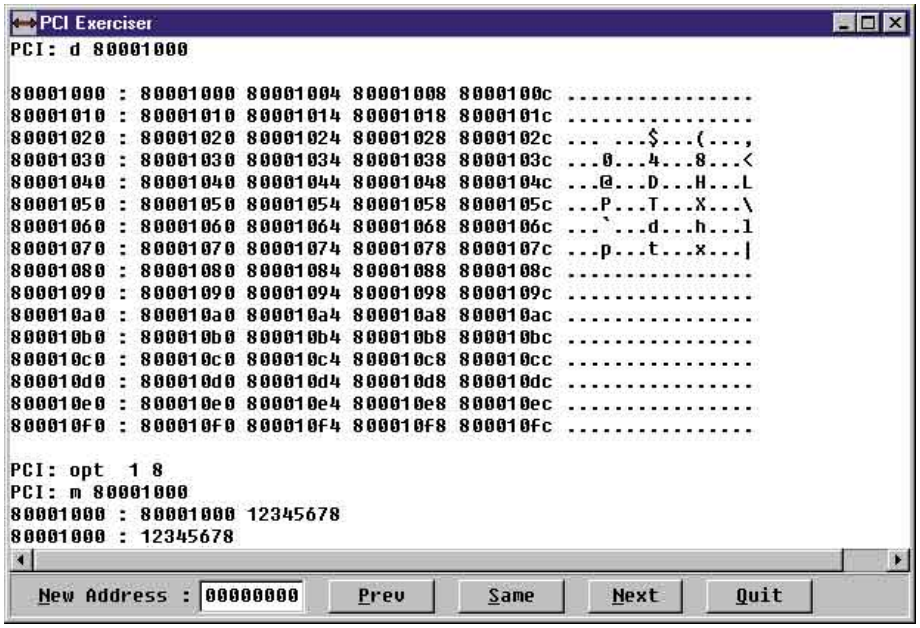
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Onboard Exerciser

- Master, Target and Interrupter for 32-bit and 64-bit PCI up to 66.7MHz and PCI-X up to 100MHz.
- Target at user defined address with 8 MB zero-wait-state burst memory.
- Built-in Script Recording and Playback capability.
- Memory Tests with walking ones/zeros, random patterns, etc.
- DMA transfers between Exerciser and target, or between two bus targets.
- Generate and handle interrupts.
- Supports Burst and Single cycles.
- Trigger analyzer if Memory Test fails.
- Start Exerciser on Analyzer Trigger

APPLICATIONS:

- Test ASIC and FPGA designs under development.
- Emulate planned, but not yet available boards.
- Automated Tests during manufacturing.
- Insert Bus traffic load to analyze system performance effects.



64-BIT EXERCISER

The PBT-615 CX and DX models feature a built-in advanced 64-bit Exerciser that functions as a Bus Master interface with DMA, a Target interface with 8MBytes of memory and an Interrupter. The exerciser supports 64-bit and 32-bit PCI up to 66.7 MHz. A 100 MHz PCI-X exerciser is also provided in the PBT-615DX model. The exerciser is controlled via dialog boxes through the user-interface, or self-running with the built-in script recording and playback capability with programmable delay and loop functions.

SIMULTANEOUS EXERCISING & ANALYSIS

The Exerciser is a separate functional unit of the PBT-615 board, which can start and run totally independently and concurrently with the analyzer. Similarly, the Target interface is another separate functional unit with 8MBytes of memory that can be accessed by other PCI-X/PCI agents at any time, with a base address specified by the user. The BIOS of the host system will not need to initialize the PBT-615.

BUS MASTER WITH POWERFUL DMA

The Bus Master has two DMA engines, allowing the user to test transactions to several target devices concurrently. Normally, the DMA controllers transfer data between the local memory and PCI-X/PCI memory. However, a unique feature of the PBT-615 Exerciser is the ability to transfer data with DMA from one PCI device to another. Up to 8Mbytes of data can be transferred per DMA command, with peak burst data rates of 800MB/s (PBT-615DX).

MANIPULATE DATA IN PCI MEMORY

A comprehensive set of commands are available to the user to inspect, manipulate and test data in PCI-X/PCI and local memory. There are also commands to load, dump and compare data between PCI-X/PCI or local memory and files on the Windows host PC. Explicit memory test commands are also provided, using data patterns such as random or walking ones/ zeros. If an error is found, the exerciser can trigger the onboard state analyzer and the optional 500 MHz Timing Analyzer for immediate review of the failing cycle(s). The module may also generate interrupts, IntAck and Special Cycles on the PCI-X/PCI bus.

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PLUG AND PLAY

The Exerciser is totally standalone and self-contained as seen from the PCI-X/PCI bus. This means that the BIOS of the host system will not need to configure the PBT-615. All parameters such as Target Address window/(BAR), etc. are set by software through user commands.

SCRIPT FUNCTION ALLOWS AUTOMATED TESTING

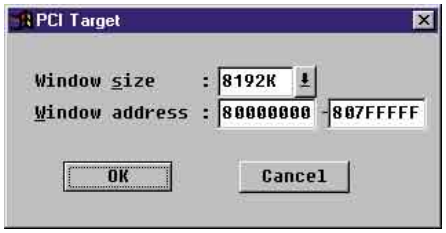
A built-in script engine allows test scripts to be created with a convenient record and playback function. Scripts are recorded by manually running through the various commands of the exerciser. Several scripts can be stored and retrieved for later use. Each script consists of sequences of bus cycles of any kind, with varying sizes, cycle types, etc. The script playback function can be set to run single, multiple or infinite playbacks, while the analyzer part of the product may perform bus monitoring in the background. This makes the PBT-615 ideal for running automated tests during design verification or production test of PCI devices, adapters and motherboards.

EMULATE A BOARD UNDER DESIGN

In many cases a board intended for a specific system is not available. The Exerciser can emulate this card as a Target or as a Master. This way the software design can progress without waiting for the hardware. The Exerciser also contains a target interface that has its own address decoder for a user defined address window. This may respond to accesses from another module.

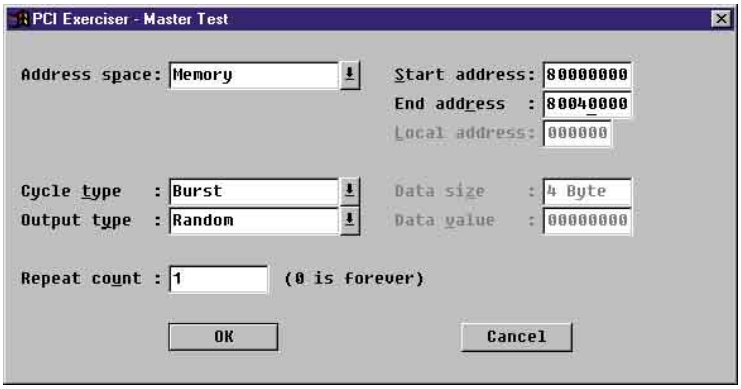
TARGET MEMORY

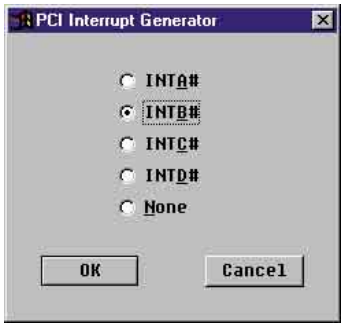
The module contains 8 MBytes of target memory that can be located anywhere in the PCI address map by a command in the user interface. Data can be written to and read from this memory as single cycles or as zero-wait-state burst cycles (after initial latency) for a peak bandwidth of 800MB/s.

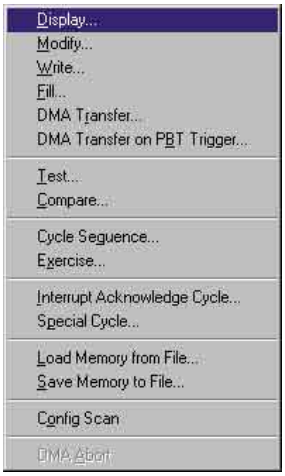


GENERATE PCI INTERRUPTS

The Exerciser can generate any of the four PCI Interrupt lines INTA#, INTB#, INTC#, and INTD#. When an interrupt is generated, it can be turned off through the Exerciser user I/F, or it may remain asserted until another PCI device explicitly turns it off by writing to a certain address of the Exerciser Target. The status of the interrupts asserted by the Exerciser are indicated on the status line of BusView.







Partial List of available commands

- Display PCI-X/PCI memory in hex and ASCII.
- Modify PCI-X/PCI memory.
- Display Local user memory.
- Modify Local user memory.
- Fill PCI-X/PCI memory.
- Test PCI-X/PCI memory and IO space.
- Initiate DMA between local and PCI-X/PCI mapped memory.
- Map local user memory (as Target Memory) into PCI-X/PCI address space.
- Generate PCI-X/PCI interrupts.
- Sequence cycles.
- Exercise cycles.
- Change PCI-X/PCI access parameters.
- PCI-X/PCI Config Scan.

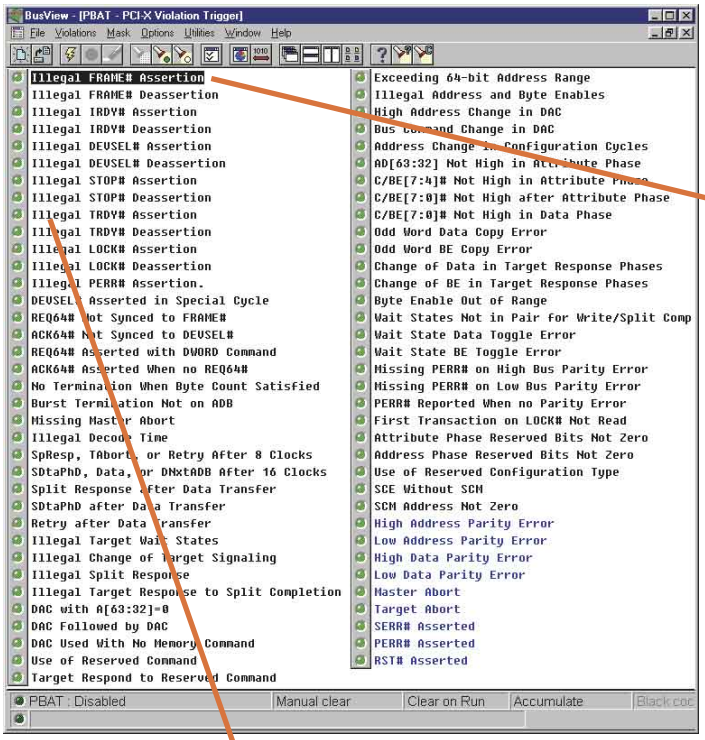
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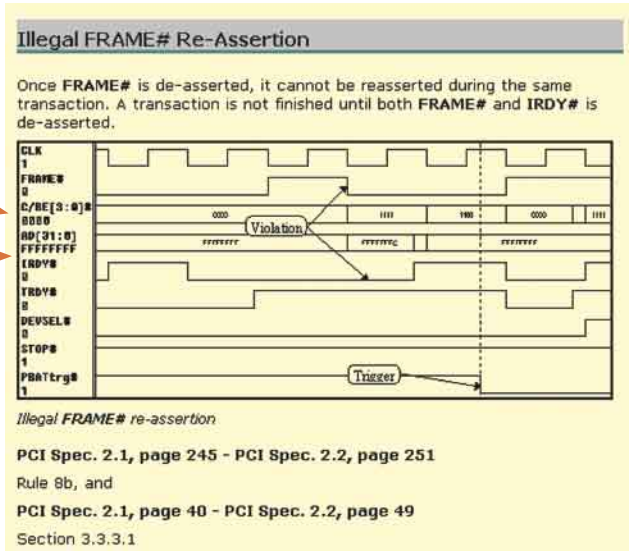
Onboard Protocol Checker

The PBT-615 CX and DX models feature a built-in protocol checker for PCI-X and PCI. This versatile feature automatically detects up to 71 PCI-X and 45 PCI protocol errors, helping the user to track down bus hardware errors without the need to understand the nature of the problem.

The protocol checker can run in the background when other analyzer functions of the PBT-615 are active. As an example, the state analyzer, the 500MHz Timing Analyzer (if installed) and bus utilization statistics can all be active at the same time while the protocol checker runs in the background, screening the bus for errors.

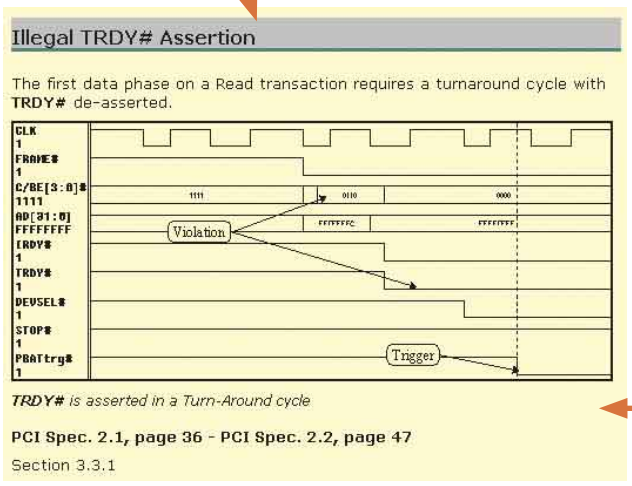
If the protocol checker is used as the trigger source for the analyzer(s), the state and timing analyzers will then provide a comprehensive picture of the bus activity around the point when an error was found. This helps the user to identify and correct the problem.

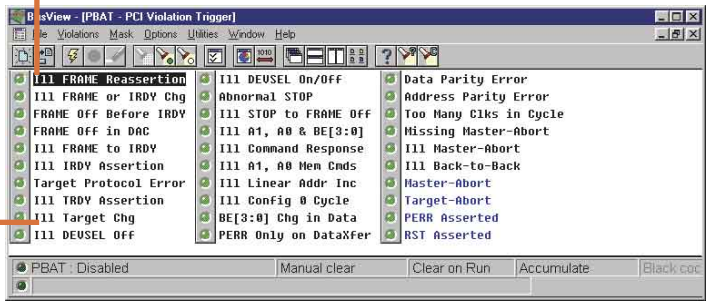




A total of up to 71 PCI-X protocol violations (see figure at left) and 45 PCI protocol violations (below) are automatically detected by the onboard protocol checker on the PBT-615.

(Note: In the window below several entries cover multiple violations)





When a violation is found, the user may pull up a detailed explanation of it in the On-line Help system. This includes reference to the affected rules in the PCI-X/PCI specifications. See yellow boxes.

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PTIMBAT500-PB

500MHz Timing Analyzer Anomaly Trigger

Piggyback module for PBT-615

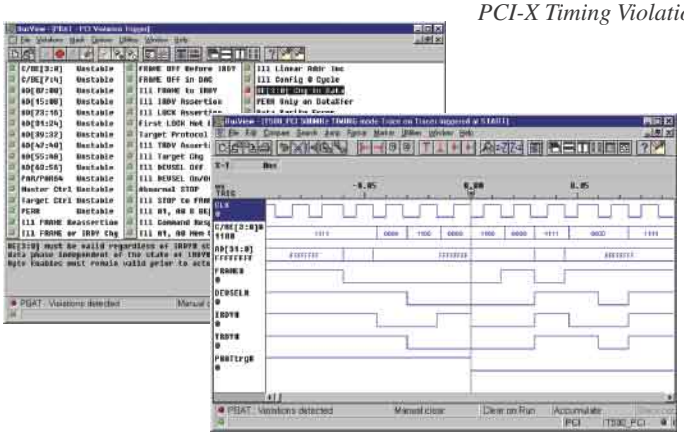


PTIMBAT500-PB

The PTIMBAT500-PB is an optional piggyback module for the PBT-615, with features aimed at advanced timing characterization and fault detection of PCI-X and PCI systems. The module contains two independent functional blocks (see figure below), one is a 500MHz Timing Analyzer, the other is a sophisticated Anomaly Trigger unit.

500MHz TIMING ANALYZER

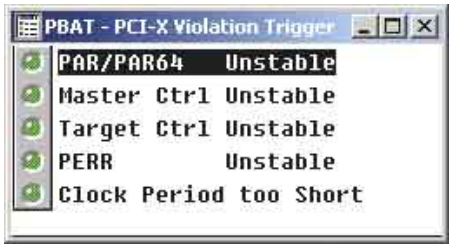
The Timing Analyzer provides 64 channels of high speed sampling of the PCI-X/PCI bus at a speed of 500 Megasamples per second. Designed for demanding hardware debugging and timing analysis, the timing analyzer features an extremely deep trace memory of 16 MSamples on all channels and less than 1ns skew between channels. The timing analyzer is triggered by cross triggers either from the onboard Anomaly Trigger, from the State Analyzer of the PBT-615 or from an external Trigger Signal. The timing analyzer may be set for different pre-/post-trigger ratios, allowing optimal display of events that occur both prior to and after the trigger event.



The 500MHz Timing Analyzer provides a detailed view of the PCI-X and PCI bus signals with 2.0ns resolution. By having the onboard Anomaly Trigger module trigger the Timing Analyzer when violations are found, the user gets an immediate display of the faulty cycle.

ANOMALY TRIGGER

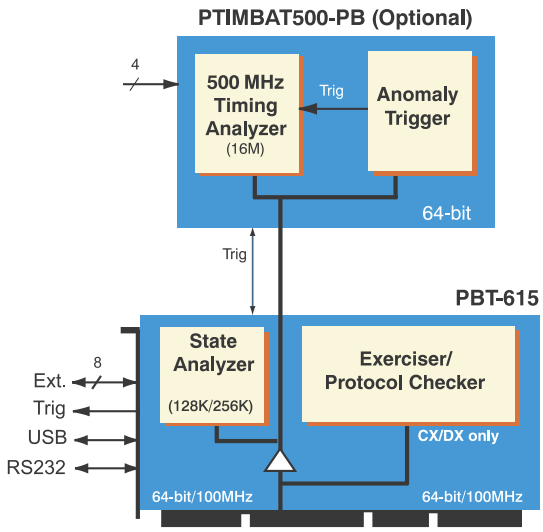
The anomaly trigger of the PTIMBAT500-PB goes one step further than the built-in protocol checker capabilities of the PBT-615 CX and DX, by also providing Timing Violation detection. This works by screening the bus signals for setup and hold time violations relative to the bus clock, in steps as short as 50ps. This can be used in two ways, either by leaving the Timing Checker running in the background, with a set limit for setup and hold times, or to employ the unit to explicitly measure the setup/hold times (scan function).



The PTIMBAT500-PB complements the PBT-615 onboard Protocol Checker with a Timing Checker. The window above shows the Timing Violations detected for PCI-X. The Master and Target Unstable items each cover three control signals. This gives a total of nine PCI-X Timing Violations.

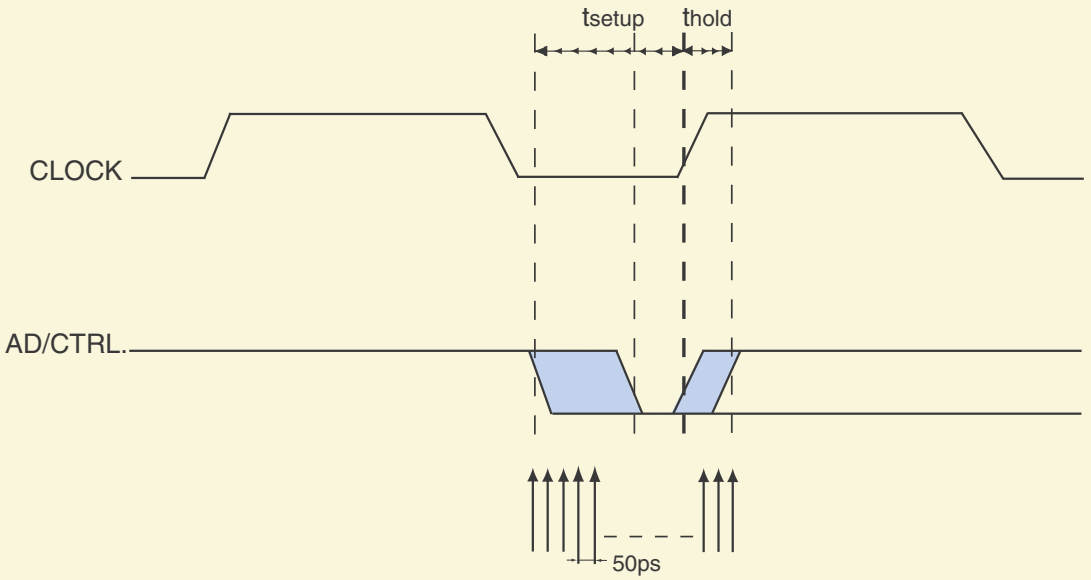
Features:

- 500 MHzTiming Sampling of 64 PCI-X/PCI signals
- Ultra-deep 16M x 64 ch. Trace Buffer
- Upper and lower part of 64-bit PCI-X/PCI selectable
- Triggered from Anomaly Trigger, State Analyzer or External signal
- Automatically detects 84 PCI Anomalies, including 45 Protocol and 39 Timing Violations

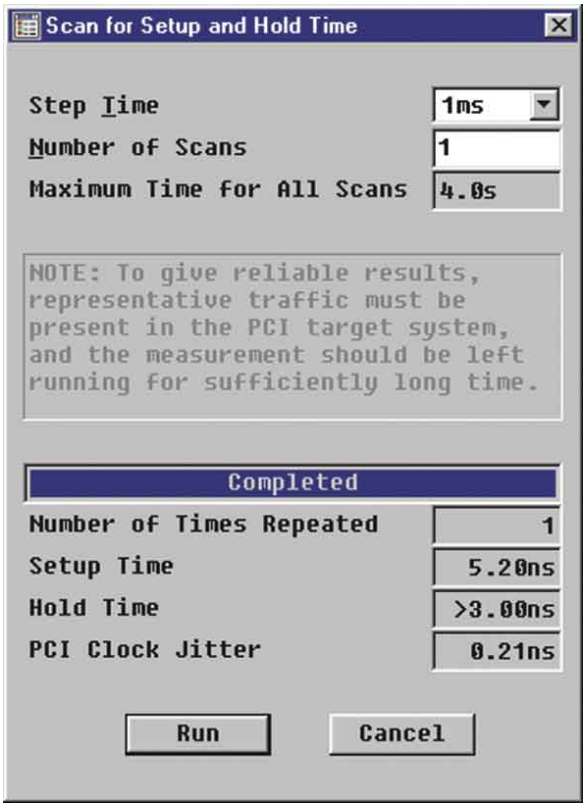


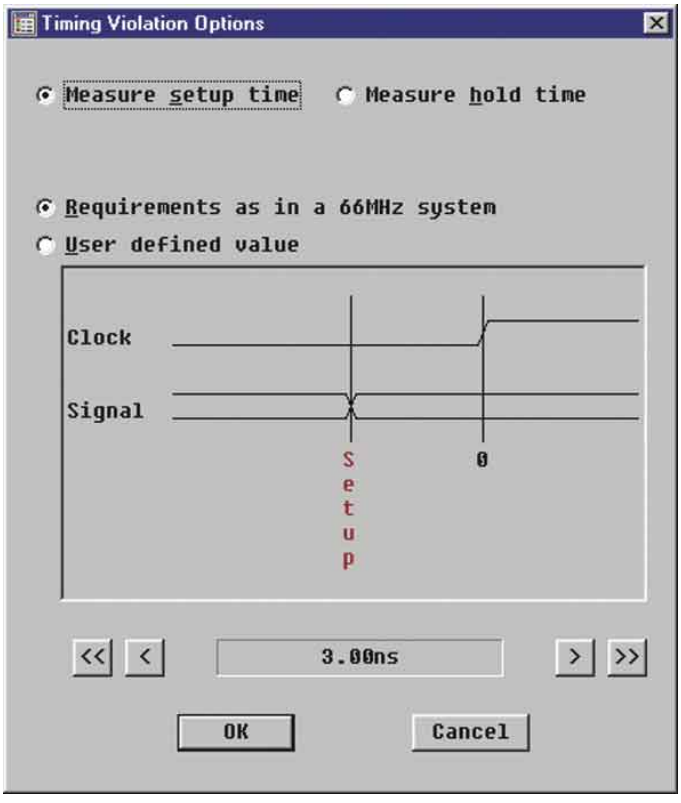
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ADJUSTABLE SETUP & HOLD TIME MEASUREMENTS IN 50ps STEPS:



Sampling point adjustable in 50ps steps, value compared with value at clock edge





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PBT-0-SL

Zero-Slot Adapter



The PBT-0-SL is an adapter which allows the PBT-615 to be inserted into a PCI expansion slot together with another expansion board. This allows use of the PBT-615 even if there are no spare PCI expansion slots. The adapter is designed to operate in 66 and 33MHz systems. The “angled” design offers minimum track length and prevents mechanical conflict with the chassis. Comes in two versions, for 3V (PBT-0-SL/3) and 5V systems (PBT-0-SL/5). (For PCI-X compliant versions, please consult VMETRO.)

External Power Supply:



VMETRO offers an External Power Supply unit for all of our bus analyzers. This may be useful for systems with a marginal power supply.

Part#: No 401-EPSU

PCI Analyzers for other form factors:

Please contact VMETRO or your local sales representative/distributor for information about VMETRO’s other bus analyzers.

CompactPCI



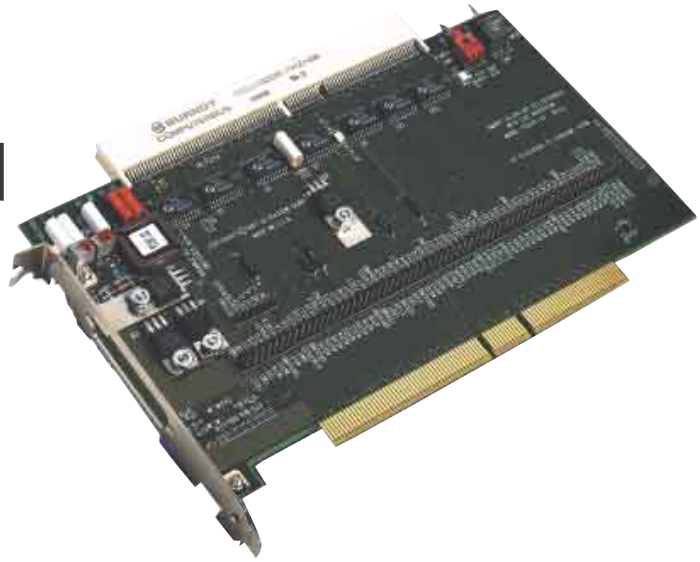
PMC



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PCIEXT64U

PCI Extender Board



Features:

- 64-bit and 32-bit PCI
- Live insertion of DUT
- Current Limiter
- Supports PCI clock speeds up to 66 MHz
- Test points for all PCI signals
- Slot power ON/OFF switch eliminates rebooting
- Isolation Buffer Enable Power Monitor Test Points
- Separate Power Supply Terminals allow optional connection to external power supply testing.

Auto Overload Protect:

- Board has selectable power limit switch with 10, 15 and 35 watt cutoff valves, with RED overload LED.

Universal Card:

- For systems with 5V or 3.3V signaling

INTRODUCTION

The PCIEXT64U is a high-speed 64-Bit PCI Bus Extender Card with switchable bus isolation switches supporting both 32 and 64-bit PCI Cards. This allows for ”hot insertion” of the boards that are being tested without having to power down or reboot the host system.

High PCI signal integrity requirements are met with both high speed trace layout parameters (controlled high impedance and minimal inductance ground) and active bus isolation with low capacitance, resistance and delay which insures minimal effect on boards which are being tested. Special power monitoring and current limiting features help insure a highly robust debug environment.

The advanced Power Measurement function features Overload and Voltage protection integrated on the board. These features allow accurate real-time power measurement of the board-under-test while safe guarding the host system with selection of three board power overload threshold points. Power On Reset parameters for 3 and 5 volts can be set to hold Reset active until proper voltage levels are reached.

The PCIEXT64U provides test points for logic analyzer hookup on all PCI signal lines, and contains low-resistance FET switches on all address, data and strobe lines, isolating the board-under-test from the system’s bus and preventing failures of the board-under-test from crashing the system. The pass-through PCI Extender feature and mezzanine feature allows any PCI-bus board to be installed in the same slot location as the PCIEXT64U and perform extended test functions.

Software for all Windows versions is included which aids in utilizing the live insertion capabilities of the extender. This software can store the contents of the PCI configuration registers of the board-under-test. Then, when this board is removed, and another one inserted (without the need to reboot the system), this software initializes the new board’s configuration space with the same configuration as the replaced board, so that system operation may proceed as if no substitution had taken place.

In addition to the above features, the PCIEXT64U powers up the board-under-test in a “soft-start” manner, in which the voltages rise at a controlled rate over a 100 microseconds period, preventing the system from crashing due to the board-under-test’s inrush current when the extender’s slot power switch is turned on. Previous generation live insertion extenders could sometimes cause system resets when a board-under-test with excessive bypass capacitance was switched on via the extender.

Finally, the PCIEXT64U has a special mode in which the user can optionally power up the board-under-test without enabling the bus buffers. This allows users to program FPGAs and CPLDs on the board without the risk of crashing the host system during the period before and during device programming.

SPECIFICATIONS

Pass Through Connector:
All signal, power and ground lines in the full 64-bit PCI Bus (including Reserved Signals) are passed through to a standard 64-Bit PCI connector, allowing any PCI Bus board to share the slot with the PCIEXT64U. The 96 PCI signals are:

AD(63:00), INTA#, INTD#, PRSNT1#, PRSNT2”, RST#, CLK,REQ#, GNT#, C/BE(3:0), IDSEL, FRAME#, IRDY#, TRDY#, DEVSEL#, STOP#, LOCK#, PERR#, SDONE, SBO#, SERR#, PAR, REQ64#, ACK#.

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Specifications & Ordering Information

PBT-615, ANALYZER PART

PCI-X/PCI bus:	32/64-bit, up to 100MHz
Trace Memory:	128K x 128 bits (Model B) 256K x 128 bits (Model CX/DX)
Input channels:	93 bus signals, plus 8 ext. inputs on pin header.
PCI-X/PCI clock requirements:	Max. 100MHz, min. 12MHz, Min. 4ns low or high pulse width. 11ms PLL lock time.
Signal levels:	615B/CX: 5V or 3.3V 615DX: 3.3V
Monitored signals:	AD[31::0], AD[63::32], C/BE[3::0]#, C/BE[7::4]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, PAR, PAR64, PERR#, SERR#, RST#, INTA#, INTB#, INTC#, INTD#, LOCK#, ACK64#, REQ64#, REQ#, GNT#, IDSEL, PME#. (Plus GNT3:0#, REQ3:0#, IDSEL via pin headers).
Trigger:	4 word recognizers covering all 93 PCI signals and 8 Ext. inputs. RANGE & NOT operator on Address/Data.
Range:	Four A32 address ranges, Four D32 data ranges. Inside/Outside.
Sequencer:	32 levels with If, Else, Elsif, Goto, Count, Delay, Trigger, Store, Sampling mode, Halt.
Trigger position:	0%, 25%, 50%, 75%, 100%
Occurrence counters:	Four 20-bits (in Sequencer).
Delay counters:	Three 20-bits (in Sequencer).
Event counters:	Five 20-bits (for Statistics), one can run at all times.
Time Tag:	Range: 30ns-9min@33MHz,15ns-4min30sec@66MHz. 3 min@100MHz Resolution: 30ns@33MHz, 15ns@66MHz, 10ns@100MHz
Latency Tag:	Counts latency (wait states) from FRAME# to TRDY# asserted. Max count: 64clks.
Trigger Output:	TTL level trigger output with programmable polarity, level or pulse. May pulse on each stored sample. Available on pin header on back panel.
External Inputs:	Eight TTL level inputs on pin header on back panel.

PBT-615, EXERCISER PART

PCI bus:	32/64 bit, up to 66.7MHz (PBT-615CX/DX)
PCI-X bus:	32/64 bit, up to 100MHz (PBT-615DX)
Master:	Zero-wait-states, 800MB/s @100MHz peak burst rate, 32-bits Address, 3 DMA Controllers.
Target:	8MBytes memory, 800MB/s peak burst rate. @100MHz

PBT-615 PROTOCOL CHECKER PART

PCI bus:	32/64 bit, up to 66.7MHz (PBT-615CX/DX)
PCI-X bus:	32/64 bit, up to 100MHz (PBT-615CX/DX)
PCI-X Violations:	71 (DX)/68 (CX) Protocol Violations
PCI Violations:	45 Protocol Violations (PBT-615CX/DX)

PBT-615, GENERAL

PCI Loading:	615B: 10pF (Max) 615CX/DX: 16pF (Max)
Interfaces:	One RS232C serial port, 1200-38400b/s, aut. adjusted. (Cable included). One USB port, 12 Mb/s.
Power supply requirements :	+5VDC +/-5% from PCI backplane or from ext. power supply via back panel inlet.
	615B: 1.5A typ. idle 1.9A typ. sampling
	615CX: 1.9A typ. idle 2.4A typ. sampling
	615DX: 2.1A est. idle 2.8A est. sampling
Dimensions:	174.6 x 106.7mm (Short card) One PCI slot.
Compliant to:	PCI Rev. 2.2 PCI-X rev. 1.0a

PTIMBAT500-PB

PCI-X/PCI bus:	32-bit, or upper or lower part of 64-bit PCI-X/PCI selectable, up to 100MHz
Trace Memory:	16M x 64 bits.
Input channels:	58 bus signals 4 ext inputs.
Trigger position:	12.5%, 25%, 50%, 75%, 87.5%
Signal-to-signal skew:	<1ns
Trigger output:	TTL level, activ low.
Ext inputs:	Four TTL, activ low. Via pin Headers
PCI-X Violations:	9 Timing Violations
PCI Violations:	45 Protocol Violations 39 Timing Violations 3 Warning Triggers
Timing Violation resolution:	50ps
Timing Violation accuracy:	500ps
Power supply:	2.7A idle/3.6A sampling @ 5V 0.3 A @ 12V (for fan unit)
Compliant to:	PCI Rev. 2.2 PCI-X Rev. 1.0
NOTE:	The PTIMBAT500-PB is delivered with a fan unit that mounts on the PBT-615, adding 55 mm to the length of the analyzer.

ORDERING INFORMATION

PBT-615B	PCI-X & PCI Analyzer, 128K Trace Buffer. (For systems with 5V or 3.3V signaling)*
PBT-615CX	PCI-X Analyzer & Protocol Checker. PCI Analyzer, Exerciser & Protocol Checker. 256K Trace Buffer. (For systems with 5V or 3.3V signaling)*
PBT-615DX	PCI-X & PCI Analyzer, Exerciser & Protocol. Checker 256K Trace Buffer. (For systems with 3.3V signaling only)*
PTIMBAT500-PB	500 MHz / 16M Timing Analyzer & 50ps. Timing Checker for PCI-X & PCI (incl. PCI Protocol Checker)
401-EPSU	External Power Supply (All cables included.)
PBT-0-SL/X	Zero-Slot Adapter for 3V or 5V systems (x=3 or 5)
PCIEXT64U	PCI Extender Board

** BusView™ - Graphical User-Interface for Windows, included.*

WARRANTY

All VMETRO analyzer products have one year warranty.

Specifications subject to change without notice. V1.2001.

BusView is a registered trademark of VMETRO, Inc., USA. Windows is a trademark of Microsoft Corp. USA. The PTIMBAT500-PB is jointly developed by Ultraview Corp. and VMETRO.

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