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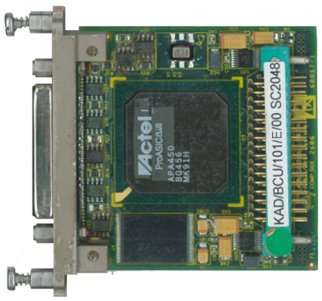
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Find the *Curtiss-Wright / ACRA Control KAD/BCU/101/C/02* at our website: ***Click HERE***

KAD/BCU/101

IRIG-106 backplane controller and encoder

CURTISSWRIGHTDS.COM



Key Features

- 100% IRIG-106 compliant encoder
- Fully software programmable: Up to 10 PCM codes at up to 20 Mbps; 5 to 250K words per major frame and 5 to32K words per minor frame; 4 to 64 bits and parity (odd/even/none) programmable word by word
- Supports any sync word and sub-frame strategy
- ARINC-573/717 compatible output
- Can operate as a master or a slave in distributed system

Applications

- Encoding data in IRIG-106 Ch.4 PCM stream

Overview

The KAD/BCU/101 functions as two modules in one; an encoder and a backplane controller. The encoder is functionally identical to the KAD/ENC/005 and encodes data from any Acra KAM-500 module in an IRIG-106 Chapter 4 PCM stream.

Parameters to be transmitted are stored in pre-defined locations in RAM. Each parameter has a word definition that includes the bits per word, Most Significant Bit (MSB) (sent first or last), and parity. The encoder has differential ended RS-422 outputs for clock and data, along with buffered TTL outputs for NRZ-L and the bit/word/minor-frame/major-frame pulses. It also supports Cyclical Redundancy Checking (CRC) insertion at the end of minor frames.

Up to 15 formats (instruction sequences), can be stored at any time. Format selection is via four single ended discrete (0-5V) input pins on the I/O (Input/Output) connector. As up to 64 chassis can be programmed using a single programming link, there are also six discrete I/O pins to set a chassis number. These six inputs are pulled to ground internally if left open circuit.

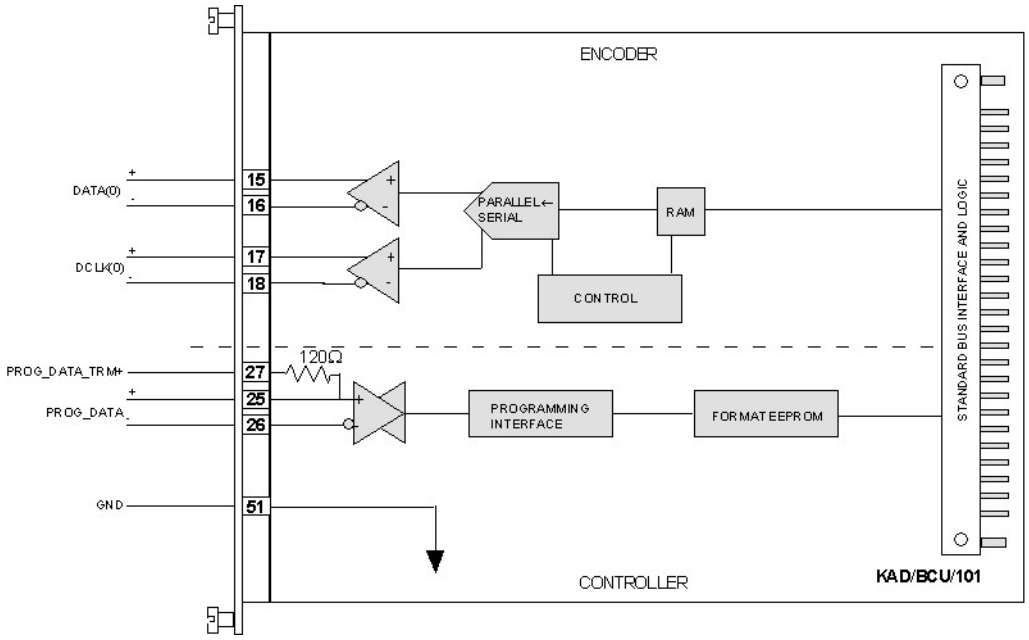


Figure 1: Encoder shown with differential ended PCM outputs only; controller shown with programming I/O only

Specifications

All values provided in the following specification tables are valid within the operating temperature range specified under “Environmental ratings” in the “General specifications” table.

TABLE 1	General specifications				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Slots	–	–	1	–	Use in controller slot only (J2).
Mass					
	–	75	–	g	
	–	2.65	–	oz	Design metric is grams.
Height above chassis					For recommended clearance requirements see the *CON/KAD/002/CP* data sheet.
bare connector	–	–	11	mm	
bare connector	–	–	0.43	in.	Design metric is millimeters.
Access rate	–	–	2	Msps	Maximum combined access rate for read and write.
Power consumption					
+5V	261	–	950.4	mA	The maximum value shown here is when all PCM outputs are enabled. Disabling a PCM output reduces power consumption by 100 mA. (See “PCM encoder outputs” on page 9.)
±7V	0	–	0	mA	
+12V	0	–	8.8	mA	
-12V	0	–	0	mA	
total power	1.3	–	4.86	W	Particular combinations of chassis and Acra KAM-500 modules may have power or current limitations. For details, see *TEC/NOT/016 - Power dissipation, TEC/NOT/049 - Power estimation*, and the relevant chassis data sheet.
Environmental ratings					See *Environmental Qualification Handbook*.
operating temperature	-40	–	85	°C	Chassis base/side plate temperature.
storage temperature	-55	–	105	°C	

TABLE 2	RS-422 inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	1	–	
Signaling rate					
X_SYNC_IN	–	1	–	Mbps	

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TABLE 2	RS-422 inputs (continued)				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Input voltage					
operating range	-7	–	12	V	Do not exceed operating range.
logic 0	–	–	-0.2	V	V_{IN+} - V_{IN-}.
logic 1	0.2	–	–	V	V_{IN+} - V_{IN-}.
overvoltage protection	-60	–	60	V	Voltages outside of this range can damage input.
ESD protection	-15	–	15	kV	Human Body Model.
Input resistance					
between inputs	–	270	–	kΩ	Module powered on.
between inputs	–	270	–	kΩ	Module powered off.
between inputs	–	120	–	kΩ	Module powered on and inputs terminated.
between inputs	–	120	–	kΩ	Module powered off and inputs terminated.
each input to GND	–	345	–	kΩ	Module powered on.
each input to GND	–	160	–	kΩ	Module powered off.

TABLE 3	BTTL inputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Inputs	–	–	11	–	
Signaling rate					
FORMAT[3:0]	–	–	500	kHz	Must be stable for 8 µs before start of acquisition cycle.
CHASSIS_ID[5:0]	–	–	–	–	Is assumed never to change while powered on.
MEM-TRIGGER	–	–	1	MHz	Minimum pulse width, signal active high.
Input voltage					
operating range	0	–	5.5	V	
logic 0	–	–	0.8	V	
logic 1	2	–	–	V	
overvoltage protection	-40	–	40	V	Voltages outside of this range can damage input.
Input resistance					
each input to GND	100	–	–	kΩ	Module powered on.
each input to GND	50	–	–	kΩ	Module powered off.

TABLE 4	High-speed RS-422 outputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Outputs	–	–	8	–	
Signaling rate					
DATA[3:0]	–	–	20	Mbps	RZ, NRZ-L/M/S, RNRZ-L 15.
DATA[3:0]	–	–	8	Mbps	Biø-L/M/S, DM-M/S.
DCLK[3:0]	–	–	20	MHz	
Output voltage					
operating range	-15	–	20	V	
logic 0	–	–	-2	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
logic 1	2	–	–	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
short circuit current	–	–	250	mA	
short circuit duration	90	–	–	s	Only one output may be shorted at a time.
overvoltage protection	-27	–	27	V	
ESD protection	-5	–	5	kV	Human Body Model.
Output resistance	–	65	–	Ω	R_{LOAD} = 100Ω.

TABLE 5	Low-speed RS-422 outputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Outputs	–	–	2	–	
Signaling rate					
X_SYNC_OUTA	–	1	–	Mbps	
X_SYNC_OUTB	–	1	–	Mbps	
Output voltage					
operating range	-7	–	12	V	
logic 0	–	–	-2	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
logic 11	2	–	–	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
short circuit current between outputs	–	–	66	mA	
short circuit current between output and GND	–	–	104	mA	
short circuit duration	∞	–	–	s	Only one output may be shorted at a time.
overvoltage protection	-60	–	60	V	
ESD protection	-15	–	15	kV	Human Body Model.
Output resistance	–	25	–	Ω	

TABLE 6	BVDD outputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Outputs	–	–	1	–	
Range	4.8	5	5.1	V	
Current output					
compliance[1]	–	–	12	mA	For driving chassis and format lines.
short circuit current	–	–	23	mA	
short circuit duration	∞	–	–	s	To GND.
Output resistance	–	220	–	Ω	

1. Currents in excess of the maximum value result in output voltages below the minimum voltage required to be detected as a logic 1 for a standard BTTL input.

TABLE 7	BTTL outputs				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Outputs	–	–	6	–	
Signaling rate					
DATA	–	–	16	Mbps	
DCLK	–	–	16	MHz	
NRZ_L	–	–	16	Mbps	
WORD_PULSE	–	–	16	MHz	High for last bit of any word.
MINOR_PULSE	–	–	4	MHz	High for last word of minor frame.
MAJOR_PULSE	–	–	4	MHz	High for last word of major frame.
Output voltage					
logic 0	–	–	0.2	V	Sinking 0.1 mA through 100Ω output resistance.
logic 1	4.8	–	–	V	Sourcing 0.1 mA through 100Ω output resistance.
short circuit current	–	–	50	mA	
short circuit duration	∞	–	–	s	To GND.
Output resistance	100	–	–	Ω	

TABLE 8	RS-485				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Channels	–	–	1	–	
Signaling rate					
PROG_DATA	–	–	1	Mbps	
Input voltage					
operating range	-7	–	12	V	
logic 0	–	–	-0.2	V	V_{IN+} - V_{IN-}.
logic 1	0.2	–	–	V	V_{IN+} - V_{IN-}.
overvoltage protection	-60	–	60	V	
ESD protection	-15	–	15	kV	Human Body Model.

TABLE 8	RS-485 (continued)				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Output voltage					
operating range	-7	–	12	V	
logic 0	–	–	-2	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
logic 1	2	–	–	V	V_{0+} - V_{0-} ; R_{LOAD} = 100Ω.
short circuit current between outputs	–	–	66	mA	
short circuit current between output and GND	–	–	104	mA	
short circuit duration	∞	–	–	s	Only one output may be shorted at a time.
Input resistance					
between inputs	–	270	–	kΩ	Module powered on/off.
between inputs	–	120	–	kΩ	Module powered on/off and inputs terminated.
each input to GND	–	345	–	kΩ	Module powered on.
each input to GND	–	160	–	kΩ	Module powered off.
Output resistance	–	25	–	Ω	

TABLE 9	Synchronization specification				
PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITION/DETAILS
Time accuracy					
instantaneous error	–	–	125	ns	After X-SYNC synchronization achieved to a KAM/TCG/102.
instantaneous error	–	–	250	ns	After X-SYNC synchronization achieved to a KAD/BCU/101.
Time to synchronize	0.2	–	4,000	ms	Up to two acquisition cycles.

Setting up the KAD/BCU/101

All module setup can be defined in XML using XidML® schemas (see http://www.xidml.org).

Instrument settings

SETUP DATA	CHOICE	DEFAULT	NOTES
Manufacturer	-	-	-
Name	ACRA CONTROL	ACRA CONTROL	Name of manufacturer.
PartReference	KAD/BCU/101/E	KAD/BCU/101/E	The instrument part reference.
SerialNumber	AB1234	AB1234	Unique name for each module.
Settings	-	-	-
DAU ID	0 to 63	0	An ID which identifies the DAU, typically set on DAU controllers such as CAIS and PCM controllers.
PCM Channel 1 Enable	True False	True	Enables PCM-OUT channel 1. (Electrical copy of Channel 0. See “PCM encoder outputs” section for further information.)
PCM Channel 2 Enable	True False	True	Enables PCM-OUT channel 2. (Electrical copy of Channel 0. See “PCM encoder outputs” section for further information.)
PCM Channel 3 Enable	True False	True	Enables PCM-OUT channel 3. (Electrical copy of Channel 0. See “PCM encoder outputs” section for further information.)
ARINC 717/573 Mode	True False	False	When enabled DCLK output becomes inverse of PCM output.
Shunt Mode	True False	False	Enable Shunt Mode. Used by modules supporting simulated shunt across their sensors.
Channels	-	-	-
PCM-OUT(3:0) PCM Output	-	-	IRIG 106 Chapter 4 PCM output.
Settings	-	-	-
Stream ID	00 to FFFFFFFF	FFFFFFFF	iNET-X stream ID for selected channel if a packet is generated via the assertion of Packetization Enabled. This setting is only supported in DAS Studio 3.
Packetization Enabled	True False	False	Enables the transmission via an iNET-X transmitter module (for example KAD/ETH/102) of an iNET-X packet containing the contents of this channel. This setting is only supported in DAS Studio 3.
PCM Code	NRZ-L NRZ-M NRZ-S DM-M DM-S Bi-Phase-L Bi-Phase-M Bi-Phase-S RNRZ-L-15 RZ	NRZ-L	Specifies the PCM encoding used.
Clock Phase	0 180	0	Indicates the phase of the data clock in degrees.

SETUP DATA	CHOICE	DEFAULT	NOTES
Polarity	True False	True	Specifies the polarity used to transmit, where True means that data is not inverted.
Bit Rate	500 to 20000000	6400000	Specifies the number of bits transmitted per second.
X_SYNC X_SYNC bi-directional	-	-	Chassis synchronization signal out.
Settings	-	-	-
Cable Length	0 to 20	0	The length of the cable carrying the X_SYNC signal in meters.
Delay	1 to 10	7	The delay on the X_SYNC signal in nano seconds/meter.
X_SYNC Inhibit	True False	False	Overrides chassis ID and sets module to be an X_SYNC slave rather than an X_SYNC master.
PROG RS-422 Input	-	-	Connection used to program the system configuration.

Parameter definitions

NAME/DESCRIPTION	BASE UNIT	DATA FORMAT	BITS	REGISTER DEFINITION
Global Parameters				
IrigTime48 48-bit wide IRIG time word.	BitVector	BitVector	48	R[47:0]
TimeHi Time in hours and minutes at the start of the acquisition cycle.	BitVector	BitVector	16	R[47:32] R[15:13] Reserved - Reserved for future use. R[12:7] Hours - BCD Hours 0 to 23. R[6:0] Minutes - BCD Minutes 0 to 59.
TimeLo Time in seconds and centiseconds at the start of the acquisition cycle.	Second	BCD	16	R[31:16] R(15) Reserved - Reserved for future use. R[14:8] Seconds - Seconds 0 to 59. R[7:0] Centiseconds - Centiseconds 0 to 99.
TimeMicro Time in microseconds at the start of the acquisition cycle.	Second	BCD	16	R[15:0] R[15:0] Microseconds - Microseconds 0 to 9999.
Status Present status of KAD/BCU/101.	BitVector	BitVector	16	R[15:0] R(15) Mem trigger status - MEM_TRIGGER pin status. 0: Not triggered. 1: Trigger active. R(13) X_SYNC in lock - X_SYNC in lock. 0: Not in lock. 1: In lock. R(11) X_SYNC Error - Errors in X_SYNC since last read. 0: X_SYNC Ok. 1: Error with X_SYNC signal. R[10:8] Reserved - Reserved for future use. R[7:4] Mode - Current mode. R[3:0] Reserved - Reserved for future use.
ReadCounter Increments every read.	Count	OffsetBinary	16	R[15:0]

NOTE: It is recommended that names are less than 20 characters, have no white space or contain any of the following five characters "/><\.

Getting the most from the KAD/BCU/101

The KAD/BCU/101 is divided into two parts; a backplane controller and a PCM encoder. The backplane controller organizes data transfer over the Acra KAM-500 backplane, and the PCM encoder encodes data in a PCM stream.

Backplane controller inputs and outputs

The KAD/BCU/101 has the following backplane controller inputs and outputs:

PROG_DATA±

This differential ended RS-485 bi-directional bus is for data transfer during programming (not terminated internally). The associated pins are electrically repeated on the connector to ease use in distributed systems.

CHASSIS_ID[5:0]

These six single ended BTTL inputs are for setting the chassis number in distributed systems. When left unconnected, these inputs set the chassis number to 0, which is the ID number for the master chassis in a distributed master/slave system. (See “Addressing multiple chassis” on page 11.)

Backplane controller and PCM encoder inputs

The following inputs affect both the backplane controller and the PCM encoder:

FORMAT[3:0]

These four single ended BTTL inputs are for setting the format (see “Understanding formats” on page 10). When left unconnected, these inputs set the format number to 0. After the format select lines change, the new format takes effect on the first bit of the first word of the next major frame. Fifteen formats are available (0_{16} to E_{16} in hexadecimal format; FORMAT(0) is the Least Significant Bit [LSB]).

X_SYNC_IN±

This differential ended RS-422 input is for a slave chassis (CHASSIS_ID[5:0] ≠ 0 in a distributed system) and is connected to the X_SYNC_OUT± of the X_SYNC generating unit. A synchronization sequence is transmitted at the end of each major frame to synchronize operation in a distributed system (see “Synchronization of multiple chassis” on page 11).

PCM encoder outputs

The KAD/BCU/101 has the following four PCM encoder outputs. These four outputs are electrical copies of each other; three of them can be disabled to save power consumption of 300 mA (100 mA each) on the 5 volt line.

DATA[3:0]±

These four differential ended outputs comprise three RS-422 outputs and a PCM coded data output. DATA(3) is internally terminated with a 120Ω resistor. DATA[3:1] can be disabled in software in order to reduce power consumption. As the RS-422 standard doesn't require termination at the driver, and because a new and improved RS-422 device is being used, DATA[2:0] are not internally terminated. DATA(3) is internally terminated with a 120Ω resistor for future use. DATA[3:1] are electrical copies of DATA(0).

DCLK[3:0]±

These are four differential ended RS-422 outputs. These differential Data CLocK (DCLK) signals consist of a transition at the start and center of each bit transmitted. DCLK(3) is internally terminated with a 120Ω resistor. DCLK[3:1] can be disabled in software in order to reduce power consumption. As the RS-422 standard doesn't require termination at the driver, and because a new and improved RS-422 device is being used, DCLK[2:0] are not internally terminated. DCLK(3) is internally terminated with a 120Ω resistor for future use. DCLK[3:1] are electrical copies of DCLK(0).DATA

This is a single ended BTTL output with 100Ω resistor in series.

DCLK

This is a single ended BTTL clock output with 100Ω resistor in series. It becomes the inverse of the DATA output when the module is configured to generate an ARINC-573/717 data stream.

WORD_PULSE

This is a single ended BTTL output with 100Ω resistor in series. It’s high for the last bit of each word. Its falling edge is aligned to the end of the last bit of each word.

MINOR_PULSE

This is a single ended BTTL output with 100Ω resistor in series. It’s high for the last word of each minor frame. Its falling edge is aligned to the end of the last bit of each minor frame.

MAJOR_PULSE

This is a single ended BTTL output with 100Ω resistor in series. It’s high for the last word of each major frame. Its

falling edge is aligned to the end of the last bit of each major frame.

Timing, bit-rates and commutation

The following figure shows examples of timing for NRZL and Bi-Phase L (BIØ-L). For maximum bit-rates and supported PCM transmission, see “Specifications” on page 2.

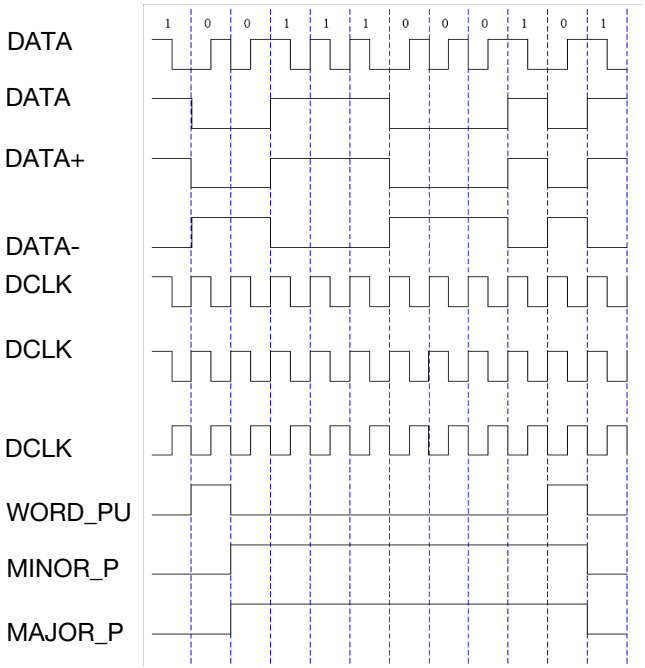


Figure 2: Timing for outputs

The KAD/BCU/101 allows variable word lengths and non-standard commutation (that is, samples of a specific parameter not evenly spaced in the PCM frame). To avoid difficulties with minimum word transit time, we recommend using a default word length (for example, 16 bits) and evenly spaced commutation.

Minimum word transmit time

The minimum word transmit time is 500 ns for the KAD/BCU/101. Therefore at 20Mbps the minimum word size is 10 bits (20Mbps × 500ns = 10 bits). In the example of a 16-bit parameter fragmented in a 2 × 12-bit subframe, the 4-bit LSB has also to be considered in the minimum word transmit time.

NOTE: Word size cannot go above 16 bits, therefore any sync word which is more then 16 bits is split into two words.

ARINC-573 setup

When the ARINC-573/717 mode of operation is selected, the DCLK output becomes the logical inverse of the DATA output and is used as the DATA- output for the ARINC-573/717 system. The DATA output is used as the DATA+ output for the ARINC-573/717 system.

Understanding formats

Formats are user-created configurations used by Acra KAM-500 equipment. They are designed using software tools and programmed into the hardware. Typical formats contain information about the following:

- PCM frame rate and PCM code used
- The number of bits per word
- The number of words per minor frame
- The number of minor frames in a major frame
- Parameters and sample rates for modules active in that format

In the format example in the following figure, a chassis contains one backplane controller and three data acquisition modules. All modules have six channels.

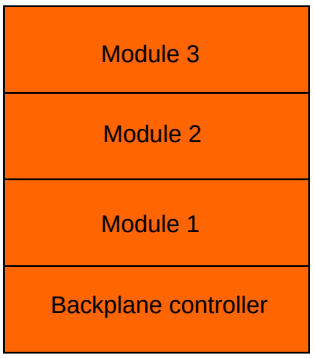


Figure 3: Format example

During a series of tests, there could be two distinct test scenarios.

Scenario 1

MinorFrame0	M1 Ch.1	M1 Ch.2	M1 Ch.3		M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.4	M3 Ch.5	M3 Ch.6		Sync Pattern
MinorFrame 1	M1 Ch.1	M1 Ch.2	M1 Ch.3									Sync Pattern
MinorFrame 2	M1 Ch.1	M1 Ch.2	M1 Ch.3		M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.4	M3 Ch.5	M3 Ch.6		Sync Pattern
MinorFrame 3	M1 Ch.1	M1 Ch.2	M1 Ch.3									Sync Pattern
MinorFrame 4	M1 Ch.1	M1 Ch.2	M1 Ch.3		M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.4	M3 Ch.5	M3 Ch.6		Sync Pattern
MinorFrame 5	M1 Ch.1	M1 Ch.2	M1 Ch.3									Sync Pattern
MinorFrame 6	M1 Ch.1	M1 Ch.2	M1 Ch.3		M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.4	M3 Ch.5	M3 Ch.6		Sync Pattern
MinorFrame 7	M1 Ch.1	M1 Ch.2	M1 Ch.3									Sync Pattern

M = Module; Ch. = Channel

Figure 4: Major frame structure (1)

In the scenario illustrated in the previous figure, the information of interest is as follows:

- Channels 1/2/3 on Module 1 sampled at 2048 sps
- Channels 4/5/6 on Module 2 and Module 3 sampled at 1024 sps

Scenario 2

MinorFrame0	M1 Ch.4	M1 Ch.5	M1 Ch.6	M3 Ch.5	M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.5	Sync Pattern
MinorFrame 1				M3 Ch.5				M3 Ch.5	Sync Pattern
MinorFrame 2	M1 Ch.4	M1 Ch.4	M1 Ch.6	M3 Ch.5				M3 Ch.5	Sync Pattern
MinorFrame 3				M3 Ch.5				M3 Ch.5	Sync Pattern
MinorFrame 4	M1 Ch.4	M1 Ch.4	M1 Ch.6	M3 Ch.5	M2 Ch.4	M2 Ch.5	M2 Ch.6	M3 Ch.5	Sync Pattern
MinorFrame 5				M3 Ch.5				M3 Ch.5	Sync Pattern
MinorFrame 6	M1 Ch.4	M1 Ch.4	M1 Ch.6	M3 Ch.5				M3 Ch.5	Sync Pattern
MinorFrame 7				M3 Ch.5				M3 Ch.5	Sync Pattern

M = Module; Ch. = Channel

Figure 5: Major frame structure (2)

In the scenario illustrated in the previous figure, the information of interest is as follows:

- Channels 4/5/6 on Module 1 sampled at 1024 sps
- Channels 4/5/6 on Module 2 sampled at 512 sps
- Channel 5 on Module 3 sampled at 4096 sps

A separate format can be created for each of the above scenarios as in these examples:

(Scenario 1) Format 0 (FORMAT[3:0] = [0,0,0,0])

(Scenario 2) Format 1 (FORMAT[3:0] = [0,0,0,1])

The Acra KAM-500 system changes to the appropriate format if the format select lines equal one of these values. There are 15 available formats for user application.

Addressing multiple chassis

There are six chassis select lines permitting you to define any address from 0-63. Any slot can be used to distribute information to and from two additional chassis using the appropriate Curtiss-Wright equipment.

CHASSIS_ID[5:0] must be unique for each chassis in the distributed system, otherwise the system cannot be programmed or used correctly.

CHASSIS_ID[5:0] = 000000 is used to identify the master chassis.

Synchronization of multiple chassis

Synchronization of multiple chassis is achieved using X_SYNC. X_SYNC is a broadcast synchronization signal with a 1 µs resolution, transmitted by the X_SYNC source and received by all X_SYNC targets. X_SYNC contains information about the time, format used, and the start of the acquisition cycle.

The controller in the master chassis (CHASSIS_ID[5:0] = 0) generates X_SYNC if no other X_SYNC source is installed in the master chassis.

If an X_SYNC source is present in the master chassis, the KAD/BCU/101 in the master chassis acts as an X_SYNC slave, X_SYNC being provided by the alternative X_SYNC source.

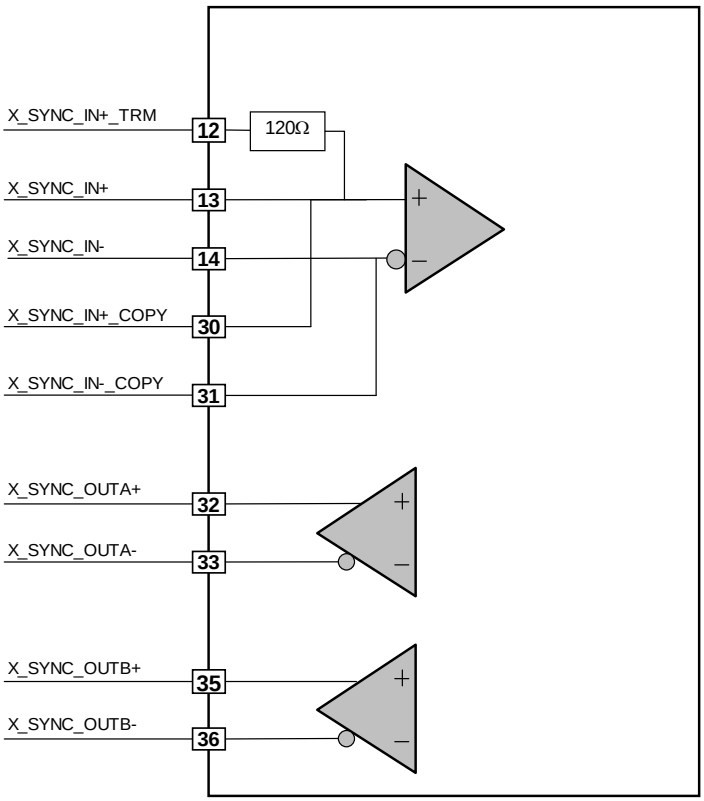


Figure 6: X_SYNC in the KAD/BCU/101

Considerations when implementing a distributed system

Distributed systems often have chassis separated by distances of many feet. Sending X_SYNC over these cables results in delays. To compensate for this, review the *Cables* data sheet for the cable used to determine the delay induced by that cable.

NOTE: To reduce crosstalk noise, we recommend using high quality, shielded twisted pair cabling between chassis.

The delay is calculated as cable length (feet) multiplied by delay parameter per foot. These details can be entered into the KSM-500 setup window when creating the distributed system format.

The resolution for the adjustment of X_SYNC is 125 ns. A maximum of 1.5 µs can be used as a delay. Consider the following scenarios:

Master with single slave scenario

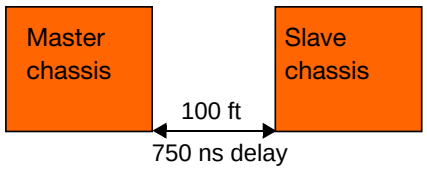


Figure 7: Master with single slave

In the previous figure, a master and slave chassis are separated by 100 feet of cable, and the cable has a propagation delay of 7.5 ns/foot. The delay in sending X_SYNC to the slave is 750 ns. In this case, the master acquisition cycle is delayed by 750 ns so that the slave and master trigger simultaneously.

Master with two slaves scenario

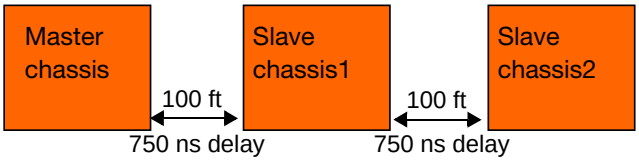


Figure 8: Master with two slaves

In the previous figure, a master and two slaves are each separated by 100 feet of cable, and the cable has a propagation delay of 7.5 ns/foot. The delay in sending X_SYNC to Slave chassis1 is 750 ns, and a further delay of 750ns in sending X_SYNC to Slave chassis2.

In this case, the master acquisition cycle is delayed by 2 × 750 ns = 1.5 µs, and the delay is programmed into Slave chassis1 as 750 ns so that both slaves and the master trigger simultaneously.

Wiring termination

For help wiring the X_SYNC_IN_TRM+ and PROG_DATA_TRM+, see Figure 5, “Recommended wiring diagram for the distributed Acra KAM-500 system,” in the *Acra KAM-500 Databook*.

Memory recording trigger (MEM-TRIGGER)

The MEM-TRIGGER input controls the state of Mem Trigger Status (bit R[15]) in the Status register. This pin can be used to provide an external input to the Data Acquisition Unit, allowing memory modules to be triggered by an operator-controlled switch or external circuitry.

CRC generation

The KAD/BCU/101 supports insertion of CRC at the end of every minor frame (CRC generation is supported in KSM-500 only).

The KAD/BCU/101 only supports CRC insertion when using a CRC-CCITT (Comité Consultatif International de Télégraphique et Téléphonique) polynomial with the following specifications:

- Width = 16 bits
- Truncated polynomial = 0x1021
- Initial value = 0xFFFF
- Input data is not reflected
- Output CRC is not reflected
- No XOR (eXclusive OR) is performed on the output CRC

Connector pinout of the KAD/BCU/101

PIN	NAME	SEE SPECIFICATIONS TABLE	COMMENT
1	FORMAT(0)	BTTL inputs	Format select line; internally pulled to 0; LSB
2	FORMAT(1)	BTTL inputs	Format select line; internally pulled to 0
3	FORMAT(2)	BTTL inputs	Format select line; internally pulled to 0
4	CHASSIS_ID(0)	BTTL inputs	Chassis identifier/address; internally pulled to 0; LSB
5	CHASSIS_ID(1)	BTTL inputs	Chassis identifier/address; internally pulled to 0
6	CHASSIS_ID(2)	BTTL inputs	Chassis identifier/address; internally pulled to 0
7	CHASSIS_ID(3)	BTTL inputs	Chassis identifier/address; internally pulled to 0
8	FORMAT(3)	BTTL inputs	Format select line; internally pulled to 0; MSB
9	GND	Internal ground	
10	BVDD	BVDD outputs	5V buffered with 220Ω resistor; used to set FORMAT and CHASSIS_ID
11	MEM-TRIGGER	BTTL inputs	Trigger for memory recording; internally pulled to 0
12	X_SYNC_IN_TRM+	RS-422 inputs	Synchronization in; with internal 120Ω resistor
13	X_SYNC_IN+	RS-422 inputs	Synchronization in; not internally terminated
14	X_SYNC_IN-	RS-422 inputs	Synchronization in; not internally terminated
15	DATA(0)+	High-speed RS-422 outputs	PCM output 0
16	DATA(0)-	High-speed RS-422 outputs	PCM output 0
17	DCLK(0)+	High-speed RS-422 outputs	Bit clock for PCM output 0
18	DCLK(0)-	High-speed RS-422 outputs	Bit clock for PCM output 0
19	WORD_PULSE	BTTL outputs	High for last bit of word
20	MINOR_PULSE	BTTL outputs	High for last word of minor frame
21	MAJOR_PULSE	BTTL outputs	High for last word of major frame
22	DATA	BTTL outputs	PCM output or DATA+ for ARINC-573 out
23	DCLK	BTTL outputs	Bit clock for PCM or DATA- for ARINC-573 out
24	NRZ_L	BTTL outputs	Uncoded PCM output
25	PROG_DATA+	RS-485	Programming data line; not internally terminated
26	PROG_DATA-	RS-485	Programming data line; not internally terminated
27	PROG_DATA_TRM+	RS-485	Programming data line; with internal 120Ω resistor
28	PROG_DATA+_COPY	RS-485	Copy of Pin 25
29	PROG_DATA-_COPY	RS-485	Copy of Pin 26
30	X_SYNC_IN+_COPY	RS-422 inputs	Copy of Pin 13
31	X_SYNC_IN-_COPY	RS-422 inputs	Copy of Pin 14
32	X_SYNC_OUTA+	Low-speed RS-422 outputs	Synchronization out; internally terminated with 120Ω
33	X_SYNC_OUTA-	Low-speed RS-422 outputs	Synchronization out; internally terminated with 120Ω
34	DATA(1)+	High-speed RS-422 outputs	PCM output 1
35	X_SYNC_OUTB+	Low-speed RS-422 outputs	Synchronization out; internally terminated with 120Ω
36	X_SYNC_OUTB-	Low-speed RS-422 outputs	Synchronization out; internally terminated with 120Ω
37	CHASSIS_ID(4)	BTTL inputs	Chassis identifier/address; internally pulled to 0
38	CHASSIS_ID(5)	BTTL inputs	Chassis identifier/address; internally pulled to 0; MSB
39	DATA(1)-	High-speed RS-422 outputs	PCM output 1
40	DCLK(1)+	High-speed RS-422 outputs	Bit clock for PCM output 1
41	DCLK(1)-	High-speed RS-422 outputs	Bit clock for PCM output 1
42	DATA(2)+	High-speed RS-422 outputs	PCM output 2
43	DATA(2)-	High-speed RS-422 outputs	PCM output 2
44	DCLK(2)+	High-speed RS-422 outputs	Bit clock for PCM output 2
45	DCLK(2)-	High-speed RS-422 outputs	Bit clock for PCM output 2
46	DATA(3)+	High-speed RS-422 outputs	PCM output 3; internally terminated with 120Ω
47	DATA(3)-	High-speed RS-422 outputs	PCM output 3; internally terminated with 120Ω
48	DCLK(3)+	High-speed RS-422 outputs	Bit clock for PCM output 3; internally terminated with 120Ω
49	DCLK(3)-	High-speed RS-422 outputs	Bit clock for PCM output 3; internally terminated with 120Ω
50	CHASSIS	Chassis	
51	GND	Internal ground	
52	CHASSIS	Chassis	Double-density connector only

Ordering information

PART NUMBER	DESCRIPTION
KAD/BCU/101/E	IRIG-106 backplane controller and encoder (with 52-way double-density connector)
KAM/BCU/101/E	IRIG-106 backplane controller and encoder (with 51-way micro-miniature connector)

For KAD module orders, one ACC/ASY/022/C programming cable is included with each order, while a standard mating connector, CON/KAD/002/CP, is included with each KAD module in the order. For KAM module orders, one ACC/ASY/021/04 programming cable is included with each module in the order, while a standard mating connector, ACC/CON/008/04, is included with each KAM module in the order. Their part numbers will be added to the Confirmation of Order unless an alternative is specified (see the *Cables* data sheet). In this data sheet, KAD/BCU/101 refers to both the KAD and KAM versions of the module.

Revision history

REVISION	DIFFERENCES	STATUS
KAD/BCU/101/E	Improved noise immunity on X_SYNC lines	Recommended for new programs
KAD/BCU/101/D	Increased allowable bit rates and added a read counter; supports CRC insertion at the end of minor frames	Not recommended for new programs
KAD/BCU/101/C	Extended common mode drivers for PCM and X_SYNC	Not recommended for new programs
KAD/BCU/101/B	Supports ADC/005 programming (requires kProgram 1.6 or later) and supports distributed system with external synchronization	Not recommended for new programs
KAD/BCU/101	First release	Not recommended for new programs

Supporting software

SOFTWARE	DETAILS
DAS Studio 3	User interface for setup and management of data acquisition, network switches, recorders and ground stations in an integrated environment
KSM-500	This module is supported by the KSM-500 suite of software tools

Related documentation

DOCUMENT	DETAILS
DOC/DBK/001	Acra KAM-500 Databook
DOC/HBK/002	Environmental Qualification Handbook
DOC/MAN/018	KSM-500 Databook
DOC/MAN/030	DAS Studio 3 User Manual
TEC/NOT/016	Power dissipation
TEC/NOT/024	Evolution of Pulse Code Modulation
TEC/NOT/027	IRIG 106-96 Chapter 4
TEC/NOT/049	Power estimation

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