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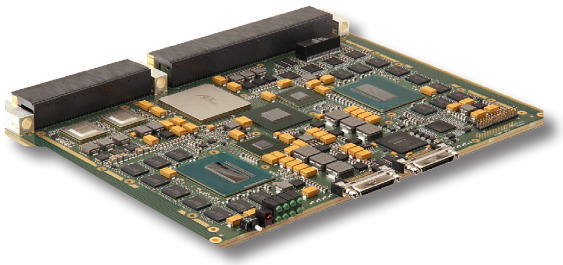
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Find the *Curtiss-Wright Champ-AV9* at our website: ***Click HERE***

# CHAMP-AV9

## Intel Core i7 Multi-processor OpenVPX Digital Signal Processing Board

CURTISSWRIGHTDS.COM



### Key Features

- 6U OpenVPX-compliant
- 2 x Gen4 Intel Core i7 Quad-Core processors
- 614 to 1280 GFLOPS peak computing performance
- 16 GB DDR3 SDRAM with ECC
- 4 x 40 Gigabit Ethernet or InfiniBand data plane interfaces at an aggregate 112 Gbps
- 2 x 16-lane PCIe 3.0 expansion plane interfaces
- Power management features
- VxWorks BSP and Linux LSP
- Rugged air-cooled and conduction-cooled versions
- TrustedCOTS

### Applications

- Radar processing
- Signal Intelligence (SIGINT)
- ISR
- Image processing
- Sensor processing
- Electronic warfare

## Overview

The CHAMP-AV9 combines the floating-point performance of the latest Intel® Core™ i7 processors, with the substantial bandwidth and system-enabling features of the 6U OpenVPX™ form factor. Providing a pair of Quad-Core Gen4 Core i7 processors, featuring the updated AVX 2.0 instruction units and redesigned on-chip GPGPU numerical co-processor, the CHAMP-AV9 offers a 2-4x performance per size, weight and power (SWaP) improvement over previous digital signal processing (DSP) modules. A dual-channel 25 GBps DDR3 memory per CPU provides ample bandwidth to simultaneously serve CPU access and streaming I/O from the VPX backplane interfaces.

The Intel Quad-Core Gen4 Core i7 CPU's contain substantial improvements over previous generations of processors: double the floating-point performance with a fused multiply-add AVX2 instruction, ability to load two and store one operand per clock, L1 and L2 cache bandwidth doubled, faster CPU clock, and substantially improved on-chip Graphics Execution Units. The CHAMP-AV9 specifically has been upgraded to DDR 1600 and rugged implementations will incorporate thermal management solutions that minimize CPU throttling at Curtiss-Wright's benchmark L100 and L200 environments. This contrasts with competitive solutions that look good on paper, but throttle severely or are simply unable to operate at an 85°C conduction-cooled card-edge.

The CHAMP-AV9 incorporates the enhancements of the OpenVPX (VITA 65) standard with a complete suite of data plane, expansion plane, and control plane interfaces. With up to 14 GBps of data plane fabric and 32 GBps of expansion plane performance, the CHAMP-AV9 has the bandwidth required to effectively harness the power of the processors.

The CHAMP-AV9 is the DSP multi-processing component of Curtiss-Wright Defense Solution's High Performance Embedded Computing (HPEC) solution set that also includes FPGA modules, GPGPU's, mezzanine carriers, FMC and XMC I/O, fabric switching, single board computers, backplanes and enclosure packaging.

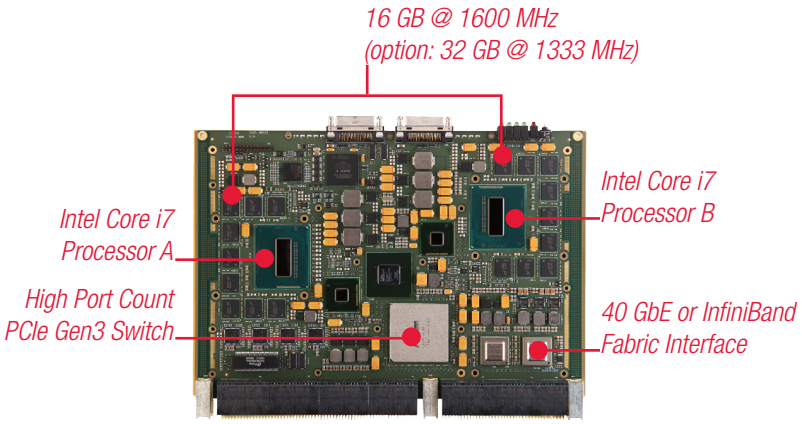



Figure 1: CHAMP-AV9 key features

# Features

## Backplane I/O

- 4 x data plane (fat pipe) ports with RDMA and up to 14 GBps bi-directional bandwidth running:
  - XAUI/10 GBase-KX4 – 4 x 10 Gigabit Ethernet port (3.125 Gbps per lane)
  - 40 GBase-KR4 – 4 x 40 Gigabit Ethernet port (10.3125 Gbps per lane)
    - DDR: 5 Gbps per lane
    - QDR: 10 Gbps per lane
    - FDR10: 10.3125 Gbps per lane
- PCI Express® (PCIe) Gen1/2/3 expansion plane with up to 32 GBps bi-directional bandwidth
- 2 x 1000Base-KX Ethernet (SerDes) control plane interfaces
- 2 x 1000Base-T Ethernet interfaces (front/rear build option)
- 2 or 4 x EIA-232 serial ports configurable to 422/485
- 2 x EIA-422/485 serial ports
- 2 x USB 2.0/3.0 interfaces
- 2 x external SATA ports: 1 (1.5 Gbps), 2 (3 Gbps), 3 (6 Gbps)
- 4 x DisplayPort 1.2 interfaces: 1.62, 2.7 or 5.4 G per lane at x1, x2 or x4 lanes
  - Each site supports 4/8 high speed serial (HSS) links for JESD204B or serial FMCs

## Front panel I/O (build option)

- Board reset
- LEDs
- 2 x SDR50 connectors, one for each CPU containing:
  - 1000Base-T Ethernet interfaces
  - EIA-232 serial port configurable to 422/485
  - USB interface
  - eSATA interface
  - DisplayPort interface

## Rear Transmission Module panel interfaces

- 2 x USB - Type A receptacle
- 2 x eSATA
- 4 x mini DisplayPort
- 2 x 1000Base-T Ethernet interfaces – RJ45
- 2 x serial ports - Micro DB9
- Board reset button

## Additional features

- 16 GB SATA (NAND) flash per processor
- 16 MB boot flash per processor
- Protected backup boot flash per processor
- 256 KB NVRAM
- 16 x LVTTL I/O signals with interrupt
- Differential discrete I/O
- 12 x general purpose timers
- Avionics watchdog timer
- 16 x semaphore registers
- Multi-board synchronous clock feature
- Intelligent Platform Management Interface (IPMI) support
- Power consumption sensors
- Temperature sensors
- User variable processor frequency to control power consumption
- TrustedCOTS™
- Secure write-protection on all non-volatile memory
- Declassify function to erase non-volatile memory

## Software support

- VxWorks 6.9.3.3 64-bit BSP supporting SMP
- Fedora™ 19 64-bit LSP
- Red Hat® Enterprise Linux® (RHEL) 7.X 64-bit LSP
- Continuum™ Vector and VSIPL-optimized DSP function library
- OFED™/Open MPI
- Gedae

## Standards

- VITA 48 1” pitch
- VITA 65



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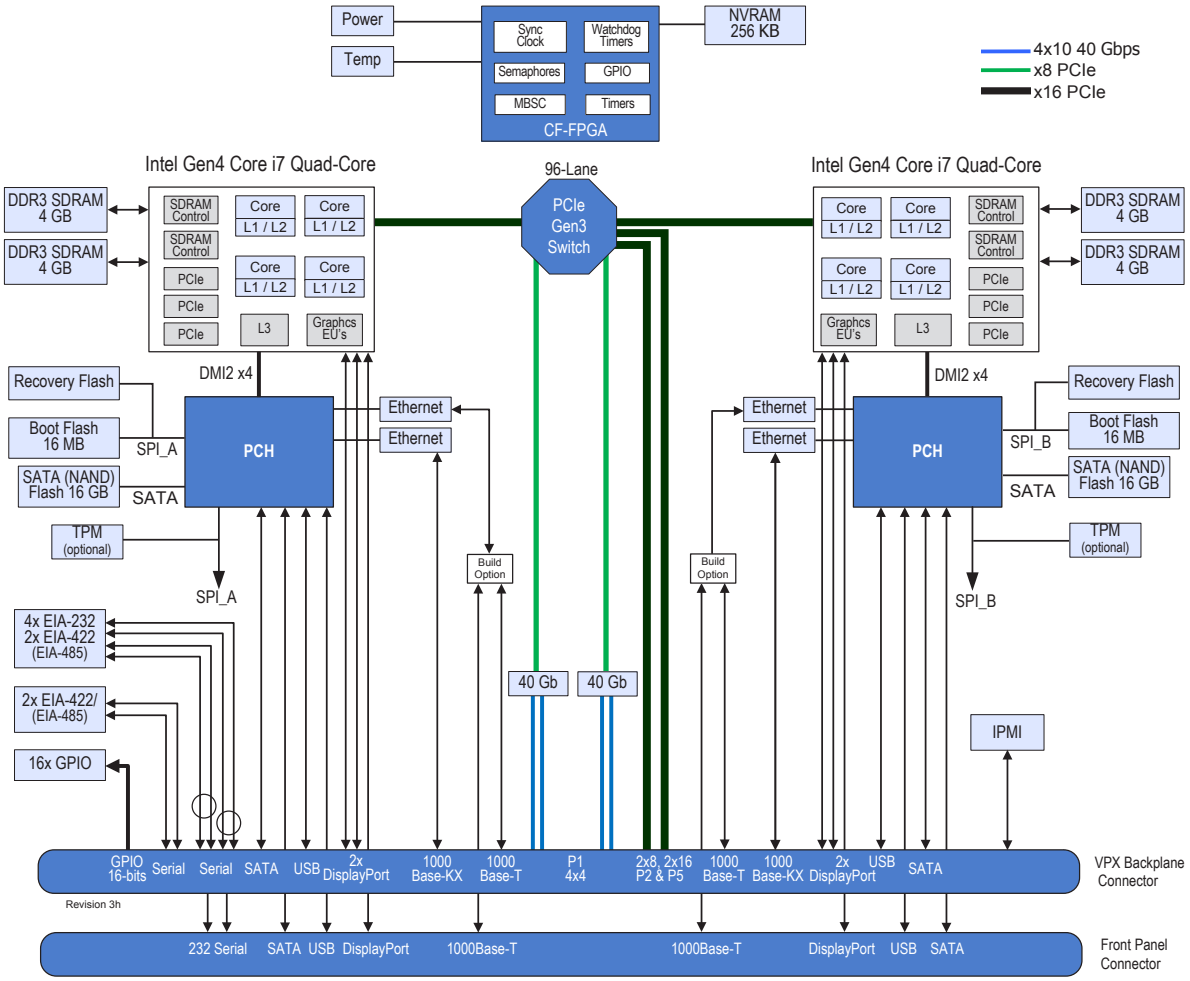



Figure 2: CHAMP-AV9 block diagram

# Quad-Core Intel Core i7 Processors

The CHAMP-AV9 incorporates two Gen4 Intel Core i7-4700EQ Quad-Core processors which are a low power embedded implementation of Intel's newest 22nm micro-architecture. Building on the floating-point leadership of its AVX instruction set, Intel has released AVX 2.0 which doubles floating-point efficiency by fusing add and multiply operations into a single SIMD instruction. At 2.4 GHz, the Core i7-4700EQ processor provides a peak 307 CPU GFLOPS. At 614 GFLOPS overall for the board, the CHAMP-AV9 supports more than twice the raw floating-point performance of the previous generation Intel DSP board. When including the capability of the on-chip Graphics Execution Units, floating-point performance increases to an unprecedented 1.28 TFLOPS, more than four times the performance of the previous generation solution. With its tremendous processing resources, the CHAMP-AV9 potentially reduces size, weight, power and cost (SWaP-C) of distributed, multi-processor, HPEC applications by two to four times.

Each core contains first level instruction and data caches (32 KB, 8-way) and a second level unified cache (256 KB, 8-way). A last level cache (6 MB 16-way) is shared between all processor cores. The Core LLC's, graphics unit, and system agent are connected via a high-speed uni-directional ring bus, internal to the CPU and decoupled from CPU frequency. The Core i7-4700EQ features Intel's Hyper-Threading Technology which enables each core to execute two software threads concurrently. Hyper-Threading results in a higher utilization rate of the CPU execution units and thus a greater rate of instructions per unit of time.

Featuring a dual-channel, 1600 MHz DDR3L SDRAM interface, each CPU has a peak memory bandwidth of 25 GBps. The Gen4 Core i7 processor features many improvements in the cache subsystem: improved prefetching, better cache line split latency and most importantly, L1 cache bandwidth doubled to 96 bytes/cycle, and L2 bandwidth doubled to 64 bytes/cycle.

# Board Connectivity

The now mature OpenVPX (VITA 65) standardizes data plane, expansion plane, and control plane serial interfaces on VPX modules. The CHAMP-AV9 is equipped with a full implementation of these interfaces.

## Data plane

Four 40 Gb ports on the P1 connector for high-speed data transfers.

## Expansion plane

32-lanes 8 Gbps PCIe 3.0 on the P2/P5 connectors for peripheral device expansion and connection to adjunct processing elements such as FPGA's or GPGPU's.

## Control plane

Gigabit Ethernet on the P4 connector for application management and administrative functions.

# Architecture

## Data plane architecture

CHAMP-AV9 combines the computing performance of the latest Intel processors with the performance of a 40 Gbps fabric. The 40 GBase-KR4 protocol, offering four lanes of 10.3125 Gbaud signaling, uses 64b/66b which is nearly 20% more efficient than previous protocols based upon 8-bit/10-bit encoding. The interface is capable of achieving throughput of around 90% of line rate with low CPU utilization due to Remote Direct Memory Access (RDMA). InfiniBand performance is similar to Ethernet, being based on converged, dual-mode silicon. RDMA provides memory-to-memory datagram transfers across the fabric so that CPU cycles are freed up to perform value-added application processing. The CHAMP-AV9 contains four 40 Gb ports fed by two x8 PCIe Gen3 ports for an aggregate throughput of 112 Gbps or 14 GBps full duplex. The four 40 Gb ports may be associated with one CHAMP-AV9 CPU or each CPU may utilize two 40 Gb ports each. For lower speed interfaces, the Ethernet ports may operate in 10 Gigabit Ethernet XAUI mode, 4-lanes at 3.125 Gbaud, and may also be set to InfiniBand mode, at various lane speeds, for use with an InfiniBand fabric.

## PCIe expansion plane architecture

The CHAMP-AV9 makes use of the Intel CPU's x16 PCIe 3.0 interfaces (16 GBps full duplex) to connect to a Gen3 PCIe switch. This allows the processors to interface to the data fabric and to PCIe endpoints via the 16-lane P2 and 16-lane P5 expansion plane connectors. The 32 switch lanes facing the P2 and P5 VPX backplane connectors may be configured as two x16 ports, four x8 ports, and eight x4 ports. The PCIe switch also allows backplane ports to be configured to PCIe 1.0 or 2.0. This configuration flexibility allows the CHAMP-AV9 to serve as host to GPGPU's, FPGA's, sensor I/O modules and PCIe peripheral devices. Figure 3 shows how the CHAMP-AV9 expansion plane provides access to two CHAMP-WB modules configured with ADC's or DAC's.

The CHAMP-AV9 expansion plane is also an ideal means to add PCIe peripherals and I/O devices. The VPX6-215 ExpressReach PMC/XMC and IPM carrier card provides AV9 access to industry-standard PMC modules and/or XMC modules. The CHAMP-AV9 may be configured to use four 8-lane PCIe ports to control four PMC or XMC mezzanine modules on the PMC/XMC mezzanine carrier. See the section below on rear transition modules (RTM) for information on configuring custom expansion plane topologies.

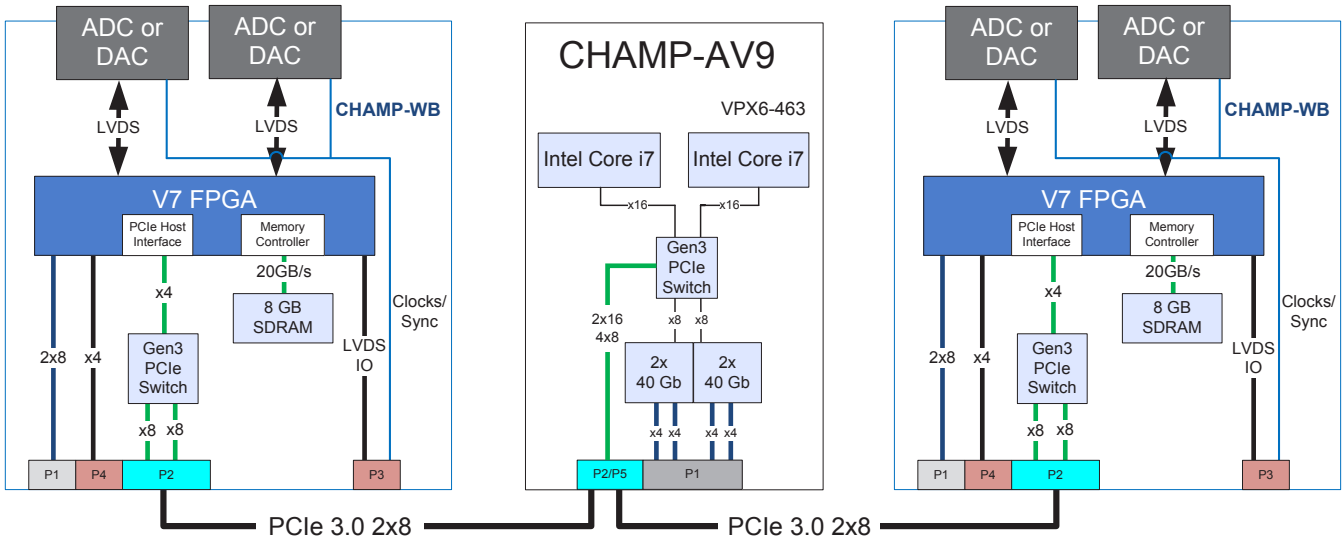



Figure 3: CHAMP-AV9 expansion plane provides 32 GBps full duplex access to sensor I/O

### Double Data Rate (DDR3) SDRAM with ECC

Each processor on the CHAMP-AV9 supports 8 GB of DDR3 SDRAM for a total of 16 GB on the board. A 32 GB variant is feasible using higher capacity DDR3-1333 DRAM. The Core i7 processor features two independent memory controllers. With two banks of DDR3-1600 SDRAM, each processor achieves a peak memory bandwidth of 25 GBps. The memory is protected with Error Checking and Correcting (ECC) circuitry that can detect and correct all single-bit errors and detect all double-bit errors. CHAMP-AV9 uses soldered-down BGA memories to avoid compromising trust and to insure maximum ruggedness.

## Memory

### Protected Boot Flash memory

Each processor is equipped with 16 MB of flash memory used to store the system BIOS and Power-on diagnostics firmware (PBIT). The boot flash device supports a minimum of 100,000 erase cycles per sector and retains data for more than 20 years. In the event of accidental corruption of the primary boot flash, both processors may boot from a secondary recovery flash in order to regain operation of the card and initiate recovery of the primary flash.

### SATA (NAND) Flash memory

A single, shared 256 KB non-volatile memory provides non-volatile storage of application state data that must not be lost when power is removed. During normal operation, application software reads/writes the serial NVRAM via BSP functions. The NVRAM is accessed like an SRAM, except that data is retained after power is removed. Both processors have access to the NVRAM device. Data written to the NVRAM is immediately non-volatile. The device is rated for a minimum of 100 trillion (1014) read/write cycles. The data retention period is 10 years. For security against inadvertent writes to NVRAM, a hardware write-protection feature is provided. The NVMRO (Non-Volatile Memory Read Only) is a system-wide signal defined in VITA 46 which may be asserted to prevent the CHAMP-AV9 NVRAM from being updated.

### Non-volatile memory security

The CHAMP-AV9, like other Curtiss-Wright Continuum products, provides for the management of non-volatile memory devices in classified circumstances. All of the non-volatile devices, boot flash, backup boot flash, NAND flash, NVRAM and FPGA PROM may be write-protected by hardware jumpers. The jumpers may be visually inspected to conform to security procedures. The firmware of the CHAMP-AV9 provides a non-volatile memory scrub function to perform a secure erase of the boot flash, NAND flash and NVRAM per NISPOM requirements.

### Gigabit Ethernet

Each processor on the CHAMP-AV9 is equipped with two Gigabit Ethernet interfaces. A 1000Base-KX interface from each CPU supports the OpenVPX control plane. These connect to an OpenVPX fabric switch. Each CPU also has a second 10/100/1000Base-T interface routed to the front panel on air-cooled variants and to the rear panel on conduction-cooled variants.

## Utility Features, Semaphores, Timers

The CHAMP-AV9 features a number of utility features to facilitate multiprocessor application software. The board provides sixteen hardware semaphore registers which are useful to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory to access the semaphores. The CHAMP-AV9 also provides six general purpose 32-bit timers. These may be configured for a timeout value between 20ns and 85sec, with a resolution of 20ns. Each timer may be configured to generate an interrupt to either processor. The current timer value may be read at any time by software.

### Avionics style watchdog timer

The CHAMP-AV9 provides two watchdog timers for each processor. Each watchdog timer is a pre-settable down-counter with a resolution of 1 µsec. Time-out periods from 0 ms to 33.6 seconds can be programmed. Initialization software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset or a system reset. Once enabled to cause a reset, the watchdog cannot be disabled. For development and maintenance purposes, a backplane signal can be asserted to disable all watchdog interrupts. The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can be configured to operate in “Avionics” mode whereby a minimum interval between writes to the watchdog register is also enforced. Writing to the watchdog register too soon or too late causes an exception event.

### Multi-board Synchronous Clock

The CHAMP-AV9 includes a special purpose counter, the Multi-board Synchronous Clock (MBSC) which may be synchronized with corresponding counters on other boards in the same system. This common time base allows a developer to timestamp messages and/or data buffers, with the knowledge that the local time is maintained at the same value by all the boards in the system. The counter can be

set to rollover to a pre-loaded value and interrupt on rollover. This feature is typically most valuable for debugging and instrumenting multi-board applications code, which can present challenges in coordinating the distribution of data items between processors. For example, the Continuum Insights Event Analysis Tool uses the MBSC to display a time-synchronized view of user-defined and system events.

### Serial ports

The CHAMP-AV9 provides four EIA-232 serial ports and two EIA-422 serial ports. Each processor has two EIA-232 serial ports, implemented with 16550-compatible UARTs within an on-board utility FPGA called the Core Functions FPGA (CF-FPGA). The EIA-232 serial ports support asynchronous communications with one transmit and one receive signal. One port from each processor is available on the front panel connector. Both ports from each processor are connected to the backplane connectors. The EIA-232 ports support operation up to 115 Kbaud. Each processor is also provided with an EIA-422/485 differential serial port utilizing a 16550-compatible UART within the Core Functions FPGA. The EIA-422/485 ports support asynchronous communications with one transmit and one receive pair each. The EIA-422/485 ports operate at up to 115 Kbaud and are connected to the backplane connectors.

### USB, SATA, DisplayPort interfaces

Each CPU on CHAMP-AV9 has one front-panel USB interface and one backplane USB 3.0 interface (four total). Each processor also has a front and rear eSATA interface (four total). Each CPU has two rear backplane and one front panel DisplayPort interface.

### LVTTL discrete digital I/O

The CHAMP-AV9 provides sixteen general purpose LVTTL I/O lines which are accessible at the backplane connector. Each bit is individually programmable to be an input, output or I/O. All bits configured as an input may be used to trigger an interrupt which is further programmable to be level- or edge-sensitive. Both levels and transition directions may be detected. The LVTLL I/O lines are terminated with an on-board pull-up resistor. The digital I/O lines are 5V tolerant.

### EIA-422 differential discrete digital I/O

The CHAMP-AV9 provides the capability to discretely control the outputs of the two EIA-422 drivers which are normally associated with EIA-422 serial channels. In a similar fashion, there are registers that can read the state of the EIA-422 receivers, independent of the serial controller. In total there are two inputs and two outputs. The inputs may be configured to generate an interrupt. When configured as discrete differential I/O, the drivers and receivers can be used as general purpose differential-mode control signals unrelated to serial I/O.

## Sensors

### Power and temperature

The CHAMP-AV9 is equipped with a suite of power and temperature sensors that provide users with visibility into the board environment. The card features current and voltage sensors for the backplane power rails, enabling the user to measure the real-time power consumption of the entire card. Since the power consumption of the board depends on many factors including the processor clock frequency, the nature of the software, SDRAM loading, and the operating temperature of the card, the ability to measure actual power for a given application eliminates guesswork in system power consumption estimates.

The CHAMP-AV9 also provides a number of temperature sensors. There are sensors for the edges and center of the board, the processor die, the I/O hub die and the Core Functions FPGA junction temperature.

### Indicator LEDs

The CHAMP-AV9 provides eight user-controllable green LEDs, four per processor. These are visible on the front panel. There is an additional red LED on the front panel to indicate a failure determined by the on-board diagnostic firmware. A backplane signal is also asserted in conjunction with the fail LED.

# Software

## System software

The CHAMP-AV9 is supported with an extensive array of software tools, libraries and middleware. CHAMP-AV9 has board support packages (BSPs) available for VxWorks and Linux.

## Continuum Software Architecture (CSA)

The CHAMP-AV9 is supported by a suite of firmware, Operating Systems (OS), RTOS BSP, communication libraries and signal processing libraries. The Continuum Software Architecture is Curtiss-Wright's suite of firmware and BSP application programming interface (API) that is common to all SBC (VME, CompactPCI® and VPX) and multi-processor boards. Developers of mixed systems will find a common set of features and software interfaces for all future processing products from Curtiss-Wright.

The Continuum Software Architecture is comprised of Continuum Firmware Monitor, OS Software, and Continuum VSIPL/Vector Library.

## Continuum VSIPL/Vector Library

The CHAMP-AV9 derives its floating-point performance from the Intel SIMD AVX/SSE vector processing unit. The Continuum Vector Library provides over 200 functions optimized for the Intel SIMD instruction set architecture, providing the foundation for most signal processing applications. Continuum Vector provides the user with a choice of APIs with support for the Vector Signal Image Processing Library (VSIPL, Core Lite) standard and the popular API established by Floating Point Systems Inc. See the Continuum Vector datasheet for detailed information.

## Open Fabric Enterprise Distribution (OFED)

The CHAMP-AV9 Linux software stack includes an API which includes all of the basic functionality needed to setup and move data over the data plane fabric. OFED is a networking open source software package that implements Remote Direct Memory Access (RDMA) and kernel bypass mechanisms to deliver high-efficiency computing, wire-speed data movement for distributed systems. OFED is a key enabler for running Open MPI, a freely downloadable, open source version of Message Passing Interface (MPI) middleware.

# Cables and RTM

The CHAMP-AV9 features a high-density, rugged front panel connector. The connector provides access to two EIA-232 serial ports, two Gigabit Ethernet ports, two USB ports, and a board reset input. An adapter cable is available (part number CBL-463-FPL-000) that breaks out the signals to a number of standard connectors.

A rear transition module (RTM) is available (part number RTM-463-000) to provide easy access to the backplane I/O signals. The RTM is a 6Ux80 mm (1101.10-compliant) module with a rear face plate and injector/ejector handles that plugs into the rear of the VPX backplane to make connections with the I/O signals emanating from the CHAMP-AV9 connectors. The RTM provides standard connectors for 1000Base-T Gigabit Ethernet (2), EIA-232 (4), USB (2), eSATA (2), DisplayPort (4) and reset. The RTM also features a number of switches and headers for access to other AV9 signals and I/O ports. The RTM is intended for development purposes and is not tested or warranted for shock and vibration.

Curtiss-Wright markets chassis variants with a 6U 6-slot straight-through backplane (part number 024-900-06-X1-01) which brings all VPX backplane signals through for access by a transition module. The CHAMP-AV9 has a second RTM which accesses many of these signals and makes them available on a rear panel using high-speed iPass™ HD connectors. This may be valuable in cabling specific data plane or expansion plane topologies which are application specific.

# Ruggedization Levels

See the Curtiss-Wright Ruggedization Guidelines factsheet for more information.

TABLE 1 Power requirements

| VOLTAGE | CURRENT |
|---|---|
| 12V (Vs1) | < 12A |
| 3.3V_AUX | < 0.3A |

Notes:

1. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).
2. The CHAMP-AV9 power consumption will vary depending on processor frequency, application usage and ambient temperature. Consult the user manual or factory for power characterization information.
3. Power consumption and weight are published after full product qualification.

# Ordering Information

The CHAMP-AV9 is ordered with the following part numbers. Additional CHAMP-AV9 board variants available, contact Curtiss-Wright Sales for details.

TABLE 2 Part numbers

| VARIANT | DESCRIPTION |
|---|---|
| VPX6-463-A04A060 | Air-cooled, L0 (0 - 50°C), 16 GB SDRAM, front panel I/O |
| VPX6-463-A14A061 | Air-cooled, L100 (-40 to +71°C), 16 GB SDRAM, rear panel Ethernet |
| VPX6-463-C24A061 | Conduction-cooled, L200 (-40 to 85°C), 16 GB SDRAM, backplane 1000Base-T, rear panel I/O only |
| DSW-463-000-BIOS | BIOS update – not required if ordering BSP |
| DSW-463-000-VXW | VxWorks BSP for the CHAMP-AV9 |
| DSW-463-001-LNX | RHEL BSP for the CHAMP-AV9 |
| DSW-463-002-LNX | Fedora Linux BSP for the CHAMP-AV9 |
| MNT-463-000-VXW | Maintenance for DSW-462-000-VXW |
| MNT-463-001-LNX | Maintenance for DSW-462-001-LNX |
| MNT-463-002-LNX | Maintenance for DSW-462-002-LNX |
| RTM6-463-000 | VPX6-463 RTM: 2 x 1000Base-T Gigabit Ethernet, 2 x EIA-232, 2 x USB, 2 x eSATA, 4 x DisplayPort |
| CBL-463-FPL-000 | Front Panel SDR50 cable adapter for VPX6-463. Two cables required for both CPU's. |
| COOL-XC6-OVP06X1AB | COOL-XC6 high power air-cooled portable tower, 6-slot 6U x 1.0" OpenVPX feed thru backplane, 12V-centric power supply |
| COOL-CC6-OVP06X1AF | COOL-CC6 high power conduction-cooled portable tower, 6-slot 6U x 1.0" OpenVPX feed thru backplane, 12V-centric power supply |



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