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HARDWARE USER'S MANUAL

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1. DMV-666/SVME-667 A/D D/A Converter Card Hardware User's Manual

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DMV-666/SVME-667

ANALOG TO DIGITAL/DIGITAL TO ANALOG

CONVERTER CARD HARDWARE USER'S MANUAL

DY-4 Systems Inc.
21 Fitzgerald Road
Nepean, Ontario, Canada
K2H 9J4
(613) 596-9911

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1. GENERAL INFORMATION

This chapter details the following information for the DMV-666/SVME-667 Analog to Digital/Digital to Analog (A/D, D/A) Converter Card:

- physical characteristics including dimensions, conduction cooling, weight, mating connectors, and card ejectors.
- environmental specifications
- power requirements
- performance of the VMEbus interface
- analog specifications.

1.1 Physical Characteristics

1.1.1 Dimensions

The DMV-666 and SVME-667 A/D, D/A Converter Cards are implemented on the same format Printed Circuit Board (PCB); the overall dimensions for the two types of boards are listed in Table 1-1, Dimensions, and illustrated in Figures 1-1 and 1-2.

Table 1-1
Dimensions

Dimension	Measurement	
Height	233 mm	(9.18 in.)
Depth	160 mm	(6.3 in.)
Thickness (SVME)	20 mm	(0.8 in.)
Thickness (DMV)	10.59 mm	(0.42 in.)
PCB Thickness	1.6 mm	(0.063 in.)

1.1.2 DMV-666 A/D, D/A Converter Card Conduction Cooling

An aluminum conduction plate is bonded to the DMV-666 A/D, D/A Converter Card to conduct heat from Circuit Card Assembly (CCA) components to the edge of the CCA. Additionally, stiffening ribs are located at the faceplate, connector edge, and across the middle of the DMV-666 A/D, D/A Converter Card. These ribs provide support during vibration and shock and assist in heat dissipation.

Wedgelocks at the card edges expand to lock the card tightly into the slots of a sealed conduction-cooled chassis.

Figure 1-3, DMV-666 A/D, D/A Converter Card Conduction Cooling Plate, illustrates these features.

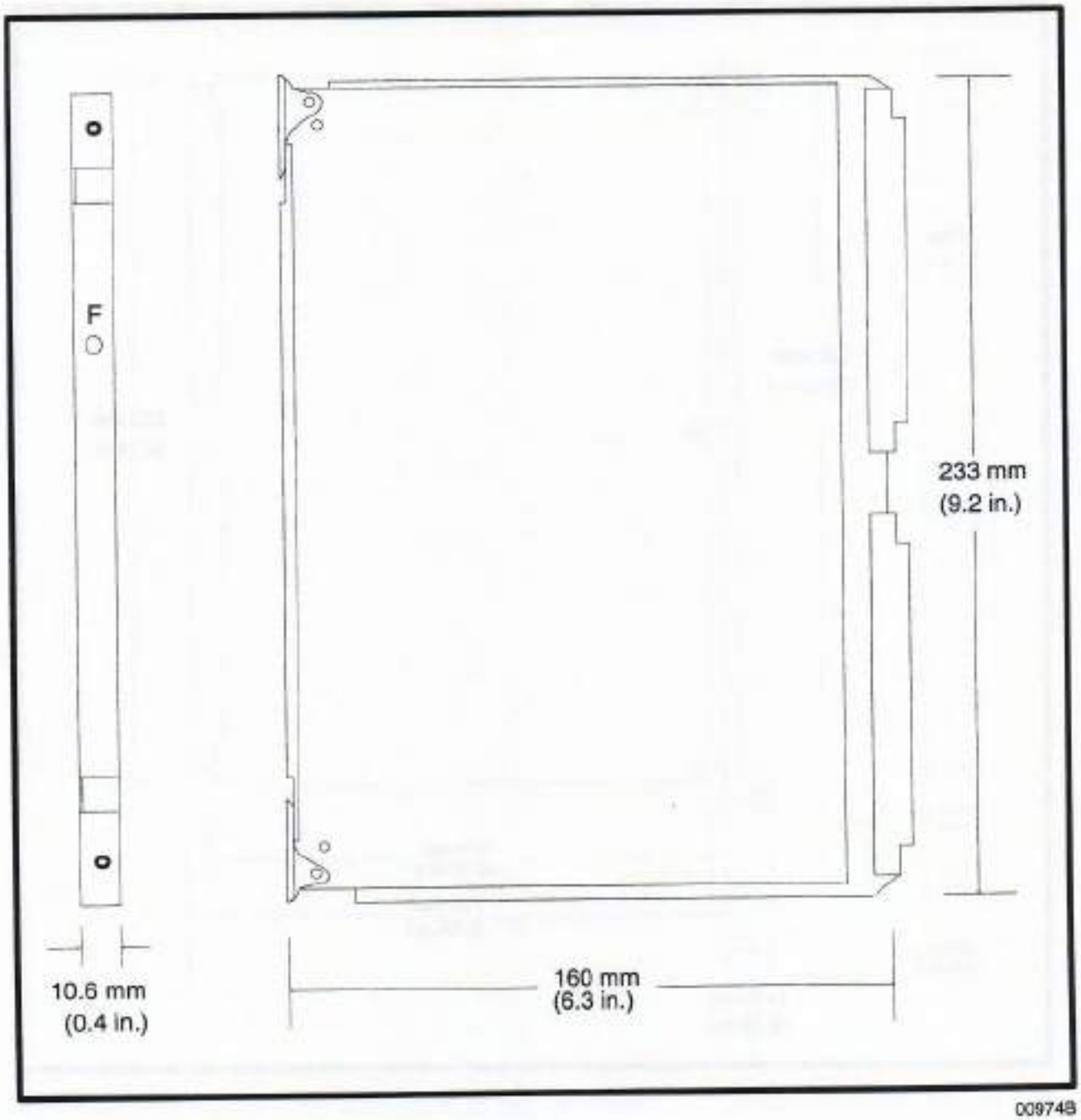


Figure 1-1: Dimensions of the DMV-666 A/D, D/A Converter Card

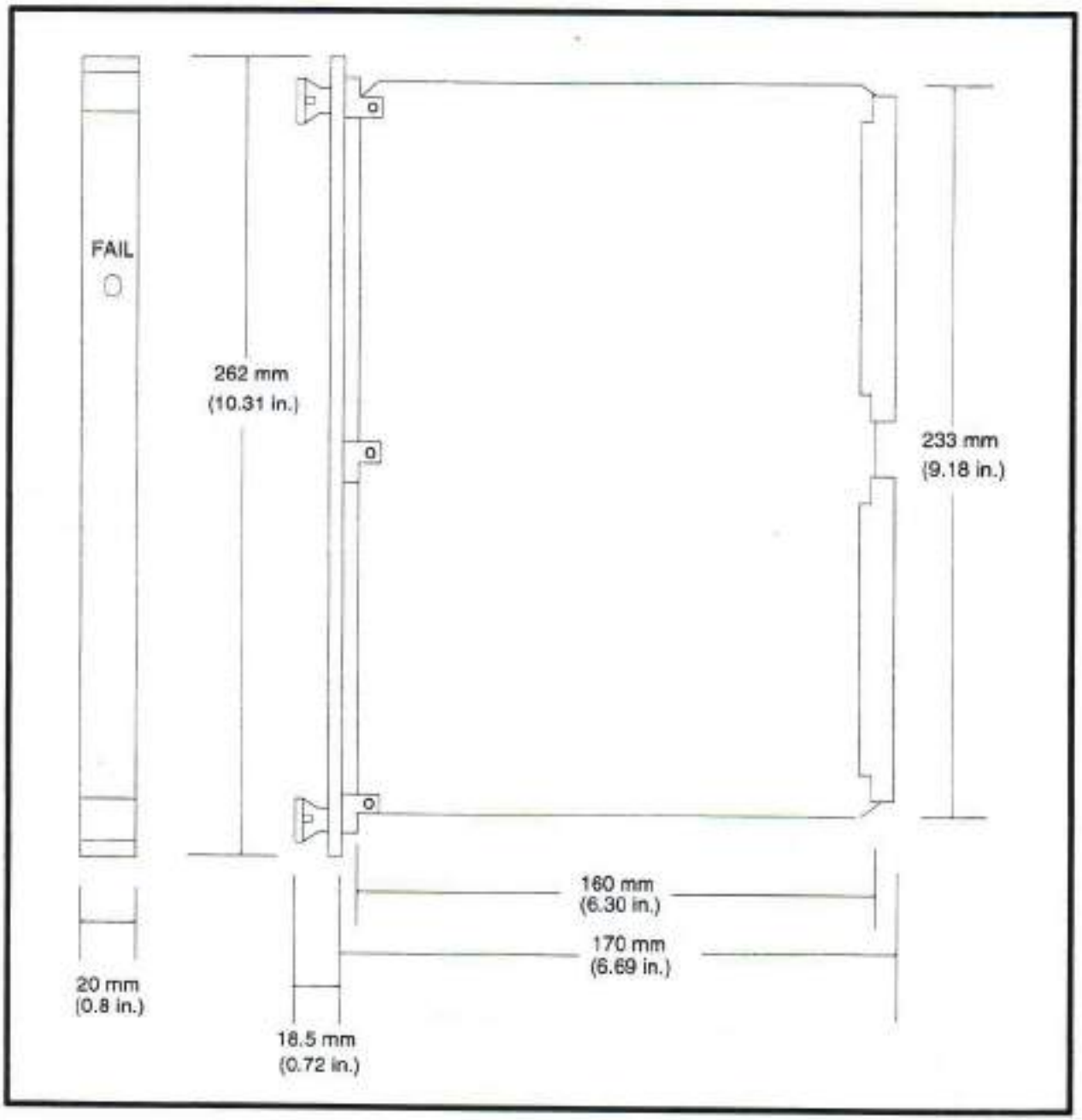


Figure 1-2: Dimensions of the SVME-667 A/D, D/A Converter Card

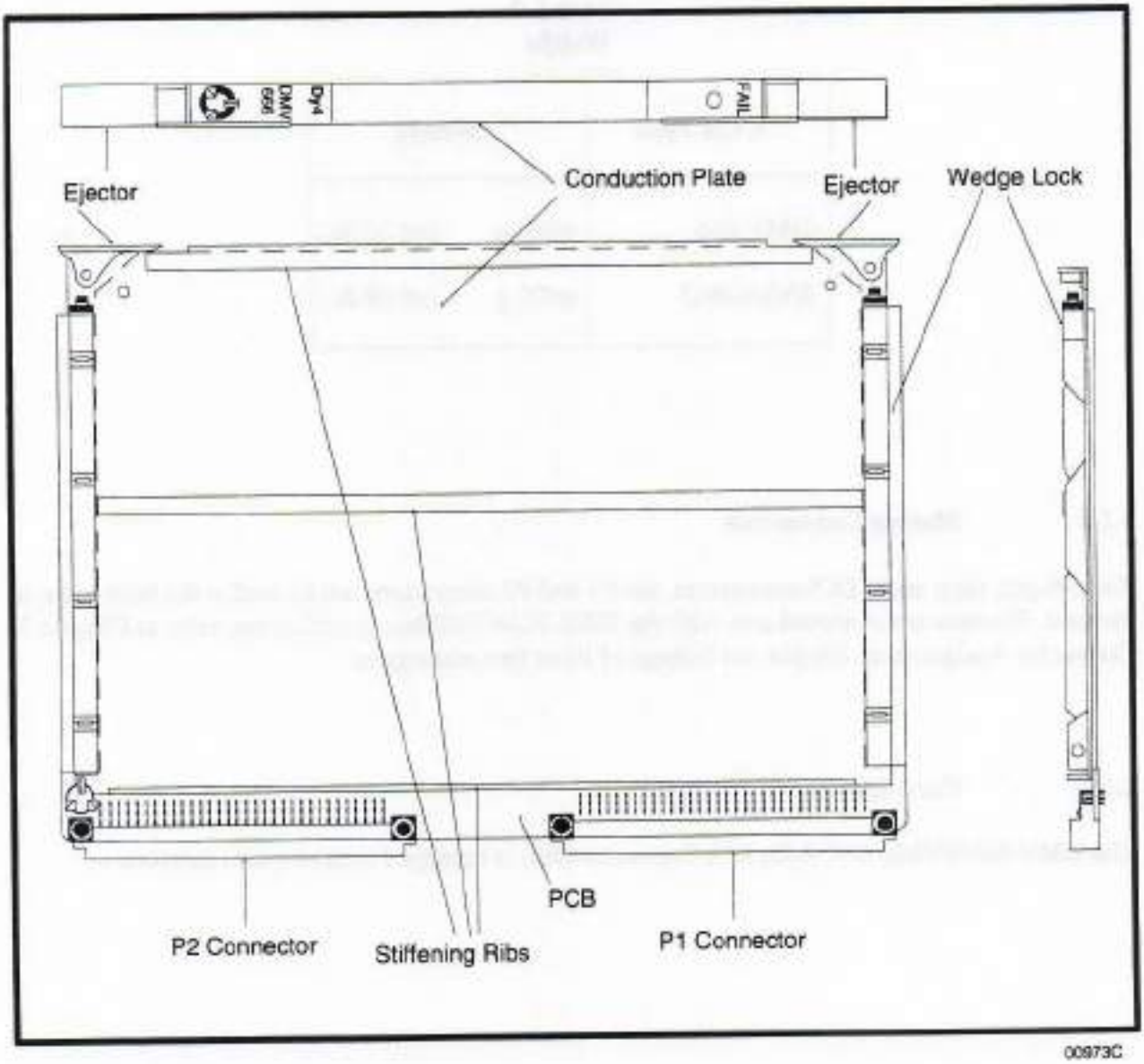


Figure 1-3: DMV-666 A/D, D/A Converter Card Conduction Cooling Plate

1.1.3 Weight

Table 1-2, Weight, tabulates the weight of the DMV-666 A/D, D/A Converter Card and the SVME-667 A/D, D/A Converter Card.

Table 1-2
Weight

CCA Type	Weight
DMV-666	<600 g (<1.32 lb.)
SVME-667	<400 g (<0.88 lb.)

1.1.4 Mating Connectors

Two 96-pin, right angle DIN connectors, the P1 and P2 connectors, are located at the back edge of the card. Pin-outs are in accordance with the IEEE 1014 VMEbus specification; refer to Chapter 5, Connector Assignments, for pin-out listings of these two connectors.

1.1.5 Card Ejectors

The DMV-666/SVME-667 A/D, D/A Converter Card is equipped with two card ejectors.

1.2 Environmental Specifications

Table 1-3, Environmental Specifications, lists the environmental conditions which the DMV-666/SVME-667 A/D, D/A Converter Card can withstand.

Table 1-3
Environmental Specifications

Environmental Conditions	SVME-667-0xx	DMV-666-3xx
Temperature: Operating Storage (64 hours) (2 years)	0°C to 50°C (air temperature) -55°C to 125°C -40°C to 100°C	-55°C to 85°C [1.] (cold wall temperature) -65°C to 125°C
Humidity:	0 to 95% non-condensing	0 to 95% non-condensing
Altitude:	sea level to 5,000 m	sea level to 21,350 m
Vibration: Sine Random	5 g/5 to 2,000 Hz 0.1 g^2/Hz 15 to 2,000 Hz	10 g/5 to 2,000 Hz 0.1 g^2/15 to 2,000 Hz
Shock:	4 g/11 ms half sine	30 g/11 ms half sine

Note: 1. As a general design objective, the junction temperature of all components on the DMV-666 A/D, D/A Converter Card is limited to 110°C maximum (when the chassis cold-wall temperature at circuit card interface is 85°C). When reliability or performance factors permit, a component's junction temperature may be allowed to marginally exceed 110°C.

1.3 Power Requirements

The power requirements for the DMV-666/SVME-667 A/D, D/A Converter Card are listed in Table 1-4, Power Requirements.

Table 1-4
Power Requirements

Voltage	SVME-667-006 Typical / Maximum Current (Amps)	DMV-666-306 Typical / Maximum Current (Amps)
+5.0 V	0.8/1.0	0.8/1.0
+12.0 V	0.15/0.25	0.15/0.25
-12.0 V	0.15/0.25	0.15/0.25

1.4 Performance

This section contains the performance specifications for various features of the DMV-666/SVME-667 A/D, D/A Converter Card.

1.4.1 VMEbus Interface

1.4.1.1 Bus Access Time

The DMV-666/SVME-667 A/D, D/A Converter Card access time (defined as DSA* to DTACK* at card edge) is a maximum of 500 ns for register accesses.

1.4.1.2 Interrupt Propagation Time

The IACK daisy-chain through the DMV-666/SVME-667 A/D, D/A Converter Card, IACKIN* TO IACKOUT*, is a maximum of 250 ns.

1.5 Analog Specifications

Table 1-5
Analog Specifications

Electrical Specifications Input Impedance	±32 V Input ±8 V Input ±16 mA Input	6 kΩ (see Note) 1 MΩ 500 Ω
Input Filter	±32 V Input ±8 V Input ±16 mA Input	10 kHz 3 dB point (nominal) 3 kHz 3 dB point 3 kHz 3 dB point
Conversion/Settling Time (Non-Interleaved)	27 µs	
Conversion/Settling Time (Interleaved)	20 µs	
Offset and Drift	1 LSB ≡ 2.19 mV (can be user-nulled)	
Output Swing	±8 V @ 20 mA ±10 V @ 5 mA for ±12 V supplies ≥ ±12 V	

Note: A version of the DMV-666/SVME-667 A/D, D/A Converter Card is also available with a ±40 V/±10 V input range. Consult the factory for details.

Table 1-5 contains the analog specifications for the DMV-666/SVME-667 A/D, D/A Converter Card.

2. FUNCTIONAL DESCRIPTION

This chapter provides a functional description of the hardware features on the DMV-666/SVME-667 A/D, D/A Converter Card and contains the following sections:

- features
- VMEbus slave interface
- Analog Input Characteristics
- Analog to Digital Converter Module
- Digital to Analog Converter Module
- Interrupts
- BI-mode®.

2.1 Features

- VMEbus A16, D16, and D08 (EO) slave interface
- 12-bit Analog to Digital conversion
- 12-bit Digital to Analog conversion
- 8 differential inputs configurable to 16 single-ended analog inputs
- ±36 V, ±8 V, and ±16 mA input ranges
- programmable gain
- 10 µs acquisition time
- 13 µs conversion time
- input channel reference/comparison circuitry
- 8 single-ended channels of D/A conversion
- analog inputs and outputs via P2 connector
- SVME-667 Analog to Digital Converter Card available in commercial grade version
- DMV-666 Analog to Digital Converter Card uses MIL-STD-883C class B-qualified components and is conduction-cooled for MIL-E-4158, MIL-E-5400, and MIL-E-16400 environments
- P2 connector configurable VMEbus base address
- location monitor
- BI-mode®.

Refer to Figure 2-1, DMV-666/SVME-667 A/D, D/A Converter Card Block Diagram, for an illustration of the relationships between the functional blocks.

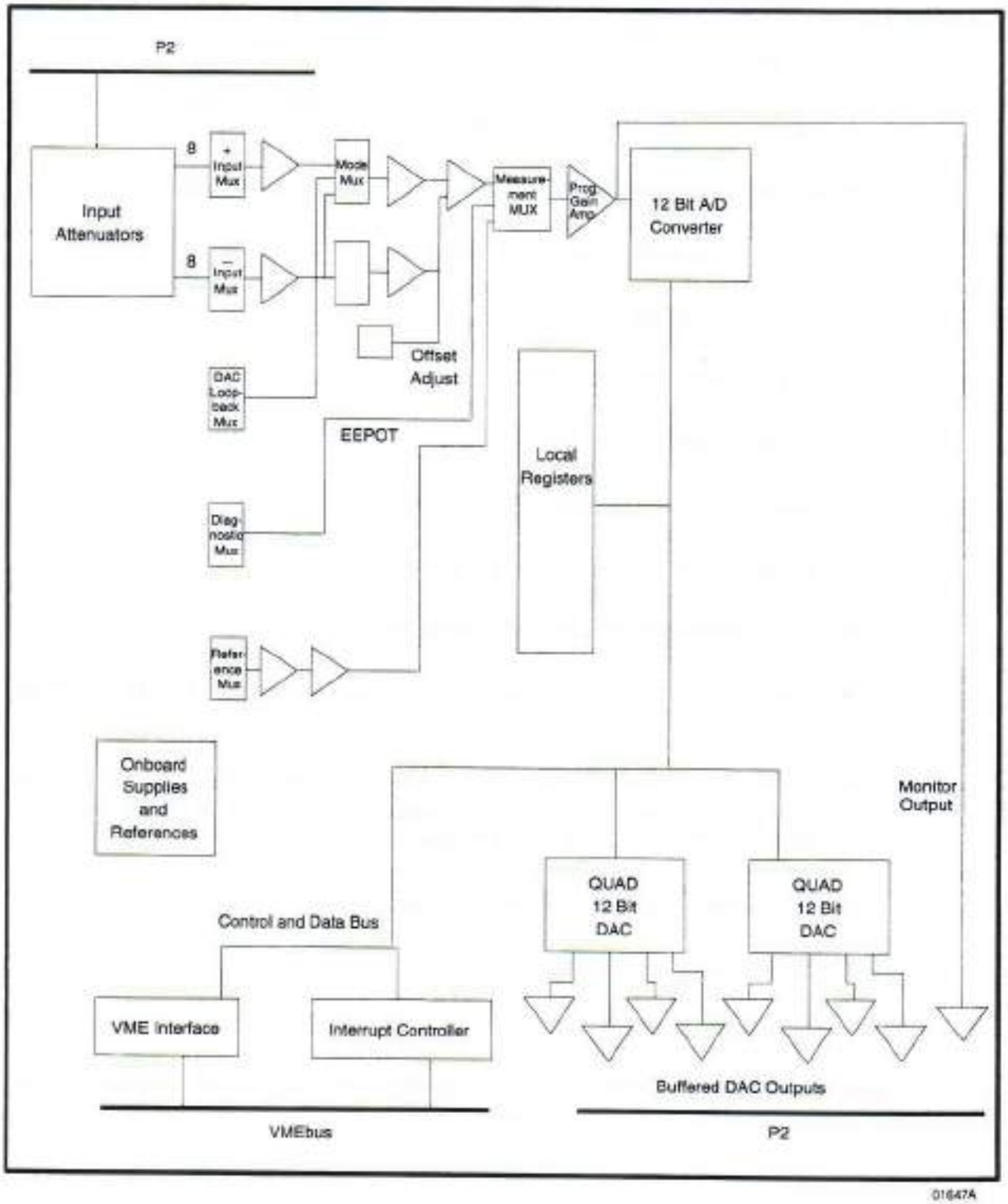


Figure 2-1: DMV-666/SVME-667 A/D, D/A Converter Card Block Diagram

2.2 VMEbus Slave Interface

The DMV-666/SVME-667 A/D, D/A Converter Card provides a VMEbus slave interface to the local bus with D16 and D08 (EO) data transfer capability.

The DMV-666/SVME-667 A/D, D/A Converter Card responds to A16 address accesses.

2.2.1 Decoding (A16 Base Address Selection)

The VMEbus A16 base address is established by the five P2 ID code bits. The system designer defines these bits by a 5-bit strapping option. The ID lines default 'high' providing an ID code of 1F (base address of F800). The A16 address space ranges from 0000 to F800 (refer to Table 2-1, VMEbus Memory Map). Refer to Table 3-1, E Assigments, in Chapter 3, for strapping information.

Address modifier lines (AM0-AM5) are monitored for valid Address Modifier (AM) codes. The board responds only to AM code 2D (short supervisory access) for A16 address space write accesses and to AM code 29 (short non-privileged access) for read accesses. Refer to Table 2-2, Address Modifier Codes for A16 Base Address.

2.2.2 VMEbus Interface Requirements

The DMV-666/SVME-667 A/D, D/A Converter Card system bus interface is compatible with the VMEbus standard as defined in IEEE 1014, except where noted. The subsequent paragraphs describe the characteristics of the bus interface.

2.2.2.1 Address Width

The control registers and location monitor respond to A16 access cycles.

2.2.2.2 Read/Write Cycle Detection

The DMV-666/SVME-667 A/D, D/A Converter Card does not respond to 32-bit data transfer cycles. Single-byte read or write accesses are valid to the control registers and location monitor. Word read and write accesses are required to access the A/D and D/A Converters.

Table 2-1
VMEbus Memory Map

ID Code	Base Address
00	0000
01	0800
02	1000
03	1800
04	2000
05	2800
06	3000
07	3800
08	4000
09	4800
0A	5000
0B	5800
0C	6000
0D	6800
0E	7000
0F	7800
10	8000
11	8800
12	9000
13	9800
14	A000
15	A800
16	B000
17	B800
18	C000
19	C800
1A	D000
1B	D800
1C	E000
1D	E800
1E	F000
1F	F800

Table 2-2
AM Modifier Codes for A16 Base Address

AM Code	Access
29	Short, non-privileged access
2D	Short, supervisory access

2.2.3 Data Transfer Bus

All signals of the data transfer bus are used in accordance with the VMEbus specification for a slave interface.

2.2.4 Arbitration Bus

The DMV-666/SVME-667 A/D, D/A Converter Card provides bus grant continuity by passing all Bus Grant In signals (BGxIN*) to the Bus Grant Out signals (BGxOUT*) in the occupied slot. Specifically, the bus grant lines are connected as follows:

- BG0IN* to BG0OUT*
- BG1IN* to BG1OUT*
- BG2IN* to BG2OUT*
- BG3IN* to BG3OUT*.

2.2.5 Utilities Bus

2.2.5.1 System Reset

The DMV-666/SVME-667 A/D, D/A Converter Card monitors the SYSRESET* signal from the VMEbus. Assertion of the SYSRESET* signal places the CCA into BI-mode® and resets the following:

- General Purpose Control Register
- Gain/Multiplexer Control Register
- A/D Control Register
- A/D Converter
- Vector Register
- IACK Sequencer PAL®.

2.2.5.2 System Fail

The VMEbus SYSFAIL* line is asserted by the DMV-666/SVME-667 A/D, D/A Converter Card when the on-board General Purpose Control Register FAIL bit is asserted.

The VMEbus signal SYSFAIL* is asserted on power-up until it is explicitly cleared.

2.3 Analog Input Characteristics

2.3.1 Analog Input Ranges and Protection

Each analog input has the following jumper-selectable input ranges and input impedance:

- ± 32 V, 6 kΩ
- ± 8 V, 1 MΩ
- ± 16 mA, 500 Ω.

Protection for each analog input enables them to withstand 70 volts peak with respect to the system ground.

Refer to Section 4.9.1, Analog to Digital Scaling, for more information on voltage ranges and A/D results.

2.3.2 Input Multiplexer

The Input Multiplexer consists of two 8 to 1 Analog Multiplexers. Any one of the 16 inputs may be selected for single-ended operation or in matched pairs for differential operation. Selection is controlled under software by a write access to the Gain/Multiplexer Control Register.

2.3.3 Reference Multiplexer

The Reference Multiplexer is an 8 to 1 multiplexer used for test and calibration purposes. It can select the input channel selected by the Input Multiplexer, or it can select one of the following inputs:

- analog calibration reference voltage
- zero reference
- +5 VDC digital supply rail monitor
- +12 VDC analog supply rail monitor
- -12 VDC analog supply rail monitor
- -5 VDC analog supply rail monitor

- ambient temperature sensor.

2.3.4 Diagnostic Multiplexer

The Diagnostic Multiplexer consists of an 8 to 1 Analog Multiplexer and is used for card testing. It is selected by a write access to the Mode Control Register. Refer to Chapter 6, Programming Interface, for programming details.

The Diagnostic Multiplexer allows access to the following signals:

- zero reference
- +4.5 V reference
- -4.5 V reference
- differential amplifier
- offset trim voltage
- +5 V analog supply monitor
- DAC 0 loopback
- DAC 4 loopback.

2.3.5 Shadow Multiplexer

The Shadow Multiplexer is a voltage divider that may be placed on the measured signal which reduces the level to 0.64 of the original level. It is used to support testing of the Analog Multiplexer inputs.

2.3.6 DAC Loopback Multiplexer

The DAC Loopback Multiplexer is an 8 to 1 Analog Multiplexer that allows access to the digital to analog converter outputs. Access to the multiplexer is achieved by software control of the Mode Control Register.

2.3.7 Input Filter

Each input has a single pole RC filter. For the ±8 V and the ±16 mA input ranges, the 3 dB point is tuned to 3 kHz (nominal). For the ±32 V input range, the 3 dB point is tuned to 10 kHz (nominal).

2.3.8 Gain Control

The DMV-666/SVME-667 A/D, D/A Converter Card is equipped with a programmable gain control (the Programmable Gain Amplifier). Gain levels of 1, 2, 4, and 8 are available by writing to the Gain/Multiplexer Control Register (refer to Chapter 6, Programming Interface).

2.4 Analog to Digital Converter Module

The Analog to Digital Converter (A/D Converter) is a 12-bit, self-calibrating device for converting analog signals to digital signals (CS5012A - Crystal Semiconductor Corporation).

The A/D Converter control inputs are software-controlled via the A/D Control Register.

A reset of the A/D Converter is dependent upon one of the following:

- reset via the A/D Control Register
- assertion of the VMEbus SYSRESET* signal.

Either 8- or 16-bit data output is selected from the A/D Converter (dependent upon the A/D Bus Width setting in the A/D Control Register).

The A/D Converter can operate in bipolar mode (positive or negative input with respect to ground) or unipolar mode (positive input only). In bipolar mode, the Most Significant Bit (MSB) is the sign bit. The selection of either bipolar or unipolar mode is made via software control by accessing the A/D Control Register.

2.5 Digital to Analog Converter Module

The DMV-666/SVME-667 A/D, D/A Converter Card offers 8 voltage-output digital to analog converter channels. Each channel is independently programmable, has a maximum resolution of 12 bits, and an output voltage range of ±8 V at 20 mA with VME supplies at +11.64 and -11.64. The range performance increases to ±9.25 at 10 mA with the same VME supplies. The output range of ±10 V can be achieved with 5 mA loads at VME supply voltages at +12.0 V and -12.0 V. (Refer to Section 4.12, Digital to Analog Converter, for more information on scaling.) Other features consist of the following:

- readback capability to allow for verification of the contents of the internal data register
- asynchronous reset to zero on the D/A outputs
- monotonic performance
- maximum linearity error of the LSB.

Each D/A channel is accessible by a VMEbus master with the outputs available at the P2 I/O connector.

2.6 Interrupts

The DMV-666/SVME-667 A/D, D/A Converter Card can generate an interrupt upon the completion of the A/D digitization cycle, or upon the completion of the track cycle. The type of interrupts are 'release on register' access.

2.6.1 Interrupt Monitor

The Interrupt Monitor is a function of the IACK Sequencer. It examines the A/D interrupt and interrupt mask lines, and asserts a VMEbus interrupt when the corresponding interrupt and interrupt mask lines are in the correct states. Under software control, any one of the seven VMEbus interrupt levels can be used. The status ID byte in the Vector Register is also software programmable.

2.6.2 IACK Sequencer

The IACK Sequencer performs the following functions:

- detects and samples a VMEbus IACK cycle
- monitors the DMV-666/SVME-667 A/D, D/A Converter Card's interrupt lines, masks bits, and the priority level
- enables the status ID byte onto the VMEbus
- enables DTACK* generation
- issues a signal to the IACKOUT driver for off-board IACK cycles
- generates a VMEbus interrupt when an A/D interrupt occurs.

2.6.3 Interrupt Acknowledge Cycles

The DMV-666/SVME-667 A/D, D/A Converter Card responds to an interrupt acknowledge cycle when the following conditions are true:

- an IACK cycle is detected
- the IACKIN* daisy-chained signal is detected
- the encoded interrupt level on A1 - A3 is the same as the DMV-666/SVME-667 A/D, D/A Converter Card's interrupt level
- the A/D device is asserting an interrupt
- the corresponding interrupt mask bit is a logic 0.

When these conditions are true, the DMV-666/SVME-667 A/D, D/A Converter Card enables its status ID byte onto the VMEbus data bus and provides a data transfer acknowledge (DTACK*).

2.7 BI-mode®

Bus Isolation Mode (BI-mode®) is a Built-In Test (BIT) facility that enables the DMV-666/SVME-667 A/D, D/A Converter Card to be isolated from the VMEbus. This means that a hardware failure on the board may not disrupt the VMEbus as VMEbus mastership signals are not driven and all daisy-chained signals are passed unaffected.

Table 2-3, BI-mode® Connector Usage, shows the configuration of VMEbus signals during BI-mode®.

2.7.1 Entry into BI-mode®

The DMV-666/SVME-667 A/D, D/A Converter Card enters BI-mode® under any of the following conditions:

- upon assertion of the VMEbus SYSRESET* line
- upon assertion of the VMEbus IRQ1* signal (if strapped)
- upon access by a VMEbus master which asserts BI-mode® via a read access to the BI-mode® entry/exit location monitor.

The DMV-666/SVME-667 A/D, D/A Converter Card contains E1 and E2 to disable IRQ1* assertion from causing entry into BI-mode®. Refer to Chapter 3, E Assignments and Functions, for more information.

2.7.2 Exit from BI-mode®

The DMV-666/SVME-667 A/D, D/A Converter Card is removed from BI-mode® upon access by a VMEbus master. This master signal deasserts BI-mode® via a write access to the BI-mode® entry/exit location monitor as long as IRQ1* is not asserted.

While the DMV-666/SVME-667 A/D, D/A Converter Card is in BI-mode®, any access by a VMEbus master other than to the BI-mode® exit location is ignored. In this case, the system controller bus time-out function generates a bus error to terminate the cycle.

2.7.3 Location Monitor

The BI-mode® entry/exit location monitor is available to the VMEbus in the A16 address space. The DMV-666/SVME-667 A/D, D/A Converter Card enters BI-mode® for any read access to the location monitor and exits BI-mode® for any write access.

Table 2-3
BI-mode® Connector Usage

Signal Name	Normal Usage	BI-mode® Usage
VMEbus General Signals		
D00 - D15	bi-directional data	tri-state
D16 - D31	not used	not used
A01 - A15	addresses, input	input
A16 - A31	not used	not used
AM0 - AM5	input	input
AS*, DS0*, DS1*	strobes, input	input
WRITE*	write, input	input
DTACK*	acknowledge, output	disabled
IACK*	input	input
IRQ1* - IRQ7*	interrupt output requests	disabled
BR0* - BR3*	NA	NA
ACFAIL*	NA	NA
SYSFAIL*	FAIL	FAIL
BBSY*	NA	NA
BCLR*	NA	NA
LWORD*	input	input
SERCLK, SERDAT	NA	NA
System Controller Signals		
SYSCLK	input	input
BERR*	NA	NA
SYSRESET*	input	input
Daisy Chain Signals		
IACKIN*	1014 usage	unaffected
IACKOUT*	1014 usage	unaffected
BGxIN*	1014 usage	unaffected
BGxOUT*	1014 usage	unaffected

3. E ASSIGNMENTS AND FUNCTIONS

This chapter describes the E (jumper block) assignments and functions. Figure 3-1, E Locations, shows the E designations for the DMV-666/SVME-667 A/D, D/A Converter Card. Table 3-1, E Assignments, lists the on-board E numbers and their functions.

Table 3-1
E Assignments

Function	Jumper Block	Reference
Analog Input Selection	E3 to E66	Channel Configuration Tables 4-2 to 4-9 in Chapter 4
Entry into/Exit from BI-mode® via IRQ1*	E1, E2	Table 3-3

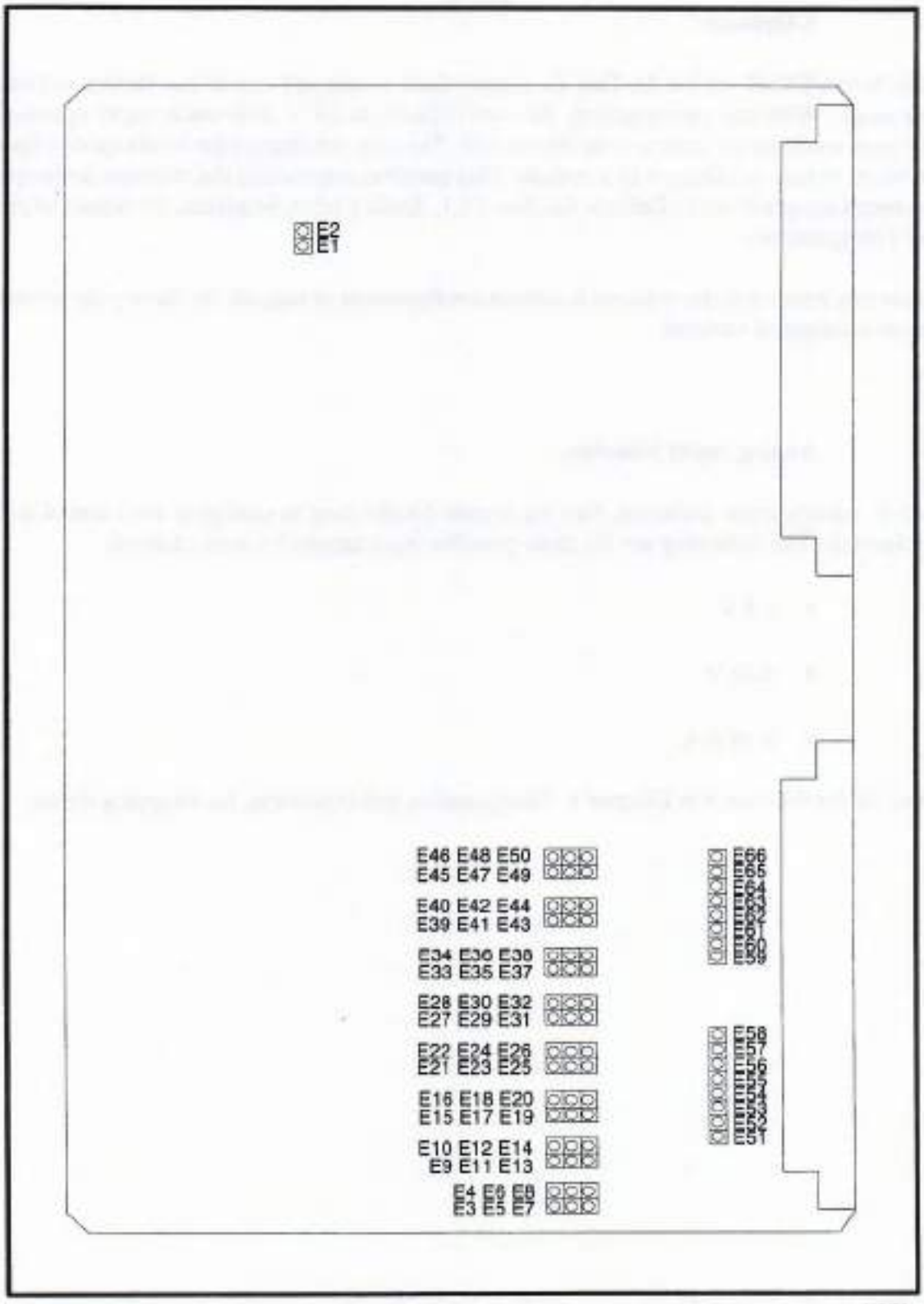


Figure 3-1: E Locations

3.1 E Options

The DMV-666/SVME-667 A/D, D/A Converter Card is shipped out of the factory without any jumper straps. With this configuration, the card defaults to ±8 V differential input operation and IRQ1* does not force the card to enter BI-mode®. The user can change the hardware configuration of the board before installing it in a system. This involves connecting the appropriate jumpers on the on-board jumper blocks . Refer to Section 3.1.1, Analog Input Selection, for details of possible jumper configurations.

The user can wire-wrap the required hardware configuration or consult the factory for information about pre-configured variants.

3.1.1 Analog Input Selection

Table 3-2, Analog Input Selection, lists the jumper blocks used to configure each one of the eight input channels. The following are the three possible input ranges for each channel:

- ±8 V
- ±32 V
- ±16 mA.

Refer to Tables 4-2 to 4-9 in Chapter 4, Configuration and Operation, for strapping details.

Table 3-2
Analog Input Selection

Channel Number	E Assignments
0	E45 to E50 E65, E66
1	E39 to E44 E63, E64
2	E33 to E38 E61, E62
3	E27 to E32 E59, E60
4	E21 to E26 E57, E58
5	E15 to E20 E55, E56
6	E9 to E14 E53, E54
7	E3 to E8 E51, E52

Note: Strapping one input of a differential pair for single-ended operation forces the other input of the differential pair into single-ended operation.

3.1.2 Entry Into/Exit From BI-mode® Via IRQ1*

In some systems, it is undesirable to allow an assertion of IRQ1* to cause the DMV-666/SVME-667 A/D, D/A Converter Card to enter BI-mode®. This feature may be enabled or disabled by configuring E1 and E2.

Table 3-3, Entry into BI-mode® Via IRQ1*, summarizes the strapping options.

Table 3-3
Entry into BI-mode® Via IRQ1*

Entry into BI-mode® via IRQ1*	Configuration
enabled	E1 to E2 strapped
disabled	E1 to E2 open

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4. CONFIGURATION AND OPERATION

This chapter outlines the configuration and operation of the DMV-666/SVME-667 A/D, D/A Converter Card. It contains the information required to operate the CCA and is divided as follows:

- ID Code Configuration
- Front-End Configuration
- Input Multiplexer
- DAC Loopback Multiplexer
- Shadow Multiplexer
- Reference Multiplexer
- Diagnostic Multiplexer
- Programmable Gain Amplifier
- Analog to Digital Converter
- Analog to Digital Converter Calibration
- Electronic Potentiometer
- Digital to Analog Converter
- Temperature Sensor
- Interrupts.

4.1 ID Code Configuration

The ID code selects the base address for address map programming on a bus slot basis. On the SVME-667 A/D, D/A Converter Card, the ID codes are configured by strapping the P2 connector. On the DMV-666 A/D, D/A Converter Card, the ID codes are available on the P2 connector only.

Table 4-1, P2 ID Code Configuration, details the configuration of the P2 connector for the different ID codes and their base addresses. Note that the ID codes and the base addresses are in hexadecimal format.

Table 4-1
P2 ID Code Configuration

ID Code	Address	P2-ID4 P2-C3	P2-ID3 P2-A3	P2-ID2 P2-C2	P2-ID1 P2-A2	P2-ID0 P2-C1
00	0000	GND	GND	GND	GND	GND
01	0800	GND	GND	GND	GND	open
02	1000	GND	GND	GND	open	GND
03	1800	GND	GND	GND	open	open
04	2000	GND	GND	open	GND	GND
05	2800	GND	GND	open	GND	open
06	3000	GND	GND	open	open	GND
07	3800	GND	GND	open	open	open
08	4000	GND	open	GND	GND	GND
09	4800	GND	open	GND	GND	open
0A	5000	GND	open	GND	open	GND
0B	5800	GND	open	GND	open	open
0C	6000	GND	open	open	GND	GND
0D	6800	GND	open	open	GND	open

Table 4-1 (Continued)
P2 ID Code Configuration

ID Code	Address	P2-ID4 P2-C3	P2-ID3 P2-A3	P2-ID2 P2-C2	P2-ID1 P2-A2	P2-ID0 P2-C1
0E	7000	GND	open	open	open	GND
0F	7800	GND	open	open	open	open
10	8000	open	GND	GND	GND	GND
11	8800	open	GND	GND	GND	open
12	9000	open	GND	GND	open	GND
13	9800	open	GND	GND	open	open
14	A000	open	GND	open	GND	GND
15	A800	open	GND	open	GND	open
16	B000	open	GND	open	open	GND
17	B800	open	GND	open	open	open
18	C000	open	open	GND	GND	GND
19	C800	open	open	GND	GND	open
1A	D000	open	open	GND	open	GND
1B	D800	open	open	GND	open	open
1C	E000	open	open	open	GND	GND
1D	E800	open	open	open	GND	open
1E	F000	open	open	open	open	GND
1F	F800	open	open	open	open	open

4.2 Front-End Configuration

4.2.1 Input Attenuation

For each of the eight input channels, there is a resistor network which selects an input range. The user can implement any one of the input ranges by configuring the jumper blocks. The following are the input ranges:

- ± 8 V 3 kHz 3 dB point
- ± 32 V 10 kHz 3 dB point
- ± 16 mA 3 kHz 3 dB point.

The selection and conversion rate of inputs is governed by the following factors:

- 3 kHz input filter bandwidth (333 µs)
- transient settling time of the amplifier chain (20 µs)
- acquisition and conversion speed of the A/D converter
  - 3.75 µs acquisition
  - 12.25 µs conversion

The selection rate of inputs is governed by the VMEbus traffic.

The following are the conversion rate limitations:

- a combination of the input bandwidth for inputs with dynamic signals
- the transient settling time for inputs scanned which have a large potential difference from the input previously selected.

For more information on sequencing and converting inputs, see Section 4.9, Analog to Digital Converter.

4.2.2 Channel Configuration

The Analog Multiplexers default on power-up in differential mode. A combination of strapping and software is required to configure an input for single-ended operation. For information on the software interface, see Section 4.3, Input Multiplexer. Each input must be strapped for the desired configuration for converted results to be accurate. Differential operation provides the following input options:

- ±8 V
- ±32 V
- ±16 mA.

Figure 4-1, Channel Configuration, augments the following discussion on channel configuration. The ±8 V differential operation requires that no straps be installed on the configuration pins for that channel.

The ±32 V differential operation requires that the two voltage divider resistors R2 and R3 be configured into the input circuit with straps across E3-E4 and E5-E6 only.

The ±16 mA input range requires that only the 500 Ω current loop resistor R5 be configured into the input circuit by strapping E1-E2 only.

Single-ended operation provides for two input ranges and configures each differential channel used to two single-ended channels. Programming of the Mode Control Register as well as the Gain/Multiplexer Control Register is required. For information on strapping configurations, see Figure 3-1, E Locations, in Chapter 3, and Tables 4-2 through 4-9 for Input Channel Configurations. Single-ended operation provides the following input options:

- ±8 V
- ±32 V.

Single-ended operation requires that the input filter be grounded. In Figure 4-1, Channel Configuration, this corresponds to strapping E8-E7. The differential input channel then becomes two single-ended channels referenced to the circuit ground.

Operation in the ±8 V range requires that no other strap be installed on that input.

Operation in the ±32 V range requires that the voltage divider resistor (R2 for the input+ input and R3 for the input- input) be configured into the circuit by shunting the corresponding jumpers E3-E4 or E5-E6. The versatility of the input circuit allows a differential input filter to be configured into two single-ended inputs of different voltage ranges. (Refer to Figure 4-1, Channel Configuration, for more information.)

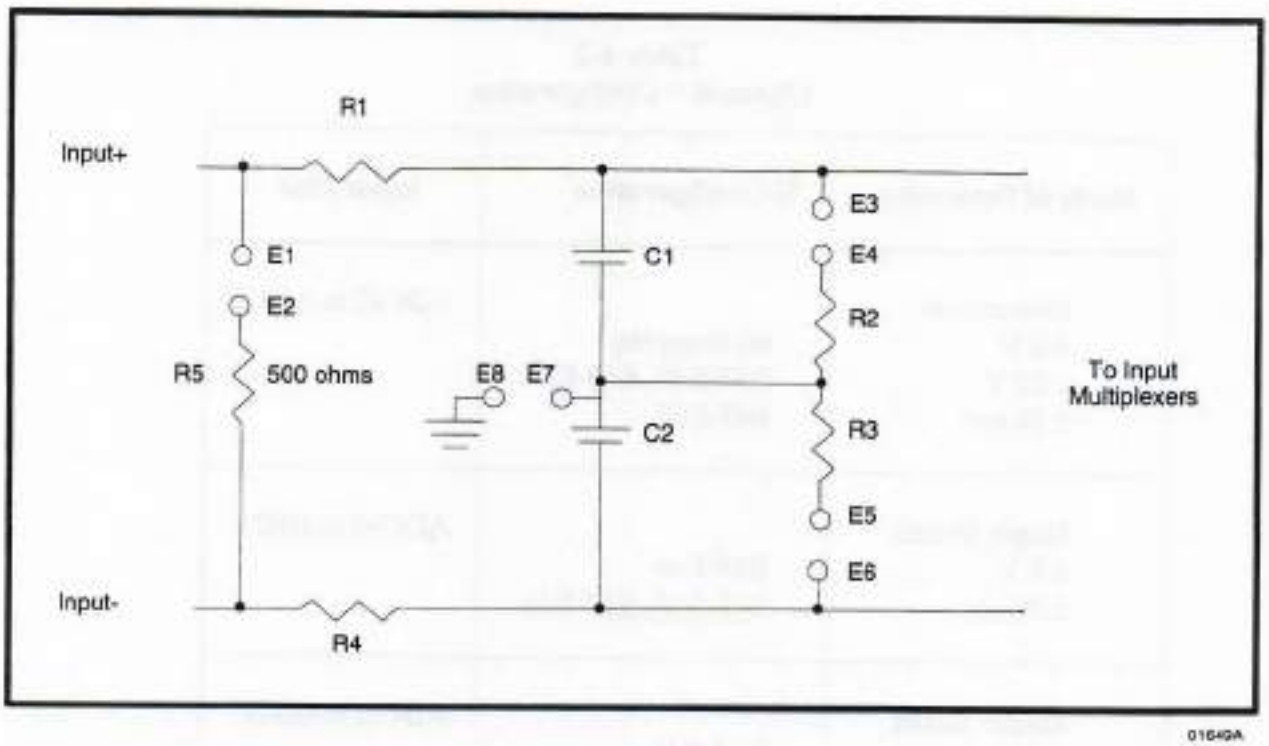


Figure 4-1: Channel Configuration

Reference designations are only applicable to this example. For actual E block numbers, refer to Figure 3-1, E Locations, in Chapter 3.

Tables 4-2 to 4-9 detail the specific E strappings for the configurations for each channel.

Table 4-2
Channel 0 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ±8 V ±32 V ±16 mA	no strapping E47-E48, E49-E50 E65-E66	ADC+0 to ADC-0
Single-Ended ±8 V ±32 V	E45-E46 E45-E46, E47-E48	ADC+0 to GND
Single-Ended ±8 V ±32 V	E45-E46 E45-E46, E49-E50	ADC-0 to GND

Table 4-3
Channel 1 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	no strapping E41-E42, E43-E44 E63-E64	ADC+1 to ADC-1
Single-Ended ± 8 V ± 32 V	E39-E40 E39-E40, E41-E42	ADC+1 to GND
Single-Ended ± 8 V ± 32 V	E39-E40 E39-E40, E43-E44	ADC-1 to GND

Table 4-4
Channel 2 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	no strapping E35-E36, E37-E38 E61-E62	ADC+2 to ADC-2
Single-Ended ± 8 V ± 32 V	E33-E34 E33-E34, E35-E36	ADC+2 to GND
Single-Ended ± 8 V ± 32 V	E33-E34 E33-E34, E37-E38	ADC-2 to GND

Table 4-5
Channel 3 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	no strapping E29-E30, E31-E32 E59-E60	ADC+3 to ADC-3
Single-Ended ± 8 V ± 32 V	E27-E28 E27-E28, E29-E30	ADC+3 to GND
Single-Endede ± 8 V ± 32 V	E27-E28 E27-E28, E31-E32	ADC-3 to GND

Table 4-6
Channel 4 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	no strapping E23-E24, E25-E26 E57-E58	ADC+4 to ADC-4
Single-Ended ± 8 V ± 32 V	E21-E22 E21-E22, E23-E24	ADC+4 to GND
Single-Ended ± 8 V ± 32 V	E21-E22 E21-E22, E25-E26	ADC-4 to GND

Table 4-7
Channel 5 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	 no strapping E17-E18, E19-E20 E55-E56	ADC+5 to ADC-5
Single-Ended ± 8 V ± 32 V	 E15-E16 E15-E16, E17-E18	ADC+5 to GND
Single-Ended ± 8 V ± 32 V	 E15-E16 E15-E16, E19-E20	ADC-5 to GND

Table 4-8
Channel 6 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	 no strapping E11-E12, E13-E14 E53-E54	ADC+6 to ADC-6
Single-Ended ± 8 V ± 32 V	 E9-E10 E9-E10, E11-E12	ADC+6 to GND
Single-Ended ± 8 V ± 32 V	 E9-E10 E9-E10, E13-E14	ADC-6 to GND

Table 4-9
Channel 7 Configuration

Mode of Operation	E Configuration	Input Pins
Differential ± 8 V ± 32 V ± 16 mA	 no strapping E5-E6, E7-E8 E51-E52	ADC+7 to ADC-7
Single-Ended ± 8 V ± 32 V	 E3-E4 E3-E4, E5-E6	ADC+7 to GND
Single-Ended ± 8 V ± 32 V	 E3-E4 E3-E4, E7-E8	ADC-7 to GND

4.3 Input Multiplexer

The Input Multiplexer stage consists of two 8 to 1 Analog Multiplexers. Input Multiplexer A is used to scan the positive inputs of the differential pairs and Input Multiplexer B is used to scan the negative inputs of the differential pairs. Each multiplexer output is buffered by a high impedance follower which feeds the Mode Multiplexer. The Input Multiplexers are both addressed with the Gain/Multiplexer Control Register bits SEL1, SEL2, and SEL3.

Configuration of the input filters as differential mode requires the Mode Control Register to be programmed to access the channels configured as differential. Configuration of the input filters as single-ended requires the Mode Control Register to be programmed to access the positive input only, or the negative input only.

4.4 DAC Loopback Multiplexer

The DAC Loopback Multiplexer is an 8 to 1 Analog Multiplexer allowing access to the Digital to Analog Converter outputs. Access to the multiplexer is achieved by software control of the Mode Control Register.

DAC values measured by the A/D Converter can be predicted as follows:

Assume that the A/D Converter is functioning in bipolar mode.

For a value greater than 800_H written to the DAC,

$$\text{ADC RESULT}_H = 800_H - ((((\text{DAC VALUE}_{10} \times 0.00219) - 4.5) \times 0.45)/0.00219)_H$$

Expected tolerance (assuming offsets were nulled before starting):

±2 LSB ±DAC gain error (±5 LSB worst case), where 1 LSB = 0.00219 volts

For a value less than 800_H written to the DAC,

$$\text{ADC RESULT}_H = 800_H + ((((\text{DAC VALUE}_{10} \times 0.00219) - 4.5) \times -0.45)/0.00219)_H$$

4.5 Shadow Multiplexer

The Shadow Multiplexer is a voltage divider that may be placed on the measured signal which reduces the level to 0.64 of the original level. This multiplexer works with the Input Multiplexer and can be enabled by the user through software control (bit 7 of the A /D Control Register. Refer to Chapter 6, Programming Interface). The Shadow Multiplexer's input channel selection is made through a bit configuration in the A/D Control Register.

Note: The Shadow Multiplexer is used for diagnostic purposes only; it cannot be used for calibration.

4.6 Reference Multiplexer

The Reference Multiplexer is an 8 to 1 multiplexer. Its input channels are defined in the following sections. Access to the Reference Multiplexer is via the Gain/ Multiplexer Control Register bits 3, 4, and 5, SEL 4, 5, and 6, respectively.

4.6.1 Input Channel 0

This input channel comes from the output of the Input Multiplexer. Selection is accomplished by choosing the required Input Multiplexer channel while maintaining SEL 4, 5, and 6 as zero.

4.6.2 Input Channel 1

This input channel measures the analog reference (A/D Converter reference). The value should read $FFF0_H$ +0/-2.

4.6.3 Input Channel 2

This input channel is the analog ground reference and may be used for card calibration. In bipolar mode, the A to D Converter result should be 8000_H. Refer to Section 4.10, A/D Converter Calibration, for details.

4.6.4 Input Channel 3

This input channel is used to monitor the VMEbus power supply. It is connected to +5 V through a voltage divider of 0.819. The expected range of values is 0550_H to $11A0_H$ in bipolar mode for the VME +5 V supply range of 5.25 V to 4.75 V.

4.6.5 Input Channel 4

This input channel is used to monitor the VMEbus +12 V power supply. It is connected to the +12 V through a voltage divider of 0.338. The expected range of values is $06B0_H$ to 1080_H in bipolar mode for the VME +12 V supply range of 12.6 V to 11.64 V.

4.6.6 Input Channel 5

This input channel is used to monitor the VMEbus -12 V power supply. It isconnected to the -12 V through a voltage divider of 0.338. The expected range of values is $F960_H$ to $EF80_H$ in bipolar mode for the VME -12 V supply range of -12.6 V to -11.64 V.

4.6.7 Input Channel 6

This input channel is used to monitor the on-card -5 V power supply. It is connected to -5 V through a voltage divider of 0.819. The expected range of values is $FAB0_H$ to $EE60_H$ in bipolar mode.

4.6.8 Input Channel 7

This input channel is connected to a temperature sensor. It can be used to shut down the system if the temperature exceeds the system temperature ratings. It is also used for card calibration. Refer to Section 4.13, Temperature Sensor, for details.

4.7 Diagnostic Multiplexer

The Diagnostic Multiplexer is accessed by asserting DMUXSEL, bit 2 of the Mode Control Register. Individual inputs are selected using bits 3, 4, and 5, SEL4, 5, and 6 of the Gain/Multiplexer Control Register.

4.7.1 Input Channel 0

This input is the analog ground reference and may be used for calibration purposes. In bipolar mode, the A/D Converter result should be 8000_H.

4.7.2 Input Channel 1

This input is the +4.500 volt reference. In either operating mode, the A/D Converter result should be $FFF0_H$, ($+0_H$, -20_H). This is a positive full scale reading.

4.7.3 Input Channel 2

This input is the -4.500 volt reference. In bipolar mode, the A/D Converter result should be 0000_H, ($+20_H$, -0_H). This is a negative full scale reading.

4.7.4 Input Channel 3

This is the output of the differential amplifier. Any result obtained from this input should be the same as that obtained from the Input Multiplexer.

4.7.5 Input Channel 4

This input is the voltage applied to the differential amplifier summing junction for the purpose of nulling the input buffer and differential amplifier offsets. This input can be used for determining that the Electronic Potentiometer is functional. It is used in production testing at the factory.

4.7.6 Input Channel 5

This input is the +5 V analog supply monitor. Its value is nominally F480 ($\pm 5_H$).

4.7.7 Input Channel 6

This input is the DAC0 output applied to the VDAC MUX. Since the value obtained here does not pass through the differential amplifier, it has a converted result of -1 times the DAC output. Therefore, assuming both the A/D Converter and DACs are in bipolar mode, a value of 0800_H programmed into DAC0 will result in a value of 8000_H from the A/D Converter. A value of $0FFF_H$ programmed into the DAC will result in a value of 0000_H. A value of 0000_H programmed into the DAC will result in a value of $FFF0_H$ from the A/D Converter.

4.7.8 Input Channel 7

This input is the DAC4 output applied to the VDAC MUX. It operates the same as Input Channel 6.

4.8 Programmable Gain Amplifier

Under software control , the Programmable Gain Amplifier can be adjusted for gains of 1, 2, 4, and 8. The gain setting is controlled by bits 6 and 7 in the Gain/Multiplexer Control Register.

The gain may be programmed at the same time that a multiplexer input selection is made. When a gain change is made, 10 µs should be allowed for the output of the amplifier to settle before performing a conversion. If the output voltage change is more than two volts, it may be necessary to perform two conversion cycles, discarding the first results. This will allow the A/D Converter to go through a complete coarse charge, fine charge, convert sequence. This will guarantee an accurate result.

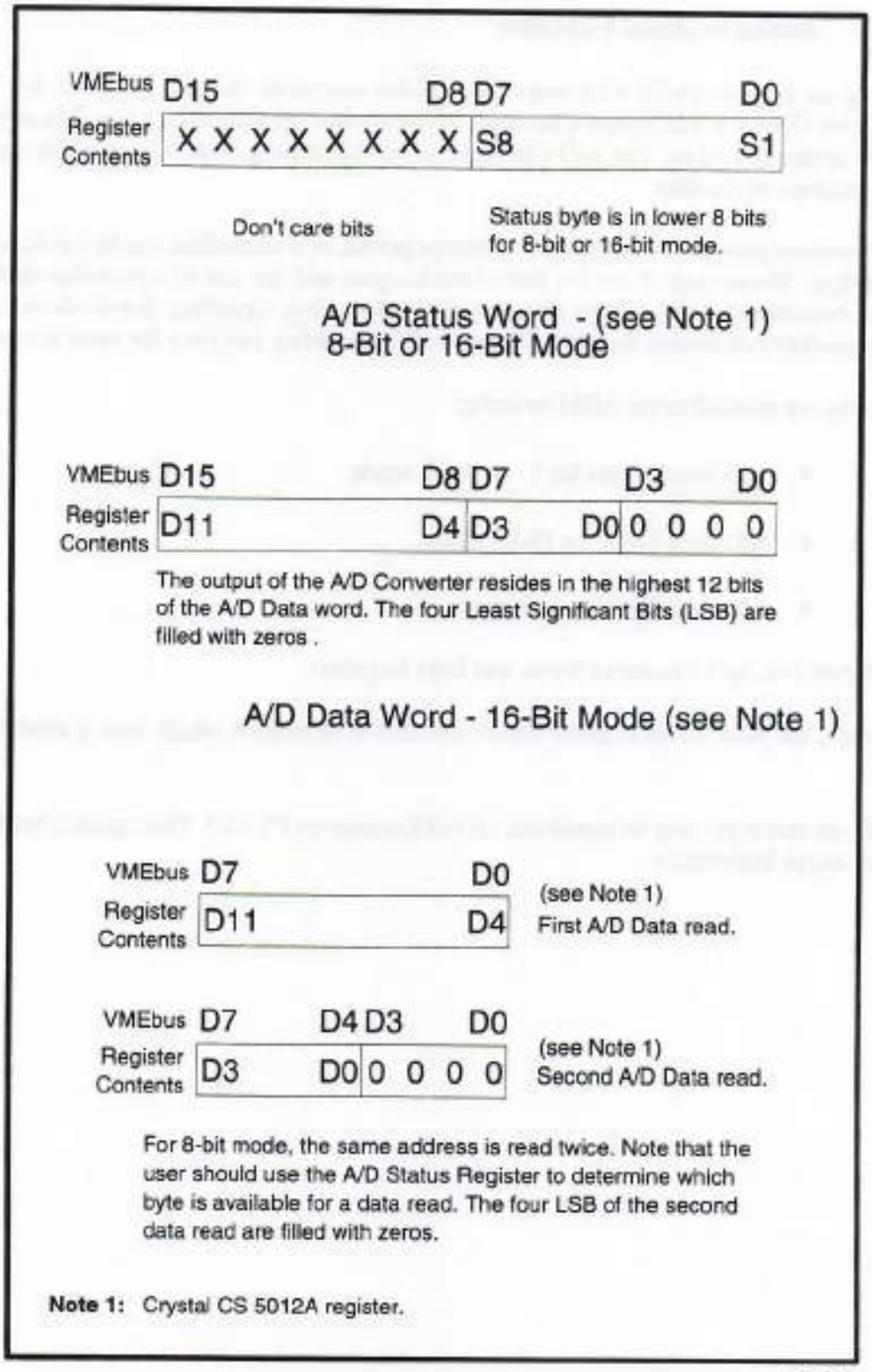


Figure 4-2: A/D Converter Status and Data Registers

4.9 Analog to Digital Converter

The Analog to Digital (A/D) Converter is a 12-bit converter designed around the Crystal Semiconductor Corp. CS 5012A A/D Converter with a conversion time of 12.25 µs. The acquisition time for the device is 3.75 µs. The A/D Converter is self-calibrating on power-up and is capable of 8-bit read accesses of the data.

The A/D Converter provides two outputs that may be polled, or if unmasked, can be used to generate VME interrupts. These outputs are the end of track-signal and the end of conversion-signal. The end of track becomes asserted 3.75 µs after an end of conversion, signalling that the device is ready to perform another conversion. Refer to Chapter 6, Programming Interface for more information.

The following are internal to the A/D Converter:

- A/D Status Word for 8- or 16-bit mode
- A/D Data Word for 16-bit mode
- A/D Data Byte for 8-bit mode.

Refer to Figure 4-2, A/D Converter Status and Data Registers.

In 8-bit mode, the A/D Status Register should be used to determine which byte is available for a data read.

The A/D Converter input may be monitored at the P2 connector P2-C13. This signal is buffered and has a 1 kΩ output impedance.

4.9.1 Analog to Digital Scaling

The A/D Converter has a reference of 4.5 volts. In bipolar mode, the scaled input voltage to the A/D Converter is ±4.5 volts over the 0 to $FFF0_H$ range. The most significant bit is the sign bit for the converted value. The A/D Converter pads the least significant nibble with zeros forcing the result to be left-justified. The scaled input voltages and their hex values are:

- +4.5 V = $FFF0_H$
- 0.0 V = 8000_H
- -4.5 V = 0000_H.

This range corresponds to 2.19 mV per bit of resolution. The scaling of the input circuit and the amplifier chain is such that, in an ideal situation where the VME power supplies are at the maximum (+12.46 and -12.46), the maximum available dynamic input range at the P2 connector would be ±10 V and ±40 V. The differential amplifier stage has a gain of 0.45 V/V. This would then correspond to ±4.5 V at the A/D Converter. Due to the variation in VME power supply voltage, however, the guaranteed dynamic range is ±8 V and ±32 V. The scaling is not adjusted for the reduced input range. The +8 V input, therefore, will result in a conversion value of $E6B0_H$ and a -8 V input will result in a conversion value of 1950_H. In either case, the 0 volt point will remain as 8000_H.

In unipolar mode, the scaled voltage input to the A/D Converter is 0 to +4.5 volts over the 0 to $FFF0_H$ range. The scaled input voltages and their hex values are:

- 0.0 V = 0000_H
- +4.5 V = $FFF0_H$.

4.9.2 Analog to Digital Conversions

To execute an Analog to Digital conversion, the user must write to the A/D Convert/Read Address. The DMV-666/SVME-667 A/D, D/A Converter Card does not care what data is written to the A/D Convert/Read Address, as long as it is write-accessed.

To obtain converted data, the user must read the same A/D Convert/Read Address.

The A/D Converter contains a track and hold amplifier that has three modes of operation. These modes of operation are controlled by the state of the A/D Converter. They are initiated by the write to the A/D Converter that starts a conversion.

The A/D Converter track and hold amplifier operates in a coarse track mode for the first 6 clock cycles (1.5 µs) after an end of conversion has been issued. The amplifier then switches to a fine track mode until the hold command is issued by writing to the A/D Converter Data Register. The hold command causes the A/D Converter to hold the tracked voltage until the conversion has been completed. Then it switches to the coarse track mode.

The following is the difference between the tracking modes:

- in coarse track mode, large voltage changes are tracked by a high slew rate buffer in the input circuit

- in fine track mode, the input buffer is switched out of the tracking circuit to minimize input offset voltages. This limits the acquisition rate to the slow rate and drive capability of the source amplifier.

It is recommended that the input multiplexer changes and the programmable gain amplifier changes be made while the A/D Converter is performing a conversion. The converter will then accurately acquire the new voltage within 3.75 µs. An alternative is to perform two conversions after making an input multiplexer change or gain change and to discard the results of the first conversion.

4.9.2.1 Sample Analog to Digital Conversion - Non-Interleaved, Polled

For a non-interleaved, polled A/D conversion, execute the following steps:

1. Set the Gain/Multiplexer Control Register for the appropriate input and gain (e.g., Input Channel 5 of the Input Multiplexer and a gain of 1 on the Programmable Gain Amplifier).
2. Wait 13 µs for settling time.
3. Initiate a conversion by writing to the A/D Convert/Read Address.
4. Poll the A/D Status Register for the end of the conversion (Convert bit (bit 0) in the A/D Status Register set to 0).
5. Read the A/D Convert/Read Address.
6. Repeat from Step 1 with new input selection and/or new gain setting.

4.9.2.2 Sample Analog to Digital Conversion - Non-Interleaved, Interrupt-Driven

For a non-interleaved, interrupt-driven A/D conversion, execute the following steps:

1. Write the interrupt vector value to the Vector Register. (The interrupt vector value goes out on the VMEbus.)
2. Enable the End of Conversion bit (bit 3) in the General Purpose Control Register.
3. Set the Gain/Multiplexer Control Register for the appropriate input and gain (e.g., Input Channel 5 of the Input Multiplexer and a gain of 1 on the Programmable Gain Amplifier).
4. Wait 13 µs for settling time.
5. Initiate a conversion by writing to the A/D Convert/Read Address.
6. Wait for the interrupt - the software program is free to perform other tasks.
7. In the Interrupt Service Routine:
    - read the A/D data (read the A/D Convert/Read Address)
    - repeat at Step 3 with new input selection and/or new gain setting.

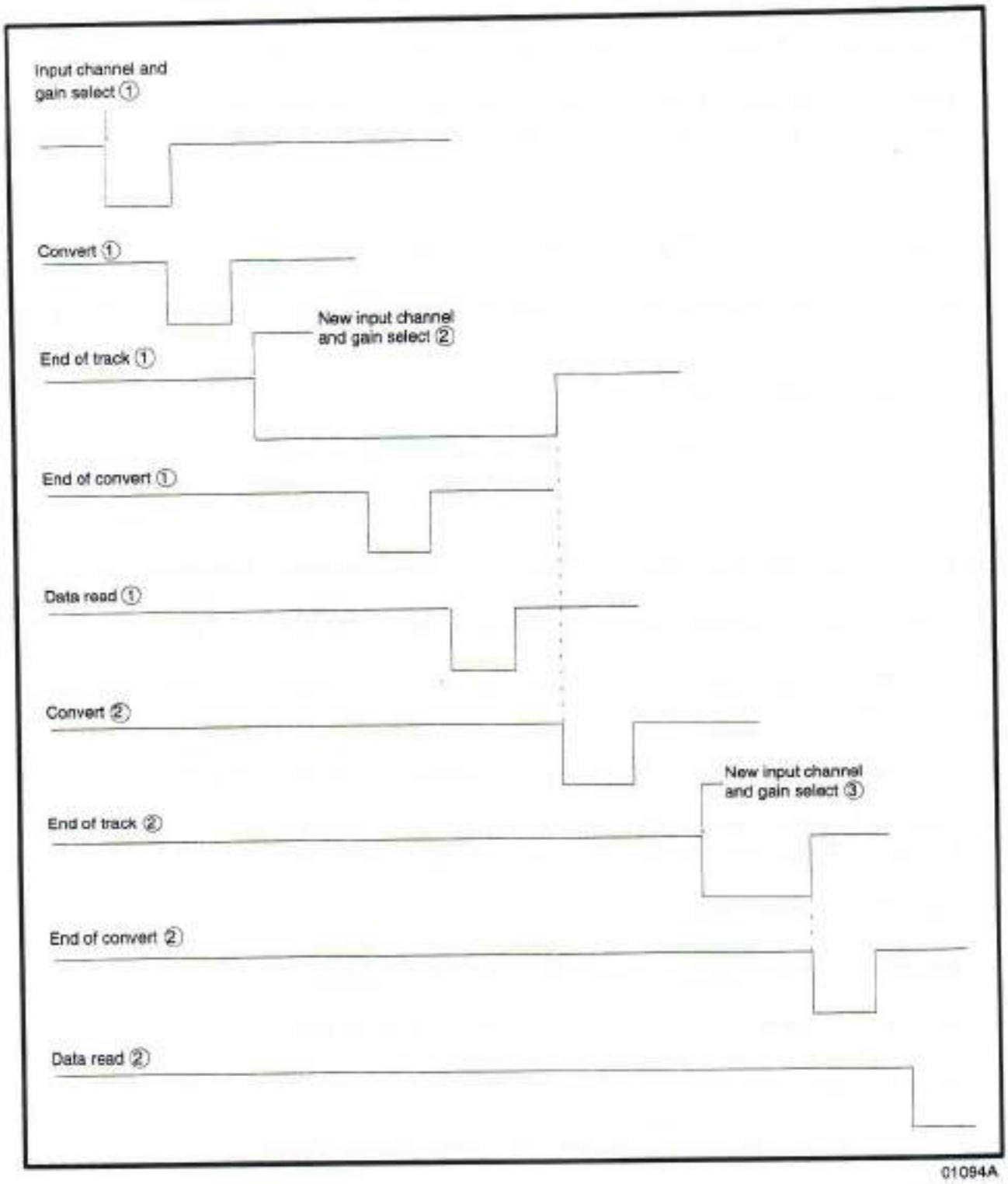


Figure 4-3: Interleaved and Polled A to D Conversion

4.9.2.3 Sample Analog to Digital Conversion - Interleaved, Polled

For an interleaved, polled A/D conversion, execute the following steps and refer to Figure 4-3, Interleaved and Polled A/D Conversion:

1. Set the Gain/Multiplexer Control Register for the appropriate input and gain (e.g., Input Channel 5 of the Input Multiplexer and a gain of 1 on the Programmable Gain Amplifier).
2. Wait 13 µs for settling time.
3. Execute the first conversion (write access the A/D Convert/Read Address).
4. Poll the A/D Status Register for the end of the first track (bit 5 in the A/D Status Register is set to 0).
5. Select the second input channel and/or gain setting.
6. Poll the A/D Status Register for the first end of the conversion (bit 0 in the A/D Status Register set to 0).
7. Execute the first data read (read the A/D Convert/Read Address).
8. Execute the second conversion (write access the A/D Convert/Read Address).
9. Poll the A/D Status Register for the end of the second track (bit 5 in the A/D Status Register is set to 0).
10. Select the third input channel and/or gain setting.
11. Poll the A/D Status Register for the second end of the conversion (bit 0 in the A/D Status Register set to 0).

4.10 Analog to Digital Converter Calibration

The following sections detail when to calibrate, what is required to perform the calibration, and how to calibrate the DMV-666/SVME-667 A/D, D/A Converter Card.

4.10.1 When To Calibrate

The user should check the calibration of the DMV-666/SVME-667 A/D, D/A Converter Card when the following occurs:

- power-up/reset
- change in temperature greater than 50°C
- possible erroneous data (user-discretion).

4.10.2 Required Inputs for Calibration

The following are required inputs for a calibration:

- An input connected to ground
- Temperature Sensor on the Diagnostic Multiplexer
- Electronic Potentiometer.

4.10.3 Method of Calibration

The following steps detail the method of calibration for the DMV-666/SVME-667 A/D, D/A Converter Card:

1. Apply a short to ground on an unused input and program the Gain/Multiplexer Control Register for the appropriate input.

2. Ensure that the Programmable Gain Amplifier is set to a gain of 1.

3. Execute a write access to the A/D Convert/Read Address.

4. Read the data from the A/D Converter (read the data at the A/D Convert/Read Address).

5. The data should be 8000 ± 1 (i.e., 7FF0 to 8010).

6. If the data is in error, calibrate the CCA by performing the following steps:

    - increment or decrement the Electronic Potentiometer

    - execute another conversion (repeat Steps 3 to 5)

Note: Between each Electronic Potentiometer adjustment, the user must wait 500 µs for settling time. Refer to Section 4.11, Electronic Potentiometer, for more information.

7. When the A/D Converter value is acceptable, store the Electronic Potentiometer value (in the EP) by executing the following steps:

    - set PCLK high

    - deselect the Electronic Potentiometer (via software-control, Bit 0 (EP Clock Bit Enable) in the A/D Control Register).

4.11 Electronic Potentiometer

The Electronic Potentiometer is a resistor ladder device of E^2 technology. It has 100 resistor steps which are changed by selecting the device, selecting the direction of travel, and then clocking the device. Each step increment changes the differential amplifier stage offset by 793 µV, therefore, it is possible to null any offsets inherent in the circuit before any absolute measurements are taken. The Electronic Potentiometer is biased between the +4.500 and -4.500 reference supplies, so it is possible to impose a positive or negative offset to the differential amplifier.

The offset is summed into the inverting input of the differential amplifier so a positive increment of the Electronic Potentiometer will result in a change in the negative direction of the differential amplifier.

The following must be considered when using the Electronic Potentiometer:

1. The system must provide VME SYSRESET* asserted on power-up and power-down to prevent the contents of the Electronic Potentiometer from being lost during power supply transitions.

2. The Potentiometer Chip Select signal, PCS, must be selected to enable programming of the Electronic Potentiometer. (PCS is Bit 0 in the A/D Control Register.)

3. On power-up of the CCA, the signal PCS must be written high to disable any inadvertant access to the Electronic Potentiometer.

4. The Electronic Potentiometer value changes on the 1 to 0 transition of the signal PCLK.

5. The Electronic Potentiometer requires 500 µs to settle before performing a conversion to check the result of the potentiometer increment/decrement.

6. Storage of the Electronic Potentiometer setting is performed by setting PCLK high and de-selecting the Potentiometer. The storage operation will take 20 ms, therefore, no changes to PCLK, PU/D, and PCS should be made during that period.

4.12 Digital to Analog Converter

The DMV-666/SVME-667 A/D, D/A Converter Card provides 8 single-ended analog output channels. These channels are capable of providing a maximum of ±10 V swing (VME power supplies at ±12 V or greater) at an output current of 5 mA. The D/A Converter outputs are buffered with short circuit protected op-amps. Note that prolonged shorts to ground may affect the long-term reliability of the devices.

The D/A Converters are configured to provide an output swing of ±10 V for full scale bipolar operation. This means that:

- a +10 V output corresponds to a value of $XFFF_H$
- a zero volt output corresponds to a value of $X800_H$
- a -10 V output corresponds to a value of $X000_H$.

The D/A Converters are 12-bit devices where the most significant nibble is don't care. The converters are capable of read/write operations, but only in word widths. Byte accesses are not disallowed, but will result in erroneous operation.

The D/A Converters may be accessed every 700 ns, but the outputs require a 20 µs period to settle before being re-addressed.

The 12-bit capability of the D/A Converters provides 4.88 mV per LSB resolution on the output. However, the limitations of the devices are as follows:

- gain error matching of any two DACs in the same package ±4 LSB
- bipolar zero matching ±2 LSB
- linearity matching ±1 LSB
- gain error over temperature between different packages ±5 LSB
- linearity error over temperature between different packages ±0.5 LSB

Note that these limitations apply to using DAC outputs in an application.

4.13 Temperature Sensor

The temperature sensor input available on Input 7 of the Reference Multiplexer is a temperature to voltage device. At 25°C the device will provide a voltage of -298 mV to the A/D Converter. This voltage will change at a rate of -1 mV per degree Celcius rise in temperature. The A/D Converter result will be (nominal):

$$-298 \text{ mV}/2.19 \text{ mV/bit} = -136 \text{ counts} = -88_H$$

$$800_H - 88_H = 778_H$$

The sensor is linear over the temperature range of -55°C to +150°C.

4.14 Interrupts

The DMV-666/SVME-667 A/D, D/A Converter Card can generate a VME interrupt on a selectable level from 0 to 7 and will place an 8-bit vector onto the VMEbus in response to an IACK cycle.

Interrupts may be generated by two signals which are derived from the A/D Converter. The first signal is the End of Track indicator which shows that acquisition is complete and that a conversion may be initiated. The second signal is the End of Conversion indicator which shows that data is ready to be read from the A/D Data Register. Both interrupts can be masked separately and operate in Release on Register Access mode. The End of Track interrupt is cleared by writing to the A/D Converter to initiate a conversion. The interrupt will recur 3.75 µs after an End of Conversion interrupt occurs.

To operate the DMV-666/SVME-667 A/D, D/A Converter Card at maximum throughput, both interrupts may be used. However, if the interrupts are not carefully controlled, the recurrance of the interrupts at 3.75 µs and 12.25 µs intervals may become a burden for the Interrupt Handler.

4.14.1 Interrupt Handler Operation

This section details a suggested sequence of starting up the DMV-666/SVME-667 A/D, D/A Converter Card to perform under interrupts. The sequence for initialization and performing the first conversion is suggested in order to prevent a spurrious interrupt from ocurring when first enabling the interrupts.

Initialize and perform the first conversion:

1. Mask End of Conversion and End of Track Interrupts.
2. Select desired interrupt level.
3. Program necessary vector.
4. Select first input to be sampled.
5. Poll for End of Track.
6. When true, initiate conversion and poll for End of Conversion.
7. At end of conversion, read and discard the result.
8. Poll for End of Track.
9. When true, initiate conversion.
10. Select next input to be converted.
11. Enable End of Conversion interrupt.

Interrupt service routine:

```
Check source of interrupt
If entered due to End of Conversion
then
    enable End of Track interrupt
    read converted result
    RTI
else service End of Track Interrupt
    initiate conversion
    select next input for conversion
    RTI
```

5. CONNECTOR ASSIGNMENTS

The pin assignments for the P1 and P2 connectors are listed in Table 5-1 and Table 5-2 respectively.

5.1 P1 Pin Assignments

Table 5-1
P1 Pin Assignments

Pin Number	Row A Mnemonic	Row B Mnemonic	Row C Mnemonic
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	(BG0IN*)	D11
5	D04	(BG0OUT*)	D12
6	D05	(BG1IN*)	D13
7	D06	(BG1OUT*)	D14
8	D07	(BG2IN*)	D15
9	GND	(BG2OUT*)	GND
10	(SYSCLK)	(BG3IN*)	SYSFAIL*
11	GND	(BG3OUT*)	(BERR*)
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	(A23)
16	DTACK*	AM0	(A22)
17	GND	AM1	(A21)
18	AS*	AM2	(A20)
19	GND	AM3	(A19)
20	IACK*	GND	(A18)
21	IACKIN*	(SERCLK)	(A17)
22	IACKOUT*	(SERDAT)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	(+5VSTDBY)	+12V
32	+5 V	+5 V	+5 V

Note: Signals in parentheses ( ) are not used by the DMV666/SVME-667 A/D, D/A Converter Card.

5.2 P2 Pin Assignments

Table 5-2
P2 Pin Assignments

Pin Number	Row A Mnemonic	Row B Mnemonic	Row C Mnemonic
1	GND	+5 V	P2ID0
2	P2ID1	GND	P2ID2
3	P2ID3	RESERVED	P2ID4
		(DISP3)	CARDFAIL*
4		(A24)	
5	DAC0	(A25)	
6	DAC1	(A26)	
7	DAC2	(A27)	
8		(A28)	
9	DAC3	(A29)	
10	DAC4	(A30)	AGND0
11	DAC5	(A31)	
12		GND	AGND1
13	ADC0A	(+5V)	ANALOG_OUT
14	ADC1A	(D16)	AGND2
15	ADC2A	(D17)	ADC0B
16		(D18)	AGND3
17	ADC3A	(D19)	ADC1B
18	ADC4A	(D20)	AGND4
19	ADC5A	(D21)	ADC2B
20		(D22)	AGND5
21	ADC6A	(D23)	ADC3B
22	ADC7A	(+5V)	AGND6
23	DAC6	(D24)	ADC4B
24		(D25)	AGND7
25	DAC7	(D26)	ADC5B
26		(D27)	ADC6B
27		(D28)	ADC7B
28		(D29)	
29		(D30)	
30		(D31)	
31		(GND)	
32		(+5V)	

Note: The signal names in parentheses are not used by the DMV-666/SVME-667 A/D, D/A Converter Card.

Table 5-3
P2 Pin Assignment Descriptions

P2 Connector Pin	Description
DAC0 to DAC7	Digital to Analog Converter outputs.
AGND0 to AGND7	Digital to Analog Converter output returns.
ADC+0 to ADC+7	Analog to Digital Converter inputs. - Positive input in differential mode. - Input to Multiplexer A in single-ended mode.
ADC-0 to ADC-7	Analog to Digital Converter inputs. - Negative input in differential mode. - Input to Multiplexer B in single-ended mode.
P2ID0 -P2ID4	VME address select inputs (pulled up if left open)

Note: In the case of single-ended operation, the input returns are to be shared with the DAC output returns AGND0 to AGND7.

5.3 P2 Pin Assignment Descriptions

Table 5-3 describes all user-definable P2 connector pins.

6. PROGRAMMING INTERFACE

This chapter describes the programming interface of the DMV-666/SVME-667 A/D, D/A Converter Card. The following are included:

- control and status registers
- BI-mode® Entry/Exit Location Monitor
- Input Selection Programming Chart.

6.1 Control and Status Registers

The following control and status registers are on the DMV-666/SVME-667 A/D, D/A Converter Card:

- Mode Control Register
- A/D Status Register (ADSR) [1].
- General Purpose Control Register (GPCR)
- Vector Register (VR)
- Gain/Multiplexer Control Register (GMCR)
- A/D Control Register (ADCR).

Table 6-1, I/O Address Locations, shows the addresses of the registers. Note that register blocks are repeated throughout the VMEbus memory space. The A/D Status Register that is paired with the A/D Data/Convert Register is repeated 64 times; the rest of the registers are imaged 128 times.

The following list of abbreviations pertains to sections 6.1.1 through 6.1.5 describing the BI-mode® entry/exit location monitor, status registers, control registers, and the vector register:

AR	access rights
RC	reset condition: status of bit following an internal reset
RO	read only: writing to these bits causes no adverse affects
R/W	read/write bit
WO	write only
NA	not applicable: the sense of these bits is unknown at reset
X	these bits are unused and unavailable
-	the value is dependent on the state of the monitored signal.

A read of a R/W location returns either the reset condition of the value previously written without inversion.

Register accesses are byte- or word-addressable as specified in each of the following register descriptions.

Table 6-1
I/O Address Locations

Register	Offset from Base	Access Type
BI_MODE Entry/Exit Location	0601	Byte
Vector Register	0503	Byte
General Purpose Control Register	0403	Byte
Gain/Multiplexer Control Register	0303	Byte
A/D Control Register	0203	Byte
A/D Status Register	0101	Byte
A/D Data Register	0102	Word/Byte
Mode Control Register	0083	Byte
DAC8	0046	Word
DAC7	0044	Word
DAC6	0042	Word
DAC5	0040	Word
DAC4	0006	Word
DAC3	0004	Word
DAC2	0002	Word
DAC1	0000	Word

6.1.1 Mode Control Register

The Mode Control Register is a read/write port that controls input-multiplexer mode, Diagnostic

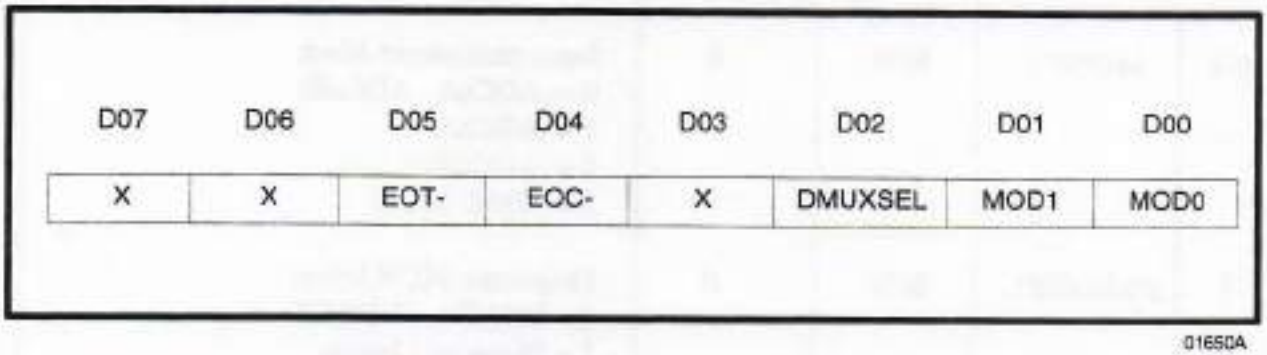


Figure 6-1: Mode Control Register

MUX group-select, and VCOM1/VCOM2 select. Figure 6-1 and Table 6-2 contain the bit information for the Mode Control Register.

Table 6-2
Mode Control Register

Bit	Bit Name	Access Rights	Reset Condition	Description
0-1	MOD0-1	R/W	0	Input-multiplexer Mode 0 = (ADCnA - ADCnB) 1 = (ADCnA) 2 = (ADCnB) 3 = VDAC-MUX
2	DMUXSEL	R/W	0	Diagnostic-MUX Select 0 = VDAC0 . . VDAC7 1 = Diagnostic Inputs
3	X	R/W	0	not used
4	EOC-	R/O	1	0 = End of conversion 1 = Conversion still in progress
5	EOT-	R/O	1	0 = End of track 1 = Still tracking or inactive
6-7	X	R/W	0	not used

6.1.2 General Purpose Control Register

The General Purpose Control Register (GPCR) is a read/write register at the same address. The GPCR provides the following functions:

- the VMEbus IRQ level for the DMV-666/SVME-667 A/D, D/A Converter Card
- the interrupt mask
- the VMEbus SYSFAIL* signal.

Figure 6-2 and Table 6-3 contain the bit information for the GPCR.

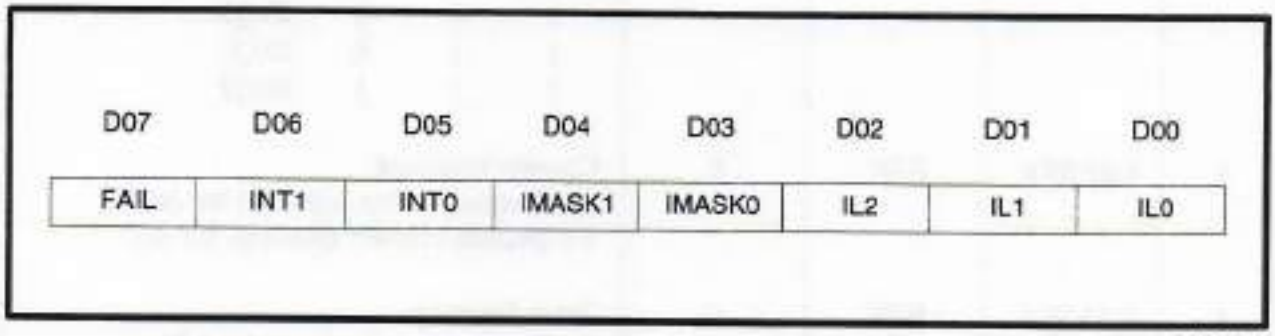


Figure 6-2: General Purpose Control Register

Table 6-3
General Purpose Control Register

Bit	Bit Name	Access Rights	Reset Condition	Description
0 - 2	IL0 - IL2	R/W	0	VMEbus Interrupt Level Select Bits These bits specify which VMEbus IRQ line is asserted when a DMV-666/SVME-667 A/D, D/A Converter Card interrupt request occurs. IL2 IL1 IL0 IRQ Line 0 0 0 No affect 0 0 1 IRQ1 0 1 0 IRQ2 0 1 1 IRQ3 1 0 0 IRQ4 1 0 1 IRQ5 1 1 0 IRQ6 1 1 1 IRQ7
3	IMASK0	R/W	0	Convert Interrupt 0 = Enable convert interrupt for A/D 1 = Disable convert interrupt for A/D
4	IMASK1	R/W	0	Track Interrupt 0 = Enable track interrupt for A/D 1 = Disable track interrupt for A/D
5	INT0	RO	0	End of Conversion 0 = End of conversion 1 = Conversion still in progress
6	INT1	RO	0	End of Track 0 = End of track 1 = inactive
7	FAIL	R/W	0	VMEbus SYSFAIL* 0 = Assert VMEbus SYSFAIL* 1 = CCA is not driving SYSFAIL*

6.1.3 Vector Register

The Vector Register (VR) is a read/write port which supplies the status-ID information for the IACK read cycles. It is 8 bits wide and is accessible on the lower 8 bits of the data bus (D00 to D07).

Figure 6-3 and Table 6-4 contain the bit information for the VR.

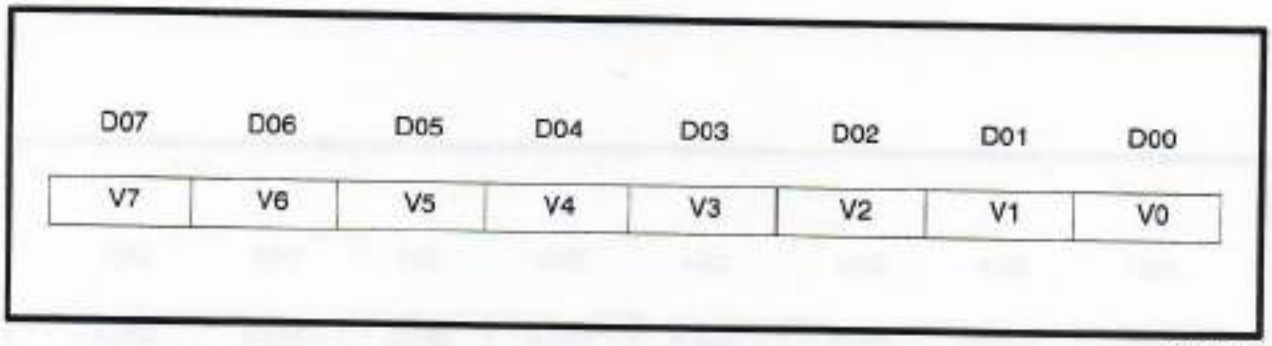


Figure 6-3: Vector Register

Table 6-4
Vector Register

Bit	Bit Name	Access Rights	Reset Condition	Description
0 - 7	V0 - V7	R/W	0	Interrupt Status ID Byte

6.1.4 Gain/Multiplexer Control Register

The Gain/Multiplexer Control Register (GMCR) is a read/write port which supplies the gain and channel number for the Programmable Gain Amplifier, Input Multiplexer, and the Diagnostic Multiplexer. The GMCR is 8 bits wide and is accessible on the lower 8 bits of the data bus (D00 to D07).

Figure 6-4 and Table 6-5 contain the bit information for the GMCR.

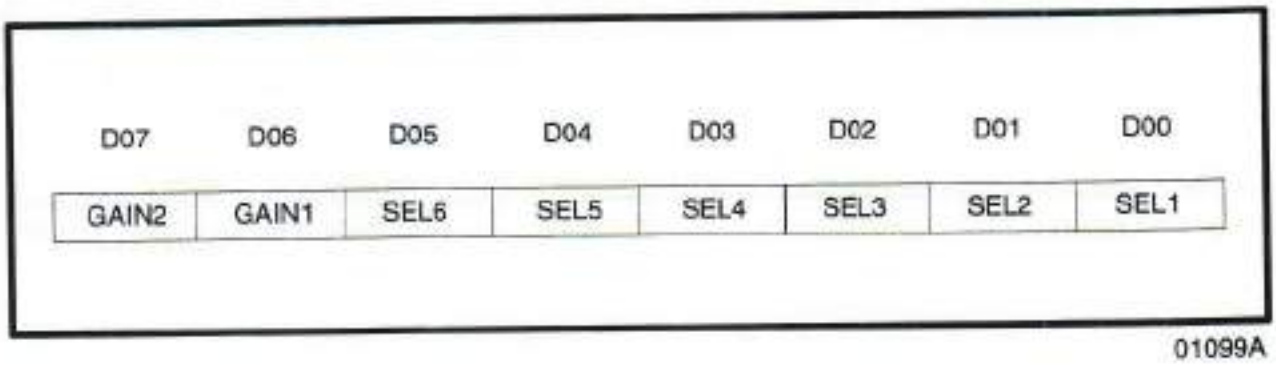


Figure 6-4: Gain/Multiplexer Control Register

Table 6-5
Gain/Multiplexer Control Register

Bit	Bit Name	Access Rights	Reset Condition	Description
0 - 2	SEL1 - SEL3	R/W	0	Input Multiplexer Channel Select These three bits select the input channel on the Input Multiplexer. SEL3 SEL2 SEL1 0 0 0 Input Channel 0 0 0 1 Input Channel 1 0 1 0 Input Channel 2 0 1 1 Input Channel 3 1 0 0 Input Channel 4 1 0 1 Input Channel 5 1 1 0 Input Channel 6 1 1 1 Input Channel 7
3 - 5	SEL4 - SEL6	R/W	0	Diagnostic and Reference Multiplexer Channel Select .
6, 7	GAIN1, GAIN2	R/W	0	These two bits select the gain for the selected channel. GAIN2 GAIN1 Gain Setting 0 0 Gain of 1 0 1 Gain of 2 1 0 Gain of 4 1 1 Gain of 8

6.1.5 Analog to Digital Control Register

The A/D Control Register (ADCR) is a read/write port which supplies the control lines to the A/D Converter and to the Electronic Potentiometer. It is 8 bits wide and is accessible on the lower 8 bits of the data bus (D00 to D07).

Figure 6-5 and Table 6-6 contain the bit information for the ADCR.

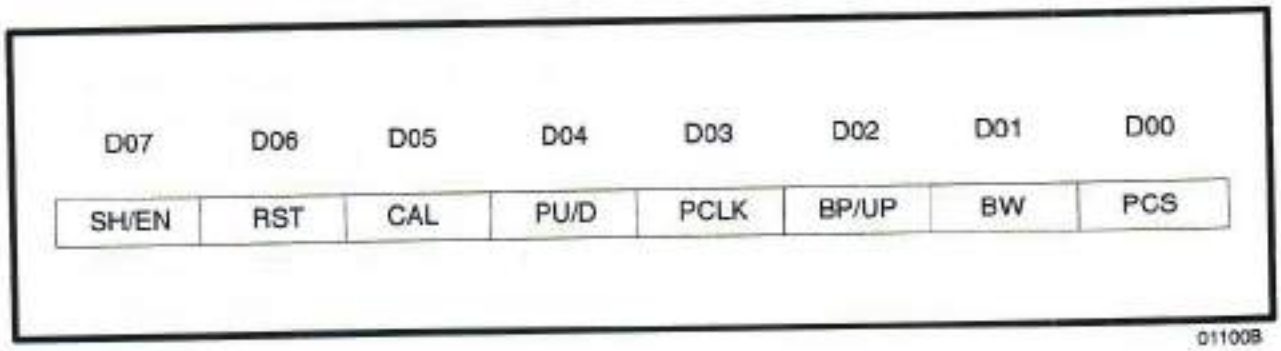


Figure 6-5: A/D Control Register

Table 6-6
A/D Control Register

Bit	Bit Name	Access Rights	Reset Condition	Description
0	PCS	R/W	0	Chip Select Potentiometer 0 = Selected 1 = Inactive
1	BW	R/W	0	Bus Width 0 = Selects A/D bus width of 8 bits 1 = Selects A/D bus width of 16 bits
2	BP/UP	R/W	0	Bipolar/Unipolar Operation 0 = Selects A/D Converter for unipolar operation 1 = Selects A/D Converter for bipolar operation
3	PCLK	R/W	0	Potentiometer Clock 0 = Increments/Decrements Potentiometer value when bit transition goes from 1 to 0 1 = Inactive
4	PU/D	R/W	0	Increment/Decrement Potentiometer 0 = sets Electronic Potentiometer to decrement when clocking 1 = sets Electronic Potentiometer to increment when clocking
5	CAL	R/W	0	Reserved
6	RST	R/W	0	A/D Converter Reset 0 = Inactive 1 = Resets the A/D Converter and initiates a calibration sequence
7	SH/EN	R/W	0	Shadow Multiplexer Enable 0 = Inactive 1 = Enables the Shadow Multiplexer

6.2 BI-mode® Entry/Exit Location Monitor

The BI-mode® entry/exit location monitor is available on the VMEbus via the A16 address space.

Software entry into BI-mode® is accomplished by the appropriate read access of the location monitor.

The DMV-666/SVME-667 A/D, D/A Converter Card exits from BI-mode® when the VMEbus master writes to the location monitor while the IRQ1* signal is negated.

Refer to Section 3.1.2, Entry Into/Exit From BI-mode® Via IRQ1*, in Chapter 3, for more information.

6.3 Input Selection Programming

Table 6-7, Input Selection Programming, details a sample programming chart of bit settings for selecting inputs.

Table 6-7
Input Selection Programming

Inputs	Bit Settings									
	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	DMS	MODE2	MODE1	SHADOW
Differential Input 0	0	0	0	0	0	0	0	0	0	0
Differential Input 1	0	0	0	0	0	1	0	0	0	0
Differential Input 2	0	0	0	0	1	0	0	0	0	0
Differential Input 3	0	0	0	0	1	1	0	0	0	0
Differential Input 4	0	0	0	1	0	0	0	0	0	0
Differential Input 5	0	0	0	1	0	1	0	0	0	0
Differential Input 6	0	0	0	1	1	0	0	0	0	0
Differential Input 7	0	0	0	1	1	1	0	0	0	0
Differential Input 0 x 0.64	0	0	0	0	0	0	0	0	0	1
Differential Input 1 x 0.64	0	0	0	0	0	1	0	0	0	1
Differential Input 2 x 0.64	0	0	0	0	1	0	0	0	0	1
Differential Input 3 x 0.64	0	0	0	0	1	1	0	0	0	1
Differential Input 4 x 0.64	0	0	0	1	0	0	0	0	0	1
Differential Input 5 x 0.64	0	0	0	1	0	1	0	0	0	1
Differential Input 6 x 0.64	0	0	0	1	1	0	0	0	0	1
Differential Input 7 x 0.64	0	0	0	1	1	1	0	0	0	1
Single-Ended Input +0	0	0	0	0	0	0	0	0	1	0
Single-Ended Input +1	0	0	0	0	0	1	0	0	1	0
Single-Ended Input +2	0	0	0	0	1	0	0	0	1	0
Single-Ended Input +3	0	0	0	0	1	1	0	0	1	0
Single-Ended Input +4	0	0	0	1	0	0	0	0	1	0
Single-Ended Input +5	0	0	0	1	0	1	0	0	1	0
Single-Ended Input +6	0	0	0	1	1	0	0	0	1	0
Single-Ended Input +7	0	0	0	1	1	1	0	0	1	0

Note: x indicates 'don't care' bits.
DMS is Diagnostic Multiplexer Select (DMUXSEL)

Table 6-7 (Continued)
Input Selection Programming

Inputs	Bit Settings									
	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	DMS	MODE2	MODE1	SHADOW
Single-Ended Input +0x0.64	0	0	0	0	0	0	0	0	1	1
Single-Ended Input +1x0.64	0	0	0	0	0	1	0	0	1	1
Single-Ended Input +2x0.64	0	0	0	0	1	0	0	0	1	1
Single-Ended Input +3x0.64	0	0	0	0	1	1	0	0	1	1
Single-Ended Input +4x0.64	0	0	0	1	0	0	0	0	1	1
Single-Ended Input +5x0.64	0	0	0	1	0	1	0	0	1	1
Single-Ended Input +6x0.64	0	0	0	1	1	0	0	0	1	1
Single-Ended Input +7x0.64	0	0	0	1	1	1	0	0	1	1
Single-Ended Input -0	0	0	0	0	0	0	0	1	0	0
Single-Ended Input -1	0	0	0	0	0	1	0	1	0	0
Single-Ended Input -2	0	0	0	0	1	0	0	1	0	0
Single-Ended Input -3	0	0	0	0	1	1	0	1	0	0
Single-Ended Input -4	0	0	0	1	0	0	0	1	0	0
Single-Ended Input -5	0	0	0	1	0	1	0	1	0	0
Single-Ended Input -6	0	0	0	1	1	0	0	1	0	0
Single-Ended Input -7	0	0	0	1	1	1	0	1	0	0
Single-Ended Input -0x0.64	0	0	0	0	0	0	0	1	0	1
Single-Ended Input -1x0.64	0	0	0	0	0	1	0	1	0	1
Single-Ended Input -2x0.64	0	0	0	0	1	0	0	1	0	1
Single-Ended Input -3x0.64	0	0	0	0	1	1	0	1	0	1
Single-Ended Input -4x0.64	0	0	0	1	0	0	0	1	0	1
Single-Ended Input -5x0.64	0	0	0	1	0	1	0	1	0	1
Single-Ended Input -6x0.64	0	0	0	1	1	0	0	1	0	1
Single-Ended Input -7x0.64	0	0	0	1	1	1	0	1	0	1

Note: x indicates 'don't care' bits.
DMS is Diagnostic Multiplexer Select (DMUXSEL)

Table 6-7 (Continued)
Input Selection Programming

Inputs	Bit Settings									
	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	DMS	MODE2	MODE1	SHADOW
VDAC MUX VDAC 0	0	0	0	0	0	0	0	1	1	0
VDAC MUX VDAC 1	0	0	0	0	0	1	0	1	1	0
VDAC MUX VDAC 2	0	0	0	0	1	0	0	1	1	0
VDAC MUX VDAC 3	0	0	0	0	1	1	0	1	1	0
VDAC MUX VDAC 4	0	0	0	1	0	0	0	1	1	0
VDAC MUX VDAC 5	0	0	0	1	0	1	0	1	1	0
VDAC MUX VDAC 6	0	0	0	1	1	0	0	1	1	0
VDAC MUX VDAC 7	0	0	0	1	1	1	0	1	1	0
VDAC MUX VDAC0x0.64	0	0	0	0	0	0	0	1	1	1
VDAC MUX VDAC1x0.64	0	0	0	0	0	1	0	1	1	1
VDAC MUX VDAC2x0.64	0	0	0	0	1	0	0	1	1	1
VDAC MUX VDAC3x0.64	0	0	0	0	1	1	0	1	1	1
VDAC MUX VDAC4x0.64	0	0	0	1	0	0	0	1	1	1
VDAC MUX VDAC5x0.64	0	0	0	1	0	1	0	1	1	1
VDAC MUX VDAC6x0.64	0	0	0	1	1	0	0	1	1	1
VDAC MUX VDAC7x0.64	0	0	0	1	1	1	0	1	1	1
REF MUX (INPUT1)	0	0	1	x	x	x	0	x	x	x
REF MUX (INPUT2)	0	1	0	x	x	x	0	x	x	x
REF MUX (INPUT3)	0	1	1	x	x	x	0	x	x	x
REF MUX (INPUT4)	1	0	0	x	x	x	0	x	x	x
REF MUX (INPUT5)	1	0	1	x	x	x	0	x	x	x
REF MUX (INPUT6)	1	1	0	x	x	x	0	x	x	x
REF MUX (INPUT7)	1	1	1	x	x	x	0	x	x	x

Note: x indicates 'don't care' bits.
DMS is Diagnostic Multiplexer Select (DMUXSEL)

Table 6-7 (Continued)
Input Selection Programming

Inputs	Bit Settings									
	SEL6	SEL5	SEL4	SEL3	SEL2	SEL1	DMS	MODE2	MODE1	SHADOW
DIAG MUX (INPUT 0)	0	0	0	x	x	x	1	x	x	x
DIAG MUX (INPUT1)	0	0	1	x	x	x	1	x	x	x
DIAG MUX (INPUT2)	0	1	0	x	x	x	1	x	x	x
DIAG MUX (INPUT3)	0	1	1	x	x	x	1	x	x	x
DIAG MUX (INPUT4)	1	0	0	x	x	x	1	x	x	x
DIAG MUX (INPUT5)	1	0	1	x	x	x	1	x	x	x
DIAG MUX (INPUT6)	1	1	0	x	x	x	1	x	x	x
DIAG MUX (INPUT7)	1	1	1	x	x	x	1	x	x	x

Note: x indicates 'don't care' bits.
DMS is Diagnostic Multiplexer Select (DMUXSEL)

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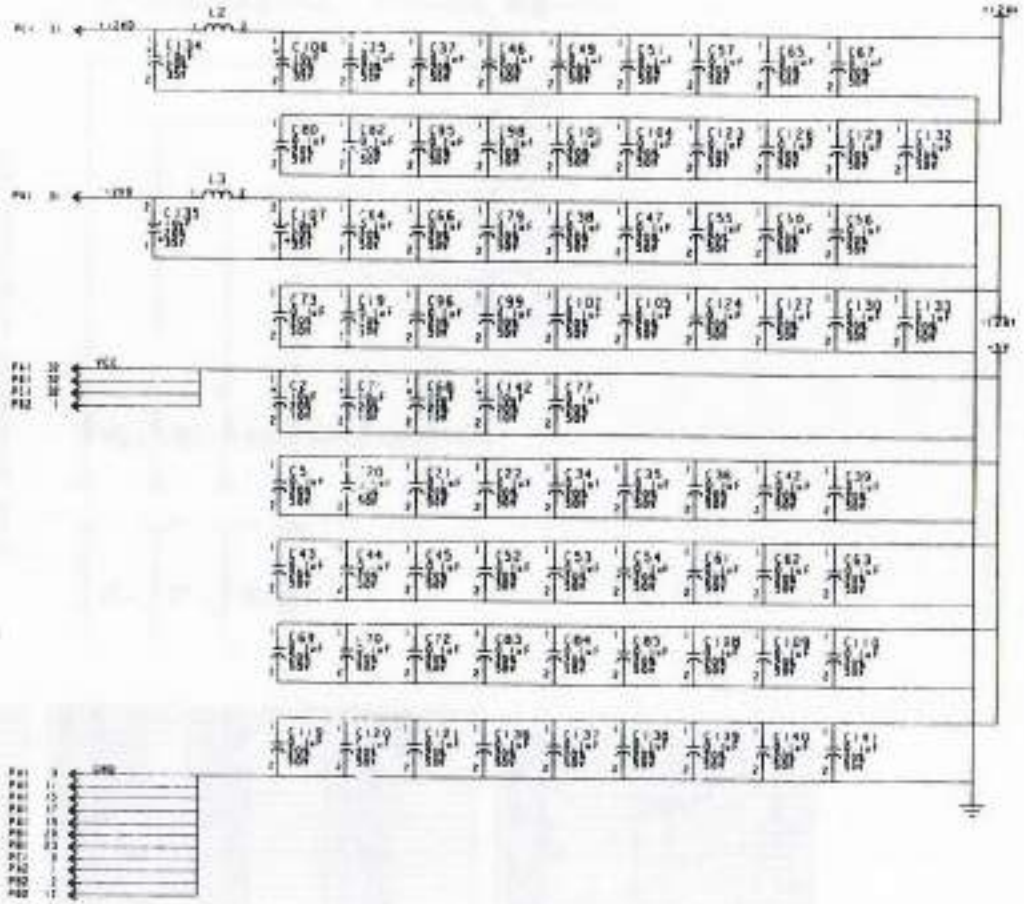
APPENDIX TO HARDWARE USER'S MANUAL

TABLE OF CONTENTS

1. Schematic Diagram DMV-666/SVME-667 Unconfigured

NOTES:

1. APPLICABLE STANDARDS/SPECIFICATIONS
   A 500-318-0010(DAR)
   B ANSI/IEEE STD 91-1984
2. REFERENCE DOCUMENTS
   A DMR-446-356 WIRING BOARD 3:0200-001
   B 1986-647-006 PRINTED WIRING BOARD 3:0442-001
3. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION PREFIX WITH UNIT NUMBER AND SUBASSEMBLY
4. SIGNALS WHICH PASS BETWEEN SHEETS MUST BE CONNECTED USING THE FOLLOWING <SHEET> OFF-PAGE SYMBOLS IDENTIFYING SIGNAL NAME (SEE LISTING) AND GRID LOCATION OF PICKUP POINT OR OTHER SHEETS
5. UNLESS OTHERWISE SPECIFIED
   RESISTANCE VALUES ARE IN OHMS
   CAPACITANCE VALUES ARE IN MICROFARADS
6. THE UNDERSCORE (_) SYMBOL DENOTES A SPACE
7. COMMON CONNECTION CIRCUIT RETURN SYMBOLS IDENTIFICATIONS ARE AS FOLLOWS:
   DIGITAL GROUND
   ANALOG GROUND
   CHASSIS GROUND



REV	STATUS OF SHEETS

SCHEMATIC DIAGRAM
UNCONFIGURED
DMR-446/SYME-667

E | 08YC3 | 410135-004

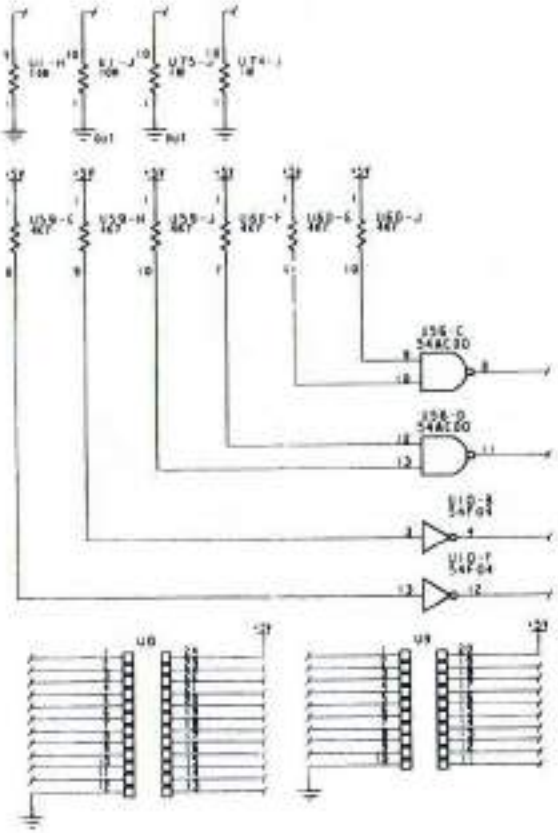
P1 SIGNAL NAMES

P2 SIGNAL NAMES

POWER TERMINAL TABLE

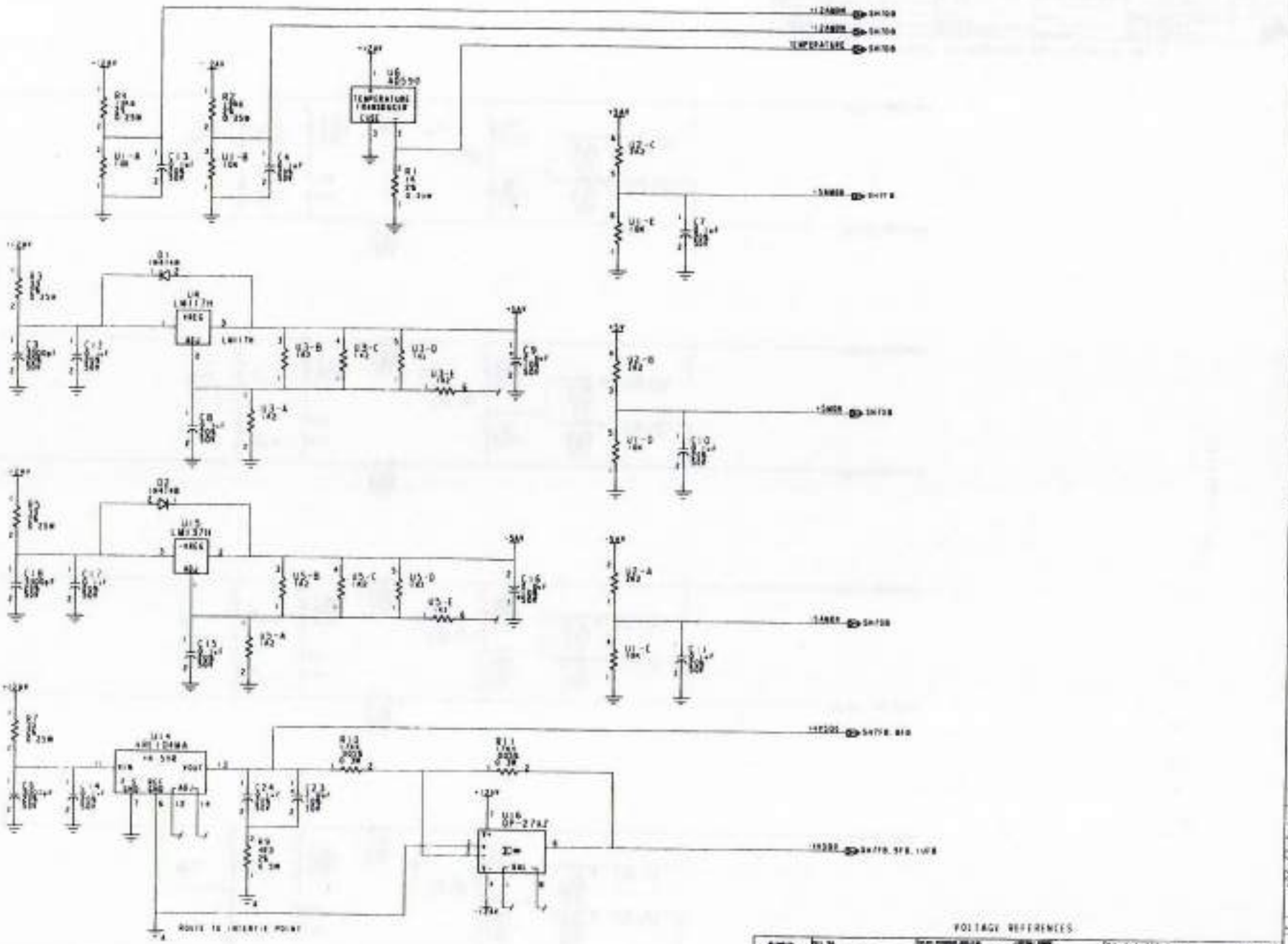
COMPONENT TABLE

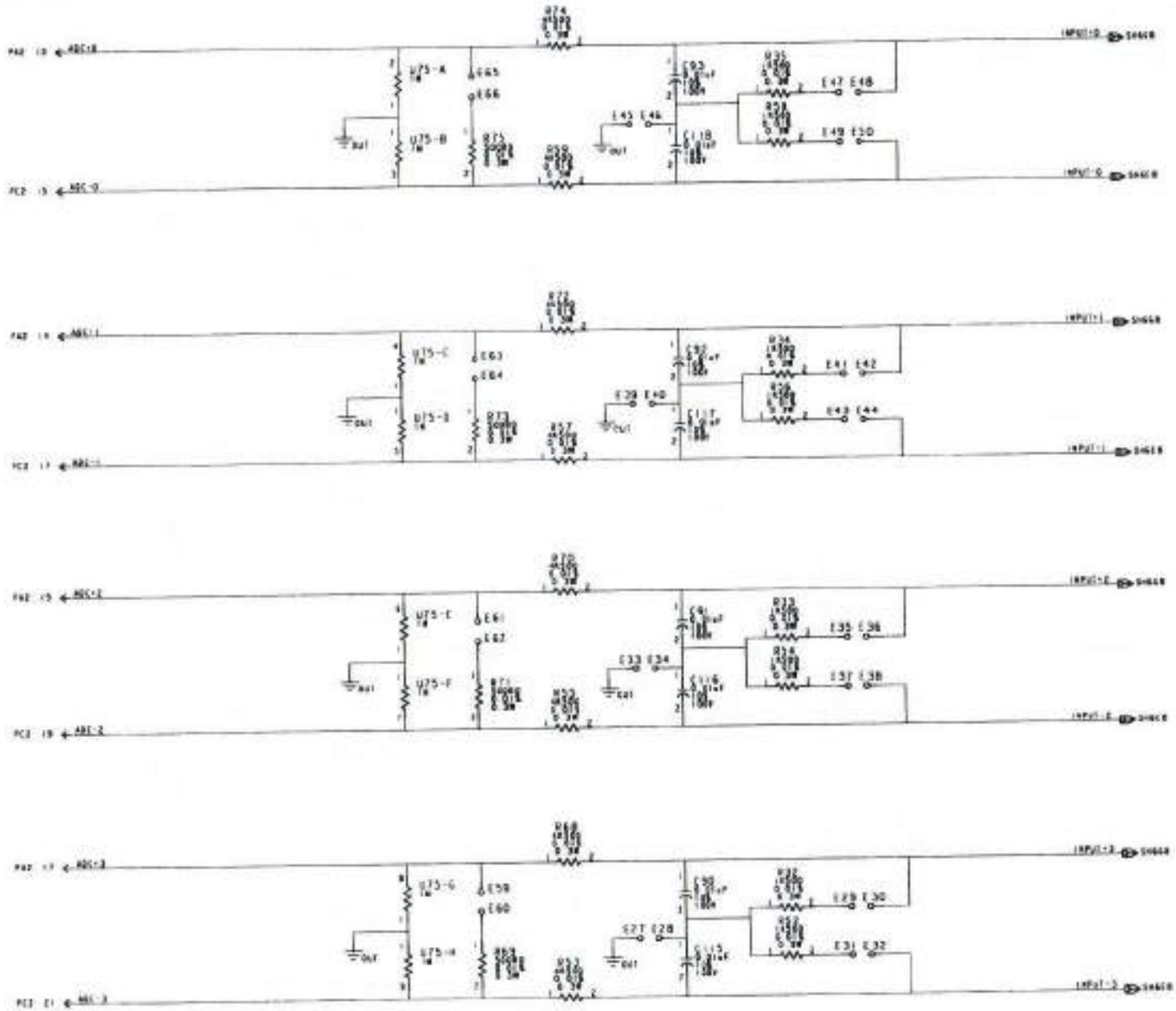




SCHEMATIC DIAGRAM
UNCONFIGURED
DMP-666/SPME-667

41035-004

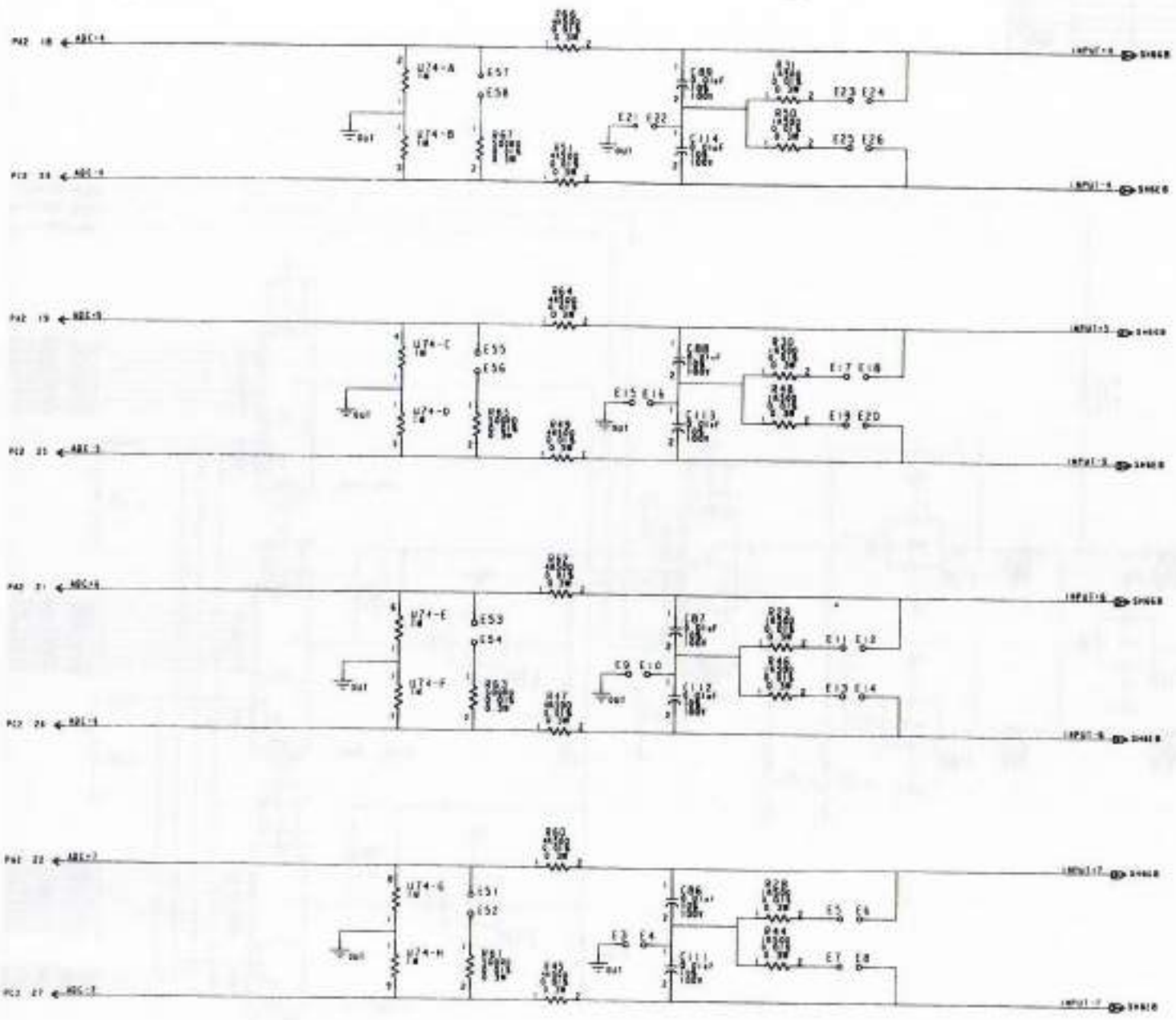

VOLTAGE REFERENCES
SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SME-667
410135-004



INPUT ATTENUATORS AND FILTERS 0 THRU 3

SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SRME-667

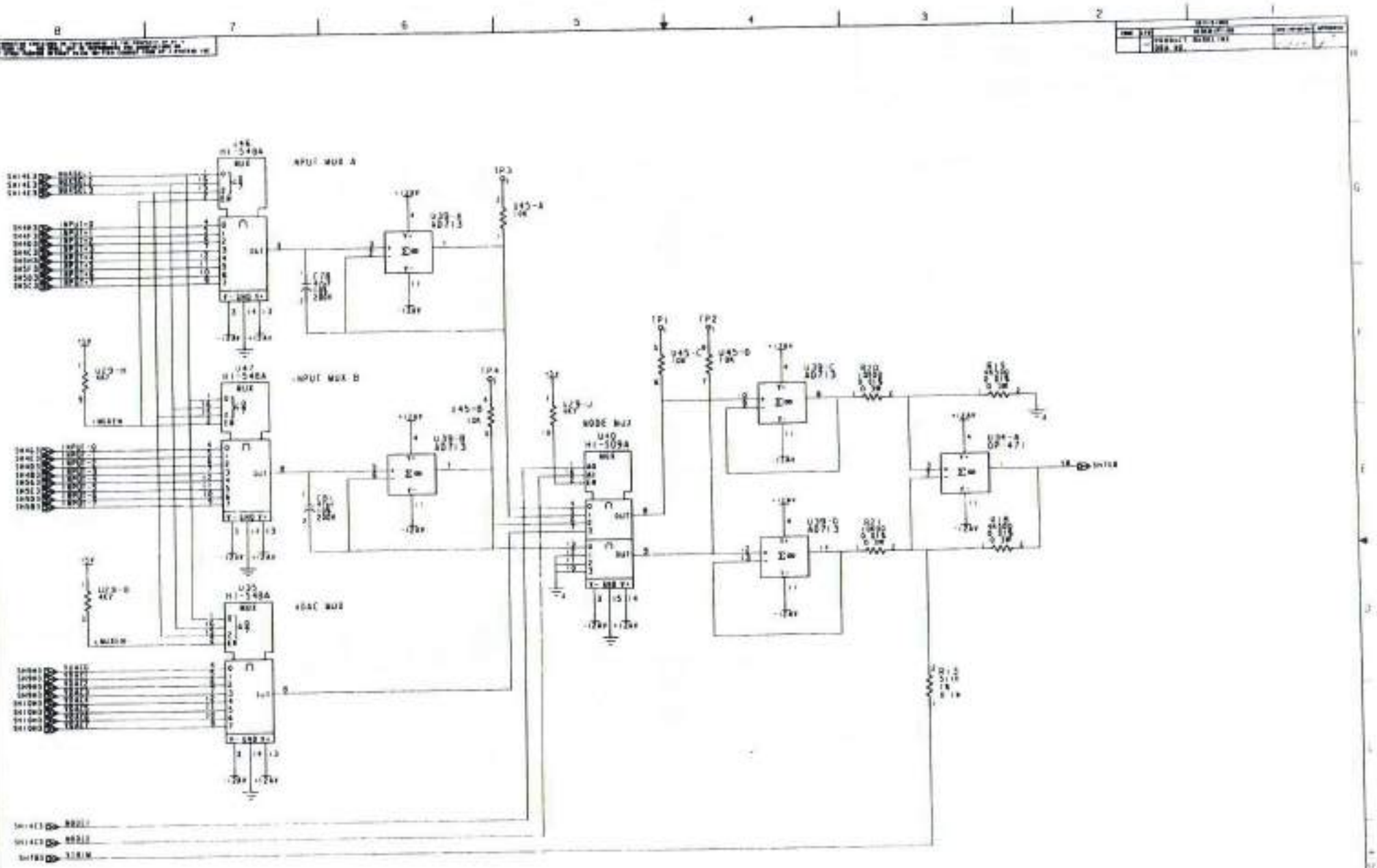
410135-004

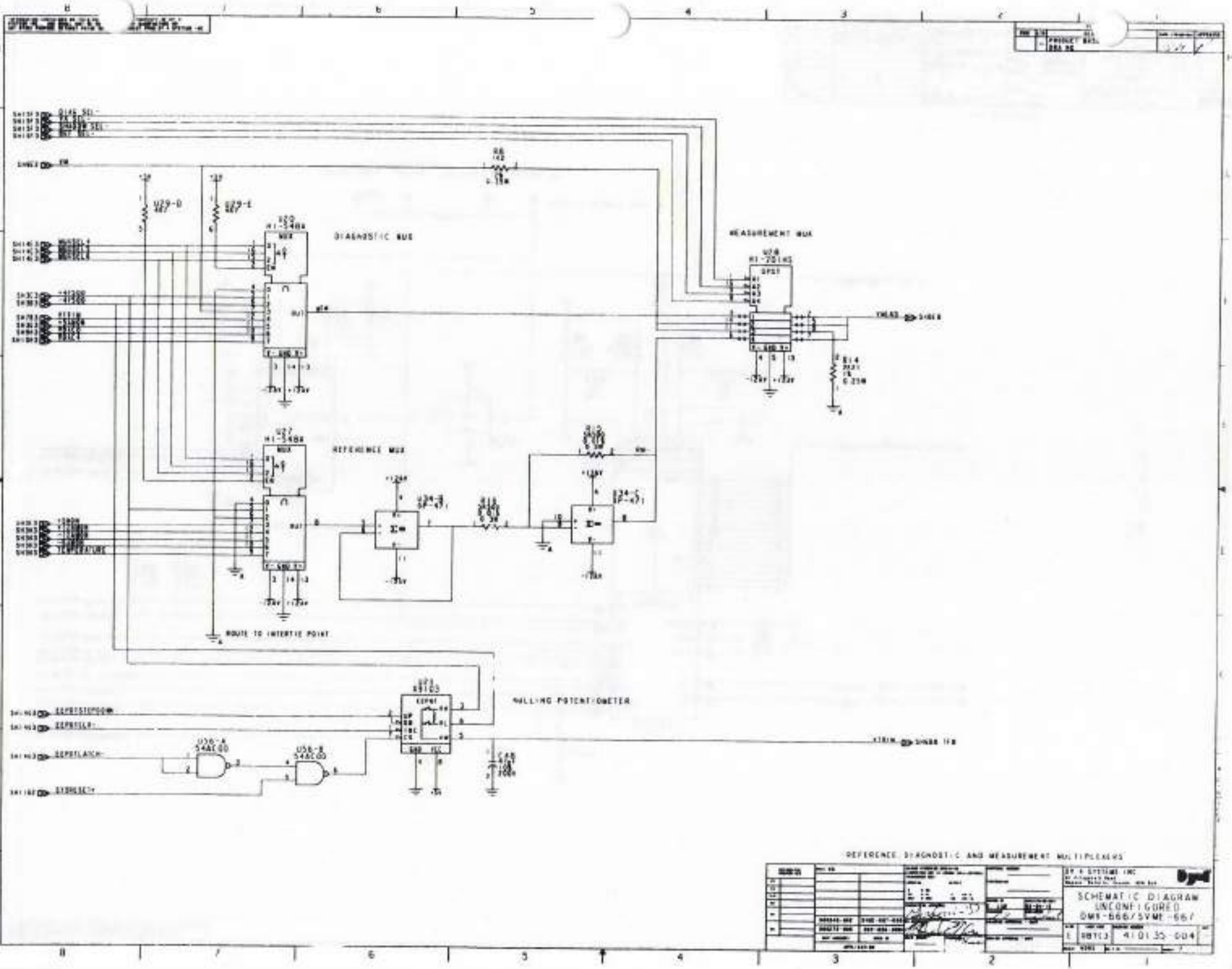


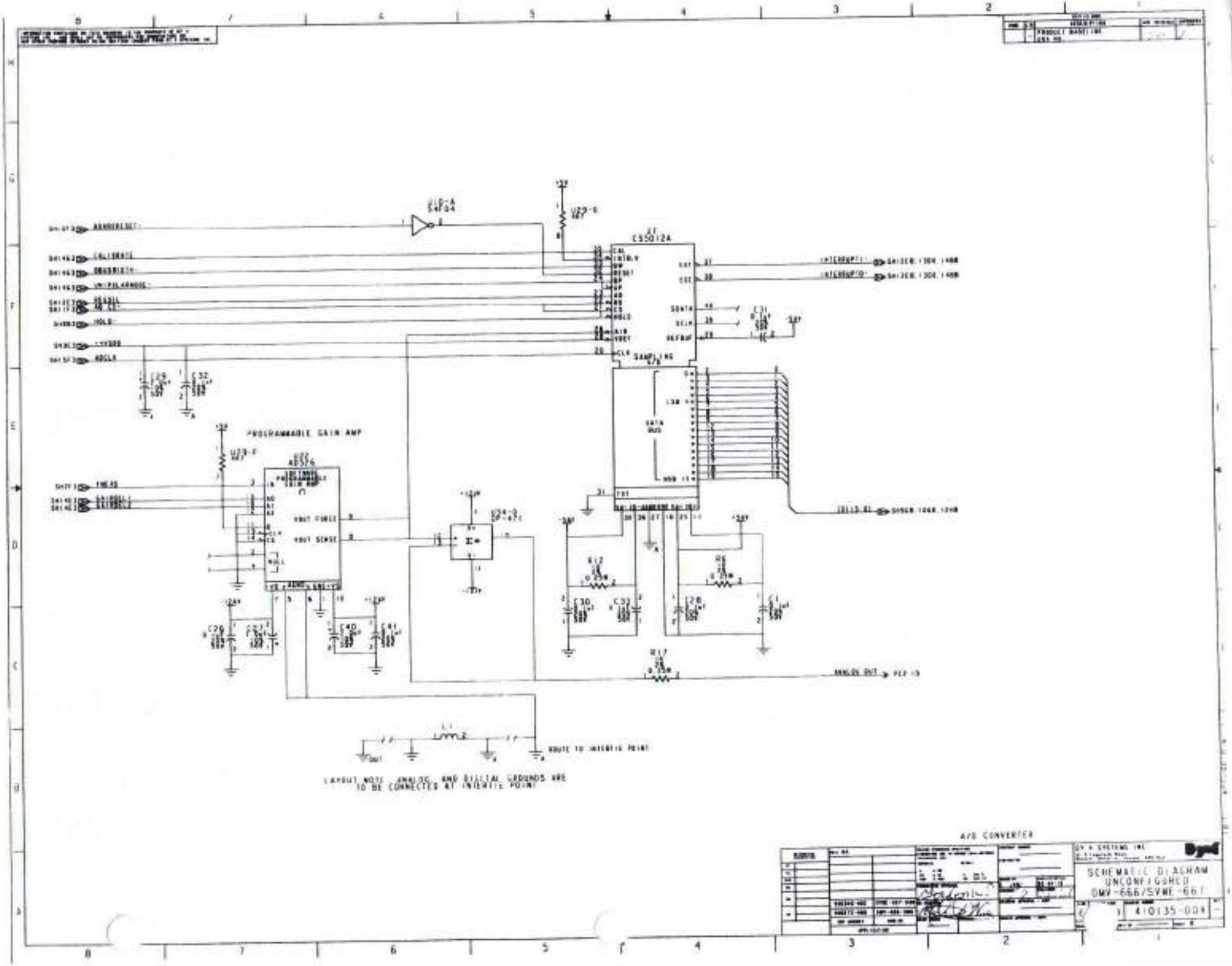
INPUT ATTENUATORS AND FILTERS 4 THRU 7

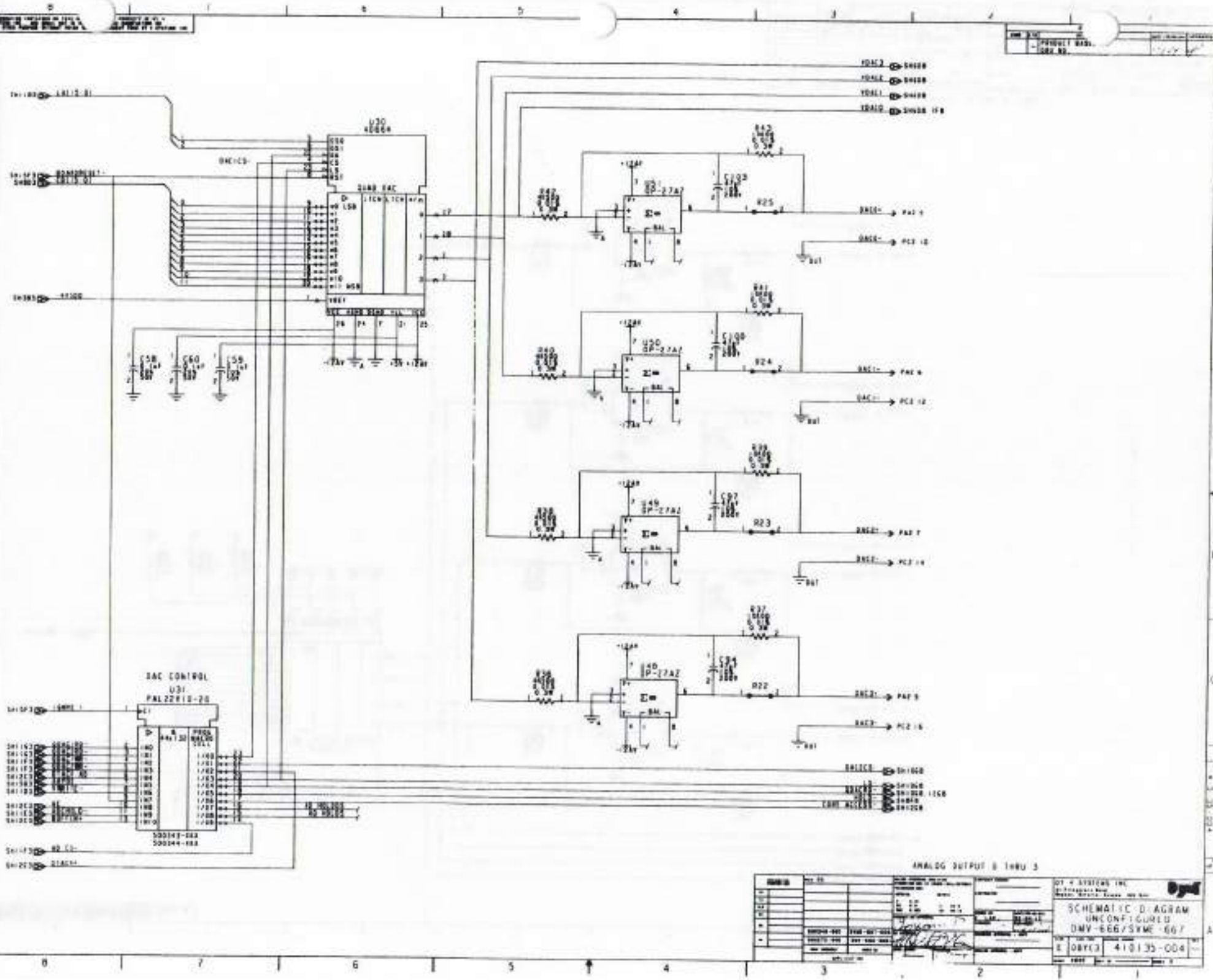
SCHEMATIC DIAGRAM
UNCONFIGURED
DWY-666/SYME-667

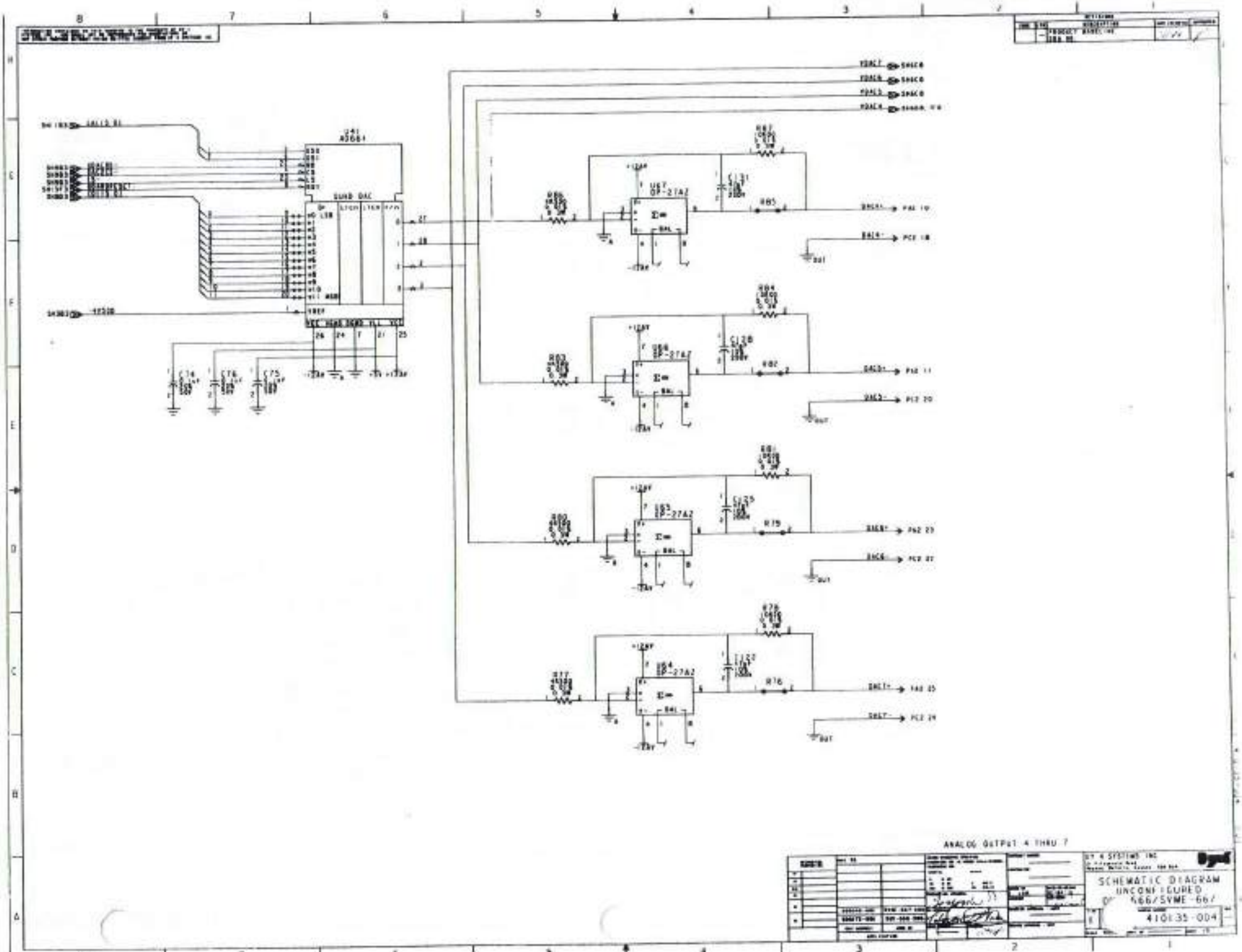
410135-004

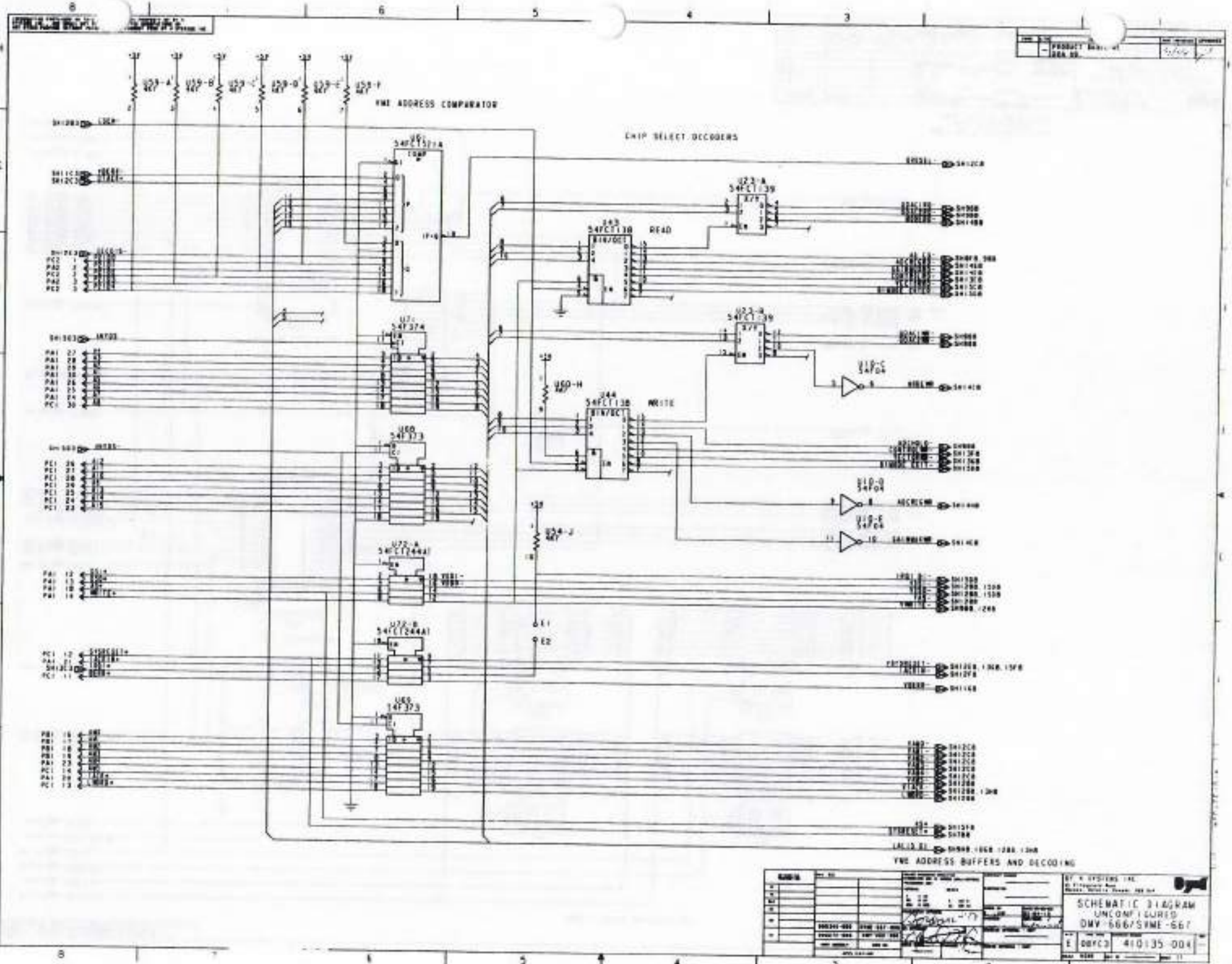

INPUT MUX A
INPUT MUX B
VDAC MUX
MODE MUX
TP1
TP2
TP3
TP4
SW16
SW14
SW13
SW12
SW11
SW10
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
INPUT, VDAC, AND MODE MULTIPLEXERS
SCHEMATIC DIAGRAM
RECONFIGURED
566/SIME-667
4101535-004

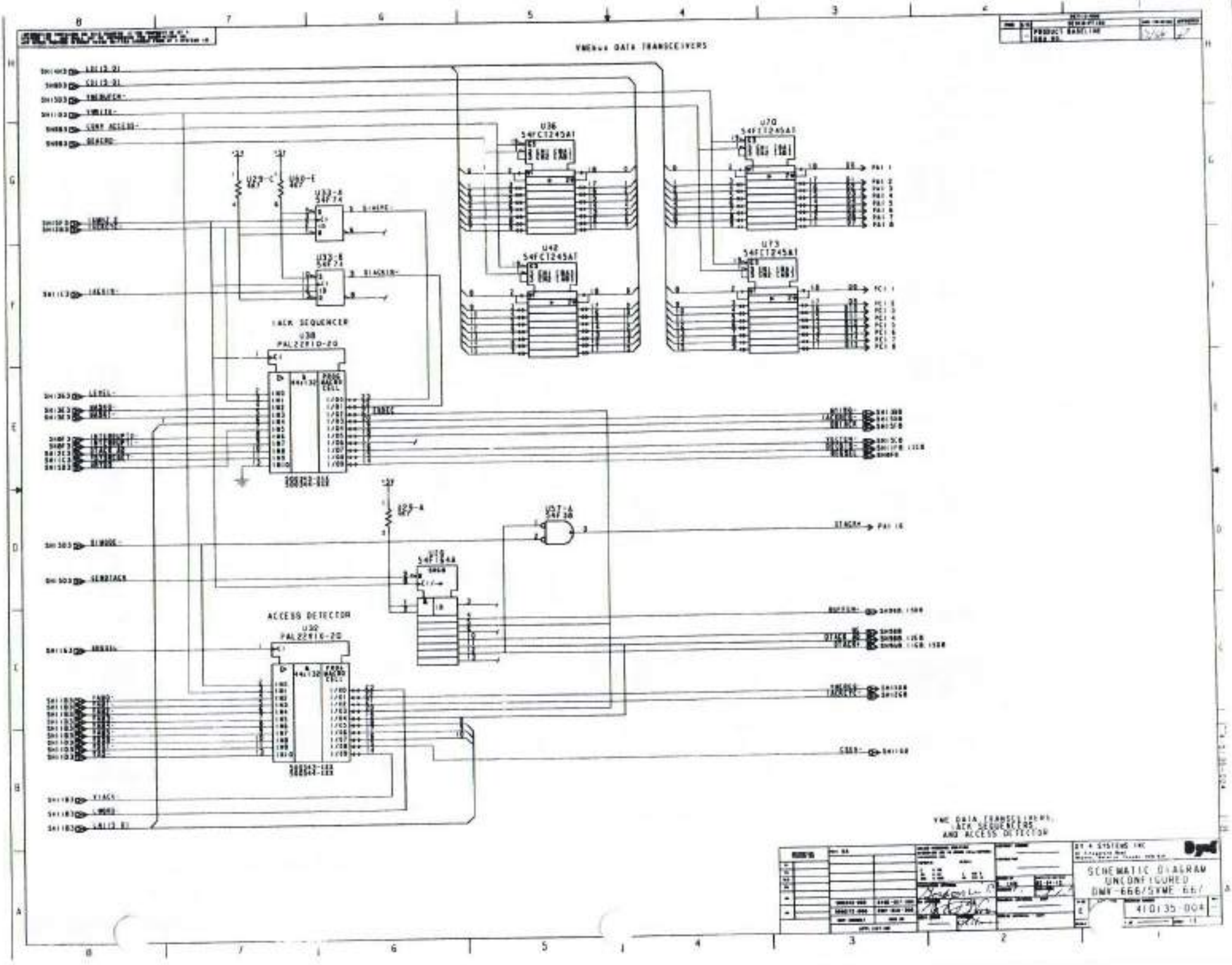

DIAGNOSTIC BUS
MEASUREMENT MUX
REFERENCE MUX
ROUTE TO INERTIA POINT
NULLING POTENTIOMETER
REFERENCE, DIAGNOSTIC AND MEASUREMENT MULTIPLEXERS
SCHEMATIC DIAGRAM
UNCONFIGURED
DMS-668/SVME-667
41 01 35-004

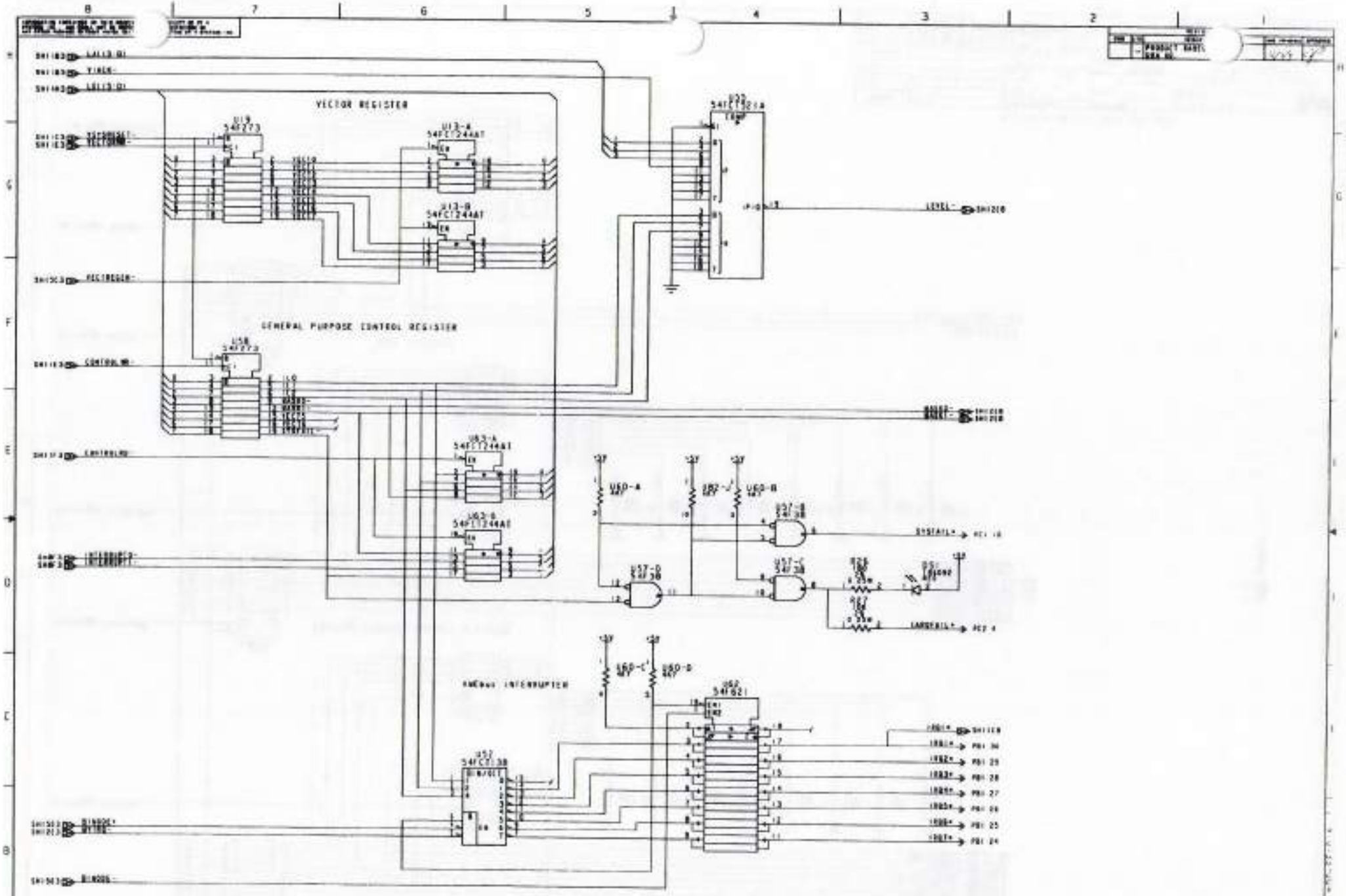

PROGRAMMABLE GAIN AMP
ANALOG INPUT
ROUTE TO CHASSIS POINT
LAYOUT NOTE: ANALOG AND DIGITAL GROUNDS ARE TO BE CONNECTED AT CHASSIS POINT
A/D CONVERTER
SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SVME-661
410135-004


DAC CONTROL
U31
PAL22V10-25
U30
40864
QUAD DAC
U40
OP-27AZ
U41
OP-27AZ
U42
OP-27AZ
U43
OP-27AZ
R22
R23
R24
R25
C91
C92
C93
C94
C58
C60
C59
ANALOG OUTPUT 8 THRU 5
SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SXME-667
410135-004


SCHEMATIC DIAGRAM
UNCONFIGURED
4101435-004
ANALOG OUTPUT 4 THRU 7


VME ADDRESS COMPARATOR
CHIP SELECT DECODERS
VME ADDRESS BUFFERS AND DECODING
SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-566/SVME-667
410135-004

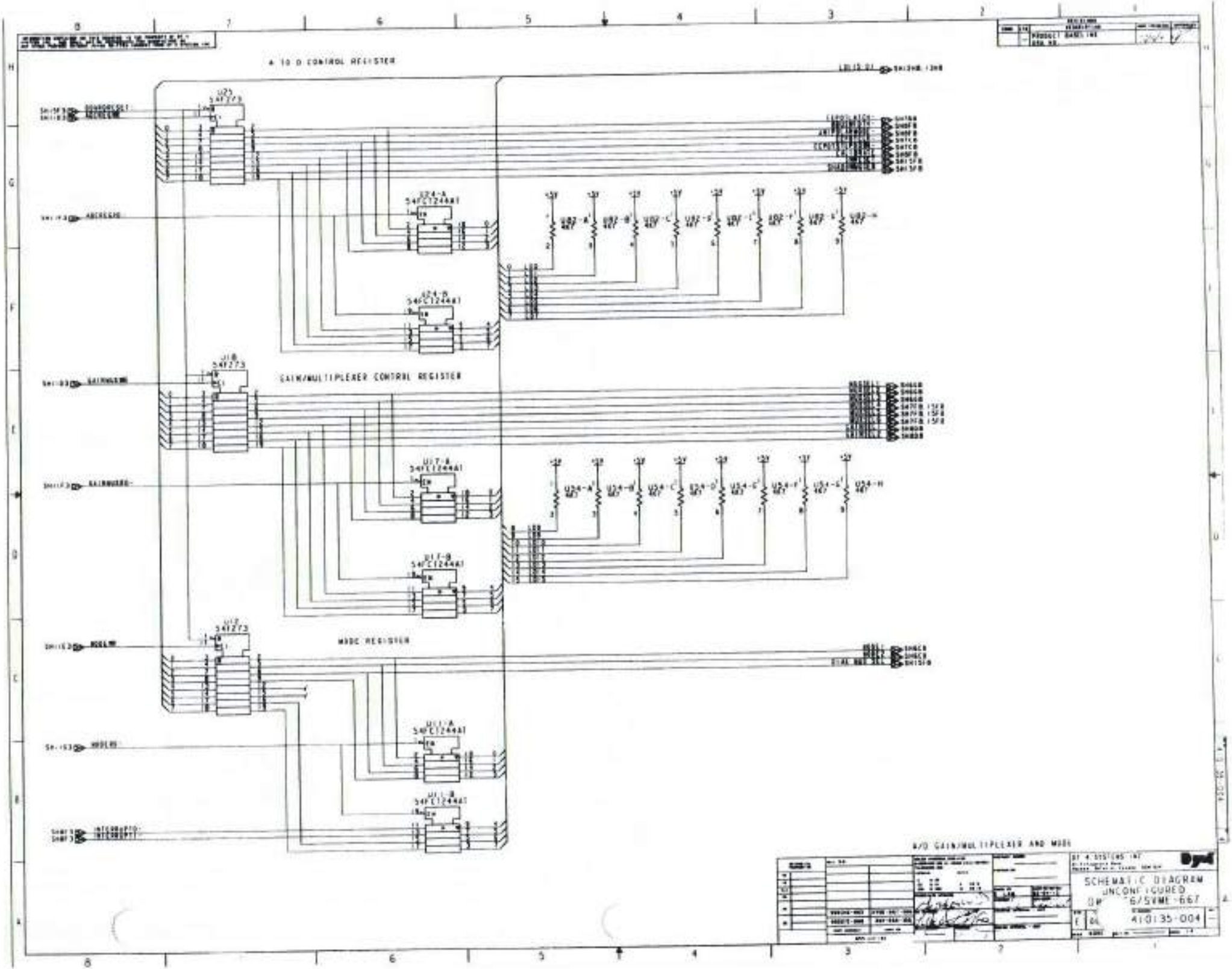

VMEbus DATA TRANSCEIVERS
U36
54FCT245AT
U42
54FCT245AT
U70
54FCT245AT
U73
54FCT245AT
U23-C
U23-E
U23-A
U32-A
54F14
U32-B
54F14
U38
PAL22R10-20
ACK SEQUENCER
U32
PAL22R16-20
ACCESS DETECTOR
U27-A
U18
54FCT646A
VME DATA TRANSCEIVERS,
ACK SEQUENCERS
AND ACCESS DETECTOR
SCHEMATIC DIAGRAM
UNCONFIGURED
DWR-666/SYME 66/
41 0135 004

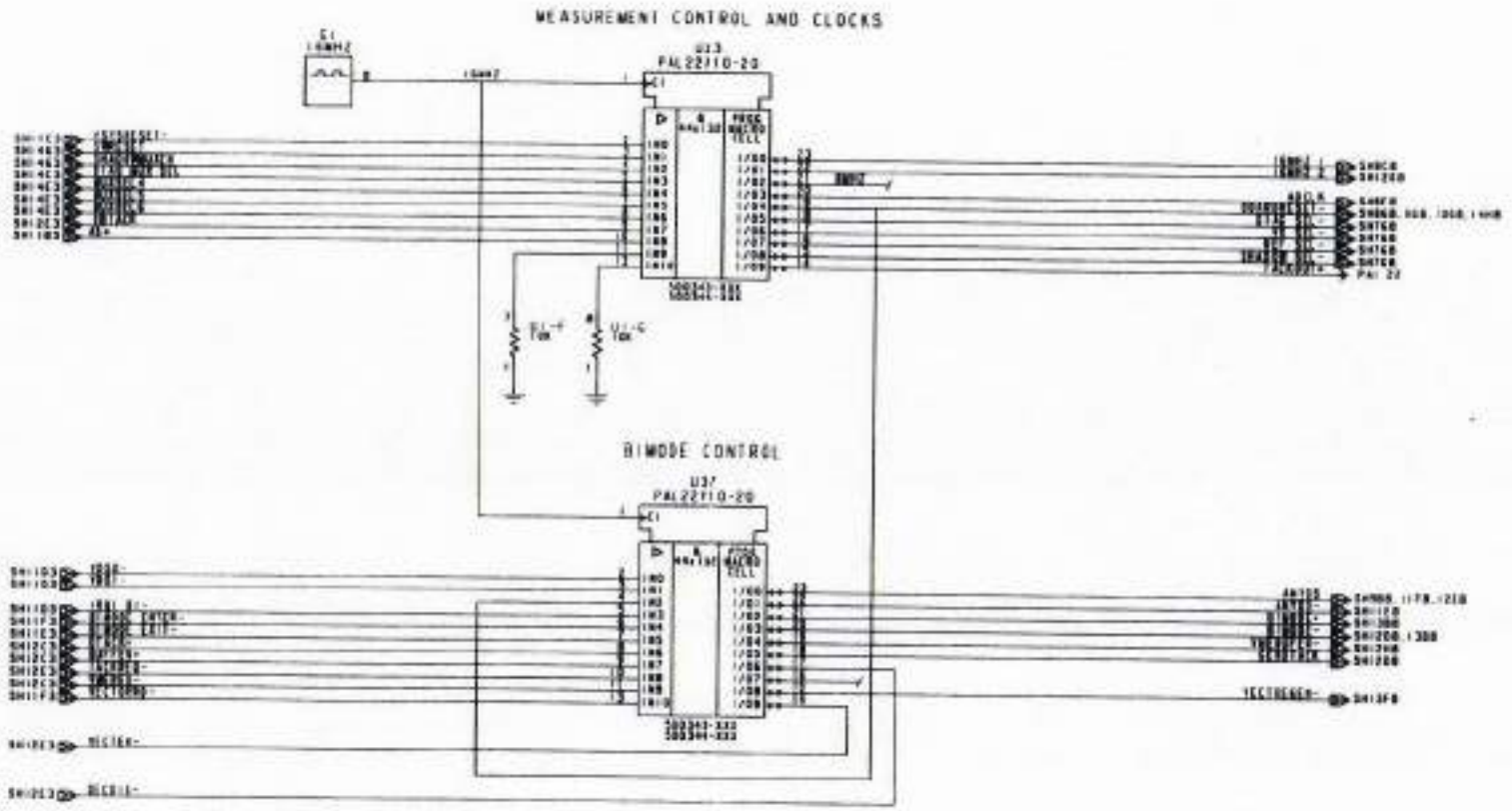


IRQ VECTOR AND CONTROL REGISTERS

SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SYME-667

DRYCO 41 0135-004


A TO D CONTROL REGISTER
GAIN/MULTIPLEXER CONTROL REGISTER
MODE REGISTER
A/D GAIN/MULTIPLEXER AND MODE
SCHEMATIC DIAGRAM
UNCONFIGURED
DP 6/SVME-667
410135-004



MEASUREMENT CONTROL, BIMODE CONTROL AND CLOCKS

DY 4 SYSTEMS INC.

SCHEMATIC DIAGRAM
UNCONFIGURED
DMV-666/SVME-667

SIZE	DWG NO	REV
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