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Find the *Curtiss-Wright / DY-4 / Ixthos IXD7232* at our website: ***Click HERE***

Data Sheet

IXD7232

Dual 21020 with I/O



Real-Time Signal Processing VME Board

- Features
- Performance by Design
- Powerful VME Interface
- I/O Flexibility
- Specifications
- Overview
- Reconfigurable Memory
- Reduced Overhead
- Performance Expandability
- Development Support

Features

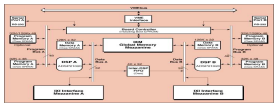
- Two IEEE 32-bit Floating Point ADSP-21020s
- 200 MFLOPS on a Single 6U Board
- High Transfer Rates - over 250 MB/s
- Modular, High-speed I/O via IXI Mezzanines
  - Analog and/or Digital
- Tri-ported Global Memory up to 64MB
- Dual RS-232 Ports Accessible from Front Panel
- Full Featured VMEbus Master/Slave Interface
- Virtually Unlimited Performance Expansion

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- 3MB Local SRAM; Each DSP Supported by:
  - 512 KB Data SRAM (0ws)
  - 960 KB Program SRAM (0ws)

- Comprehensive Software Support:
  - - C, Numeric C, and ADA Compilers
  - - Optimized Function Libraries
  - - Source and Target Debuggers
  - - OS/Host Drivers and Utilities

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Click to View Architecture Diagram

Overview

The IXD7232 is designed to provide the high throughput, application flexibility, and performance required by real-time signal processing applications. Utilizing two ADSP-21020 IEEE floating-point digital signal processor (DSP) chips from Analog Devices, this board can achieve peak processing rates of 200MFLOPS, with sustained rates of 150MFLOPS.

To maximize throughput, the IXD7232 architecture supplies each DSP with complete I/O and memory support. Each DSP has independent banks of 512KB data SRAM and 196KB (expandable to 960KB) of program SRAM. Each DSP can perform data transfers at rates up to 133MB/s, for a combined throughput of 266MB/s. DSPs can be interconnected on/between boards - providing nearly unlimited performance expansion.

A key feature of the IXD7232 is the flexibility provided by its mezzanines. Each board holds two I/O mezzanines (IXI) and a global memory mezzanine (IXM) within a single 6U slot. The large variety of IXI mezzanines allow the user to configure the board for acquiring and processing virtually any type of analog or digital signal. The memory mezzanine provides reconfigurable global memory, allowing board opt-imization for a broad range of algorithms and applications.

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The IXD7232 also provides the user with a powerful A32:D32 master/slave VME interface supporting two DMA channels and BLT. Additional features, such as configurable interrupts, RS-232 ports, timers, and board synchronization, are built into the Board Controller to simplify real-time systems integration and software development efforts.

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Performance by Design

The processing power of the IXD7232 is provided by two 32-bit floating point ADSP-21020s operating at either 25MHz or 33MHz. In one clock cycle each ADSP-21020 can simul-ta-neously perform: two external bus fetches; an ALU operation; a multiply/accumulate; and a shift. All of these operations are directed by a single 48-bit superscalar instruction. Each ADSP-21020 running at 33MHz achieves a peak per-for-mance of 100MFLOPS and sus--tain-ed rates of 75MFLOPS.

The architecture of the IXD7232 addresses the requirements of real-time systems by providing separate support for each DSP. In addition to it's own IXI I/O port, each DSP has its own memory support: 512KB data RAM (128K x 32) and 192KB of program RAM (32K x 48), expandable to 960KB. All prog-ram and data RAM banks are zero-wait state to take advantage of the ADSP-21020's modified Harvard architecture.

Maxiimum performance is obtained from both DSPs since no resource swapping or slaving is done. Processor overhead is minimized by the IXD7232's dedicated board controller, DMA capability and the inherent efficiency of the ADSP-21020.

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Reconfigurable Memory

The IXM memory mezzanine provides a recon-figurable global memory resource between the DSPs and VMEbus, allowing the IXD7232 to be optimized for a wide variety of applications. Tri-ported options include a 128KB SRAM (0ws) mezzanine, expandable to 512KB, and a 4MB DRAM (1-2ws) mezzanine, expandable to 64MB.

Custom memory mezzanines can also be developed to satisfy special application requirements. These mezzanines need not conform to

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the single-slot sizing, providing options for direct access to very large data banks.

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Powerful VME Interface

The IXD7232 VMEbus interface can act as a master on the bus or respond to bus cycles as a slave. With its 32 data bits and block level transfer capability it supports high-speed burst data rates. The board can receive any one of the seven VMEbus interrupts, and can generate an interrupt on any other level; these interrupt levels are user selectable. In addition to the hardware interrupts, two mailbox interrupts are provided. Location Monitor, Read-Modify-Write, and Address Only Cycles are also provided.

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Reduced Overhead

By performing tasks normally done by the processors, the IXD7232 Board Controller reduces overhead. In addition to providing EPROM boot capabilities and bus interface control and coordination, the Board Controller incorporates many functions, including:

DMA
: Two DMA controllers, one for each DSP, move data between the IXM global memory mezzanine and the VMEbus. Unlike conventional configurations, the DSPs on the IXD7232 do not directly access the VMEbus and, therefore, do not incur the associated control and timing overhead.

UARTs (RS-232 & Timers)
: Two UARTs, one for each DSP, provide RS-232 serial ports accessible from the IXD7232 front panel. These UARTs also contain 16-bit timers that can be used to interrupt the DSPs based on system or local events.

Interrupt Generator
: The Board Controller generates three local interrupts to each DSP. These interrupts can be programmed to be sourced from the VMEbus location monitor, either VMEbus mailbox, VMEbus interrupt or error, either DSP's internal timer, the DMAs, or the UARTs. Each source can be independently masked or disabled.

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I/O Flexibility via IXI Mezzanines

Through the use of IXI interface mezzanines, the IXD7232 can be configured to acquire and process virtually any type of analog or digital signal. The IXD7232 provides maximum I/O flexibility by supporting two IXI mezzanines, one for each DSP, within a single 6U slot.

As shown in the figure below, these IXI mezzanines provide a modular front panel signal interface with a standardized host interface capable of supporting data transfers of 133MB/s. Since there are two IXIs, signals can be moved between the front panel and the DSPs at rates over 250MB/s. Once acquired, the IXD7232's high throughput architecture then supports movement of the data between the IXIs, the DSPs, and memory.

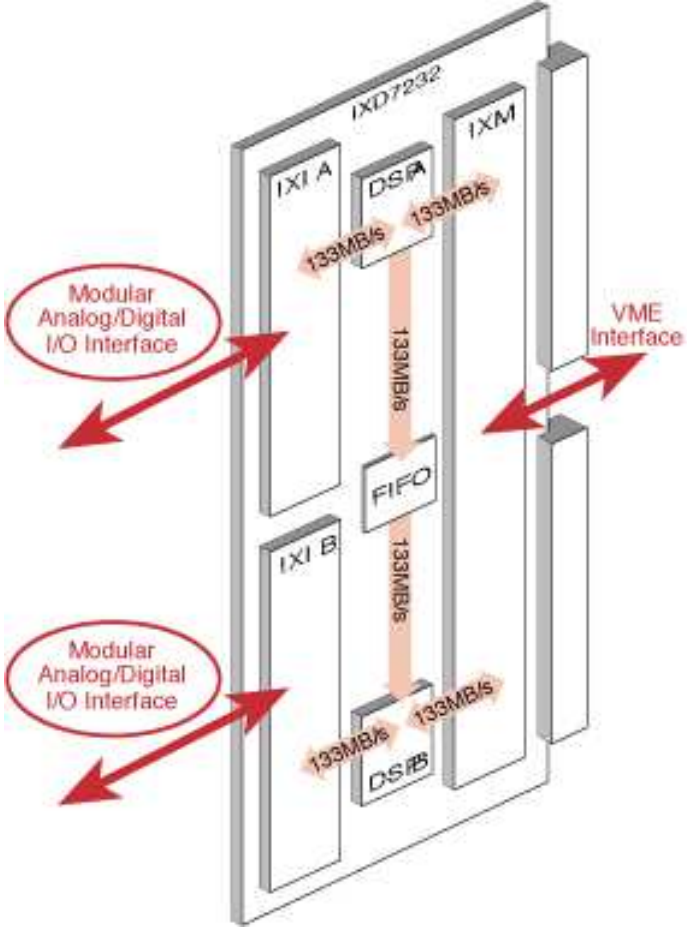
This approach to I/O integration affords the user unprecedented applications flexibility. Signals can be brought in and out each mezzanine independently, in one mezzanine and out the other, or in/out of both simultaneously - all while performing communications over the VMEbus. Signals can also be interfaced to multiple IXIs, allowing processing loads to be spread over multiple IXD7232s.

Ixthos provides a wide range of IXI mezzanines to convert signals from analog-to-digital, digital-to-analog, and/or both, sup-porting a variety of analog interfacing needs. High-speed digital interfacing are also implemented using IXI mezzanines - up to 100MBytes/s with buffering.

In the event that an application requires a signal interface not currently implemented on an IXI mezzanine, Ixthos publishes the *IXI Design Specifications*. The simple interface and open architecture allow users to develop custom IXI mezzanines for the IXD7232 with minimal effort.

The IXI standard host interface consists of 32 data bit, 24 address lines, 11 control signals, digital power, digital ground, 3 analog powers (+5, +12, -12), and analog ground. To provide timing and synchronization, the IXI host interface provides two bi-directional flags and a direct interrupt to its DSP, and two local interrupts to the board controller. These connections are made to the IXD7232 via an elastomeric connector, providing high density, low impedance, and zero insertion force.

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IXD7232 High-Speed Data Paths

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Performance Expandability

Utilizing the high-throughput architecture of the IXD7232, virtually unlimited performance expansion can be realized.

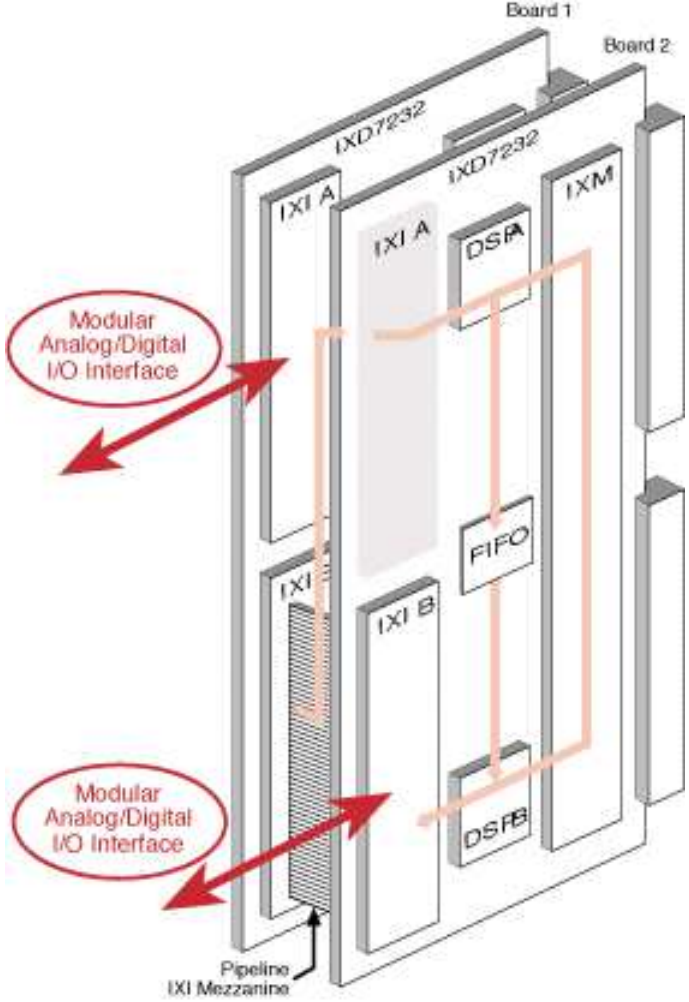
DSPs on the same board are connected through both the inter-DSP FIFO and the IXM global memory mezzanine. The board's 4K x 32 parallel FIFO provides data transfer rates of 133Mbytes/s between DSPs on the same board. Alternatively, the global memory pro-vides a large RAM bank which may be used to share data between DSPs.

Using the high-speed (133MB/s) IXI interface ports, the DSPs on multiple IXD7232s can be interconnected in almost any parallel topology including ring, mesh, cube, and array. A variety of IXI mezzanines are available to support point-to-point digital communications between DSPs, and multi-drop digital IXI mezzanines can be used to create a high-speed front panel 'sub-bus'.

Alternately, a special pipeline IXI mezzanine can be used to interconnect DSPs without interfering with the front panel, VMEbus, or P2 connector. It connects the IXI port of one DSP directly to the IXI port of another DSP on an adjacent board creating either inter-DSP FIFOs or shared SRAM. The pipeline mezzanine makes use of elastomeric connector technology (alternating layers of conducting and non-conducting silicone) to contact electrical pads on the top of one board to pads on the back of an adjacent board. The boards are mechanically fastened together with the pipeline IXI mezzanine in between.

The figure below illustrates a typical data flow (shown in red/pink) for a two board (four processor) pipeline using this interconnect scheme. A signal is received by the IXI A mezzanine on Board 1. It passes from DSP A to DSP B, then out the pipeline mezzanine located in the B IXI position. Connecting the pipeline mezzanine to IXI A pads on the back of Board 2, data then flows to DSP A on the second board and on to DSP B of the same board. The data can then be output using a third IXI mezzanine (as shown), or another pipeline mezzanine may be employed to add an additional board to the pipeline.

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Typical Pipeline Configuration

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Specifications

Processors

Two ADSP-21020s running at 25MHz or 33MHz.

Performance benchmarks of each processor @ 25/33MHz:

75/100MFLOPS Peak; 50/67MFLOPS sustained	
1024-pt complex FFT (radix 4):	0.77/0.58m
1024-pt real FFT (radix 2):	0.45/0.34ms
FIR Filter per Tap (+0.36/0.27µs for 1st):	40.0/30.0 ns
IIR Filter per Biquad (0.24/0.18µs for 1st):	0.16/0.12 µs
Division (y/x):	0.24/0.18 µs
Inverse Square Root:	0.36/0.27 µs

Memory

Each processor has its own dedicated local memory:

Data Memory:	512KB (128K x 32) 0ws SRAM
Program Memory:	192KB (32K x 48) 0ws SRAM
	(expandable to 960KB w/IXP option)
Total SRAM per DSP:	704KB, expandable to 1.47MB

Global memory, accessible to both DSPs and the VMEbus, resides on the IXM memory mezzanine. Options include:

- Tri-ported 0/1ws SRAM (32K x 32, or 128K x 32)
- Tri-ported 2ws DRAM (1M x 32, 4M x 32, or 16M x 32)

Unidirectional 0/1ws FIFO (4K x 32) between DSPs.

Socketed 32KB or 512KB JEDEC Boot EPROM.

External Interfaces

Each DSP has its own dedicated IXI port accessible to an optional interface mezzanine. Accessible from both top and bottom of board. Modular front panel allows signals to be directly interfaced to mezzanines. Each port supports:

- 133MB/s data transfer rates (4Bytes @ 33MHz)
- 32 bits of data; 24 address lines, 11 control signals
- 2 bidirectional flags and a direct interrupt to its DSP
- 2 local interrupts to/from the board controller

Two RS-232 serial ports, accessible via the front panel.

VMEbus Interface

Full-featured A32:D32 Master/Slave VMEbus interface supports:

2 Independent DMAs (1 for each processor)

1 of 7 VMEbus interrupt levels, and 2 mailbox interrupts

Block Level Transfers (D32:BLT)

Location Monitor; Address Only Cycle (MA32:ADO)

Read-Modify-Write (MD08:RMW)

Physical/Electrical

Standard 6U Eurocard, 160mm x 233mm

Typical Power: 12.5W

Operating Temperature: 0°C to 50°(0°to 70°optional)

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Development Support

The IXD7232 is supported by a comprehensive set of software development and debugging tools.

The ADI21KBUN, development software for the ADSP-21020, available for both PC and Sun/SPARC environments, provides an optimizing ANSI C compiler (GNU) with Numeric C extensions, along with an assembler, linker, librarian, simulator, and a C source-level debugger. Extensive C-callable libraries are also provided, including 150 optimized math/scientific functions, transfer routines (VME, IXI, RS-232), and board control and set-up routines.

Target debugging on the IXD7232 can be performed in three ways. In-circuit emulation is provided by the EZ-ICE emulator, which connects to the ADSP-21020 JTAG test port. Ixthos also provides two non-intrusive debug monitors for the IXD7232: IXDmon21k for single DSP debugging via the RS-232 ports and a PC host, and IXDbug21k for simultaneous debugging of multiple DSPs via a VMEbus host.

Host OS support for the IXD7232 includes drivers, loaders, libraries, and utilities. OS support is available for Solaris, LynxOS, HP-RT, VxWorks, OS-9, DOS, and others.

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The IXD7232 is also supported by a number of third-party vendors. Algorithm development tools are available from Mentor, Momentum Data Systems, and Hyperception. An ADA compiler is available from Meridian. In addition, both the SPOX DSP operating system from Spectron Microsystems, and the Virtuoso real-time multiprocessing kernal from Intelligent Systems International, are ported to the IXD7232.



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