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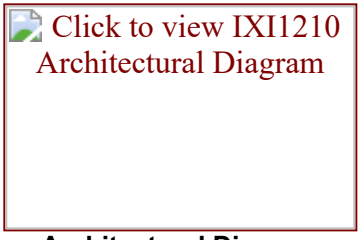
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IXI1210

12-bit, 10MHz, A/D



Board Photo



Architectural Diagram

Features

- 12-bit 10MHz A/D Conversion
  - FIFO Buffer, up to 64K Depth
  - 72 dB Spurious-free Dynamic Range
  - ±1V Input Range, Termination selectableFlexible
- Acquisition
  - Control
  - Internal/External Clock Source

General Description

The IXI1210 is a standard IXI interface mezzanine board designed for use with IXI compatible baseboards, such as the IXD and IXZ families of Signal Processing Boards. The board consists of a 12-bit, 10MHz analog-to-digital converter (ADC), two banks of fast FIFO buffers, and an acquisition controller and associated hardware. The IXI1210 is optimized for high-speed data acquisition with the ability to do snapshot acquisition. Data and external clock inputs are accessed via SMA front panel connections.

The ADC is an integrated monolithic converter (Analog Devices AD872) which can digitize at rates up to 10 MHz while maintaining a high signal-to-noise plus distortion ratio (65dB), as well as a large spurious-free dynamic range (72dB). Converted data is in two's complement format, left justified in the 32-bit field. The ADC also generates an Out Of Range indicator when the analog voltage is not within the ±1V range. A jumper allows this signal to be passed to the host interface on bit 16 of each 32-bit data word; it can be used in conjunction with the MSB to determine low or high overflow.

The on-board buffer consists of two cascaded banks of high-speed asynchronous (15ns access) FIFOs. One bank of FIFOs is required for operation, with the configuration being a 4Kx12 buffer. Using both banks of FIFOs, the buffer can currently be expanded up to a 64Kx12 depth. FIFO depths of 8Kx12 and 32Kx12 are also available.

The acquisition controller provides support for periodic acquisitions. When triggered by the baseboard or external trigger, the ADC is clocked until the buffer is filled. Once the FIFO's full flag is activated, the acquisition controller disables the sample rate clock until the buffer is emptied and another trigger is received.

The source of the sample rate clock source is jumper selectable between an on-board crystal oscillator and an external SMA front panel clock input (to acquire data synchronously with a local time base). The standard 10MHz on-board oscillator is socketed to allow field-replacement and accepts most half-size (8-pin DIP) packages.

The IXI family of interface mezzanines complies with the IXI Design Specifications published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power & ground, 3 analog powers (+5, +12, -12) & analog ground. These connections to the baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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