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IXI1241 Mezzanine

Quad 12-bit, 1.25 MHz A/D Converter

View Photo of IXI1241

Board Photo

View Architectural Diagram of IXI1241

Architectural Diagram

Features

- Quad 12-bit, 1.25MHz ADC
- Simultaneous Sampling - cascadable up to 32 channels
- FIFO Buffering, up to 32K x 12
- Unipolar or Bipolar Operation
- 70dB Signal-to-Noise Ratio
- Flexible Acquisition Control
- Internal/External Clock Source

General Description

The IXI1241 is a standard IXI interface mezzanine board designed for use with IXI compatible baseboards, such as the IXD and IXZ families of Signal Processing boards. The board consists of four 12-bit 1.25 MHz analog-to-digital converters (ADCs), a fast FIFO buffer, an acquisition controller and associated hardware. The IXI1241 is optimized for high speed simultaneous conversion of four analog channels, and provides versatile acquisition control. Four analog signal inputs and the external clock I/O are accessed via SMA front panel connections.

The ADCs are integrated monolithic converters (Analog Devices AD1671) which sample at rates up to 1.25MHz with very low aperture jitter, while maintaining a high SNR. Conversion results from the simultaneously sampled four channels are packed into a FIFO buffer which is read by the host as a 12-bit output word with optional tag bits (a channel marker and out-of-range bit).

The on-board FIFO buffer consists of a bank of high-speed (15ns access) asynchronous FIFOs. The standard configuration is a 4K deep buffer. The FIFOs may be expanded to a 32K depth.

The acquisition controller provides support for periodic, event-triggered, or continuous sampling (as long as the host continuously empties the buffer during the acquisition). The acquisition controller can be triggered by the host. When triggered, the IXI1241 stores converted data in the buffer until the FIFO is filled. The FIFO full flag or half-full flag may be used to generate a host interrupt. A host flag indicates the FIFO empty condition. The conversions may be halted at any time by the host.

The sample rate clock source is jumper selectable between an on-board source (crystal oscillator or host timer), and an external SMA front panel input (to sample synchronously with a local time base). When the converters are running off an on-board source, the external clock connector may be used as an output to drive the external clock inputs of up to 7 other IXI1241 boards, providing simultaneous sampling of up to 32 channels. The standard 5MHz on-board oscillator operates at 4X the convert frequency, and is socketed.

The IXI family of interface mezzanines complies with the IXI Design Specifications published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power & ground, 3 analog powers (+5, +12, -12) & analog ground. These connections to the baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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