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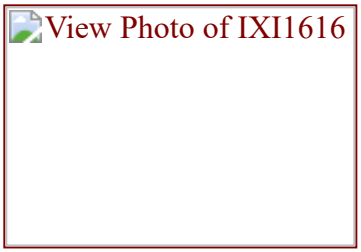
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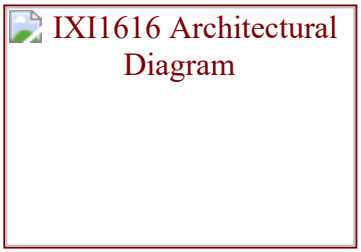
IXI1616

16-Channel, 16-Bit, 200kHz A/D Converter





Board Photo



Architectural Diagram

Features

- Sixteen 16-bit, 200kHz, A/D converters
- One or two serial TDM interfaces
- Up to 16 channels per serial stream
- Sampling rates from 10kHz - 200kHz
- Internal or external clock source
- Selectable digitization rate divider
- Analog bandwidth = 1.0MHz (full scale)
- Simultaneous sampling

General Description

The IXI1616 is a standard IXI2 interface mezzanine board designed for use with the IXI2 or Super IXI (IXI-S) compatible IXZ family of signal processing boards. The board consists of sixteen analog-to-digital (A/D) converter channels, each with 16-bits of resolution, parallel to serial shift registers, and a controller. The front panel IDC-style connector provides the analog inputs to the A/D circuitry, as well as clock, trigger, and auxiliary inputs.

Each A/D channel of the IXI1616 has a full-scale input bandwidth of approximately 1MHz. Inputs are bipolar with a full-scale amplitude of 20Vp-p (+/-10V). The IXI1616 can operate at conversion rates from 10 to 200kHz. Inputs are sampled on the rising edge of every ADC conversion clock cycle. The input conversion range is +/-10V, or 20Vp-p. The 16-bit digital output data is updated toward the end of every conversion cycle. When the A/D channel is digitizing, the 16-bit digital outputs are 3-state to decrease digital noise coupling into the analog inputs. Data is clocked into the parallel-to-serial formatter and then shifted out after the end of the conversion cycle.

The IXI1616 controller generates the digitization rate and timing for all serial port signals from the on-board crystal or from the external clock input. The controller also generates the serial port frame sync and clock signals as well as buffering the serial port data out. When all 16 channels are output on a single serial port, the controller extends the frame sync period to allow all channels of the data to be passed in each frame.

Digitization can be controlled by the combination of the IOFLAG0 and IOFLAG1 signals, or by an external trigger source, TRIGGER. The external trigger can be pulsed to trigger individual conversions or held high to enable continuous digitization. A synchronous convert clock is provided to each A/D Converter, either from the on-board crystal oscillator, or from the external clock source. The external clock source is selected by shunting jumper JM5 and is expected to be a TTL level.

The IXI family of interface mezzanines complies with the IXI Design Specifications published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power and ground, three analog powers (+5, +12, -12) and analog ground. These connections to the IXZ baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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