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IXI32G

General Purpose Digital Interface

adilogo.gif (1914 bytes)

Photo of IXI32G

Board Photo

Click to view IXI32G Architectural Diagram

Architecture Diagram

Features

- 50MBytes/sec Throughput
- Zero Wait-state Host Access
- Output Readback Capability
- Direction Programmable
- Separate Input & Output Data Latches
- Flexible Handshaking and Processor Interface

General Description

The IXI32G is a standard IXI interface mezzanine board designed for use with IXI compatible baseboards, such as the IXD and IXZ families of Signal Processing Boards. The board consists of a set of input and output latches which can pass 32-bit TTL data bidirectionally between the host processor board and the front panel connector. This interface supports zero wait state access from the host processor (@40MHz). The simplicity of both the electrical and mechanical interfaces make the IXI32G useful for digital control or general purpose I/O. A flexible strobe configuration allows several options for handshaking, such as single ended, differential and memory-access strobing. Transmit strobes can be generated using the host interrupts, flags, or write signal. When receiving, strobes can come from the front panel or be generated from the host read signal or timer interrupts. Multidrop configurations are supported up to 10 nodes with removable Thevenin terminations on all signals.

The IXI interface to the host processor on the baseboard is also configurable to allow varied use of the host flags and interrupts. The IOINT line may be used as a data receive interrupt or an output buffer empty interrupt. The TIMINT0 line may also be usedas an output buffer empty interrupt. The IOFLAG1 line may be used to tell the host when the output buffer is empty or when the input buffer is empty. The IOACK is used to restrict host access to the I/O buffers, and may be driven when a write is pending and the output has not been strobed.

The direction of the interface is programmable from the host processor via a flag line, allowing the host to dynamically change transfer direction. When transmitting, input registers may be used as a readback path to sense the output bus.

The IXI32G comes with a standard 40-pin IDC connector front panel. Standard ribbon cable may be used for passing data over short distances, or shielded ribbon cable is accommodated for longer lines or noisy environments.

The IXI family of interface mezzanines complies with the IXI Design Specifications published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power & ground, 3 analog powers (+5, +12, -12) & analog ground. These connections to the baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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