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IXI8250

Dual 8-bit 50 MHz A/D

View Photo of IXI8250

Board Photo

IXI8250 Architectural Diagram

Architectural Diagram

Features

- Dual 8-bit, 50MHz ADC
- Simultaneous Sampling
- FIFO Buffer, 8K Samples
- Fast (16ns) Access from Host
- 47dB Signal-to-Noise Ratio
- Flexible Acquisition Control
- Internal/External Clock Source

General Description

The IXI8250 is a standard IXI interface mezzanine board designed for use with IXI compatible baseboards, such as the IXD and IXZ families of Signal Processing Boards. The board consists of a 2 channel, 8-bit, 50 MHz analog-to-digital converter (ADC), two banks of fast FIFO buffers, an acquisition controller, and associated hardware. The IXI8250 is optimized for high speed data acquisition with a versatile acquisition controller. Analog signals, trigger, and external clock inputs are provided on front panel SMA connectors.

The ADC is an integrated monolithic converter (Analog Devices AD9058) which can simultaneously sample two signals at rates up to 50MHz while maintaining a high SNR.

The on-board FIFO buffer consists of a parallel 32-bit wide bank of high-speed (10ns access) synchronous FIFOs. Two samples from each channel are packed to create a single 32-bit output word from the FIFO bank (four 8-bit results, two from each channel) to the host. Thus, reading the IXI8250 at 25MHz or greater will prevent the FIFO buffer from becoming full, providing a 100Msample/sec throughput. The standard FIFO configuration is 2K x 32 (8K samples).

The acquisition controller provides support for periodic or event-triggered acquisitions. The acquisition controller can be triggered by the host processor, a host timer, or an external trigger signal. When triggered, the acquisition controller allows the converted data to be stored until the FIFO buffer is filled. Once the FIFO's full flag is activated, the acquisition controller may disable the FIFO input until the buffer is emptied. The acquisition controller may then be retriggered by either the baseboard or the external trigger input. The IXI8250 may also be used in a mode which captures pretrigger data so that the acquisition window is centered around the trigger.

The source of the sample rate clock is jumper selectable between an on-board crystal oscillator and an external SMA front panel clock input (to acquire data synchronously with a local time base). The standard 50MHz on-board oscillator is socketed to allow field replacement and accepts most half-size DIP packages.

The IXI family of interface mezzanines comply with the IXI Design Specifications published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power & ground, 3 analog powers (+5, +12, -12) & analog ground. These connections to the baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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