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IXIFPDP

Double Buffered Front Panel Data Port (FPDP™) Interface

Click to view IXIFPDP Architectural Diagram

Architecture Diagram

Features

- 32-bit Single Ended TTL Port: Multidrop Bi-Directional Interface
- Throughput 80 MByte/s
- Compatible with Industry Standard Front Panel Data Port (FPDP™)
- Ideal for Interfacing to a wide variety of COTS VME boards
- 2 Banks of SRAM, 128K x 32 bits for continuous I/O



General Description

The IXIFPDP is a standard IXI interface mezzanine designed for use with IXI compatible baseboards, such as the IXZ and IXD families of digital signal processing boards. The board supports the Front Panel Data Port (FPDP™) standard for 32-bit data transfers at a maximum of 20 MHz for an aggregate transfer rate of 80 MBytes/s. The combination of high speed and a flexible, industry standard I/O make this mezzanine an ideal interface to a wide variety of off-the-shelf data acquisition boards.
The double banks of 128K x 32 memory create a powerful swing buffer architecture, which enables continuous processing of data streams. Incoming data frames may be stored in one bank of memory while the baseboard processor directly accesses a previous frame, which was stored in the other bank. This 'ping pong' buffer scheme can be programmed to happen automatically, allowing continuous data flow.

The IXIFPDP supports multidrop configurations of up to 10 nodes. The board's features are programmable through registers, flags, and the board's current interrupts. Status is reported to the host DSP through registers. For example, the IOINT line is an interrupt tied to a full buffer condition. The IOFLAG1 line is used to tell the host DSP which bank of memory is accessible. The direction of the FPDP™ interface is programmable via a register. The IXIFPDP comes with a standard 80-pin connector on the front panel. Standard ribbon cable may be used for passing data over short distances or shielded ribbon cable for longer lines or noisy environments.

The IXI family of interface mezzanines complies with the *IXI Design Specifications* published by Ixthos. The electrical interface to an IXI mezzanine consists of 73 signals: 32 data lines, 24 address lines, 11 control lines, digital power and ground, three analog powers (+5, +12, -12) and analog ground. These connections to the IXZ baseboard are made via an elastomeric connector that provides a high density, low resistance, zero insertion force connection. Standard board separations of 0.125" to 0.375" are low enough to ensure a single-slot solution for most applications while providing enough room for double-sided population.

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