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Data Sheet

IXZ16

16 SHARC with I/O

Real-Time MultiProcessing VME Board

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Features

- 16 SHARCs™ (ADSP-21060); 4 Clusters of 4
- 1.9 GFLOPS on a Single 6U Board
- 16 off-board SHARC™ IXLinks (40MB/s each)
- Modular, High-speed I/O via 2 IXI Mezzanines
- Flexible memory structures support a total of 256MB DRAM, 8MB SRAM
  - local memory up to 2MB
  - modular global memory up to 128MB
  - additional shared memory up to 128MB
- MultiProcessor Resource (MPR)
  Provides fast, deterministic HW semaphores, signals, and states between all SHARCs™ in system
- P2 Personality Module for flexible interconnect
- Full Featured VME64 Master/Slave Interface
- Compatible & Scalable with IXZ Family Boards
- Comprehensive Multiprocessing Software:
  - GEDAE™ graphical development & analysis tool
  - Multiprocessing Applications Interface (API)
  - OS/Host Drivers, Standard I/O and Utilities
  - Run-time environment
  - Optimized C-callable Function Libraries
  - Multiprocessor Target Debuggers
  - Optimizing ANSI C Compiler
  - Multitasking DSP O/S support

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Overview

The IXZ16 is the powerhouse of the IXZ Family of VME products. Sixteen SHARC DSPs, providing up to 1.9 GFLOPS of

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peak processing power, combined with architectural flexibility, I/O, scalability, and comprehensive multiprocessing software tools, make the IXZ16 an excellent solution for either integrated, stand-alone, or multi-board DSP systems.

The IXZ16's processors are arranged in 4 clusters of 4 SHARCs. Ixthos worked with Analog Devices, Inc. to develop the advanced packaging required to achieve the processing density for the IXZ16. The four SHARCs in each cluster fit into a multi-chip module (MCM) that uses advanced ball grid array (BGA) technology.

The internal memory of the SHARC is augmented by local, global, and shared memories. The local memory can be populated with up to 2MB of 0ws SRAM per cluster. The global memory (IXQ1) is accessible to all four clusters in the VME and can be populated with up to 128MB of DRAM. In addition, this modular global memory site provides fast auxiliary dual-ported VME memory. The shared memory (IXQ2) is accessible to 2 of the 4 clusters and can provide an additional 128MB of DRAM. The global DRAM memory is accessible to all four clusters and the VME.

An integrated Board Controller decouples the SHARC clusters from the VME and associated hosts to reduce overhead and free the DSPs to process real-time data. The IXZ16 also boasts a unique MultiProcessor Resource (MPR) that tremendously facilitates the control and coordination of large numbers of SHARC clusters over multiple IXZ boards.

Unprecedented off-board interconnectivity and I/O flexibility are key features of the IXZ16. Each board holds 2 IXI I/O mezzanines in a single 6U slot, allowing the user to configure the board for acquiring and processing virtually any type of analog or digital signal. The 16 off-board SHARC IXLink ports provide up to 640MB/s of inter-processor bandwidth for building multiprocessor systems. The personality module provides for a flexible interconnect to the P2.

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Innovative MCM Packaging

The IXZ16 packs a wallop of computing punch in a single VME slot because Ixthos has developed a dense, proprietary package for the SHARC processors. Four SHARCs in each cluster fit into a MCM that uses advanced ball grid array (BGA) technology to minimize size and reduce ground bounce and inductive loops between signal pins. The small size of each MCM makes it possible to attach all SHARC MCMs directly to the baseboard, which in turn reduces susceptibility to vibration and electromagnetic interference (EMI). The MCM package also provides efficient cooling.

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Flexible Global Memory

The IXZ16 supports a flexible menu of both globally shared DRAM and dedicated SRAM memory options. Each SHARC contains up to 4Mbits of on-chip memory. Each cluster may have up to 512KWords of 0ws dedicated cluster memory. The 4 SHARC clusters and VME share a bank of up to 32 MWords (128MB) of global DRAM (IXQ1). There is also auxiliary VME memory on IXQ1 to ease memory bottlenecks between the clusters and VME. The C and D clusters have an additional memory or I/O interconnect (IXQ2). These various memory configurations allow a quarter gigabyte on-board memory.

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MultiProcessor Resource

The IXZ16 boasts a revolutionary multiprocessor coordination mechanism known as the MultiProcessor Resource (MPR). The MPR implements, in hardware, a global set of 128 signals, 16 semaphores, and 32 4-bit state registers. Unlike software implementations, the MPR ensures low-latency (<500ns), deterministic replication and coherency of these constructs. It is extendable without penalty across large numbers of SHARC clusters on multiple IXZ boards via MPR control signals

(MPC) which are brought out to the VME P2 by a personality module.

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IXLink Ports

The SHARC was designed to use its link ports for interprocessor communications. The IXLink connector/cable specification brings these ports off-board while ensuring robust signal integrity at full-speed over distances up to 3 ft. Each IXLink port is discrete, allowing users to connect them any way they wish.

Up to 16 IXLink ports are brought off the IXZ16: 4 to the front panel; 4 or 8 to the P2, and 4 or 8 to the front via IXI I/O modules. IXI and Front Panel IXLinks run at the 2x clock rate (40MB/s @40MHz).

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Serial Ports

The SHARC has two serial ports which are bi-directional, time-division multiplexed (TDM), synchronous, and high-speed (40Mbits/s @40MHz). The IXZ16 serial ports can be configured as 2 global chains – each across all 16 processors, or 4 cluster chains – 2 across each A/C and B/D clusters. The serial chains interface to the external world via the IXIs and P2. This provides for a flexible interconnect scheme for the serial interface.

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VME64 & P2 Interfaces

The IXZ16 uses the Board Controller and a VIC64 to implement a full featured VME64 master/slave interface. Features include slot 1 control, 5-row DINs, all 7 interrupt levels, BLT, and RMW, in addition to standard data transfer and addressing modes. The VME has access to the global and auxiliary memory in IXQ1.

A P2 personality module can combine with, or replace, an IXQ2 module to actively or passively interface IXQ2, serial ports, and MPC, to rows Z, A, C, and D of the 5-row P2 connector.

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Comprehensive SW Support

A full complement of software tools empower the IXZ family of processor boards. These tools allow users to efficiently develop and integrate large, complex systems within tight time-to-market constraints.

The host tools (IXZmon, HostZapi) are ported to a large and ever-growing number of host platform O/S environments including Solaris, DOS/Windows, LynxOS, VxWorks, and NT. These tools ease the development of real-time embedded DSP applications by providing powerful capabilities for standard I/O, debugging, run-time monitoring, and performance evaluation.

Ixthos also provides a powerful run-time environment (IXZrte) for the SHARC. C&endash;callable libraries (IXZapi, IXZi/o, IXZbsp) provide a simple interface to board capabilities, including MPR semaphores, signals and states. Efficient link port drivers provide feature rich, high performance message passing mechanisms and mail constructs. Finally, IXLibs-

21k provides the industry's highest performance, most comprehensive library of functions optimized for SHARC.

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Specifications

Processors

- Sixteen (16) ADSP-21060's (configured as 4 clusters of 4). Performance benchmarks of each processor:

100/120MFLOPS Peak; 67/80MFLOPS sustained	
1024-pt complex FFT (radix 4):	0.48ms
1024-pt real FFT (radix 2):	0.28ms
FIR Filter per Tap (+0.27/0.23µs for 1st):	25.0 ns
IIR Filter per Biquad (0.18/0.15µs for 1st):	0.10 µs
Division (y/x):	0.15 µs
Inverse Square Root (1/x):	0.23 µs

Memory

- Each SHARC has 0.5MB of dual-ported, 0ws internal SRAM (8MB total)
- 4 banks of 0ws local cluster SRAM up to 2MB each (8MB total)

- Modular global memory (IXQ1)
- up to 128MB DRAM accessible by all four clusters and the VME
- up top 128KB of 0ws SRAM dual-ported between VME and the 4 clusters
- Modular shared memory (IXQ2) of up to 128MB DRAM accessible by clusters C & D

External Interfaces

- 16 off-board IXLink Ports (1 per DSP) configured as either:

4: Front Panel (40MB/s); 8: P2 rows A & D (20MB/s) 4: IXIB (40MB/s) *Standard*

4: Front Panel (40MB/s); 4: IXIA; 4: IXIB (40MB/s) 4:P2 (20MB/s) *order option -f*

IXI links can be brought out to front panel via IXIlink mezzanine.

-2 IXI I/O mezzanine sites accessible by clusters A (IXIA) and B (IXIB). These sites allow modular signal interface via the front panel. Each IXI site provides:

160MB/s to cluster bus

2: 40Mb/s serial port chains

4: 40MB/s links

- 2 global serial port chains (up to 40Mb/s each) accessible via IXIA, IXIB, and/or P2
- JTAG boundary scan port connecting all 16 DSPs
- Modular P2 interface from rows Z, A, C, and D, to IXQ2

VME64 Interface

Full-featured VME64 Master/Slave interface compliant with VSO Rev. D; 5-row extended DIN connector on P1 & P2, slot 1 System Controller, all 7 interrupt levels, BLT, and RMW.

Physical/Electrical

- Standard 6U Eurocard, 160mm x 233mm

- Power: 3.3v - 33W; 5v - 5w (w/o IXIs or IXQs)
- Operating Temperature: 0C to 50C

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