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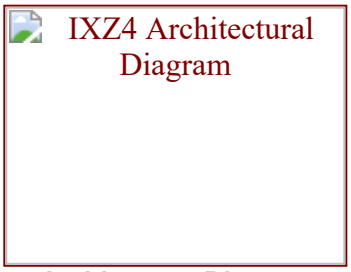
IXZ4

Real-Time MultiProcessing VME Board
Quad SHARC® with I/O





Board Photo



Architecture Diagram



Features

- 4 SHARCs™ (ADSP-2106x); 2 Clusters of 2
- 480 MFLOPS on a Single 6U Board
- 12 off-board SHARC™ IXLinks (40MB/s each)
- Modular, High-speed I/O via 2 IXI Mezzanines (Analog and/or Digital)
- Three Global Memory Sites; up to 64MB each
- MultiProcessor Resource (MPR)
  Provides fast, deterministic HW semaphores, signals, and states between all SHARCs™ in system
- P2 Personality Module for flexible interconnect
- Full Featured VME64 Master/Slave Interface
- Compatible & Scalable with IXZ Family Boards
  (I/O and Processing)
- Comprehensive Software Support:
  - Optimizing ANSI C Compiler
  - Optimized C-callable Function Libraries
  - Multiprocessor Target Debuggers
  - OS/Host Drivers, Standard I/O and Utilities
  - Multiprocessing Applications Interface (API)

General Description

The IXZ4 is the versatile workhorse of the IXZ Family of VME products. Four SHARC DSPs, providing up to 480MFLOPS of peak processing power, combined with architectural flexibility, I/O, scalability, and comprehensive multiprocessing software tools, make the IXZ4 an excellent choice as either an integrated, stand-alone DSP subsystem or a front-end I/O engine for arrays of IXZ Family boards.

The IXZ4's processors are arranged in 2 clusters of 2 SHARCs. The large dual-ported internal memories in the SHARCs are augmented by up to 3 banks of global memory. Each of the 3 IXR global memory module sites on the IXZ4 may be populated with either fast SRAM or large DRAM. The board's Global Resource Switch allows each of these IXR modules to be accessed by both cluster buses and the VMEbus -- such that 3 separate global memory accesses can occur simultaneously.

An integrated Board Controller decouples the SHARC clusters from the VMEbus and associated hosts to reduce overhead and free the DSPs to process real time data. The IXZ4 also boasts a unique MultiProcessor Resource (MPR) that facilitates coordination of large numbers of SHARC clusters over multiple IXZ boards.

Unprecedented off-board interconnectivity and I/O flexibility are key features of the IXZ4. Each board holds 2 IXI I/O mezzanines within a single 6U slot, allowing the user to configure the board for acquiring and processing virtually any type of analog or digital signal. The 12 off-board SHARC IXLink ports provide 480MB/s of scalable interprocessor connection bandwidth for building large multiprocessor systems. The IXZ4's I/O flexibility is rounded out by a versatile interrupt and flag structure in addition to a full-featured VME64 Master/Slave interface.

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