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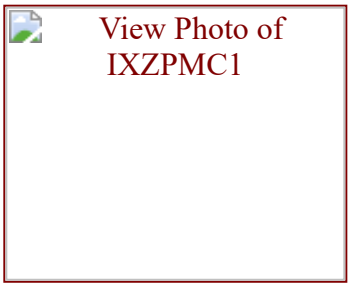
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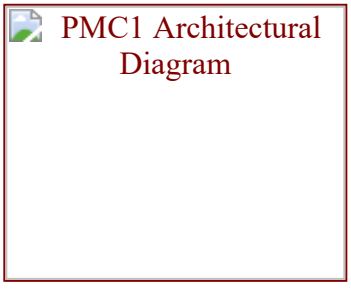
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IXZ PMC1

SHARC® PMC Module



Board Photo



Architectural Diagram

Features

- PCI Interface
  - 32-bit, 33MHz PCI bus
  - 132MB/s peak throughput
- 120 MFLOPS SHARC DSP
  - JTAG Debug Port
- 80MB/s sustained PCI-SHARC bandwidth
- 16 Mbit Flash Memory
  - stores application, diagnostic and boot code
- 128K x 32 on-board SRAM
- 32K x 32 dual-port SRAM
- Software
  - Complete Board Support Package
  - Card Level Diagnostic in FLASH
  - PCI Host Libraries and Monitor
- Up to Six Off-Board IXLink Ports
  - 4 Front Panel links up to 40MB/s
  - up to 6 P2 accessible links up to 20MB/s

General Description

The IXZPMC1 is designed to create a powerful bridge between the PCI bus and off-board SHARC link ports. The peak transfer rate from the PCI bus interface is 132MB/s, while the architecture supports a sustained throughput between the PCI bus and link ports of 80MB/s. This is accomplished by first sustaining data transfers from the PCI bus to the internal memory of the SHARC at rates of 80MB/s. This data can then be distributed over the various off-board links as required by the application.

For example, there are 4 front panel links, each of which can simultaneously carry data up to 40MB/s. These links are compatible with the standard IXZ 6U VME baseboard products (IXZ4, IXZ8 and IXZ16). Hence, this product provides the bridge between the PCI bus on a SBC or a PMC carrier card and the SHARCs on the VME 6U baseboards in the system. Ixthos' link port management software, IXZapi, can be used on both the VME baseboards and the PMC module to facilitate application development. This software platform provides for named system queues and element allocation and buffering in these queues. The user is free from managing the details of the links. Additionally, the SHARC on the IXZPMC1 provides 120MFLOPS of computing power.

A standard PMC module, the IXZPMC1 conforms to the PCI 2.1 standard and is designed to the PMC draft specified in IEEE P1386.1. It uses the Pn4 connector for mapping links and serial ports to the P2 connector.

The IXZPMC1 provides a 40MHz SHARC processor that is capable of 120MFLOPS peak and 80MFLOPS sustained. It has a 32k x 32 dual port SRAM that isolates the local processor bus from the PCI and is accessible by the SHARC at 1 wait state, and a 128k x 32 on-board SRAM that is accessible at 0 wait states. The IXZPMC1 has a JTAG port for debug, and a PCI interface that can transfer at peak rates of 132MB/s. It uses up to 4 front panel links running at up to 40MB/s, or up to 6 P2 links that run at up to 20MB/s, and has 2 off-board serial ports that run at up to 40Mbits/s.

A full featured PCI interface is provided. This includes both master and slave capabilities. All slave accesses are directed into the dual port SRAM. The PCI interface provides eight (bidirectional) mailbox registers and two

(unidirectional) doorbell registers, each with thirty-two unique doorbells. Four of these mailboxes and one doorbell register (thirty- two doorbells) can be tied to independent interrupt service routines on the SHARC.

The second of the two doorbell registers can be used to generate an interrupt on the PCI bus. Two addresses in the dual port memory are tied to interrupts, one on the SHARC and one on the PCI interface chip. An access to either one of these addresses will generate the respective interrupt and can be used to conveniently signal the end of a data transfer. The board can perform direct PCI mater transfers from the internal memory of the SHARC under control of the SHARC processor. It also performs DMA transfers and chained DMA transfers under control of the PCI interface chip. These transfers can read/write from/to the dual port SRAM. Chained descriptor blocks can be located on board or elsewhere on the PCI bus. The SHARC processor or PCI bus can be interrupted after each leg of the DMA or at the end of an entire chain.

In addition to the PCI bus, data can be transferred off-board through the SHARC links and serial ports. There are four front panel link ports that can simultaneously transfer data at rates up to 40MB/s each. Through the Pn4 connector (maps to the P2) the user can transmit on up to 6 link ports at up to 20MB/s and 2 serial ports. A 3-row DIN connector is required for access to all 6 links and the 2 serial ports.

Included with the IXZPMC1 is a Board Support Package (BSP). The BSP can be linked with the user's DSP application code. This package contains the software needed for such tasks as setting up and controlling master DMAs, initializing interrupts, flag control and LED control, etc.

Another product, PMCtools, offering a complete set of host and SHARC DSP software, is available for this board. The host software consists of a monitor (PMCmon) and a host library (PMCapi). The monitor allows users to open a communication channel with one or more PMC boards, download application code, start the application, read and write PMC memory/register space, disassemble code, process standard I/O and perform debug. PMCapi allows the user to easily write host code to control the PMC. On the DSP side, Ixthos provides three run-time libraries which can be linked with the user code: the IXZapi communications library, the standard I/O library, and the PMC run-time environment library. The IXZapi communications library provides link port control while the standard I/O library provides the standard C I/O capability for the SHARC DSPs. The run-time environment is provided to support the host code.

Ixthos has written a comprehensive Power-On-Self-Test (POST) which is stored in the PMC flash memory and can be run when the board is powered up or reset. For application development, the user can load and debug code over the PCI bus or use the in circuit emulator (ADI's EZ-ICE). For final system configuration, the application code can be loaded over the PCI bus or stored in the on-board flash.

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