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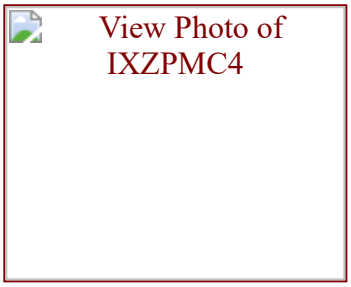
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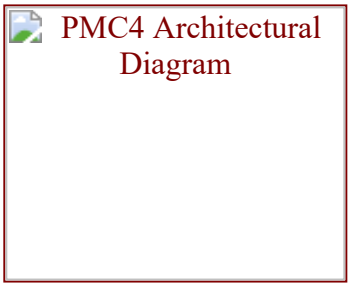
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IXZ PMC4

SHARC® PMC Module



Board Photo



Architectural Diagram

Features

- DSP Compute Engine for PCI Bus
- Four SHARC DSPs with 480 MFLOPS
  - JTAG debug port
- 32-bit, 33MHz PCI bus (132MB/s peak)
- 80MB/s sustained PCI-SHARC throughput
- 16MBit Flash Memory
- 32K x 32 dual port SRAM
- 8M x 32 DRAM or 512K x 32 SRAM
- Software
  DSP run-time libraries
  - PMC Tools
    Comprehensive host software
    Power On Self-Tests (POST)
  - Standard IXZapi link port message passing capability
  - Standard I/O
- Up to Twelve Off-Board IXLink Ports
  - up to 8 Front Panel links at 40MB/s
  - up to 4 P2 accessible links at 20MB/s
- One serial port (P2) at 40MHz

General Description

The IXZPMC4 is a powerful DSP compute engine for PCI bus baseboards containing at least one PMC slot. As an on-board processing engine, the IXZPMC4 delivers 480 MFLOPS of computing power in a convenient and economical format completely within the host board environment. The IXZPMC4 provides a new level of performance for the user's host board, a level that could only formerly be achieved through the inclusion of additional boards in the system chassis or through connection to external DSP systems.

In applications requiring off-board data communication, data can be transferred between the IXZPMC4 and other boards through the SHARC IXLink ports and serial ports. There are eight front panel IXLinks which can simultaneously transfer data at rates up to 40MB/s for an aggregate transfer rate of 320MB/s. Through the Pn4 connector (maps to the P2), the user can transmit on up to 4 link ports at up to 20MB/s and 1 serial port. A global SHARC processor flag as well as the board reset signal are also brought to the Pn4 connector.

The peak transfer rate between the PCI bus and PCI interface is 132MB/s, while the architecture supports a sustained throughput between the PCI bus and memory of 80MB/s. There are 8 front panel links which are compatible with the standard IXZ 6U VME baseboard products (IXZ4, IXZ8 and IXZ16). Ixthos' link port management software, IXZapi, can be used on both the VME baseboards and the PMC module to facilitate application development. This software platform provides named system queues and element allocation and buffering in these queues. The user is free from managing the details of the links.

The IXZPMC4 provides four 40MHz SHARC processors that are capable of 480 MFLOPS peak; a 32k x 32 dual port SRAM that isolates the local processor cluster bus from the PCI and is accessible by any of the four SHARCs; a 8M x 32-bit DRAM or a SRAM (512k x 32 or 128k x 32 is available); a JTAG port for debug; PCI interface that can transfer at peak rates of 132MB/s. It uses up to 8 front panel links running at up to 40MB/s, or up to 4 P2 links that run at up to 20MB/s, and has a single off-board serial port that runs at up to 40Mbits/s.

A full featured PCI interface is provided which includes both master and slave capabilities. All slave transfers directly access the dual-port SRAM. Eight programmable address match registers are provided to notify the SHARC processors of specific slave write access to the dual-port. A pair of these registers is dedicated to each SHARC processor. This feature can be used to conveniently notify a SHARC of a buffer-full condition. Further, the PCI interface provides eight (bidirectional) mailbox registers and two (unidirectional) doorbell registers, each with thirty-two unique doorbells.

Four of these mailboxes and one doorbell register (thirty-two doorbells) can be tied to independent interrupt service routines on the SHARC processors. The second of the two doorbell registers can be used to generate an interrupt on the PCI bus. Additionally, an address in the dual port memory is tied to an interrupt on the PCI interface chip that can be used to signal the PCI bus when a SHARC write access to this location has been made. The board can perform direct PCI master transfers from the internal memory of any of the four SHARC processors under the control of the SHARC involved in the transfer. It can also perform DMA transfers and chained DMA transfers under control of the PCI interface chip. These transfers can read/write from/to the dual port SRAM. Chained descriptor blocks can be located in local memory (i.e. SHARC internal, local DRAM, or the dual port SRAM) or elsewhere on the PCI bus. The SHARC processor or PCI bus can be interrupted after each leg of the DMA or at the end of an entire chain.

Included with the IXZPMC4 is a Board Support Package (BSP). The BSP can be linked with the user's DSP application code. This package contains the software needed for such tasks as setting up and controlling master DMAs, initializing interrupts, flag control and LED control, etc.

Another product, PMCtools, offering a complete set of host and SHARC DSP software, is available for this board. The host software consists of a monitor (PMCmon) and a host library (PMCapi). The monitor allows users to open a communication channel with one or more PMC boards, download application code, start the application, read and write PMC memory/register space, disassemble code, process standard I/O and perform debug. PMCapi allows the user to easily write host code to control the PMC. On the DSP side, Ixthos provides three run-time libraries, which can be linked with the user code: the IXZapi communications library, the standard I/O library, and the PMC run-time environment library. The IXZapi communications library provides link port control while the standard I/O library provides the standard C I/O capability for the SHARC DSPs. The run-time environment is provided to support the host code.

Ixthos has written a comprehensive Power-On-Self-Test (POST) which is stored in the PMC flash memory and can be run when the board is powered up or reset. For application development, the user can load and debug code over the PCI bus or use the in circuit emulator (ADI's EZ-ICE). For final system configuration, the application code can be loaded over the PCI bus or stored in the on-board flash.

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