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SVME/DMV-182

GETTING STARTED MANUAL

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VERSION HISTORY

Version	By	Date	Description
1	BJ	June 2003	First release.
2	BJ	September 2003	Added typical power number to “General Description” on page 1-1. Added SVME-182 weight to Table 1.2, “Maximum Card Weight,” on page 1-8. Updated image in “SVME-182 Front Panel” on page 1-10. Added paragraph to “Chassis Requirements” on page 2-2. Updated “Power Requirements” on page 2-2. Updated VME Reset information in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Updated “VME Reset Jumper” on page 2-10. Added “NoVRAM Write Protect Jumper” on page 2-18. Added more specific P0 cable installation instructions to “Ethernet2 Connection via the P0 Interface” on page 3-11 and “Connect Other Peripherals via the P0 Connector” on page 3-19. Updated “FAIL LED Stays Lit” on page 3-25.
3	BJ	December 2003	Updated to reflect new IPM naming. Added new cable and updated IPM names in Table 2.2, “Cable Part Numbers,” on page 2-3. Updated “PMC Site VIO Selection Jumpers” on page 2-14.
4	BJ	February 2004	Updated Figure 1.1, “SVME/DMV-182 Functional Block Diagram,” on page 1-2. Added “Interface Personality Module (IPM)” on page 1-3. Updated “Power Requirements” on page 2-2. Updated “Cable Requirements” on page 2-3. Added information for CBL-182-P2-009 to Table 2.2, “Cable Part Numbers,” on page 2-3. Updated Tip under “Configuring Jumpers” on page 2-5. Updated VIO Selection for PMC Site 2 in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Added information for booting from PABS to Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Updated “PMC Site VIO Selection Jumpers” on page 2-14. Added “Booting Jumper” on page 2-19. Updated “Install the PMC Modules on the Basecard” on page 3-3. Updated “Insert the Basecard in the Chassis” on page 3-4. Updated Tip under “Connect a Terminal” on page 3-4. Updated “Verify that PCI VIO is Connected” on page 3-25. Updated “Determining the Foundation Firmware Version” on page 4-2. Updated “Recovering Foundation Firmware” on page 4-5. Updated “The VMEBus Base Address” on page 4-6.
5	BJ	August 2004	Added weights for IPMs to Table 1.2, “Maximum Card Weight,” on page 1-8. Updated notes under “Configuring Jumpers” on page 2-5. Updated PABS Flash Write Protect in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Updated VIO Selection for PMC Site 2 in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Updated Boot from PABS in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Added VIO Selection information for PWB 311114-002 in Table 2.3, “Basecard Jumper Settings Summary,” on page 2-5. Indicated placement of PWB number in Figure 2.1, “SVME/DMV-182 Jumper Locations,” on page 2-7. Updated “VME Reset Jumper” on page 2-10. Updated “PMC Site VIO Selection Jumpers” on page 2-14. Updated “Booting Jumper” on page 2-19. Added “CBL-182-422/232” on page 3-17. Added “Enable CPU1” on page 3-25. (PT #2088) Updated “Verify that PCI VIO is Connected” on page 3-25.

Version	By	Date	Description
6	BJ	December 2004	Added warning to “Interface Personality Module (IPM)” on page 1-3. Updated “Updating Foundation Firmware” on page 4-5. Updated “Recovering Foundation Firmware” on page 4-5.
7	BJ	January 2004	Updated Table 3.19, “CPU0 Foundation Firmware Execution Sequence,” on page 3-23. (PT #2452) Updated Table 3.20, “CPU1 Foundation Firmware Execution Sequence,” on page 3-23. (PT #2452)
8	BJ	June 2005	Updated tip under “Connect a Terminal” on page 3-4. (PT #2835) Updated Table 3.16, “CBL-182-P0-000 P1 to J3 (Discrete Digital I/O) Signal Mapping,” on page 3-21. (PT #10037) Updated “Display the Initial Screen Message” on page 3-24.

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PREFACE

PURPOSE

This manual provides an overview of the many features of the SVME/DMV-182 Single Board Computer. After explaining the capabilities of the SVME/DMV-182, the manual provides the procedure for correctly installing and checking out the card's operation.

This manual is intended for the reader who has a technical understanding of hardware engineering fundamentals and a basic understanding of the VMEbus architecture.



Cross Reference

More in-depth technical information about the SVME/DMV-182 hardware is provided in the *SVME/DMV-182 Hardware User's Manual*, document number 812058, which is included in the documentation package.



Note

This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

SCOPE

This document contains the following chapters:

Chapter 1 - Product Overview. Provides general information about the features and functions of the SVME/DMV-182.

Chapter 2 - Pre-Installation Tasks. Discusses tasks that must be performed prior to installing the SVME/DMV-182 in a chassis. Provides information on jumper configurations, cabling, and power requirements.

Chapter 3 - Hardware Installation. Explains how to install the SVME/DMV-182 in a chassis and verify that it is operating correctly.

Chapter 4 - Card Communications. Explains how to determine the hardware and Foundation Firmware configuration of the card, how to run diagnostics, and how to restore the SEEPROM and Foundation Firmware. Explains how to change the SVME/DMV-182's VME base address and how to communicate with other cards over the VMEbus.

CONVENTIONS USED IN THE DOCUMENTATION PACKAGE

This document and the accompanying documents in the documentation package use various icon conventions and abbreviations in order to make the documents clearer and easier to read. These conventions cover typography for such elements as sample software code and keystrokes, signal meanings, and graphical elements for important information such as warnings or cautions.

Typographic Conventions

Table 1 lists the typographical conventions used in the documentation package.

TABLE 1: Typographical Conventions

Item	Convention	Example
Keystrokes	Keys are listed as they appear on most keyboards, surrounded by < > marks. Combinations of key-strokes appear within a single set of < > brackets.	Type < Ctrl-Alt-C > to return to the previous menu. Type < Esc > to exit.
Filenames	Filenames are italicized.	Open the *es.h* file.
Directory names	Directory names show the full directory path. The last directory in the path does not have a backslash following it. Directory names are italicized.	Go to the *c:\windows\temp\backup* directory.
Monitor Displays and Code Samples	Monitor displays and code samples appear in a monospace font.	`c:\temp>`
Button and Window Labels	Button and Window labels appear in bold.	Click the **Finish** button.

Signal Conventions

Table 2 shows symbols which can follow a signal name. For example, the asterisk (*) is used with a VMEbus signal name, such as BERR*.

TABLE 2: Signal Conventions

Symbol	Description
*	The signal is active LOW and is connected to the VMEbus.
/	The signal is active LOW and is connected to the local bus only, and not directly to the VMEbus.
[no symbol]	The signal is active HIGH (with no indication as to whether the signal is connected to the VMEbus or local bus).
#	The signal is active LOW and is connected to the PCI bus.

Abbreviations

Table 3 lists the abbreviations used when describing the size of a memory device or a range of addresses.

TABLE 3: Abbreviations

Abbreviations	Description
1 Kbyte	1,024 bytes
1 Mbyte	1,024 Kbytes
1 Gbyte	1,024 Mbytes

Memory Addresses

Unless stated otherwise, all memory addresses are shown in hexadecimal notation.

Icons

The following icons are used throughout the documentation package:



Warning

The warning icon indicates procedures in the manual that, if not carried out, or if carried out incorrectly, could result in physical injury, cause electrical damage to equipment, or cause a non-recoverable corruption of data. Warnings include instructions on how to prevent such damage. Please observe warning icons and read the accompanying text completely before carrying out the procedure.



Caution

The caution icon indicates non-catastrophic incidents, complex practices or procedures which, if not observed, could result in damage to the hardware. Cautions include specific instructions for avoiding or minimizing these incidents.



Note

The note icon highlights exceptions and special information.



Tip

Tips provide extra information on the subject matter. This could include hints on how to use your card to its maximum potential.



Cross Reference

Cross references to other documents are used when discussing a subject that is fully addressed by another, more authoritative document. Cross references are also used for document chapters and sections.

REFERENCE DOCUMENTATION

Please refer to the CD-ROM included in the documentation package for additional reference information, supplied in Adobe Acrobat-readable format. Included on the CD-ROM are documents relating to the standard Foundation Firmware, a user's manual for the Universe PCI to VMEbus interface, and a helpful guide to using the VMEbus (among other things).

You'll also find copies of the relevant cable assembly drawings there.



Note

The CD-ROM provides a copy of the Adobe Acrobat 4.0 reader software, including the Acrobat Search plug-in, to enable you to get the most out of your CD-ROM by enabling full-text searches of the information.

In addition, the *SVME/DMV-182 Hardware User's Manual*, document number 812058, provides additional technical detail about the SVME/DMV-182.

1 PRODUCT OVERVIEW

GENERAL DESCRIPTION

The SVME/DMV-182 continues the evolution of CWCEC's industry-leading MIL/rugged line of PowerPC-based Single Board Computers (SBCs). Packed with features to satisfy the real-world requirements of defense/aerospace systems integrators, the SVME/DMV-182 is designed with performance, reliability, and ease of use in mind.

The SVME/DMV-182 provides a highly integrated, powerful PowerPC architecture in a single-slot solution with high processing performance, industry standard I/O, and the flexibility of user-specific I/O which traditionally required multiple cards.

The SVME/DMV-182 introduces a dual-CPU architecture, a capacity of up to 128 Mbytes of direct memory-mapped Flash, and the DSP capabilities of AltiVec technology, all at a low power dissipation of only 40 Watts (typical). Providing up to 1 Gbyte of high-performance DDR SDRAM combined with the high system integrity of Error Checking and Correction (ECC), the SVME/DMV-182 is ready for the challenges of avionics, tactical ground vehicle, and rugged naval applications.

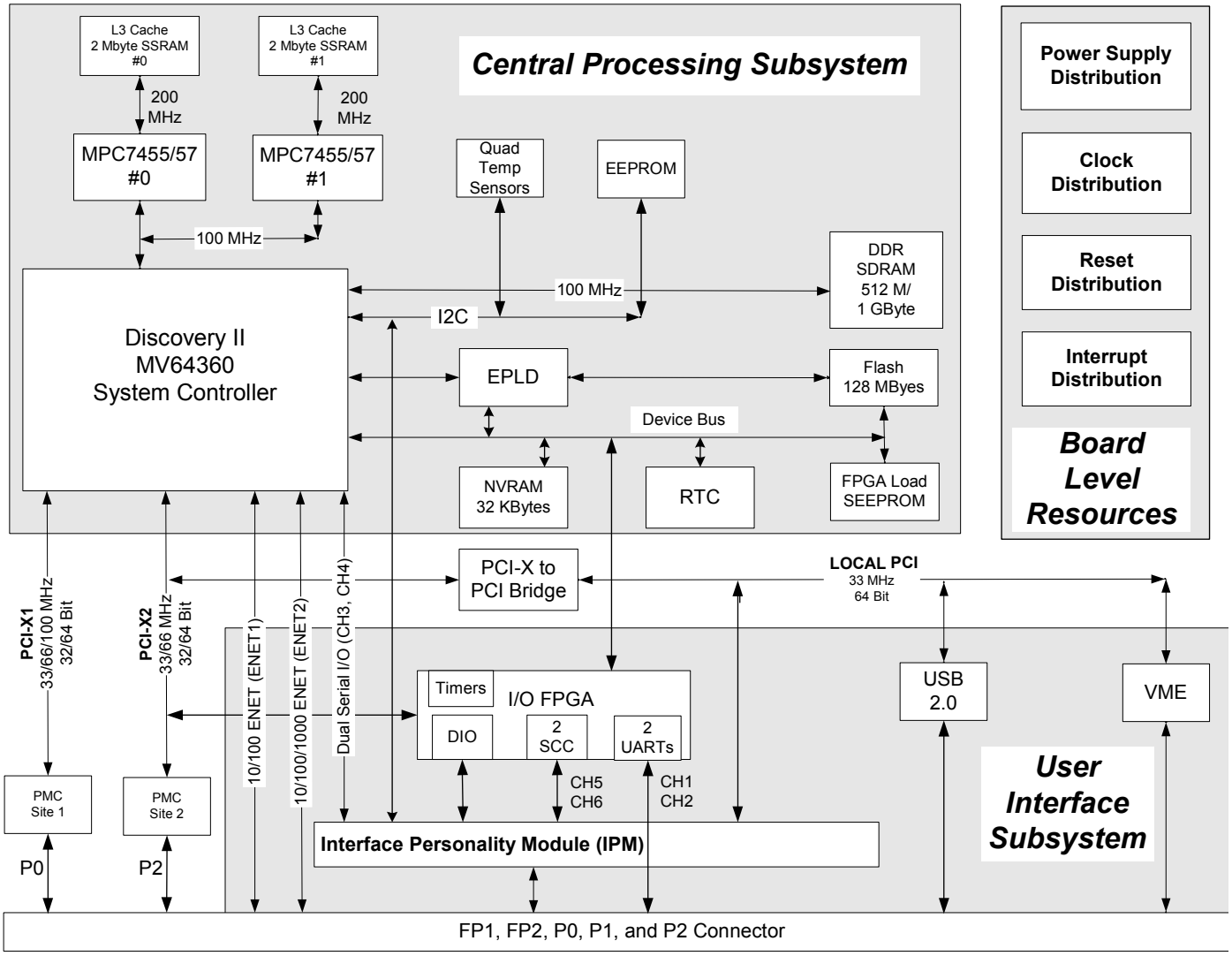
For retrofit and technology insertion applications, the SVME/DMV-182 offers a common I/O feature set and the option of pinout compatibility to earlier generations of CWCEC PowerPC SBCs. As a member of CWCEC's continuously evolving stream of PowerPC SBCs, the SVME/DMV-182 supports the life-cycle model of successive technology insertions throughout a platform's life time.

The SVME/DMV-182 provides a site for an Interface Personality Module (IPM). The IPM, in combination with the I/O FPGA provides a flexible I/O interface for the SVME/DMV-182. The combination can also provide additional functionality.

The SVME/DMV-182's design features address the real-time, mission-critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage and high functional density.

Figure 1.1 illustrates the SVME/DMV-182 architecture.

FIGURE 1.1: SVME/DMV-182 Functional Block Diagram



Cross Reference

Please refer to Chapter 1 of the *SVME/DMV-182 Hardware User's Manual,* document number 812058, for a detailed description of each of the functional blocks in the above diagram.

Note

This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

ABOUT PMC

PMC, an open industry-standard mezzanine module with a PCI interface, allows system designers to increase the SVME/DMV-182's functionality by utilizing CWCEC PMCs, available third party PMC products, or by developing their own PMC-based modules.

INTERFACE PERSONALITY MODULE (IPM)

The SVME/DMV-182 provides a site for an Interface Personality Module (IPM). The IPM, in combination with the I/O FPGA provides a flexible I/O interface for the SVME/DMV-182. The combination can also provide additional functionality. Figure 1.4 on page 1-7 shows the location of the PMC sites and Interface Personality Module (IPM).



Warning

IPMs must be installed and removed only at the factory.



Cross Reference

The *SVME/DMV-182 Hardware User's Manual* includes appendices which describe the available IPMs.

SUPPORT FOR CWCEC COMMON FEATURES

The SVME/DMV-182 supports CWCEC Systems' common architecture feature set, including the capability of a compatible pinout with previous PowerPC products (SVME/DMV-178/179/181) and a feature-rich VME64x VMEbus interface with Built-In-Test (BIT). These features bring benefits in performance as well as supporting technology insertion, reducing program logistics and maintenance costs.

Tundra's Universe II interface chip provides a PCI to VMEbus bridge which implements all VMEbus interface functions with software-programmable features. Based on the popular SCV64, the Universe II device combines low-latency access to the VMEbus with high sustained throughputs. Additional Built-In-Test (BIT) hardware features verify correct operation to a high confidence level.

The Universe II internal FIFOs support write posting, enabling efficient interprocessor messaging thereby minimizing overhead in real-time software. Geographical address inputs available as part of the VME64 extensions can be used for VMEbus base address configuration.

PHYSICAL CHARACTERISTICS

Figure 1.2 shows the location of the major components and the connectors on the component side of the SVME/DMV-182 PWB. Figure 1.3 shows the major components on the solder side of the SVME/DMV-182 PWB.

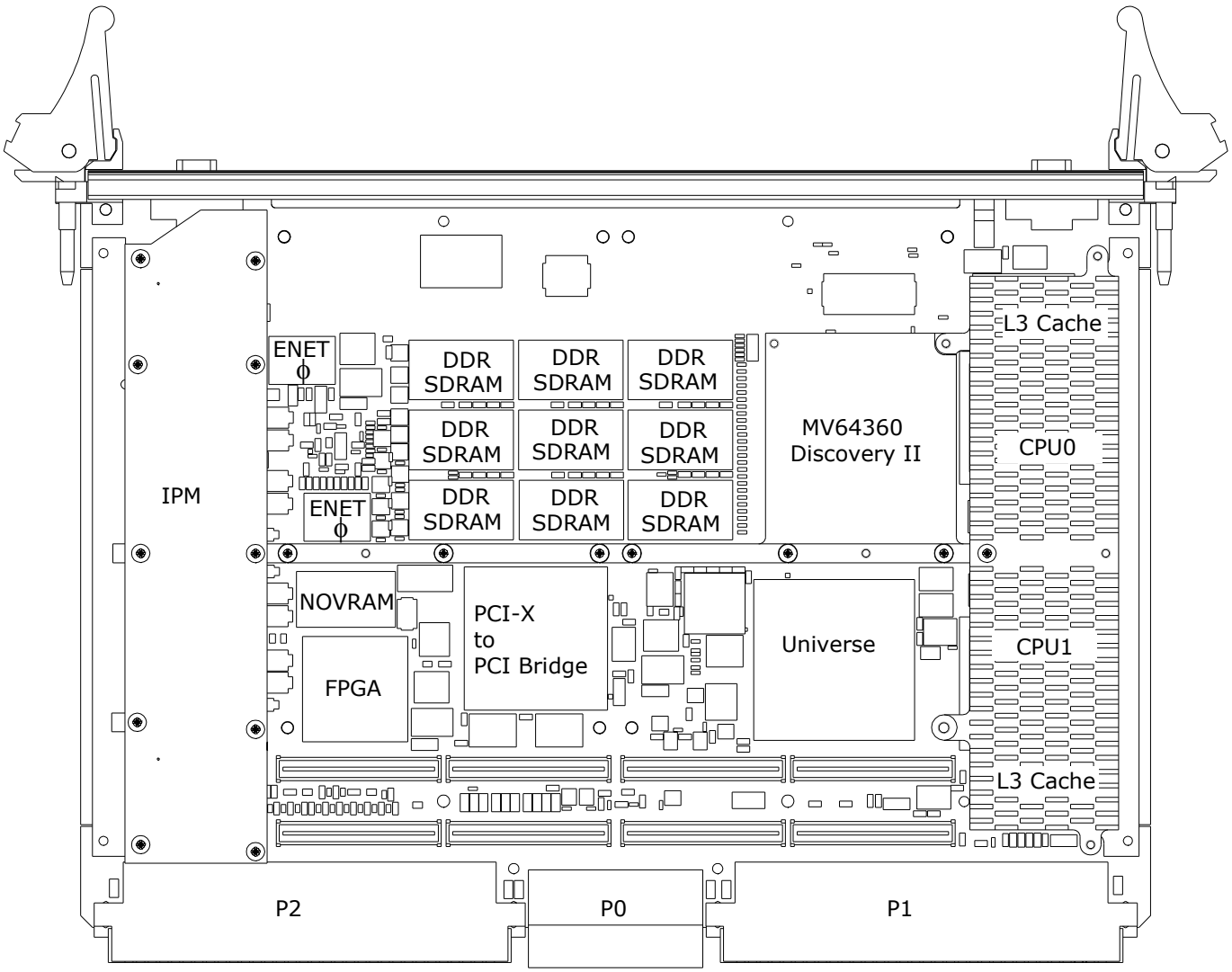


FIGURE 1.2: View of SVME-182 Component Side

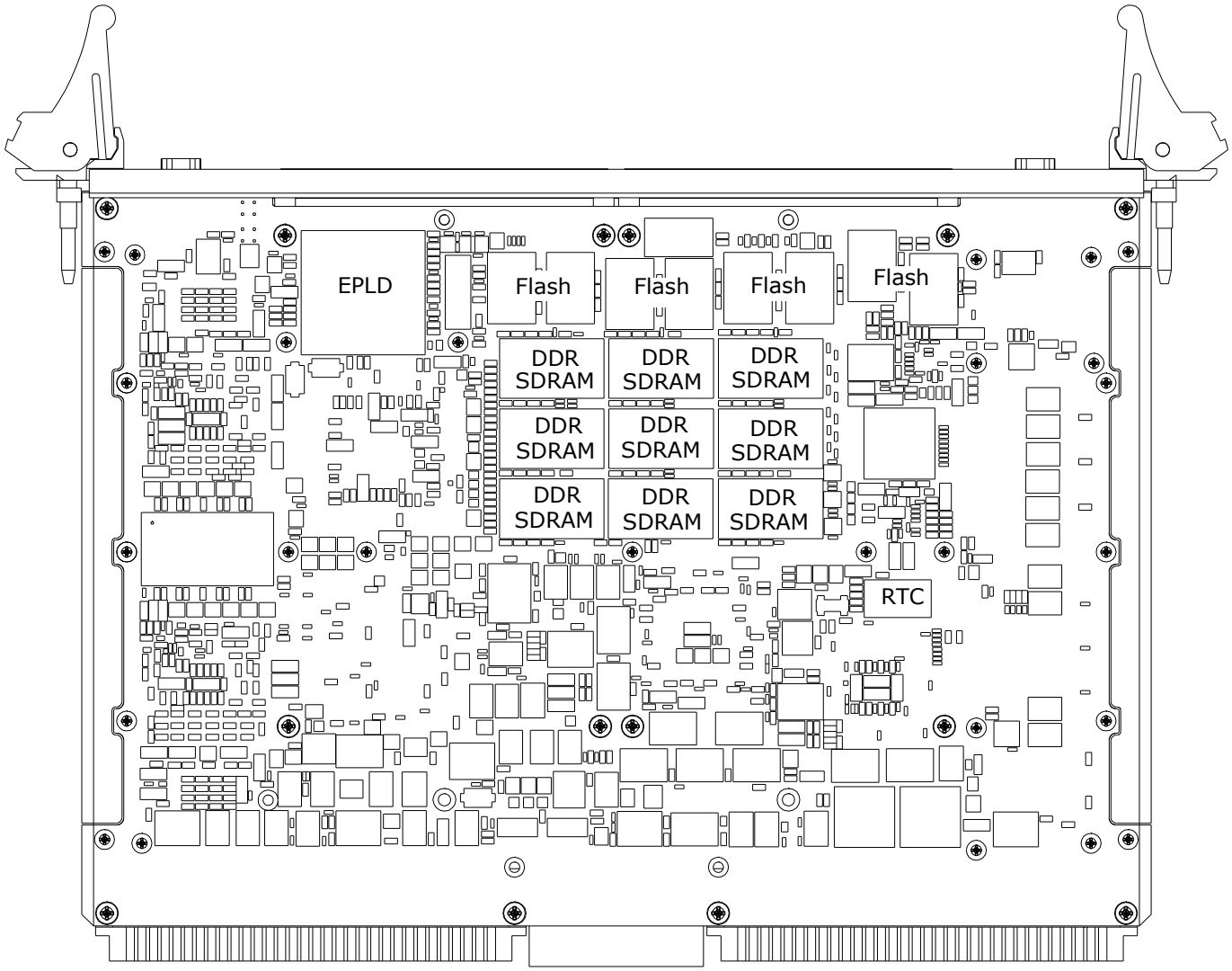
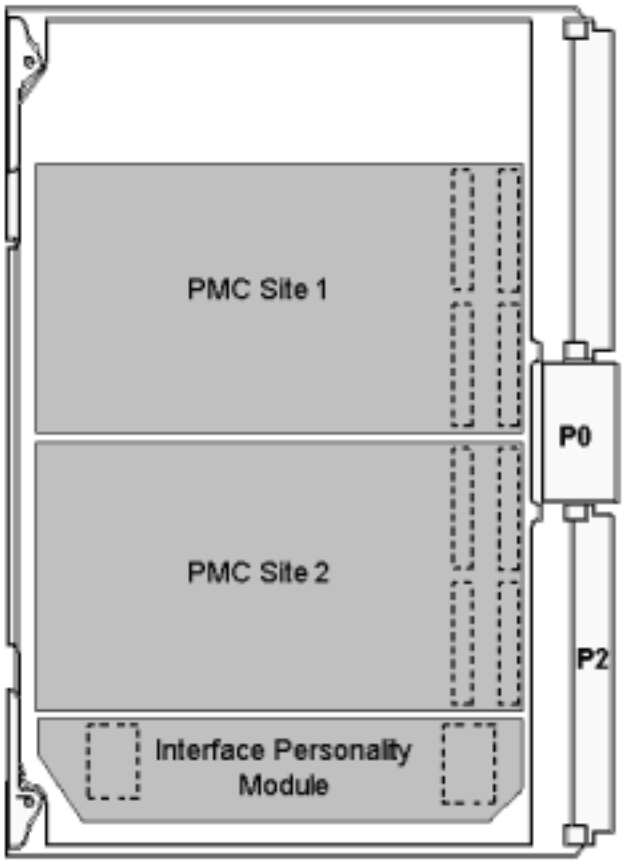


FIGURE 1.3: View of SVME-182 Solder Side

Figure 1.4 shows the location of the PMC sites and Interface Personality Module (IPM).

FIGURE 1.4: Location of PMC Modules and Interface Personality Module



Dimensions

The SVME/DMV-182 is built on a VMEbus-compatible double-height (6U) Printed Wiring Board (PWB). Table 1.1 lists the dimensions of the SVME/DMV-182.

TABLE 1.1: Dimensions of the SVME/DMV-182

Parameter	Dimensions
Height	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)
Thickness	20.0 mm (0.8 in.)

Weight

The maximum weights of the SVME/DMV-182 and the associated IPMs are specified in Table 1.2.

TABLE 1.2: Maximum Card Weight

Card Type	Weight
SVME-182 (no IPM or PMC modules present)	520 g
Mode 4 IPM (16-bit SCSI) and Mounting Hardware (SVME type)	38 g
Mode 6 IPM (Serial) and Mounting Hardware (SVME type)	35 g
Mode 9 IPM (Dual 1553) and Mounting Hardware (SVME type)	43 g
DMV-182 (no IPM or PMC modules present)	750 g
Mode 4 IPM (16-bit SCSI) and Mounting Hardware (DMV type)	37 g
Mode 6 IPM (Serial) and Mounting Hardware (DMV type)	30 g
Mode 9 IPM (Dual 1553) and Mounting Hardware (DMV type)	42 g

Mating Connectors

Table 1.3 summarizes these connectors, providing a brief description and an indication of what functions/interfaces are supported by each.

TABLE 1.3: Summary of SVME/DMV-182 Connectors, Functions Supported

Connector Designation	Description	Supported I/O Configurations
FP1	9-pin front panel connector (SVME-182 only) compatible with P1 of the front panel cable set, CBL-182-FPL-000.	EIA-232 serial Channels 1 and 2, card reset
FP2	9-pin front panel connector (SVME-182 only) compatible with P2 of the front panel cable set, CBL-182-FPL-000.	10/100BaseT Ethernet interface (ENET1), USB1
J7, J8, J15, J16	connectors for PMC module site 2, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 2 I/O signals are accessible via the basecard P2 connector, rows A and C.
J9, J10, J17, J18	connectors for PMC module site 1, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 1 I/O signals are accessible via the basecard P0 connector.
P2 (see Tip)	160-pin (5 x 32) right-angle DIN connector, row B pin assignments in accordance with the ANSI/VITA 1-1994 VME64 VMEbus specification, remaining rows employed for user I/O.	VMEbus interface, EIA-232 interfaces (Channels 1 and 2), EIA-422/485 interfaces (Channels 3 and 4), SCSI interface, Ethernet 10Base-T or 100Base-T interface (ENET1), PMC Site 2 I/O signals (standard factory configuration).
P1	160-pin (5 x 32) right-angle DIN connector, pin assignments in accordance with the ANSI/VITA VME64x VMEbus specification	VMEbus interface.
P0 (see Tip)	95-pin (5 x 19) AMP connector, part number 98-3165-105-01.	Discrete Digital I/O interface, Ethernet 10/100/1000Base-T interface (ENET2), PMC Site 1 I/O signals, USB2 (standard factory configuration).



Cross Reference

For complete descriptions of all the basecard mating connectors, including detailed pinout listings and electrical characteristics of signals, refer to Chapter 2 of the *SVME/DMV-182 Hardware User's Manual*, document number 812058.

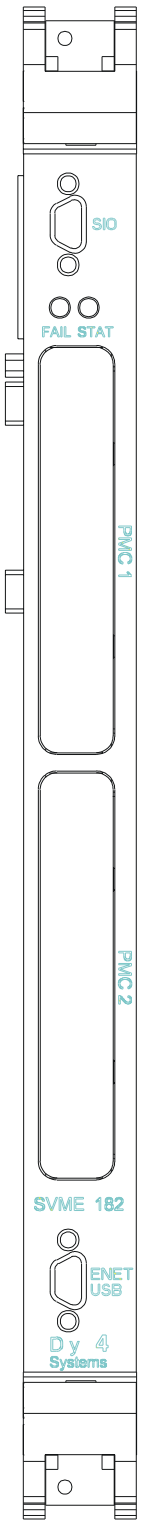
You should consult the *Product Release Notes* for your particular card variant, which contains information describing any variant-specific alterations to the interface configuration of your card, if any have been implemented.



Tip

The Technical Documentation CD-ROM includes a pinout configurator utility. This 32-bit Windows utility generates the P0 and P2 pinouts based on the Interface Personality Module (IPM) and the PMC modules installed on the SVME/DMV-182.

SVME-182 Front Panel



FP1 Connector: (At the top, marked "SIO") Used in conjunction with the front panel cable set, CBL-182-FPL-000, the FP1 connector provides connections for two serial channels and a card reset input.

Red FAIL LED: The red FAIL LED indicates that the SVME/DMV-182 is driving the SYSFAIL* signal on the VMEbus. The LED will turn on after an internal RESET during the power-on sequence or after a System Reset.The SYSFAIL* signal is controlled by the Universe II device. For further details on the SYSFAIL* signal, refer to the *Universe II User's Manual*, provided on the SVME/DMV-182 Technical Documentation CD-ROM.

Green STAT LED: The green STAT LED indicates the state of the Status LED bit in bit 0 of the LEDs Register. The LED will turn on after an internal RESET during the power-on sequence or after a System Reset. If the Status LED control bit is 1, then the LED is on. If the Status LED control bit is 0, the LED is off. For further details on the Status LED control bit, refer to Chapter 3 of the *SVME/DMV-182 Hardware User's Manual*, document number 812058, provided in this documentation package.

PMC Slots: Two openings are provided on the SVME-182 front panel to provide access to connectors that may be incorporated on optional PMC modules that may be installed on the basecard PWB. If there are no PMC modules mounted, the openings are filled with bezels.

FP2 Connector: (At the bottom, marked "ENET USB") Used in conjunction with the front panel cable set, CBL-182-FPL-000, the FP2 connector provides connections for ENET1 (10BaseT/100BaseT) and USB1.

OVERVIEW OF SUPPLIED FIRMWARE AND SOFTWARE

Foundation Firmware

The SVME/DMV-182 is programmed with the following Foundation Firmware (FF/W) modules:

- ***General Purpose Monitor (GPM)***: provides comprehensive monitoring and debug functions, which can be accessed from a terminal connected to the SVME/DMV-182 serial channel 1 interface
- ***Card Level Diagnostics (CLD)***: provides diagnostic routines which work with your card's Built-In-Test functions
- ***Configuration Boot Manager (CBM)*:** provides the facility to change the SVME/DMV-182 boot parameters.



Cross Reference

Refer to the *Foundation Firmware User's Manual* and the *FF/W Release Notes (*included in the Technical Documentation CD-ROM) for additional information.

Board Support Packages, Drivers

Support is provided for the VxWorks operating system. The VxWorks boot loader (which is current at the time of manufacturing) is pre-loaded on the SVME/DMV-182 hardware. The VxWorks Board Support Package (BSP) is provided on its own CD-ROM.



Cross Reference

Refer to the *Release Notes* and the *BSP Software User's Manual* provided on the SVME/DMV-182 BSP CD-ROM for additional information.

2 PRE-INSTALLATION TASKS

INTRODUCTION

This chapter explains how to configure the SVME/DMV-182 before it is installed in a VME chassis. Specifically, this chapter provides the following information:

- checking cable and power requirements;
- unpacking the card; and
- modifying the SVME/DMV-182 jumper settings.

CHECKING HARDWARE REQUIREMENTS

Ensure that the following requirements have been met prior to installation:

CHASSIS REQUIREMENTS

The SVME-182 is designed to be installed in a standard 6U VME-64x VMEbus chassis and backplane which operates in a free-air or forced-air cooling environment. The DMV-182 is conduction-cooled, and is therefore designed to be installed in a VME conduction-cooled chassis.

10 CFM of airflow is required to adequately cool the SVME-182 in a Level 100 environment. Operating in the less severe Level 000 environment will require less airflow to keep all components within their recommended operating ranges.

POWER REQUIREMENTS

Table 2.1 shows the power requirements for different variants of the SVME/DMV-182. For proper operation, the +5 V supply must be as specified in the VME specification. If the supply is above this range, it could damage the SVME/DMV-182.

TABLE 2.1: Power Requirements

Processor	Voltage	Maximum Current	Typical Current
SVME/DMV-182-x600 Two PowerPC 7457 @ 1.0 GHz 1 Gbyte DRAM No PMCs No IPMs	+5 VDC	9 A	7 A



Note

The SVME/DMV-182 uses on-card voltage regulators to provide the required low voltages to devices on the SVME/DMV-182. If PMC modules requiring 3.3 V are to be used on the SVME/DMV-182, the backplane into which the SVME/DMV-182 is installed must be properly configured to provide 3.3 V power at the P1 connector.

CABLE REQUIREMENTS

The cables available to interface with the SVME/DMV-182 are listed in Table 2.2 on page 2-3. You can also make your own cables using the SVME/DMV-182 connector pin assignments documented in Chapter 2 of the Hardware User's Manual.

Cabling Considerations



Cross Reference

Consult the Product Release Notes for the card to determine which IPM (if any) is installed. Make sure to order cables appropriate for the IPM used.



Cross Reference

See "Connect a Terminal" on page 3-4 for information about how to use the standard cables available for the SVME/DMV-182.

TABLE 2.2: Cable Part Numbers

Part Number	Connects To	Description
CBL-182-FPL-000	Front Panel FP1 and FP2 (SVME-182 only)	**FP1:** 2 x EIA-232 Reset Switch **FP2:** Ethernet 1 (10/100BaseT) USB 1
CBL-182-P0-000	P0	PMC1 I/O Ethernet 2 (10/100/1000BaseT) 14 Discrete Digital I/O USB 2 Reset Switch
CBL-182-P2-000	P2 with no IPM	PMC2 I/O 2 x EIA-232
CBL-SBC-P2-000	P2 with Mode 1 IPM (serial, 8-bit SCSI) (standard I/O)	PMC2 I/O 8-bit SCSI via 16-bit SCSI connector 2 x EIA-232 2 x EIA-422/485
CBL-SBC-P2-002	P2 with Mode 4 IPM (serial, 16-bit SCSI)	PMC2 I/O 16-bit SCSI 2 x EIA-232 1 x EIA-422/485
CBL-SBC-P2-003	P2 with Mode 6 IPM (Serial)	PMC2 I/O 2 x EIA-232 4 x EIA-422/485
CBL-182-P2-009	P2 with Mode 8 or Mode 9 IPM (1553)	PMC2 I/O 2 x EIA-232 2 x EIA-422/485 2 x MIL-STD-1553

UNPACKING THE CARD


Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until just before the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

To unpack the card from its protective package, follow these steps:

1. Unpack the card from the shipping carton in a suitable work area. If the shipping carton appears to be damaged, request that an agent of the shipper or carrier be present during unpacking and inspection.
2. Find the packing list. Verify that all the items on the list are present.
3. Save the packing material for storing or reshipping the card.

CONFIGURING JUMPERS



Cross Reference

Depending on your application, it may be necessary to modify the default jumper settings on your SVME/DMV-182. Details are provided in the remainder of this chapter.



Tip

For the initial configuration, insert jumpers J2 , J3, J4, J5, J6, TC1A, and TC2A and remove jumper J1. Configure jumpers J11 through J14 according to the version of the PWB and the PMCs mounted on it. See Table 2.3.



Note

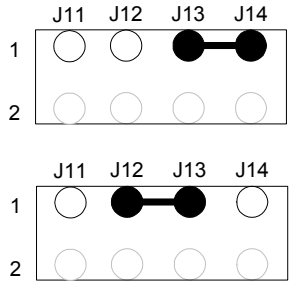
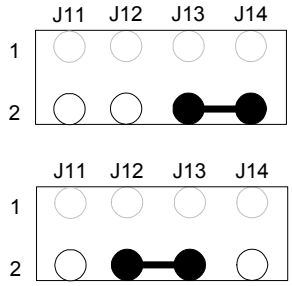
This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

Table 2.3 lists user-configurable basecard jumper settings. Figure 2.1 on page 2-7 shows the locations of the jumpers. More in-depth descriptions of these jumper settings are provided later in this chapter.

TABLE 2.3: Basecard Jumper Settings Summary

Option	Jumper Setting
Backup FPGA Boot PROM: Use backup FPGA boot PROM Use normal FPGA boot PROM	 Insert J1. Remove J1.
PABS Flash Write Protect: Write-enable PABS Flash area Protect PABS Flash area	 Remove J2. Insert J2.
VME Reset: Card generates VME resets Card generates card-only resets	 Insert J3. Remove J3.
Change the CPU1 Execution Sequence: (see page 3-23 for more information) Boot to application Boot to GPM only	 Remove J4. Insert J4.
Change the CPU0 Execution Sequence: (see page 3-23 for more information) Normal boot Boot to GPM only	 Remove J5. Insert J5.
Application Flash Write Protect: Write-enable application Flash area Protect application Flash area.	 Remove J6. Insert J6.
VIO Selection for PMC Site 1 (PWB 311114-001): 5 V VIO 3.3 V VIO	 Insert J11. Remove J12. Insert J12. Remove J11. **WARNING:** Make sure that **only one** of these jumpers is inserted.

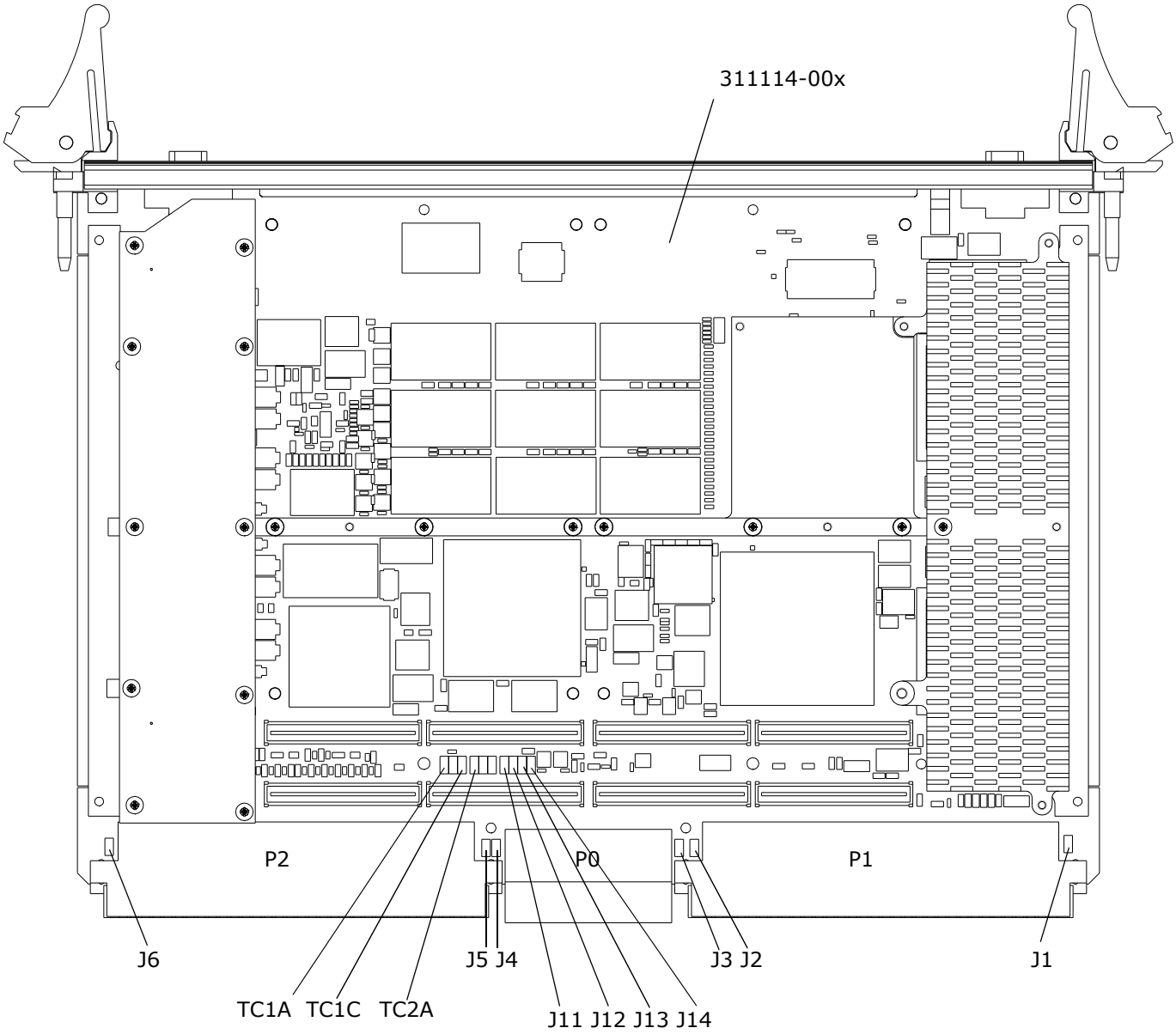
TABLE 2.3: Basecard Jumper Settings Summary (Continued)

Option	Jumper Setting
VIO Selection for PMC Site 1 (PWB 311114-002): 5 V VIO 3.3 V VIO	
VIO Selection for PMC Site 2 (PWB 311114-001): 3.3 V VIO	Insert J13. Remove J14. **WARNING:** VIO on this site must be set to 3.3 V. The site is 5 V tolerant but VIO must be set to 3.3 V.
VIO Selection for PMC Site 2 (PWB 311114-002): 5 V VIO 3.3 V VIO	
Watchdog Timer (CPU0) Power-up Behaviour: Watchdog timer is disabled following power-up Watchdog timer is enabled following power-up	 Insert TC1A. Remove TC1A.
Watchdog Timer (CPU1) Power-up Behaviour: Watchdog timer is disabled following power-up Watchdog timer is enabled following power-up	 Insert TC2A. Remove TC2A.
NoVRAM Write Protect: Protect NoVRAM Allow writes to NoVRAM	 Insert TC1C. Remove TC1C.
Boot from Protected Access Boot Site (PABS) (PWB 311114-001): Boot from PABS Normal Boot	 Connect P0-A10 to GND. Leave P0-A10 unconnected.
Boot from Protected Access Boot Site (PABS) (PWB 311114-002): Boot from PABS Normal Boot	 Connect P0-A10 to GND or insert J11. Leave P0-A10 unconnected and remove J11.

Note

All remaining jumpers are reserved for factory use or configuration only.

FIGURE 2.1: SVME/DMV-182 Jumper Locations



BACKUP FPGA BOOT PROM JUMPER

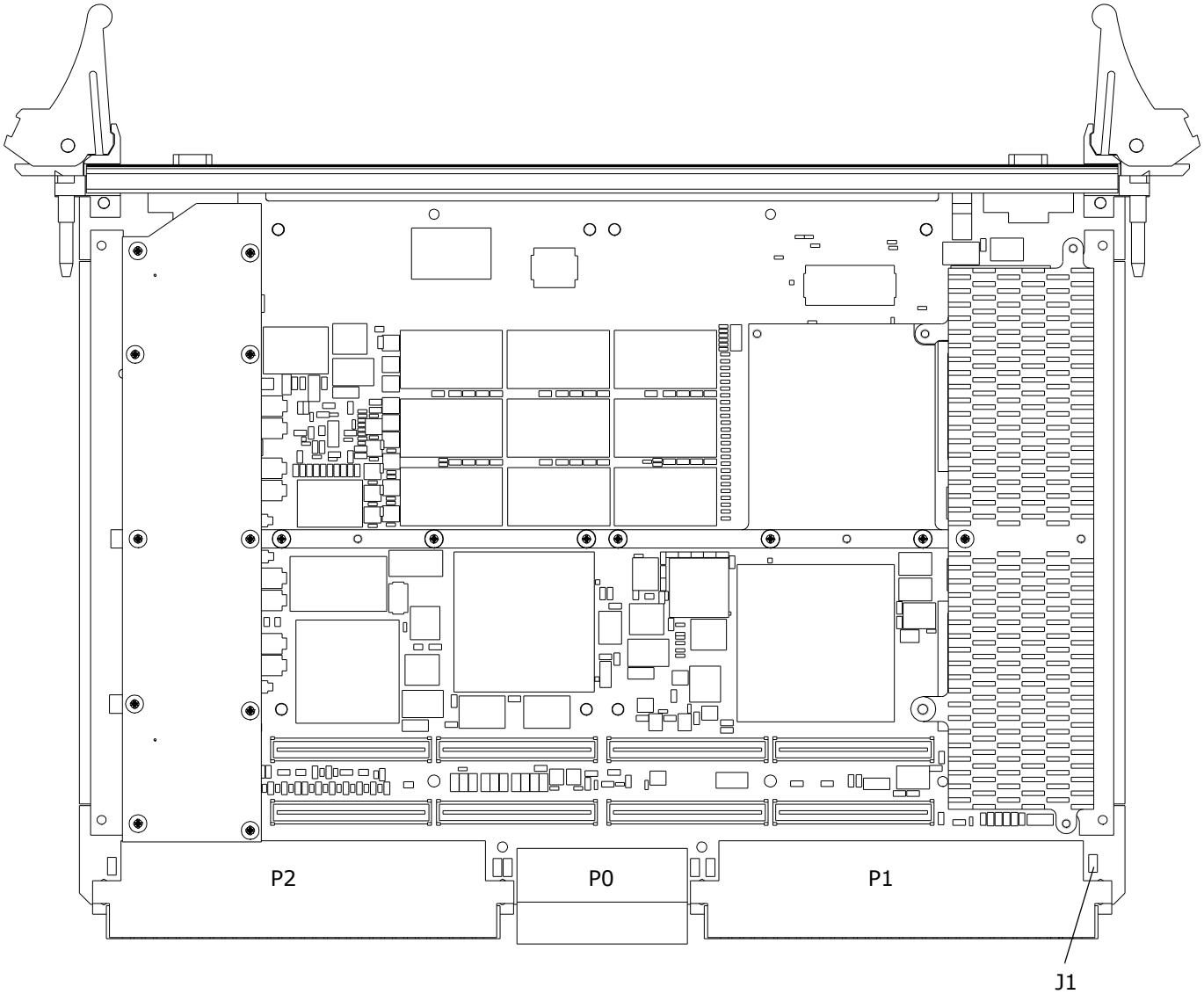
The SVME/DMV-182 provides a jumper to use the backup FPGA boot PROM.

To use the normal FPGA boot PROM, remove the jumper J1. To use the backup FPGA boot PROM, install the jumper J1.

TABLE 2.4: Backup FPGA Boot PROM Jumper

Option	Jumper Settings
Backup FPGA Boot PROM: Use backup FPGA boot PROM Use normal FPGA boot PROM	 Insert J1. Remove J1.

FIGURE 2.2: Backup FPGA Boot PROM Jumper



PABS FLASH WRITE PROTECT JUMPER

The SVME/DMV-182 provides a jumper to protect the PABS (Protected Access Boot System) Flash area.

For normal operation insert the jumper J2 so that the PABS is write-protected. To program the PABS Flash, remove the J2 jumper.

Cross Reference

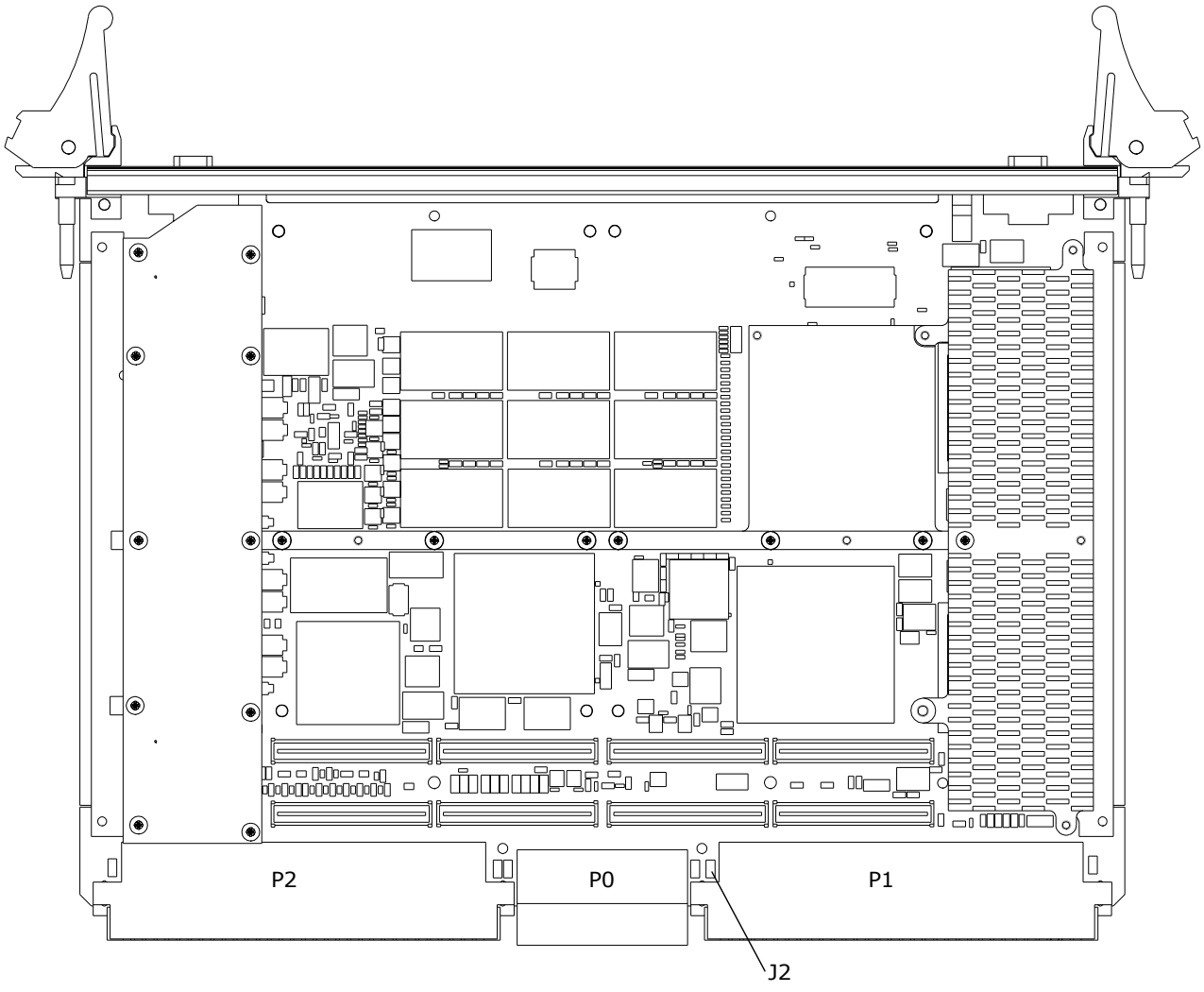
The state of the J2 jumper is shown in the FLASH_BOOT_WP* bit in the EPLD Miscellaneous Control register.

See Chapter 3 of the SVME/DMV-182 Hardware User's Manual for more information.

TABLE 2.5: PABS Flash Write Protect Jumper

Option	Jumper Settings
PABS Flash Write Protect: Write-enable PABS Flash area Protect PABS Flash area	 Remove J2. Insert J2.

FIGURE 2.3: PABS Write Enable Jumper



VME RESET JUMPER

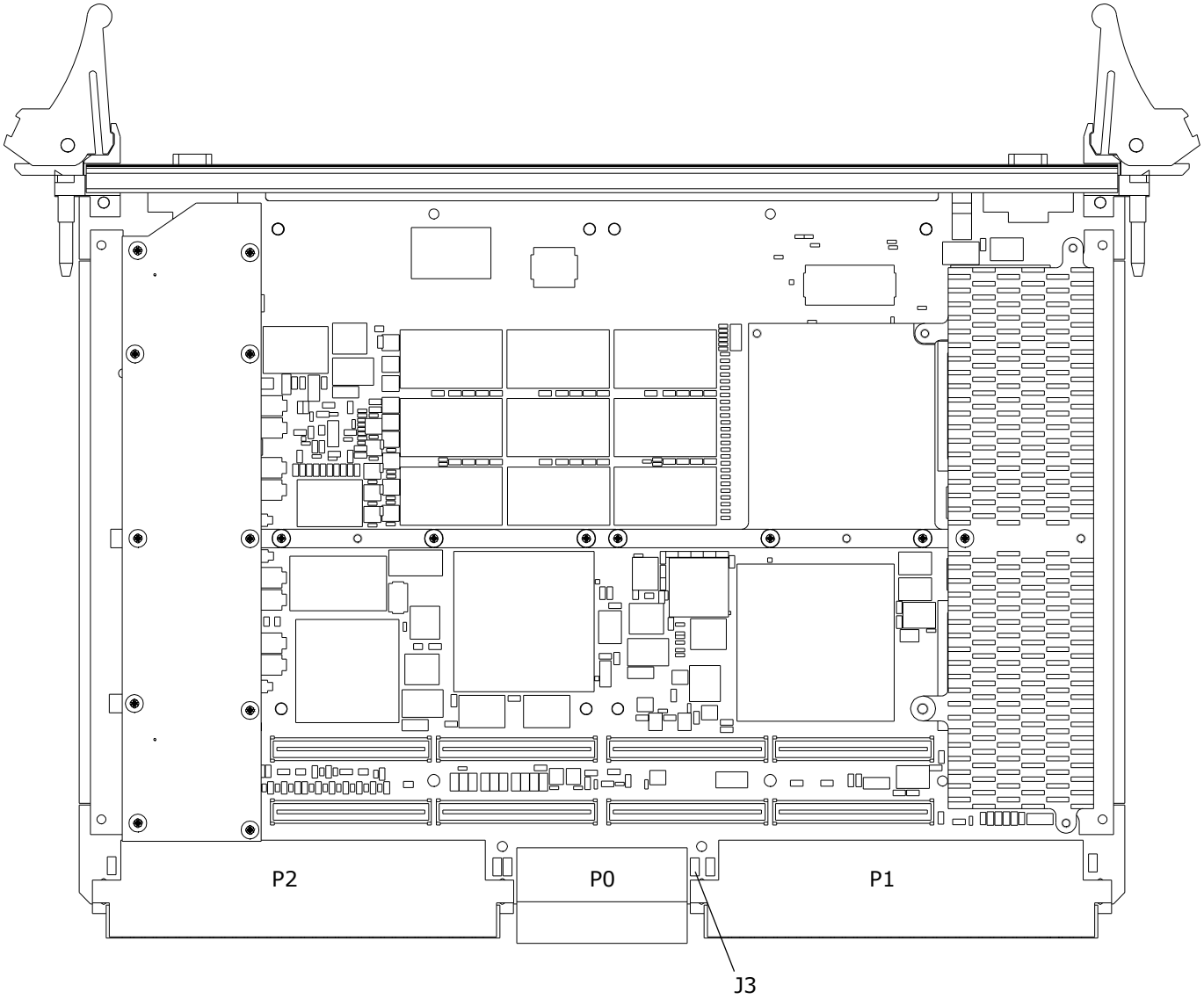
Insert J3 to allow the card to generate VME resets (SYSRESET*). During development, you may want to configure the card so that it does not generate VME resets. In this case, the reset will be card-only.

When VME resets are enabled, the front panel reset input generates a VME reset.

TABLE 2.6: VME Reset Configuration

Option	Jumper Setting
VME Reset: Card generates VME resets Card does not generate VME resets	 Insert J3. Remove J3.

FIGURE 2.4: VME Reset Configuration



EXECUTION SEQUENCE CONTROL JUMPERS

The SVME/DMV-182 has software-readable jumpers J4 and J5. J5 is used to control the Foundation Firmware execution sequence for CPU0. J4 is used to control the Foundation Firmware execution sequence for CPU1.

The onboard Foundation Firmware checks the state (connected or open) of the jumpers on power-up and uses this to select an execution sequence. For CPU0, the execution sequence also depends on the state of the serial channel 1 DSR input. See page 3-23.



Cross Reference

For information on the code executed, refer to the *SVME/DMV-182 FF/W Release Notes*.



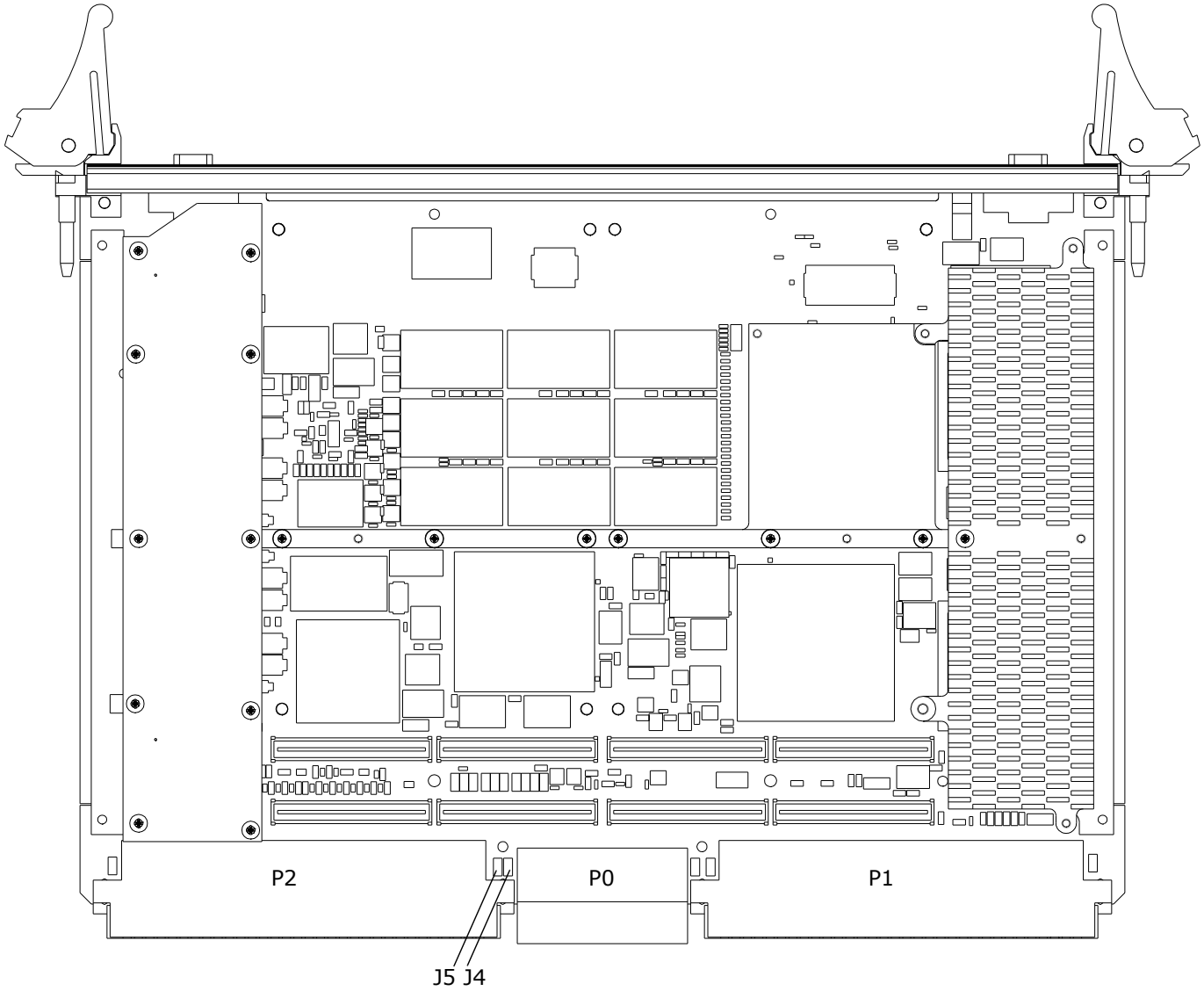
Note

This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

TABLE 2.7: Execution Sequence Configuration

Option	Jumper Setting
Change the CPU1 Execution Sequence: (see page 3-23 for more information) Boot to application Boot to GPM only	 Remove J4. Insert J4.
Change the CPU0 Execution Sequence: (see page 3-23 for more information) Normal boot Boot to GPM only	 Remove J5. Insert J5.

FIGURE 2.5: Execution Sequence Control Jumpers



APPLICATION FLASH WRITE PROTECT JUMPER

The SVME/DMV-182 provides a jumper to protect the application Flash. "Application Flash" means all Flash areas except the PABS Flash. (The application Flash is in the range 0xF002 0000 to 0xF7EF FFFF.)

For normal operation, insert jumper J6 to write-protect the application Flash. To write-enable the application Flash, remove the J6 jumper.

Cross Reference

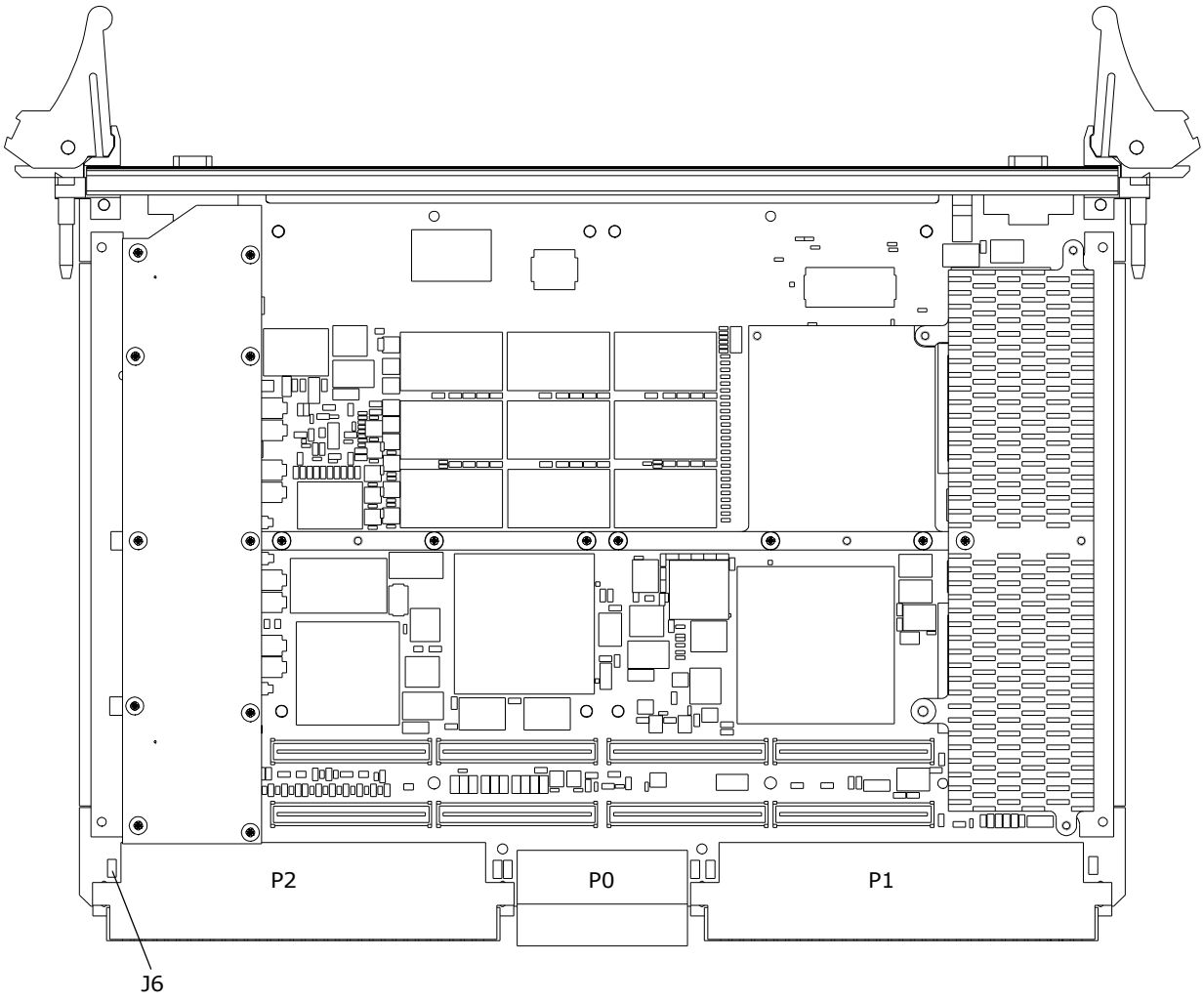
The state of the J6 jumper is shown in the FLASH_ALL_WE* bit in the EPLD Miscellaneous Control register.

See Chapter 3 of the SVME/DMV-182 Hardware User's Manual for more information.

TABLE 2.8: Application Flash Write Protect Jumper

Option	Jumper Settings
Application Flash Write Protect: Write-enable Flash bank Protect Flash bank.	 Remove J6. Insert J6.

FIGURE 2.6: Application Flash Write Protect Jumper



PMC SITE VIO SELECTION JUMPERS

There are jumpers to select the VIO voltage for PMC sites 1 and 2.

The PMC sites are not keyed. The Discovery II signals at 3.3 V. PMC site 2 can accommodate universal, 5 V, or 3.3 V PMCs, regardless of whether the PMCs are 5 V tolerant or not. PMC site 1 is not 5 V-tolerant when VIO is connected to 3.3 V.

Note

The Discovery II always signals at 3.3 V. It cannot damage a 3.3 V PMC.

According to the PCI specification, 3.3 V PMCs do not use VIO.

For universal PMCs, connect VIO to 3.3 V.

Warning

There is a risk of damaging the Discovery II if a 5 V PMC is installed in site 1 while VIO is connected to 3.3 V.

TABLE 2.9: VIO Selection Jumpers - PWB 311114-001

Option	Jumper Settings
VIO Selection for PMC Site 1: 5 V VIO 3.3 V VIO	 Insert J11. Remove J12. Insert J12. Remove J11.
VIO Selection for PMC Site 2: 3.3 V VIO	 Insert J13. Remove J14. **WARNING:** VIO on this site must be set to 3.3 V. The site is 5 V tolerant but VIO must be set to 3.3 V.

TABLE 2.10: VIO Selection Jumpers - PWB 311114-002

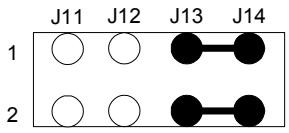
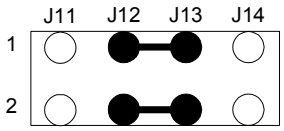
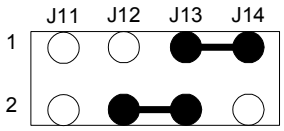
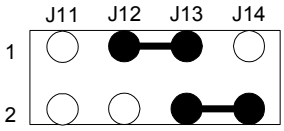
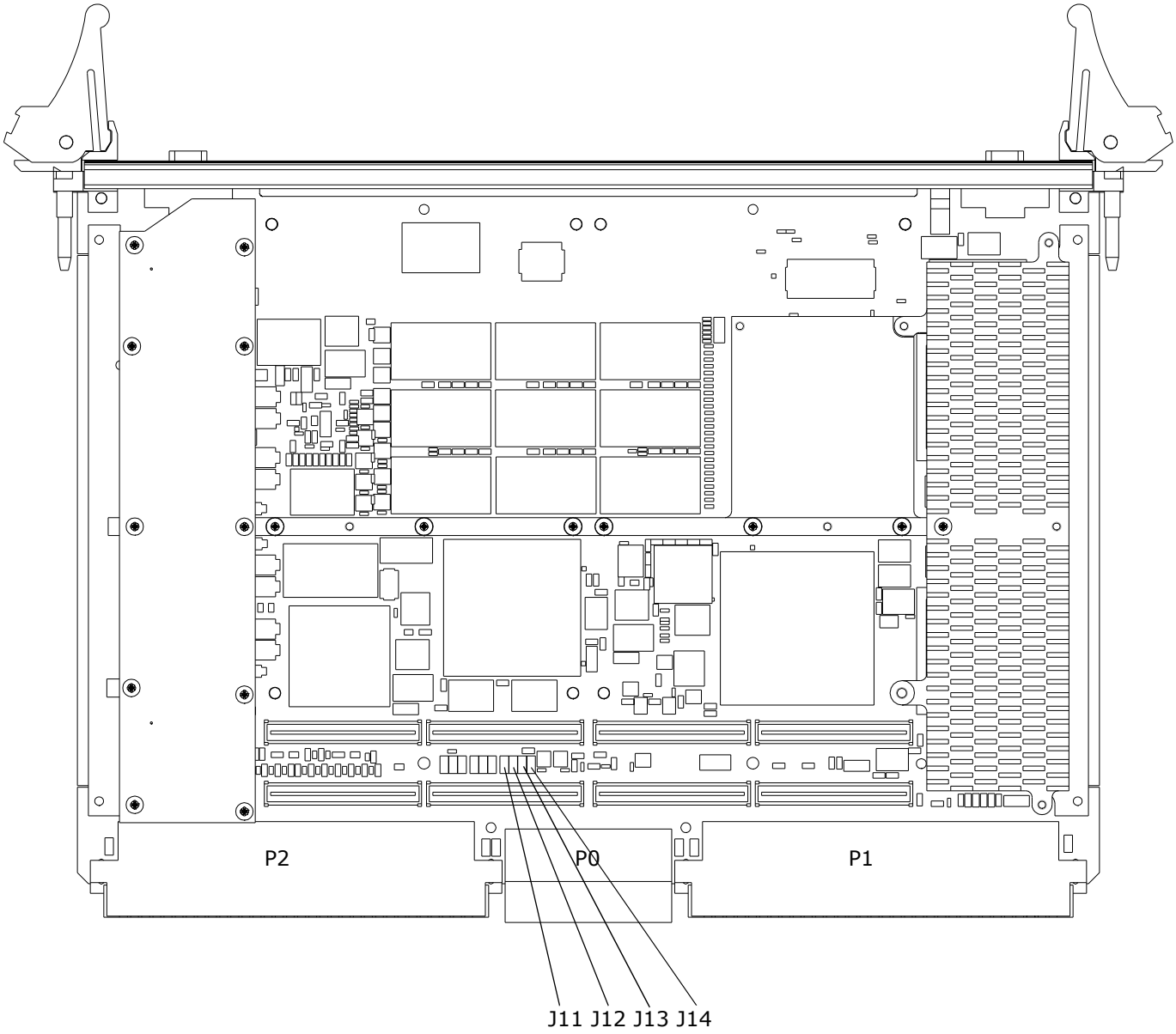
Jumper Settings	Result
	PMC Site 1: 5 V Vio PMC Site 2: 5 V Vio
	PMC Site 1: 3.3 V Vio PMC Site 2: 3.3 V Vio
	PMC Site 1: 5 V Vio PMC Site 2: 3.3 V Vio
	PMC Site 1: 3.3 V Vio PMC Site 2: 5 V Vio

FIGURE 2.7: PMC Site VIO Selection Jumpers



WATCHDOG TIMER POWER-UP RESET BEHAVIOUR SELECTIONS

The SVME/DMV-182 watchdog enabled/disabled states are selected by the watchdog jumpers.

With the watchdog jumper installed, the watchdog timer is disabled following power-up reset. The mode of operation (interrupt or reset) is selected by the watchdog control register. See Chapter 3 of the Hardware User's Manual for more information.



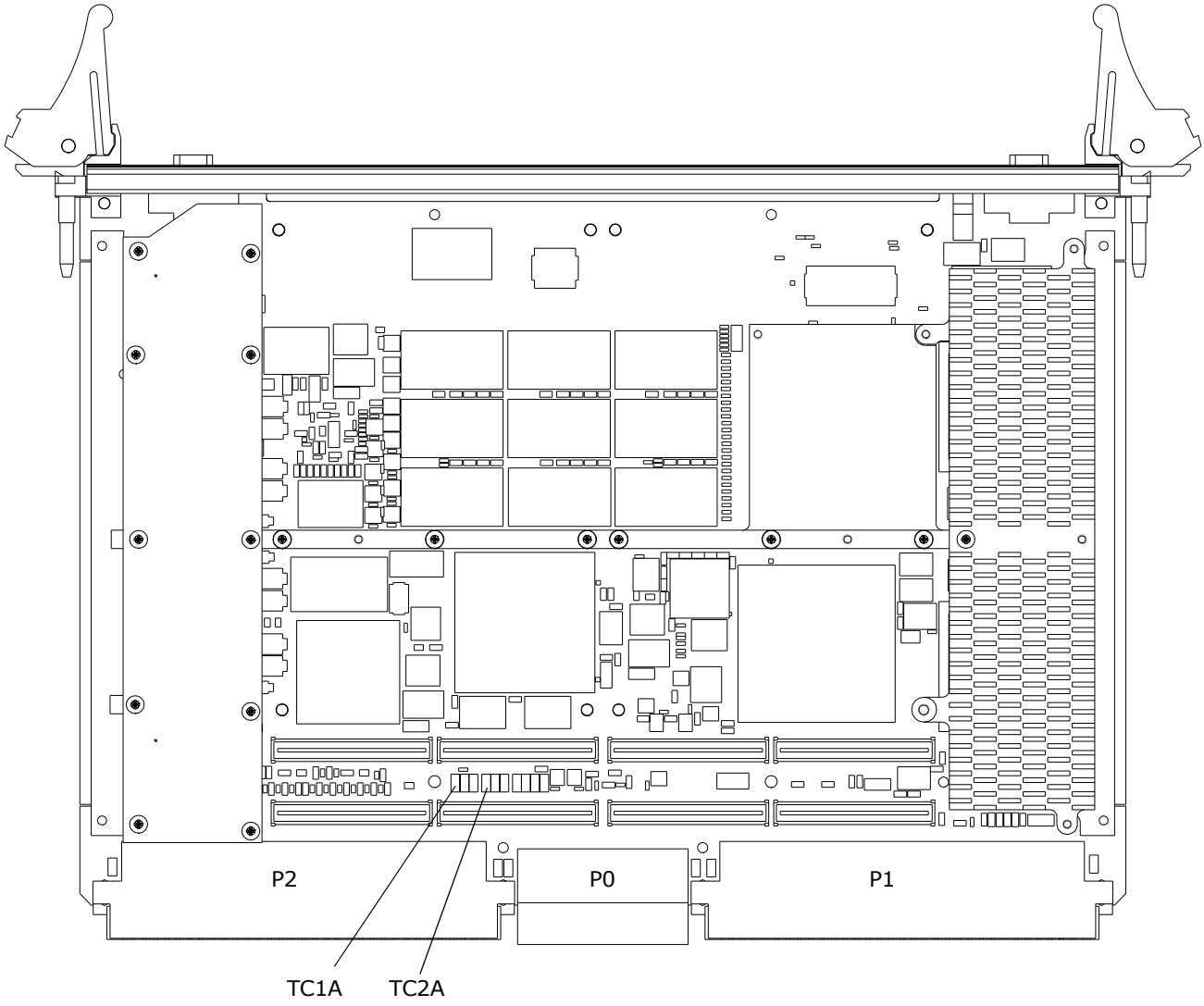
Note

This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

TABLE 2.11: Watchdog Timer Power-up Behaviour

Option	Jumper Settings
Watchdog Timer (CPU0) Power-up Behaviour: Watchdog timer is disabled following power-up Watchdog timer is enabled following power-up	 Insert TC1A. Remove TC1A.
Watchdog Timer (CPU1) Power-up Behaviour: Watchdog timer is disabled following power-up Watchdog timer is enabled following power-up	 Insert TC2A. Remove TC2A.

FIGURE 2.8: Watchdog Timer Power-up Behaviour Jumpers



NOVRAM WRITE PROTECT JUMPER

The SVME/DMV-182 provides a jumper to protect the NoVRAM. (The NoVRAM is 0x8000 bytes large. It appears twice in the range 0xE003 0000 to 0xE003 FFFF.)

Cross Reference

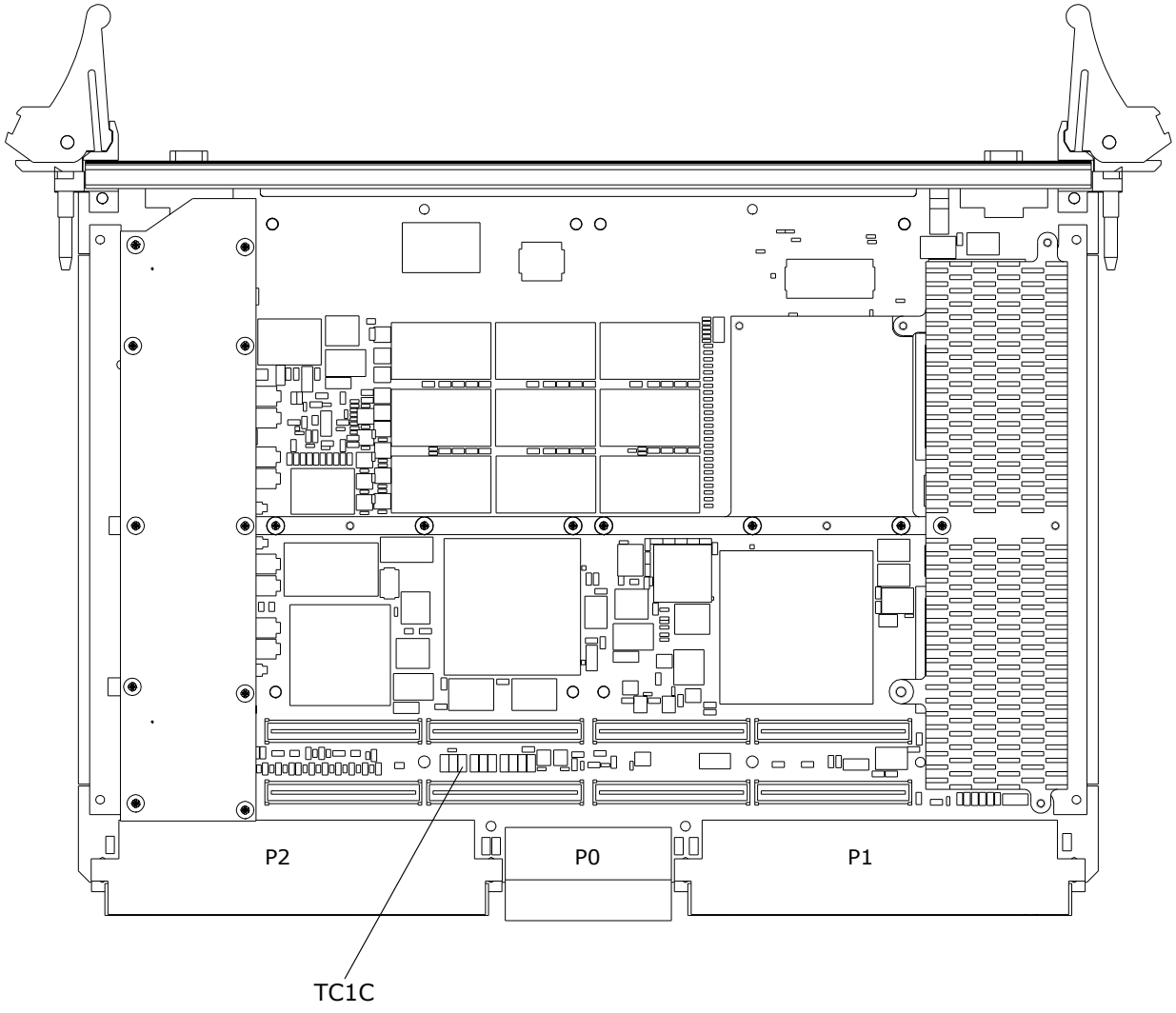
The state of the TC1C jumper is shown in the JMPR_NVRAM_WP bit in the EPLD Reset register.

See Chapter 3 of the SVME/DMV-182 Hardware User's Manual for more information.

TABLE 2.12: NoVRAM Write Protect Jumper

Option	Jumper Settings
NoVRAM Write Protect: Allow writes to NoVRAM Protect NoVRAM	 Remove TC1C. Insert TC1C.

FIGURE 2.9: NoVRAM Write Protect Jumper



BOOTING JUMPER

The SVME/DMV-182 Flash is implemented using AMD Am29PDL128G-compatible devices. These devices include write protection that protects the lowest 128 Kbyte Flash sector (0xF000 0000 through 0xF001 FFFF) and the highest 128 Kbyte Flash sector (0xF7FE 0000 through 0xF7FF FFFF) (PABS). This write protection mechanism is used for a Protected Access Boot System (PABS) on the SVME/DMV-182. It provides a backup boot capability for the SVME/DMV-182. To boot from the PABS, connect backplane pin P0-A10 to ground.

Normally, the SVME/DMV-182 boots from normal Flash. However, if the Foundation Firmware is corrupted, you may boot from the Protected Access Boot Site. Once you have booted the card you may use FFWUPD or NVMP to reprogram the normal Flash. You can then power off the card and remove the link to allow normal booting.

For PWB 311114-001, use the settings described in Table 2.13 to select the bank used for booting. For PWB 311114-002, use the settings described in Table 2.14 to select the bank used for booting.

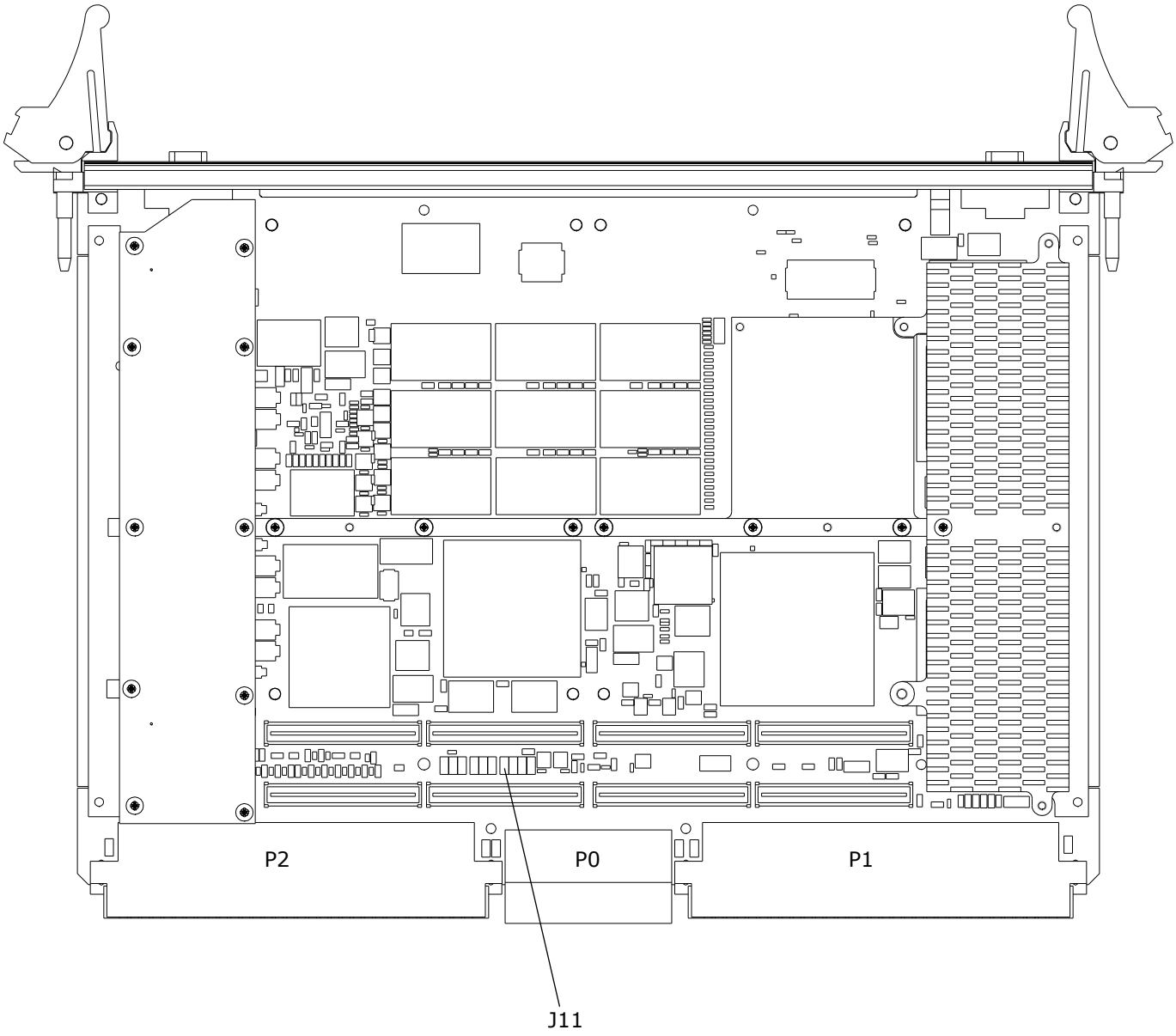
TABLE 2.13: Booting Configuration - PWB 311114-001

Option	Jumper Settings
Boot SVME/DMV-182 from normal Flash.	Leave P0-A10 disconnected.
Boot SVME/DMV-182 from Permanent Alternate Boot System.	Connect P0-A10 to GND.

TABLE 2.14: Booting Configuration - PWB 311114-002

Option	Jumper Settings
Boot SVME/DMV-182 from normal Flash.	Leave P0-A10 disconnected and remove J11.
Boot SVME/DMV-182 from Permanent Alternate Boot System.	Connect P0-A10 to GND or insert J11.

FIGURE 2.10: Booting Jumper - PWB 311114-002 Only



3 HARDWARE INSTALLATION

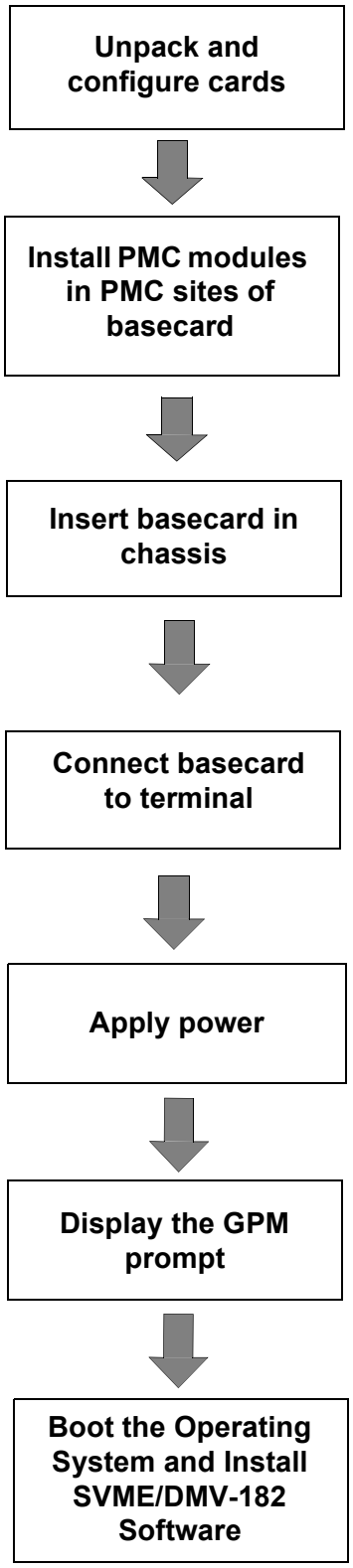
INTRODUCTION

This chapter explains how to install the SVME/DMV-182 in a VME chassis and get it running. Specifically this chapter describes the following procedures:

- inserting the card into a chassis;
- connecting a terminal to the card via a serial communications cable;
- turning on the power and confirming that the Power-up Built-In Test (PBIT) has completed successfully;
- displaying the initial screen message and establishing the card's VME base address; and
- troubleshooting installation problems.

INSTALLATION PROCEDURE SUMMARY

Below is a summary of the installation procedure described in this chapter. If you are experienced, you may wish to use it as a quick installation procedure.



INSTALLATION PROCEDURE

BEFORE YOU BEGIN...



Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until just before the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

Turn the power off before inserting or removing cards from the VME chassis. Failure to do so could damage the card circuitry or cause personal injury.

UNPACK AND CONFIGURE THE CARDS

Before installing the card into a chassis, ensure that you complete the pre-installation tasks described in Chapter 2 of this manual and the pre-installation tasks described in the User's Manuals for the PMC modules.

INSTALL THE PMC MODULES ON THE BASECARD

If the PMC modules are not already installed on the basecard, install them in a PMC slot of your basecard using the appropriate mounting kits.

When the PMC module is mounted in slot 1 (near the P0 connector), its I/O signals are available on the backplane P0 connector. When the PMC module is mounted in slot 2 (near the P2 connector), its I/O signals are available on the backplane P2 connector. See Figure 1.4, "Location of PMC Modules and Interface Personality Module," on page 1-7.



Cross Reference

See the *SVME/DMV-182 Generic Drawing* or the *User's Manual* for your PMC module for instructions. The documents for interoperable PMCs are included on the Technical Documentation CD-ROM.

CHOOSE A VME SLOT LOCATION

Select Slot 1, the left-most slot in the VME chassis, if you want the basecard to be the System Controller (SYSCON).

If you intend to use another card as the SYSCON, select the left-most unoccupied slot.

All VME cards should be installed in adjacent slots. Depending on the backplane used, leaving empty slots may cause problems with interrupts and Bus Grant signals. (This is generally a problem with older style VME backplanes.)

INSERT THE BASECARD IN THE CHASSIS

Ensure that the chassis power is turned off before inserting the card.

SVME-182

An SVME basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors on this faceplate facilitate insertion of the basecard into the 160-contact, 5-row connectors for P1 and P2.

Ensure the basecard is completely and firmly seated. Then tighten the screws at the top and bottom of the faceplate.

DMV-182

With DMV basecards, you must use a significant amount of insertion force to mate the backplane connectors with the VME backplane. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Ensure the basecard is completely and firmly seated. Then use a torque driver/wrench to tighten the wedgelocks at the top and bottom of the card. The required torque is 6 in-lbs.

CONNECT A TERMINAL

In order to access the features available within the embedded firmware on the SVME/DMV-182, you will need to attach a terminal or PC-emulated equivalent to each CPU on the card. Use Serial Channel 1 to communicate with CPU0. Use Serial Channel 2 to communicate with CPU1. You can connect a terminal to the SVME/DMV-182 in one of the following ways:

- via the front panel FP1 connector using a serial cable such as CBL-182-FPL-000 (for the SVME-182 version product only);
- via the P2 connector using a P2 interface cable such as CBL-SBC-P2-000 (for both SVME and DMV-182 version products).



Tip

Default serial communication parameters are 9600 N, 8, 1 (9600 baud, no parity, 8 bits, 1 stop bit). Flow control should be "none".

See the SCFG command in the *Foundation Firmware User's Manual* for instructions on changing these parameters.

To change the power-up default settings, use the Configuration Boot Monitor. This is described in the *Foundation Firmware User's Manual.*

Ordering Cables

The cable assemblies described in Table 2.2 on page 2-3 are available by ordering individual cables by their part numbers. Should you need to develop your own cabling solution, please refer to Chapter 2 of the Hardware User's Manual for complete interface pinout listings for the FP1, FP2, P0, and P2 interfaces.

Serial Communications via the Front Panel FP1 Connector

The SVME-182 has two 9-pin connectors on the front panel. FP1 provides access to EIA-232 serial channels 1 and 2.

Figure 3.1 illustrates the front panel and CBL-182-FPL-000 cable set. The signal mapping for Serial Channel 1 is shown in Table 3.1. The signal mapping for Serial Channel 2 is shown in Table 3.2.

FIGURE 3.1: SVME-182 Front Panel I/O Cable (CBL-182-FPL-000)

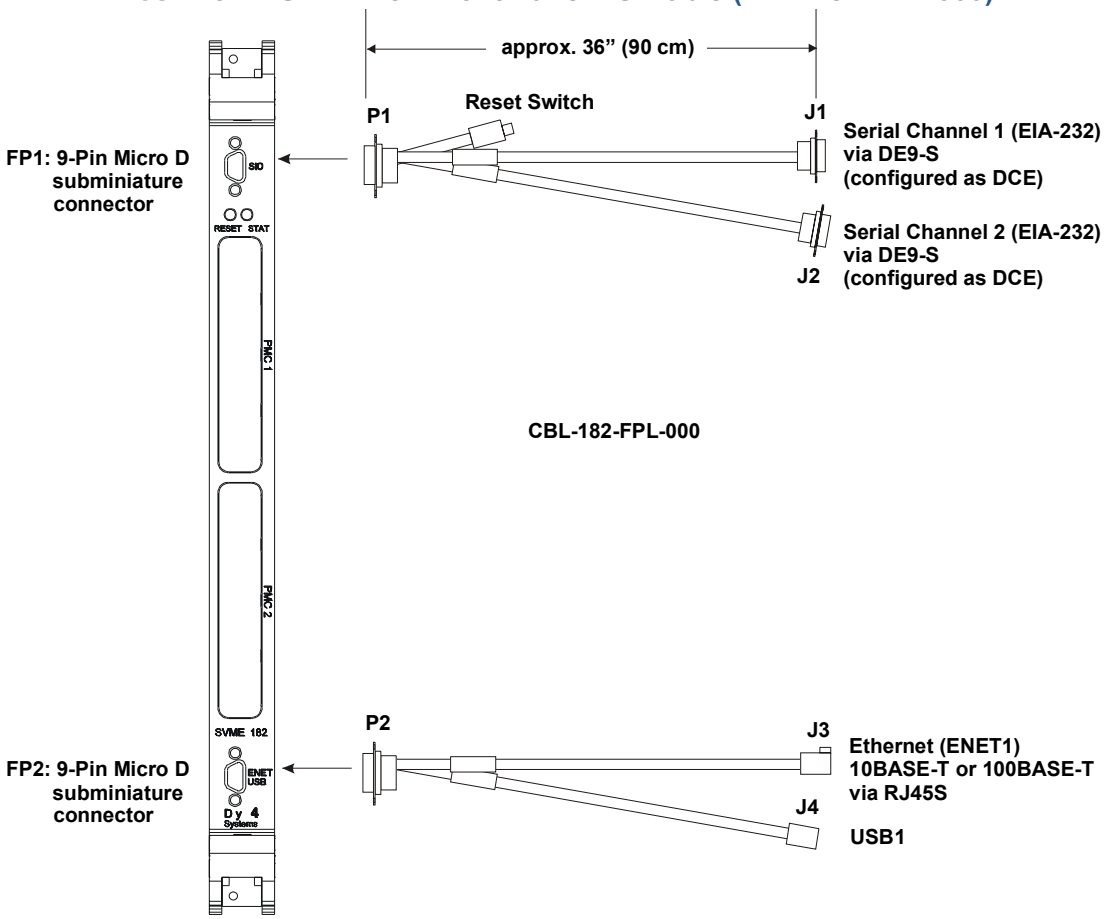


Table 3.1: Front Panel Cable P1 to J1 Signal Mapping

Signal Name	SVME-182 FP1 Connector	Cable P1 Connector	Serial Channel 1 J1 Connector
GND	FP1-5	P1-1	J1-5
CH1DSR	FP1-7	P1-7	J1-4
CH1RXD	FP1-6	P1-6	J1-3
CH1TXD	FP1-8	P1-8	J1-2

Table 3.2: Front Panel Cable P1 to J2 Signal Mapping

Signal Name	SVME-182 FP1 Connector	Cable P1 Connector	Serial Channel 2 J2 Connector
GND	FP1-5	P1-1	J2-5
CH2RXD	FP1-3	P1-3	J2-3
CH2TXD	FP1-2	P1-4	J2-2

Note

The SVME-182 EIA-232 serial channels are configured as DTE (Data Terminal Equipment). The EIA-232 serial channels on personal computers and terminals are also configured as DTE. A null modem is required for communication between two DTEs.

The front panel cable provides the required null modem connections.

Cross Reference

The CH1DSR signal is used to control the power-up execution sequence of CPU0. See "Control the Power-Up Execution Sequence" on page 3-23 for more information.

Serial Communications via the P2 Connector

For an SVME/DMV-182 with a Mode 1 IPM (serial, 8-bit SCSI), connection from the SVME/DMV-182 P2 interface to the terminal is provided by the P2 I/O cable assembly, CBL-SBC-P2-000. For a card with a different IPM, use an appropriate cable as shown in Table 2.2 on page 2-3.

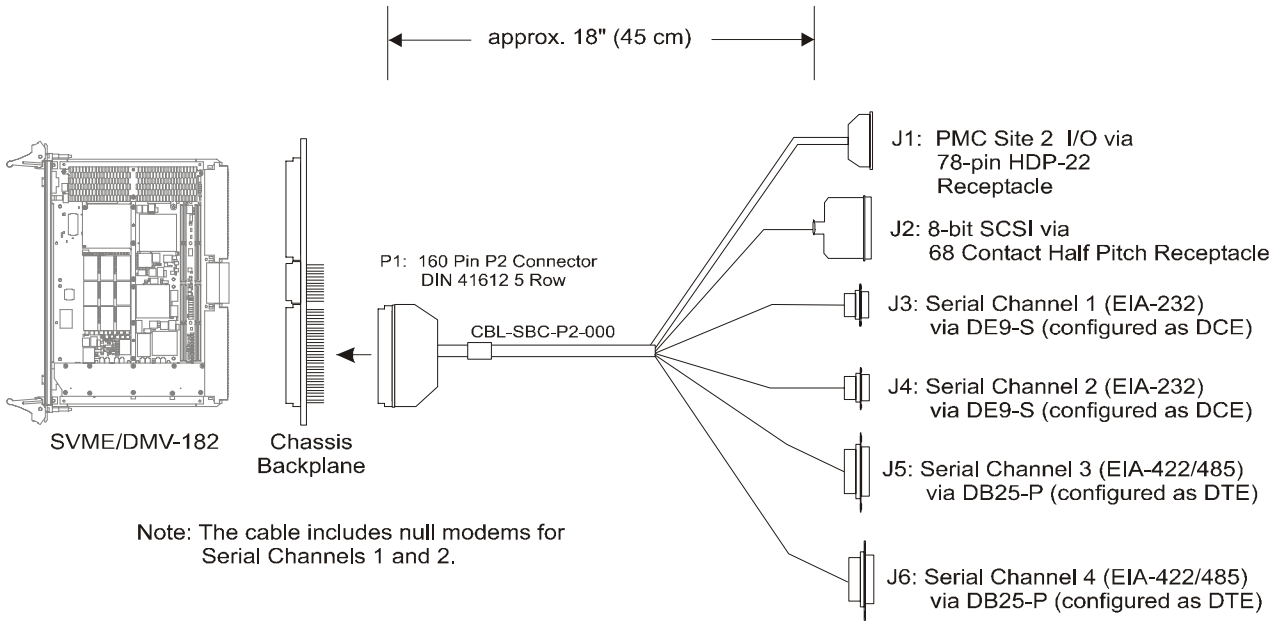
Cross Reference

Consult the Product Release Notes to determine the IPM installed on the card.

Information on the other P2 cables is provided on the Technical Documentation CD-ROM under "Drawings".

Install the P2 I/O cable assembly by carefully pressing the cable P1 connector onto the P2 backplane connector stakes as shown in Figure 3.2. The cable J3 connector is used to connect CPU0 to a terminal. The cable J4 connector is used to connect CPU1 to a terminal.

Figure 3.2 Serial Connections via P2



CBL-SBC-P2-000 J3 (Serial Channel 1) Connector Pinouts

The mapping of Serial Channel 1 EIA-232 signals from the CBL-SBC-P2-000 P1 connector to the DE9-S connectors (CBL-SBC-P2-000 J3) is shown in Table 3.3.

Table 3.3: CBL-SBC-P2-000 P1 to J3 (Serial Channel 1) Signal Mapping

Signal Name	SVME/DMV-182 P2 Connector	Cable P1 Connector	Serial Channel 1 J3 Connector
CH1TXD	P2-D17	E17	J3-2
CH1RXD	P2-D18	E18	J3-3
CH1DSR	P2-D19	E19	J3-4
GND	P2-B31	C31	J3-5

CBL-SBC-P2-000 J4 (Serial Channel 2) Connector Pinouts

The mapping of Serial Channel 2 EIA-232 signals from the CBL-SBC-P2-000 P1 connector to the DE9-S connector (CBL-SBC-P2-000 J4) is shown in Table 3.4.

Table 3.4: CBL-SBC-P2-000 P1 to J4 (Serial Channel 2) Signal Mapping

Signal Name	SVME/DMV-182 P2 Connector	Cable P1 Connector	Serial Channel 2 J4 Connector
CH2TXD	P2-D30	E30	J4-2
CH2RXD	P2-Z19	A19	J4-3
GND	P2-B31	C31	J4-5



Note

The tables show connection information for the **cable**. The pin numbering conventions for the P1 connector of the cable are **not** the same as for the backplane P2 connector. For backplane pinout information, see Chapter 2 of the Hardware User's Manual.



Note

The SVME/DMV-182 EIA-232 serial channels are configured as DTE (Data Terminal Equipment). The EIA-232 serial channels on personal computers and terminals are also configured as DTE. A null modem is required for communication between two DTEs.

The P2 cable provides the required null modem connections.



Cross Reference

The CH1DSR signal is used to control the power-up execution sequence. See "Control the Power-Up Execution Sequence" on page 3-23 for more information.

CONNECT TO A NETWORK

Some features available within the embedded firmware on the SVME/DMV-182, require connecting the CPUs to an Ethernet network. You can connect the SVME/DMV-182 to a network as follows:

- via the front panel FP2 connector using cable set CBL-182-FPL-000 (for the SVME-182 version product only); this port is used to communicate with CPU0; and
- via the P0 connector using cable CBL-182-P0-000 (for both SVME and DMV-182 version products); this port is used to communicate with CPU1.



The FP2 connector provides access to ENET1, the 10/100BaseT Ethernet port.

The P0 connector provides access to ENET2, the 10/100/1000BaseT Ethernet port.

ENET1 is also accessible on the P2 connector, but the standard cables do not provide access to it.

Ordering Cables

The cable assemblies described in Table 2.2 on page 2-3 are available by ordering individual cables by their part numbers. Should you need to develop your own cabling solution, please refer to Chapter 2 of the Hardware User's Manual for complete interface pinout listings for the FP1, FP2, P0, and P2 interfaces.

Ethernet1 Connection via the Front Panel FP2 Connector

The SVME-182 has two 9-pin connectors on the front panel. FP2 provides access to ENET1 which is used by CPU0.

Figure 3.3 illustrates the front panel and CBL-182-FPL-000 cable set. The signal mapping for ENET1 is shown in Table 3.5.

FIGURE 3.3: ENET1 Connection via Front Panel

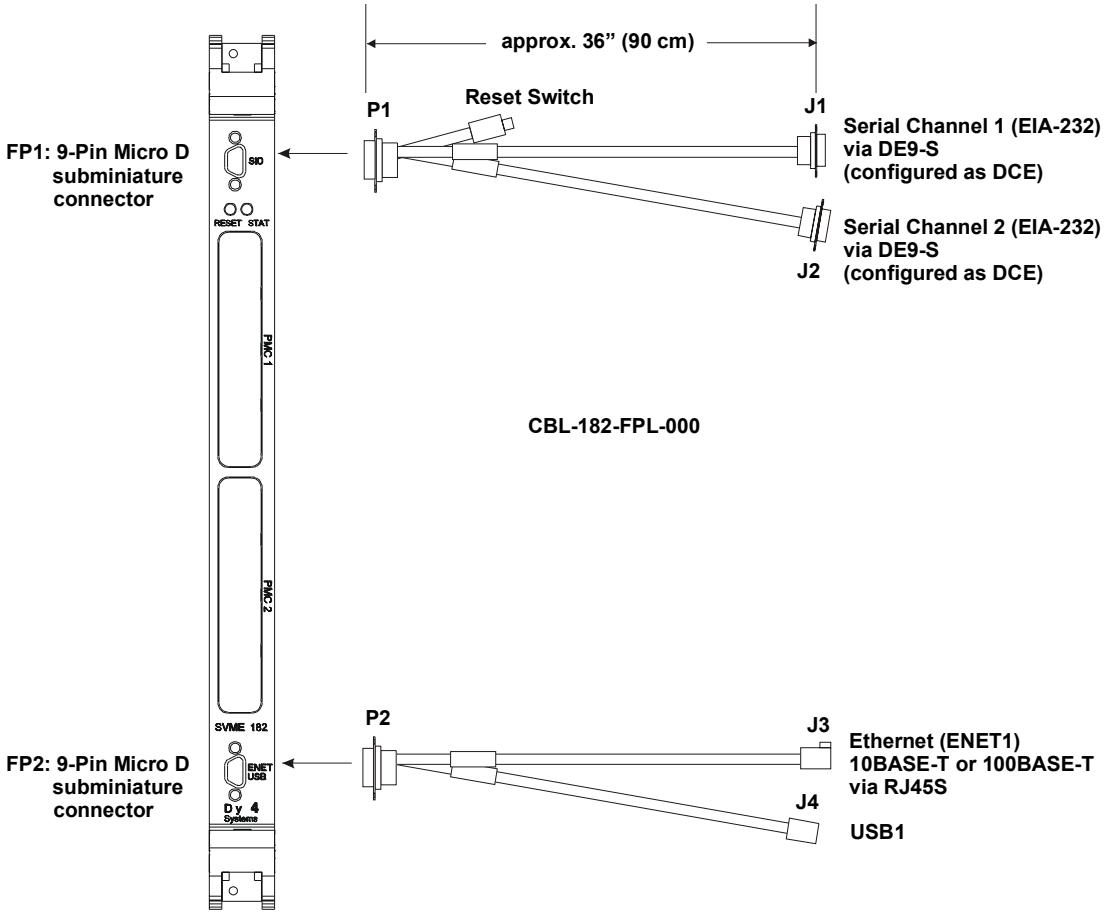


Table 3.5: Front Panel Cable P2 to J3 Signal Mapping

Signal Name	SVME-182 FP2 Connector	Cable P2 Connector	Ethernet1 J3 Connector
ENET1_RXD-	FP2-1	P2-5	J3-6
ENET1_RXD+	FP2-2	P2-4	J3-3
ENET1_TXD+	FP2-5	P2-1	J3-1
ENET1_TXD-	FP2-4	P2-2	J3-2

Ethernet2 Connection via the P0 Interface

Connection with the SVME/DMV-182 P0 interface is provided by the standard CBL-182-P0-000 cable assembly. This Ethernet port is used by CPU1.

Install the CBL-182-P0-000 cable assembly by carefully pressing the cable P1 connector onto the P0 backplane connector stakes. The cable P1 connector has a tag labelled "Pin 1". Connect the cable so that this tag is at the top of the chassis P0 connector.

SVME/DMV-182 basecard-related functions are available via this cable, as described below in Figure 3.4.

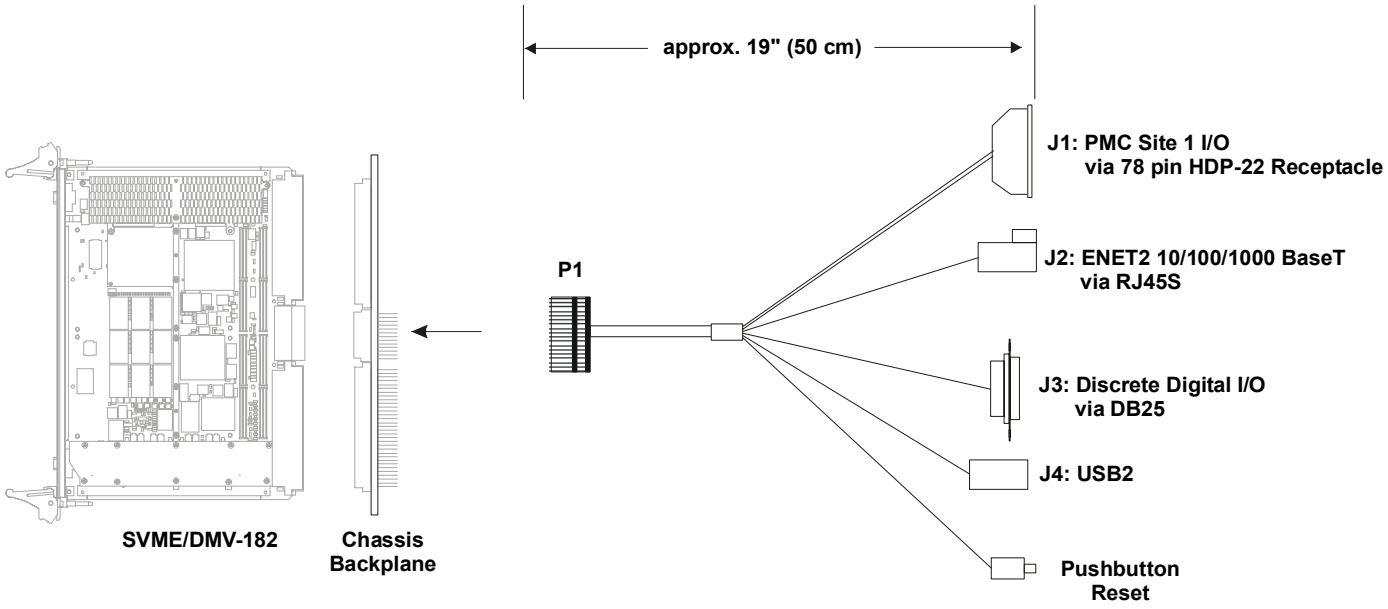
Note

The cable J2 connector may be connected to a 10/100/1000BaseT Ethernet port.

Warning

Exercise care when inserting and extracting the P0 I/O cable as the P0 backplane pins can be easily bent if the cable connector is not properly aligned.

FIGURE 3.4: ENET2 Connection via P0



The mapping of Ethernet 2 signals from the CBL-182-P0-000 P1 connector to the RJ45 connector (CBL-182-P0-000 J2) is shown in Table 3.6.

Table 3.6: CBL-182-P0-000 P1 to J2 (Ethernet RJ45) Signal Mapping

Signal Name	SVME/DMV-182 P0 Connector	Cable P1 Connector	Cable J2 Connector
ENET2_TRD(0)+ /ENET2_TXD+	P0-B2	P1-B2	J2-1
ENET2_TRD(0)- /ENET2_TXD-	P0-A2	P1-A2	J2-2
ENET2_TRD(1)+ /ENET2_RXD+	P0-B3	P1-B3	J2-3
ENET2_TRD(1)- /ENET2_RXD-	P0-A3	P1-A3	J2-6
ENET2_TRD(2)+	P0-B1	P1-B1	J2-4
ENET2_TRD(2)-	P0-A1	P1-A1	J2-5
ENET2_TRD(3)+	P0-D1	P1-D1	J2-7
ENET2_TRD(3)-	P0-C1	P1-C1	J2-8

CONNECT OTHER PERIPHERALS VIA THE FRONT PANEL FP1 AND FP2 CONNECTORS

The SVME-182 has two 9-pin connectors on the front panel. FP1 provides a reset switch and access to two EIA-232 serial channels (1 and 2). FP2 provides an Ethernet 10BaseT or 100BaseT interface (ENET 1) and a USB port (USB 1). The front panel cable set (CBL-182-FPL-000) routes the different interfaces to separate connectors. Figure 3.5 illustrates the front panel and CBL-182-FPL-000 cable set.

The signal mapping for the CBL-182-FPL-000 cable is shown in Tables 3.1, 3.2, 3.7, and 3.8.

Figure 3.5 Other Connections via FP1 and FP2

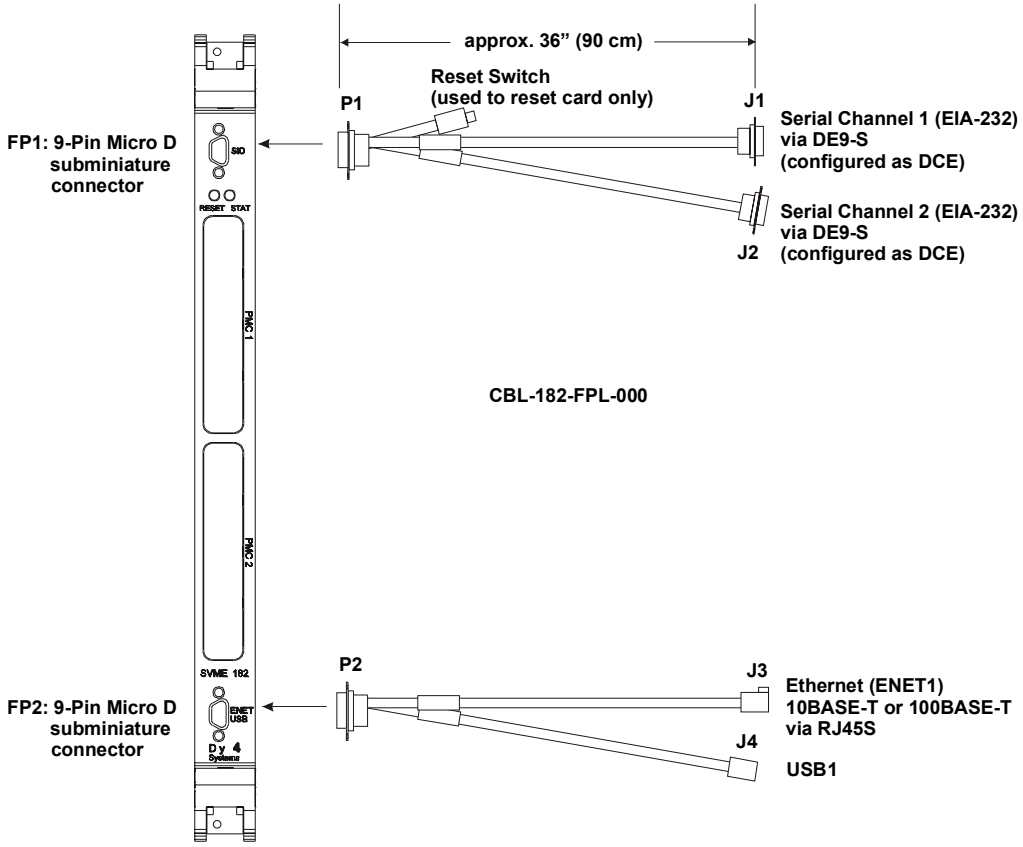


Table 3.7: Front Panel Cable P1 to PB1 Signal Mapping

Signal Name	SVME-182 FP1 Connector	Cable P1 Connector	Reset Pushbutton PB1 Switch
GND	FP1-5	P1-1	PB1-2
FP_RESET-	FP1-9	P1-9	PB1-1

Table 3.8: Front Panel Cable P2 to J4 Signal Mapping

Signal Name	SVME-182 FP2 Connector	Cable P2 Connector	USB1 J4 Connector
USB1+	FP2-8	P2-8	J4-3
GND_USB1	FP2-9	P2-9	J4-4
VCC_USB1	FP2-6	P2-6	J4-1
USB1-	FP2-7	P2-7	J4-2

CONNECT OTHER PERIPHERALS VIA THE P2 CONNECTOR

For an SVME/DMV-182 with a Mode 1 IPM (serial, 8-bit SCSI), connection with the SVME/DMV-182 P2 interface is provided by the CBL-SBC-P2-000 cable assembly. For a card with a different I/O mode, use an appropriate cable as shown in Table 2.2 on page 2-3.

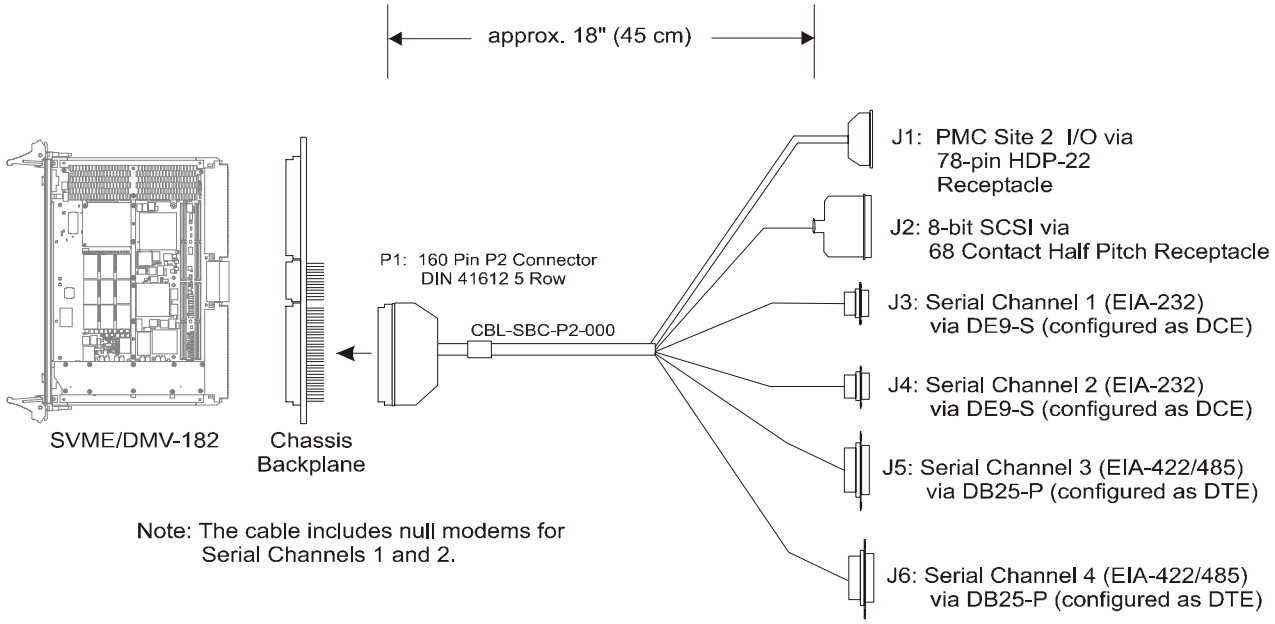
Cross Reference

Consult the Product Release Notes to determine the I/O mode of the card.

Information on the other P2 cables is provided on the Technical Documentation CD-ROM under "Drawings".

Install the CBL-SBC-P2-000 cable assembly by carefully pressing the cable P1 connector onto the P2 backplane connector stakes. SVME/DMV-182 basecard-related functions are available via this cable, as shown in Figure 3.6.

Figure 3.6 SVME/DMV-182 P2 Cable Connections



Warning

Exercise care when inserting and extracting the P2 I/O cable as the P2 backplane pins can be easily bent if the cable connector is not properly aligned.

Note

Tables 3.9 through 3.13 show connection information for the **cable**. The pin numbering conventions for the P1 connector of the cable are **not** the same as for the backplane P2 connector. For backplane pinout information, see Chapter 2 of the Hardware User's Manual.

Table 3.9: CBL-SBC-P2-000 I/O Cable Connector Information

Connector	Manufacturer's Part Number	Description	Function
P1	ERNI 024070	DIN 41612, 5 row Connector	P2 Connector
J2	Assmann AK-Y1301	Half Pitch 68 Contact Male SCSI Receptacle	8-bit SCSI (Using 16-bit SCSI Connector)
J3, J4	AMP 205203-1	D SUB Receptacle DE9S	EIA-232
J5, J6	AMP 205208-1	D SUB Receptacle DB25P	EIA-422/485
J1	AMP 748569-1	78 Contact HDP-22 Receptacle	PMC I/O

CBL-SBC-P2-000 J5, J6 (Serial Channels 3, 4) Connector Pinouts

The mapping of Serial Channels 3 and 4 EIA-422 signals from the CBL-SBC-P2-000 P1 connector to the DB25-P connectors (CBL-SBC-P2-000 J5, J6) is shown in Table 3.10.

Table 3.10: CBL-SBC-P2-000 P1 to J5, J6 (Serial Channel 3, 4) Signal Mapping

Signal Name	SVME/DMV-182 P2 Connector	Cable P1 Connector	Serial Channel 3 and 4 J5, J6 Connectors
CH3TXD_A	P2-D11	E11	J5-2
CH3TXD_B	P2-D12	E12	J5-14
CH3RXD_A'	P2-D14	E14	J5-3
CH3RXD_B'	P2-D13	E13	J5-16
CH3TXC_A	P2-D15	E15	J5-15
CH3TXC_B	P2-D16	E16	J5-24
CH3RXC_A'	P2-Z21	A21	J5-17
CH3RXC_B'	P2-Z23	A23	J5-25
GND	P2-B12	C12	J5-7
CH4TXD_A	P2-D26	E26	J6-2
CH4TXD_B	P2-D27	E27	J6-14
CH4RXD_A'	P2-D21	E21	J6-3
CH4RXD_B'	P2-D20	E20	J6-16
CH4TXC_A	P2-D22	E22	J6-15
CH4TXC_B	P2-D23	E23	J6-24
CH4RXC_A'	P2-D25	E25	J6-17
CH4RXC_B'	P2-D24	E24	J6-25
GND	P2-B12	C12	J6-7



Note

The EIA-422 TXD and RXD signals on the cable J6 connector are **not** on the pins specified by the EIA-530 standard. If you require connectors compliant with EIA-530, build a cable adapter using the information in Table 3.11.

Table 3.11: Signal Mapping from Cable J5, J6 Connectors to EIA-530

Signal Name	Cable J5, J6 Connector	EIA-530 Standard Connector (without null modem)	EIA-530 Standard Connector (with null modem)
TXD_A	2	2	5
TXD_B	14	14	17
RXD_A'	3	5	2
RXD_B'	16	17	14
GND	7	7	7

CBL-182-422/232

CBL-182-422/232 is a 422/232 adapter cable which connects to the EIA-422 serial channel connectors of the 182 P2 cable.

Signal Name	P2 Cable J5, J6 Connector CBL-182-422/232 P1	CBL-182-422/232 J1
TXD	14	2
RXD	3	3
GND	7	7

CBL-SBC-P2-000 J2 (SCSI) Connector Pinouts

The mapping of SCSI signals from the CBL-SBC-P2-000 P1 connector to the 68-contact half pitch SCSI connector (CBL-SBC-P2-000 J2 Connector) is shown in Table 3.12.

Table 3.12: CBL-SBC-P2-000 P1 to J2 (68-Contact D SUB) Signal Mapping

Signal Name	SVME/DMV -182 P2 Connector	Cable P1 Connector	SCSI J2 Connector	Signal Name	SVME/DMV -182 P2 Connector	Cable P1 Connector	SCSI J2 Connector
-DB(0)	P2-Z1	A1	40	GND	P2-Z22	A22	16
GND	P2-Z2	A2	6	GND	P2-Z24	A24	20
-DB(1)	P2-Z3	A3	41	GND	P2-Z26	A26	21
GND	P2-Z4	A4	7	GND	P2-Z28	A28	22
-DB(2)	P2-Z5	A5	42	GND	P2-Z30	A30	23
GND	P2-Z6	A6	8	GND	P2-Z32	A32	24
-DB(3)	P2-Z7	A7	43	-ATN	P2-D1	E1	55
GND	P2-Z8	A8	9	-BSY	P2-D2	E2	57
-DB(4)	P2-Z9	A9	44	-ACK	P2-D3	E3	58
GND	P2-Z10	A10	10	-RST	P2-D4	E4	59
-DB(5)	P2-Z11	A11	45	-MSG	P2-D5	E5	60
GND	P2-Z12	A12	11	-SEL	P2-D6	E6	61
-DB(6)	P2-Z13	A13	46	-C/D	P2-D7	E7	62
GND	P2-Z14	A14	12	-REQ	P2-D8	E8	63
-DB(7)	P2-Z15	A15	47	-I/O	P2-D9	E9	64
GND	P2-Z16	A16	13	TERMPWRB	P2-D10	E10	17
-DB(P)	P2-Z17	A17	48	TERMPWRB	P2-D10	E10	18
GND	P2-Z18	A18	14	TERMPWRB	P2-D10	E10	51
GND	P2-Z20	A20	15	TERMPWRB	P2-D10	E10	52

Note

The SVME/DMV-182 provides TERMPWR as specified in SCSI-2.

When connecting a SCSI peripheral, make sure to configure the peripheral to accept TERMPWR from the SCSI bus. This is a jumper setting on the SCSI peripheral.

CBL-SBC-P2-000 J1 (PMC Site 2 I/O) Connector Pinouts

The mapping of PMC site 2 I/O signals from the CBL-SBC-P2-000 P1 connector to the 78-contact HDP-22 receptacle (CBL-SBC-P2-000 J1) is shown in Table 3.13.



Note

In the following table, PMC_XX indicates the signal on pin XX of the Pn4/Jn4 connector of the module in PMC site 2.

Table 3.13: CBL-SBC-P2-000 P1 to J1 (PMC I/O) Signal Mapping

Signal Name	SVME/DMV -182 P2 Connector	Cable P1 Connector	Cable J1 Connector	Signal Name	SVME/DMV -182 P2 Connector	Cable P1 Connector	Cable J1 Connector
PMC_01	P2-C1	P1-D1	J1-9	PMC_33	P2-C17	P1-D17	J1-71
PMC_02	P2-A1	P1-B1	J1-16	PMC_34	P2-A17	P1-B17	J1-38
PMC_03	P2-C2	P1-D2	J1-31	PMC_35	P2-C18	P1-D18	J1-48
PMC_04	P2-A2	P1-B2	J1-17	PMC_36	P2-A18	P1-B18	J1-60
PMC_05	P2-C3	P1-D3	J1-10	PMC_37	P2-C19	P1-D19	J1-70
PMC_06	P2-A3	P1-B3	J1-18	PMC_38	P2-A19	P1-B19	J1-61
PMC_07	P2-C4	P1-D4	J1-3	PMC_39	P2-C20	P1-D20	J1-49
PMC_08	P2-A4	P1-B4	J1-19	PMC_40	P2-A20	P1-B20	J1-44
PMC_09	P2-C5	P1-D5	J1-11	PMC_41	P2-C21	P1-D21	J1-15
PMC_10	P2-A5	P1-B5	J1-20	PMC_42	P2-A21	P1-B21	J1-39
PMC_11	P2-C6	P1-D6	J1-6	PMC_43	P2-C22	P1-D22	J1-50
PMC_12	P2-A6	P1-B6	J1-36	PMC_44	P2-A22	P1-B22	J1-55
PMC_13	P2-C7	P1-D7	J1-12	PMC_45	P2-C23	P1-D23	J1-32
PMC_14	P2-A7	P1-B7	J1-37	PMC_46	P2-A23	P1-B23	J1-56
PMC_15	P2-C8	P1-D8	J1-13	PMC_47	P2-C24	P1-D24	J1-51
PMC_16	P2-A8	P1-B8	J1-1	PMC_48	P2-A24	P1-B24	J1-57
PMC_17	P2-C9	P1-D9	J1-29	PMC_49	P2-C25	P1-D25	J1-74
PMC_18	P2-A9	P1-B9	J1-2	PMC_50	P2-A25	P1-B25	J1-40
PMC_19	P2-C10	P1-D10	J1-14	PMC_51	P1-C26	P1-D26	J1-68
PMC_20	P2-A10	P1-B10	J1-4	PMC_52	P1-A26	P1-B26	J1-41
PMC_21	P2-C11	P1-D11	J1-30	PMC_53	P2-C27	P1-D27	J1-33
PMC_22	P2-A11	P1-B11	J1-21	PMC_54	P2-A27	P1-B27	J1-58
PMC_23	P2-C12	P1-D12	J1-42	PMC_55	P2-C28	P1-D28	J1-78
PMC_24	P2-A12	P1-B12	J1-22	PMC_56	P2-A28	P1-B28	J1-59
PMC_25	P2-C13	P1-D13	J1-77	PMC_57	P2-C29	P1-D29	J1-73
PMC_26	P2-A13	P1-B13	J1-5	PMC_58	P2-A29	P1-B29	J1-75
PMC_27	P2-C14	P1-D14	J1-23	PMC_59	P2-C30	P1-D30	J1-63
PMC_28	P2-A14	P1-B14	J1-24	PMC_60	P2-A30	P1-B30	J1-76
PMC_29	P2-C15	P1-D15	J1-69	PMC_61	P2-C31	P1-D31	J1-64
PMC_30	P2-A15	P1-B15	J1-43	PMC_62	P2-A31	P1-B31	J1-65
PMC_31	P1-C16	P1-D16	J1-45	PMC_63	P2-C32	P1-D32	J1-66
PMC_32	P1-A16	P1-B16	J1-62	PMC_64	P2-A32	P1-B32	J1-67

CONNECT OTHER PERIPHERALS VIA THE P0 CONNECTOR

Connection with the SVME/DMV-182 P0 interface is provided by the standard CBL-182-P0-000 cable assembly.

Install the CBL-182-P0-000 cable assembly by carefully pressing the cable P1 connector onto the P0 backplane connector stakes. The cable P1 connector has a tag labelled "Pin 1". Connect the cable so that this tag is at the top of the chassis P0 connector.

SVME/DMV-182 basecard-related functions are available via this cable, as described below in Figure 3.7.

Warning

Exercise care when inserting and extracting the P0 I/O cable as the P0 backplane pins can be easily bent if the cable connector is not properly aligned.

FIGURE 3.7: Expanded I/O via P0

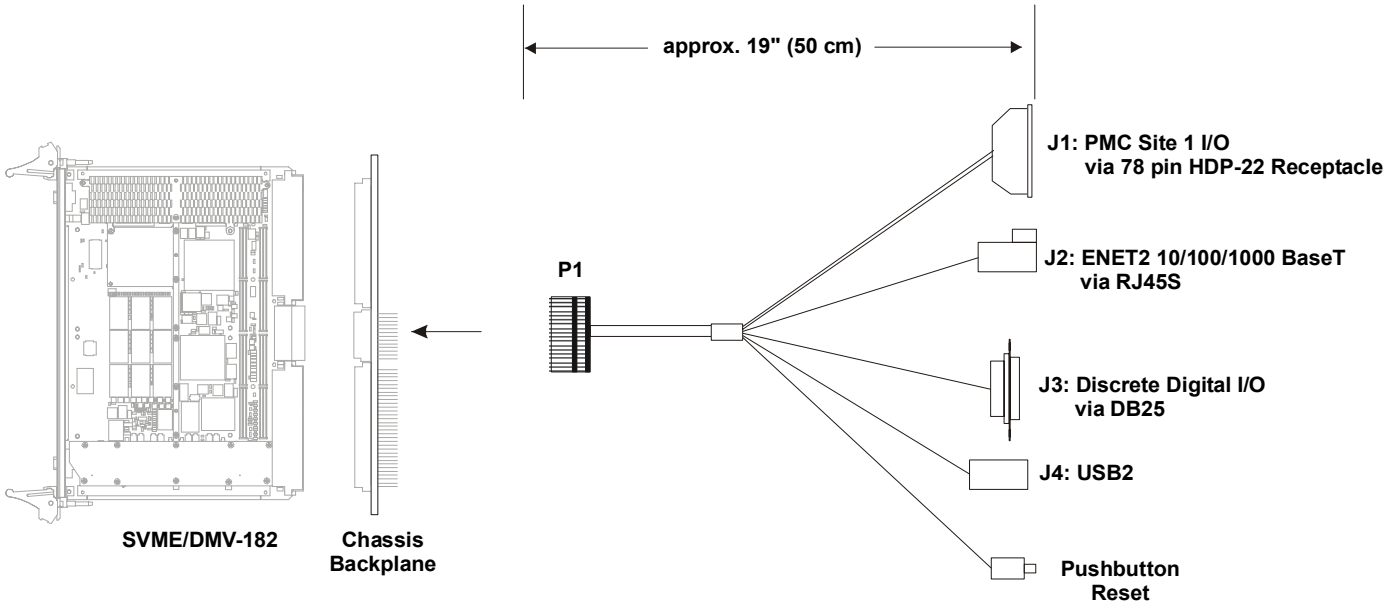


Table 3.14: CBL-182-P0-000 Cable Connector Information

Connector	Manufacturer's Part Number	Description	Function
P1	AMP 98-3165-105-01	95-contact 5-row Connector	95-Pin P0 Connector
J1	AMP 78569-1	78-contact HD-22 Receptacle	PMC Site 1 I/O
J2	PANDUIT CJ588IW	Connector jack, unshielded	Ethernet2
J3	AMP 205207-1	D-Sub Receptacle DB25	Discrete Digital I/O
J4	ASSMANN AU-Y1005	USB Connector	USB2
SW1	SwitchCraft 921K	Pushbutton Reset	Reset Switch

CBL-182-P0-000 J1 (PMC Site 1 I/O) Connector Pinout

The mapping of PMC Site 1 I/O signals from the CBL-182-P0-000 P1 connector to the 78-pin PMC Site 1 I/O connector (CBL-182-P0-000 J1) is shown in Table 3.15.



Note

In the following table, PMC_XX indicates the signal on pin XX of the Pn4/Jn4 connector of the module in PMC site 1.

Table 3.15: CBL-182-P0-000 P1 to J1 (PMC Site 1 I/O) Signal Mapping

Signal Name	SVME/DMV -182 P0 Connector	Cable P1 Connector	Cable J1 Connector	Signal Name	SVME/DMV -182 P0 Connector	Cable P1 Connector	Cable J1 Connector
PMC_01	P0-E4	P1-E4	J1-9	PMC_33	P0-C13	P1-C13	J1-71
PMC_02	P0-D4	P1-D4	J1-16	PMC_34	P0-B13	P1-B13	J1-38
PMC_03	P0-C4	P1-C4	J1-31	PMC_35	P0-A13	P1-A13	J1-48
PMC_04	P0-B4	P1-B4	J1-17	PMC_36	P0-E14	P1-E14	J1-60
PMC_05	P0-A4	P1-A4	J1-10	PMC_37	P0-D14	P1-D14	J1-70
PMC_06	P0-E5	P1-E5	J1-18	PMC_38	P0-C14	P1-C14	J1-61
PMC_07	P0-D5	P1-D5	J1-3	PMC_39	P0-B14	P1-B14	J1-49
PMC_08	P0-C5	P1-C5	J1-19	PMC_40	P0-A14	P1-A14	J1-44
PMC_09	P0-B5	P1-B5	J1-11	PMC_41	P0-E15	P1-E15	J1-15
PMC_10	P0-A5	P1-A5	J1-20	PMC_42	P0-D15	P1-D15	J1-39
PMC_11	P0-E6	P1-E6	J1-6	PMC_43	P0-C15	P1-C15	J1-50
PMC_12	P0-D6	P1-D6	J1-36	PMC_44	P0-B15	P1-B15	J1-55
PMC_13	P0-C6	P1-C6	J1-12	PMC_45	P0-A15	P1-A15	J1-32
PMC_14	P0-B6	P1-B6	J1-37	PMC_46	P0-E16	P1-E16	J1-56
PMC_15	P0-A6	P1-A6	J1-13	PMC_47	P0-D16	P1-D16	J1-51
PMC_16	P0-E7	P1-E7	J1-1	PMC_48	P0-C16	P1-C16	J1-57
PMC_17	P0-D7	P1-D7	J1-29	PMC_49	P0-B16	P1-B16	J1-74
PMC_18	P0-C7	P1-C7	J1-2	PMC_50	P0-A16	P1-A16	J1-40
PMC_19	P0-B7	P1-B7	J1-14	PMC_51	P0-E17	P1-E17	J1-68
PMC_20	P0-A7	P1-A7	J1-4	PMC_52	P0-D17	P1-D17	J1-41
PMC_21	P0-E8	P1-E8	J1-30	PMC_53	P0-C17	P1-C17	J1-33
PMC_22	P0-D8	P1-D8	J1-21	PMC_54	P0-B17	P1-B17	J1-58
PMC_23	P0-C8	P1-C8	J1-42	PMC_55	P0-A17	P1-A17	J1-78
PMC_24	P0-B8	P1-B8	J1-22	PMC_56	P0-E18	P1-E18	J1-59
PMC_25	P0-A8	P1-A8	J1-77	PMC_57	P0-D18	P1-D18	J1-73
PMC_26	P0-E12	P1-E12	J1-5	PMC_58	P0-C18	P1-C18	J1-75
PMC_27	P0-D12	P1-D12	J1-23	PMC_59	P0-B18	P1-B18	J1-63
PMC_28	P0-C12	P1-C12	J1-24	PMC_60	P0-A18	P1-A18	J1-76
PMC_29	P0-B12	P1-B12	J1-69	PMC_61	P0-E19	P1-E19	J1-64
PMC_30	P0-A12	P1-A12	J1-43	PMC_62	P0-D19	P1-D19	J1-65
PMC_31	P0-E13	P1-E13	J1-45	PMC_63	P0-C19	P1-C19	J1-66
PMC_32	P0-D13	P1-D13	J1-62	PMC_64	P0-B19	P1-B19	J1-67

CBL-182-P0-000 J3 (Discrete Digital I/O) Connector Pinout

The mapping of discrete I/O signals from the CBL-182-P0-000 P1 connector to the DB25-s connector (CBL-182-P0-000 J3) is shown in Table 3.16.

Table 3.16: CBL-182-P0-000 P1 to J3 (Discrete Digital I/O) Signal Mapping

Signal Name	SVME/DMV-182 P0 Connector	Cable P1 Connector	Cable J3 Connector
DIO(0)	P0-A9	P1-A9	J3-1
DIO(1)	P0-B9	P1-B9	J3-2
DIO(2)	P0-B10	P1-B10	J3-3
DIO(3)	P0-C9	P1-C9	J3-4
DIO(4)	P0-C10	P1-C10	J3-5
DIO(5)	P0-D9	P1-D9	J3-6
DIO(6)	P0-D10	P1-D10	J3-7
DIO(7)	P0-E9	P1-E9	J3-8
DIO(8)	P0-E10	P1-E10	J3-9
DIO(9)	P0-E2	P1-E2	J3-10
DIO(10)	P0-E3	P1-E3	J3-11
DIO(11)	P0-A19	P1-A19	J3-12
DIO(12)	P0-A11	P1-A11	J3-13
DIO(13)	P0-E1	P1-E1	J3-14
GND	P0-C2	P1-C2	J3-17

CBL-182-P0-000 J4 (USB2) Connector Pinout

The mapping of USB2 signals from the CBL-182-P0-000 P1 connector to the USB connector (CBL-182-P0-000 J4) is shown in Table 3.17.

Table 3.17: CBL-182-P0-000 P1 to J4 (USB2) Signal Mapping

Signal Name	SVME/DMV-182 P0 Connector	Cable P1 Connector	Cable J4 Connector
VCC_USB2	P0-B11	P1-B11	J4-1
USB2+	P0-C11	P1-C11	J4-3
USB2-	P0-D11	P1-D11	J4-2
GND_USB2	P0-E11	P1-E11	J4-4

CBL-182-P0-000 SW1 (Reset Switch) Connector Pinout

The mapping of reset signals from the CBL-182-P0-000 P1 connector to the SW1 connector (CBL-182-P0-000 SW1) is shown in Table 3.18.

Table 3.18: CBL-182-P0-000 P1 to SW1 (Reset Switch) Signal Mapping

Signal Name	SVME/DMV-182 P0 Connector	Cable P1 Connector	Cable SW1
FP_RESET-	P0-C3	P1-C3	SW1-1
GND	P0-C2	P1-C2	SW1-2

CONTROL THE POWER-UP EXECUTION SEQUENCE

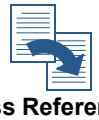
The power-up execution sequence for the Foundation Firmware depends on the settings of the jumpers J4 and J5 and the state of the Serial Channel 1 DSR line. The factory-default power-up sequences are shown in Tables 3.19 and 3.20. Power-up sequences may be modified using GPM's Configuration Boot Manager. (Consult Chapter 4 of the Foundation Firmware User's Manual for more information.)

Table 3.19: CPU0 Foundation Firmware Execution Sequence

J5 State	DSR State	Execution Sequence
CPU0 User Link (J5) off	DSR negated (cable out)	PBIT → Default Application → GPM When the SVME/DMV-182 boots, CPU0 executes PBIT and then calls the default application. If the default application returns, it returns to GPM.
CPU0 User Link (J5) off	DSR asserted (terminal connected to SVME/DMV-182 Serial Channel 1)	PBIT → GPM → Default Application → GPM When the SVME/DMV-182 boots, CPU0 executes PBIT and then GPM. Type "rts" at the GPM prompt to call the default application. If the default application returns, it returns to GPM.
CPU0 User Link (J5) on	DSR negated (cable out)	Default Application → GPM When the SVME/DMV-182 boots, CPU0 calls the default application immediately. If the default application returns, it returns to GPM.
CPU0 User Link (J5) on	DSR asserted (terminal connected to SVME/DMV-182 Serial Channel 1)	GPM → Default Application → GPM When the SVME/DMV-182 boots, CPU0 calls GPM.

Table 3.20: CPU1 Foundation Firmware Execution Sequence

J4 State	Foundation Firmware Release	Execution Sequence
CPU1 User Link (J4) off	FF/W 9 (Rel 1.4 and lower)	Application When the SVME/DMV-182 boots, CPU1 calls the default application.
CPU1 User Link (J4) on	FF/W 9 (Rel 1.4 and lower)	GPM → Default Application When the SVME/DMV-182 boots, CPU1 executes GPM. Type "rts" at the GPM prompt to call the default application.
	FF/W 10 (Rel 1.5 and higher)	CPU1 always boots directly into the application.



Cross Reference

Power-up Built-In-Test (PBIT) is an application that is run at power-up to execute a preconfigured list of Card Level Diagnostics (CLD). For more information about PBIT, see the *Foundation Firmware User's Manual,* included on the Technical Documentation CD-ROM.



Note

This manual describes dual-CPU variants of the SVME/DMV-182. For a single-CPU variant, simply ignore all references to CPU1.

Foundation Firmware Used During Power-Up

The card can run the following programs during power-up:

- **Power-up Built-In Test (PBIT)**: PBIT tests all major subsystems on the card. Test results are placed in the Diagnostic Results Table (DRT).
- **General Purpose Monitor (GPM)**: The GPM is the standard monitor shipped with most SBCs. This allows users to examine memory, download and execute programs and communicate with other boards in the VME system.
- **Default Application**: This is any user application programmed into the on-board Flash. The VxWorks boot loader is initially programmed as the default application for both CPUs.

INITIATE THE POWER-UP SEQUENCE

This section describes the normal power-up behaviour of the SVME/DMV-182.

Power-Up

Switch the VME chassis on.

Initial LED Activity

Immediately on power-up, both the red FAIL LED and green STATUS LED will light up.

Once the card passes its initial diagnostics, PBIT turns the red FAIL LED off. If a diagnostic fails, the red FAIL LED remains lit. In either case, the green STATUS LED remains lit.



Cross Reference

If the red FAIL LED stays on after power-up, then PBIT has found one or more problems or the selected execution sequence did not include PBIT. Refer to the Troubleshooting section on page 3-25 for information on locating the problem.

DISPLAY THE INITIAL SCREEN MESSAGE

After control is transferred to the GPM, the GPM will display a sign-on message similar to the following:

```
SVME/DMV-182 PowerPC 7455 General Purpose Monitor, Version 9.0
Copyright 2004 Dy 4 Systems Inc.doing business as Curstiss-Wright
Controls Embedded Computing

Type ? for help

(CPU 0) 48000000*
```



Note

The last line is the initial prompt which shows the VMEbus base address of the card. In this example the base address is 0x4800 0000. If the VME base address is not appropriate for your system, you may change it. See “VMEbus Base Addresses” on page 4-7 for more information.



Note

Type '?' at the prompt to display the help screen for the GPM. For more detailed information on using the GPM, refer to the *Foundation Firmware User’s Manual*.

ENABLE CPU1

Beginning with Foundation Firmware Release 1.4, CPU1 is disabled by default. To enable CPU1 follow these steps:

1. At the GPM prompt, type

   ```
   cbm
   ```

2. Select **Configure Preferences**.
3. Select **CPU Mode**.
4. Select **Dual CPU**.
5. Select **Exit**.
6. Select **Exit**.

TROUBLESHOOTING

VERIFY INSERTION IN CHASSIS

Power down the chassis. Make sure that the card is properly seated in the VME chassis. Because of the five-row backplane, a considerable amount of insertion force is required.

VERIFY THAT PMC MODULE HAS 3.3 V POWER

If there is a PMC module mounted on the SVME/DMV-182, it will cause unpredictable behaviour if it is not properly powered. Many PMC modules require 3.3 V power. If this is the case, ensure that 3.3 V is present on the P1 connector of the backplane. PMC 3.3 V power is obtained from the backplane, **not** the basecard.

VERIFY THAT PCI VIO IS CONNECTED

Make sure that a PCI_VIO jumper is connected for each occupied PMC site. (See page 2-14.)

FAIL LED STAYS LIT

If the red FAIL LED stays lit after power-up, then PBIT found one or more problems or PBIT was not run. The ASCII Diagnostic Results Table (DRT) lists the results of all CLD tests run during PBIT. Each line of the displayed DRT describes a test and its overall result. Use the GPM *DRT* command to display the DRT by entering this command at the prompt:

```
DRT <Enter>
```



Cross Reference

If the red FAIL LED is off, the DRT will confirm that all its tests passed. Refer to the *Foundation Firmware User's Manual* and the *Product Release Note* for more information on the CLD routines.

If the CLD does not report any results, check the power-up sequence being run. See page 3-23.

SIGN-ON MESSAGE GARBLED

If the sign-on message is garbled, check that your terminal settings match 9600 8, N, 1 (9600 baud, 8 data bits, no parity, 1 stop bit). Also, ensure that you are using a cable compatible with the ones listed in Table 2.2 on page 2-3.

ADDITIONAL INFORMATION



Cross Reference

Additional troubleshooting information (for example how to run Card Level Diagnostics to isolate problems) is available in Chapter 4 of this manual.

Refer also to the troubleshooting wizard on the Technical Documentation CD-ROM or on Tech*Net* (www.technet.dy4.com). To access the wizard via Tech*Net,* select "FAQs".

THE NEXT STEP



Cross Reference

Once the hardware is correctly configured and installed in the chassis, the next step is to install the Board Support Package (BSP) software. See the section "BSP Installation Procedure," in Chapter 1 of your BSP Software User's Manual, which is included in Acrobat pdf format on your BSP CD-ROM.

4

CARD COMMUNICATIONS

INTRODUCTION

This chapter provides the following information about using the SVME/DMV-182's General Purpose Monitor (GPM):

- determining the version of Foundation Firmware on the card;
- determining the configuration of the card;
- running diagnostics;
- restoring Foundation Firmware;
- the VMEBus base address; and
- Ethernet address.

DETERMINING THE FOUNDATION FIRMWARE VERSION

To determine the version of Foundation Firmware programmed on your card, type

```
cit
```

at the GPM prompt. This will display the image number as shown in Figure 4.1.

FIGURE 4.1: CIT Command

```
(CPU 0) 48000000* cit
Image #: 602666-100
       Rev: -
      Date: 2003/08/21

   CBOOT #: N/A     Rev: N/A     Date: N/A
Assembly #: N/A     Rev: N/A     Date: N/A

(CPU 0) 48000000*
```

DETERMINING THE CONFIGURATION OF THE CARD

To determine the hardware map of the card, type

```
map
```

at the GPM prompt. This will display a hardware map of the card and its PMC modules as shown in Figure 4.2.

FIGURE 4.2: GPM MAP Command

```
(CPU 0) 48000000* map

                  Hardware map for the SVME/DMV-182

                  Base Addr.     Size      LM Addr.
                  ----------  ----------  ----------
              A24:  0x00480000  0x04000000  0x00000000
              A32:  0x48000000  0x40000000  0x00000000
                  ----------  ----------  ----------
      AM29PDL128:  0xF0000000  0x08000000
            DRAM:  0x00000000  0x20000000
          NOVRAM:  0xE0030000  0x00008000
                  ----------  ----------  ----------

             Vendor Device HDR    Config        Memory Space Allocation
 Device name   ID     ID   TYPE Base Addr   BAR  PCI Base     Size      Type
 ----------- ------ ------ ---- ----------  --- ---------- ---------- -------
 GT-64360    0x11AB 0x6460 0x80 0x80001800   0  0x00000000 Unknown    Memory
                                             2  0x01000000 Unknown    Memory
                                             4  0x14000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x80001900   0  0x01000000 Unknown    Memory
                                             2  0x01800000 Unknown    Memory
                                             4  0x0FFC0000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x80001A00   0  0x1C000000 Unknown    Memory
                                             2  0x1C800000 Unknown    Memory
                                             4  0x1D000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x80001B00   0  0xFF000000 Unknown    Memory
                                             2  0xFF800000 Unknown    Memory
                                             4  0x40000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x80001C00   0  0x22000000 Unknown    Memory
                                             2  0x24000000 Unknown    Memory
                                             4  0x20000000 Unknown    I/O
                                             5  0x14000000 Unknown    I/O
 GT-64360    0x11AB 0x6460 0x80 0x80001D00
 GT-64360    0x11AB 0x6460 0x80 0x80001E00
 GT-64360    0x11AB 0x6460 0x80 0x80001F00
 GT-64360    0x11AB 0x6460 0x80 0x81000000   0  0x00000000 Unknown    Memory
                                             2  0x01000000 Unknown    Memory
                                             4  0x14000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x81000100   0  0x01000000 Unknown    Memory
                                             2  0x01800000 Unknown    Memory
                                             4  0x0FFC0000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x81000200   0  0x1C000000 Unknown    Memory
                                             2  0x1C800000 Unknown    Memory
```

```
                                                4  0x1D000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x81000300      0  0xFF000000 Unknown    Memory
                                                2  0xFF800000 Unknown    Memory
                                                4  0x40000000 Unknown    Memory
 GT-64360    0x11AB 0x6460 0x80 0x81000400      0  0x12000000 Unknown    Memory
                                                2  0xF2000000 Unknown    Memory
                                                4  0x10000000 Unknown    I/O
                                                5  0x14000000 Unknown    I/O
 GT-64360    0x11AB 0x6460 0x80 0x81000500
 GT-64360    0x11AB 0x6460 0x80 0x81000600
 GT-64360    0x11AB 0x6460 0x80 0x81000700
 IBM29P2994  0x1014 0x01A7 0x01 0x81001000      0  0x90100000 0x00100000 Memory
 Universe    0x10E3 0x0000 0x00 0x81012000      0  0xE0080000 0x00001000 I/O
                                                1  0x90000000 0x00001000 Memory

(CPU 0) 48000000*
```

RUNNING DIAGNOSTICS

If the red Fail LED on the front panel remains lit, type

```
cld
```

at the GPM prompt. This will run Card Level Diagnostics and display the results as shown in Figure 4.3.

FIGURE 4.3: CLD Results

```
(CPU 0) 48000000* cld

CLD complete: 1 diagnostic was executed

Summary: Pass
RAM data convergence: Pass
RAM address convergence: (0x01000000-0x01002000) Pass
RAM misaligned transfer: Pass
RAM read/write: (0x01000000-0x01002000) Pass

(CPU 0) 48000000*
```

UPDATING FOUNDATION FIRMWARE

See the instructions in the Foundation Firmware Release Notes.

RECOVERING FOUNDATION FIRMWARE

See the instructions in the Foundation Firmware Release Notes.

THE VMEBUS BASE ADDRESS

By default, the VMEbus base address of the SVME/DMV-182 is selected by geographical addressing. The Foundation Firmware Configuration Boot Manager allows you to change the address assigned to each slot. See the Foundation Firmware User's Manual for details.

GEOGRAPHICAL ADDRESSING

The SVME/DMV-182 supports the geographical addressing method for determining the VMEbus slot ID when used in backplanes compliant with the VME64 Extensions. The VME64 Extensions specifies six pins on the backplane (five geographical address pins and one geographical address parity pin) which may be used to specify the VME address.

When selected for geographical addressing, the SVME/DMV-182 firmware reads the geographical address and generates a unique ID code. The SVME/DMV-182 calculates its base address using this ID code and a table maintained by the Foundation Firmware Configuration Boot Manager. See Table 4.2 on page 4-7.

Refer to Table 4.1 for the standard VME64 Extensions P1 backplane configuration.

TABLE 4.1: VME64 Extensions Geographical Address Pin Assignments

Slot Index (Hex)	GAP* Pin P1 pin d9	GA4* Pin P1 pin d17	GA3* Pin P1 pin d15	GA2* Pin P1 pin d13	GA1* Pin P1 pin d11	GA0* Pin P1 pin d10
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
A	GND	Open	GND	Open	GND	Open
B	Open	Open	GND	Open	GND	GND
C	GND	Open	GND	GND	Open	Open
D	Open	Open	GND	GND	Open	GND
E	Open	Open	GND	GND	GND	Open
F	GND	Open	GND	GND	GND	GND
10	Open	GND	Open	Open	Open	Open
11	GND	GND	Open	Open	Open	GND
12	GND	GND	Open	Open	GND	Open
13	Open	GND	Open	Open	GND	GND
14	GND	GND	Open	GND	Open	Open
15	Open	GND	Open	GND	Open	GND

VME BASE ADDRESSES

The default 32-bit base addresses for each slot index are shown in hexadecimal format in Table 4.2.

TABLE 4.2: VMEbus Base Addresses

Slot Index (Hex)	Extended Address (A32)
00	Reserved
01	4000 0000
02	4800 0000
03	5000 0000
04	5800 0000
05	6000 0000
06	6800 0000
07	7000 0000
08	7800 0000
09	8000 0000

ETHERNET MAC ADDRESSES

Each SVME/DMV-182 card is pre-programmed with two unique Ethernet MAC addresses (one for each Ethernet port). The three high bytes are 00H, 80H, 7FH (the CWCEC manufacturer number) and the lower three bytes form a unique number.



Cross Reference

The BSP Software User's Manual explains how to determine (and change) the Ethernet MAC addresses of the card.

The Ethernet address may also be changed using the Foundation Firmware Configuration Boot Manager. See the Foundation Firmware User's Manual for more information.

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