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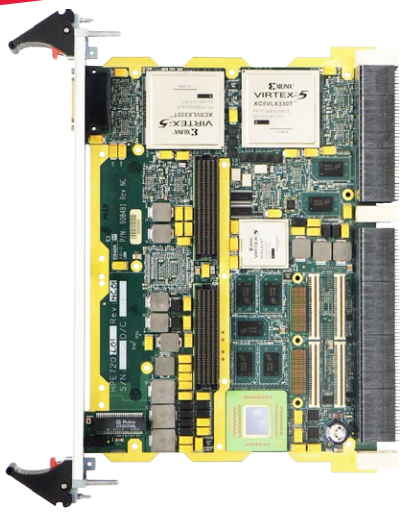




Data Sheet

HPE720

Dual Xilinx® Virtex®-5 FPGA & MPC8640D VPX Processor Card



Applications

- Signal Intelligence (SIGINT)
- Image Processing
- Electronic Warfare (EW)
- Radar Processing

Features

- FPGA and Power Architecture based processing
- Freescale Power Architecture MPC8640D processor
- Dual Xilinx Virtex-5 SX240T, LX330T FPGAs
- Dual mezzanine sites with support for FMC (VITA 57), PMC and XMC (VITA 42)
- Serial RapidIO fabric
- 6U VPX REDI (VITA 48)
- Air-cooled Level 0

Benefits

- Dense FPGA resources combined with general purpose processing
- Maximum I/O flexibility to front panel and backplane
- Support for multi-processing applications
- For use in deployed or commercial environments

Overview

The HPE720 is a high-performance hybrid processing engine, blending the benefits of the largest Xilinx® Virtex®-5 FPGAs with a Freescale™ Power Architecture™ MPC8640D (dual-core AltiVec™) processor. Demanding applications can use the dense FPGA resources of the HPE720 to process tasks that can take advantage of high-performance algorithms partitioned across the FPGAs and dual-core processor. When complex algorithms are partitioned into FPGAs, an increase in performance leads to a dramatic reduction in slot count and system cost. The HPE720 includes an MPC8640D processor to handle floating-point calculations, additional processing, data analysis, decision making, and system control. It is this combination of processing resources that allows the HPE720 to function as a standalone board or as an integrated part.

The HPE720 combines dense processing resources with robust I/O to the front panel, mezzanines, and backplane to maximize the effectiveness of these resources. Mezzanine support includes an FMC site (VITA 57) and a PMC/XMC/FMC site. FMC is a standard to allow designers to take advantage of advances in the latest I/O (ADCs, DACs, etc.) and couples this I/O directly to FPGAs. This allows users to take advantage of the low latency and high-bandwidth supported by FPGAs, while the inherent flexibility of FMC eases design for multiple I/Os and allows for dissipating heat more effectively.

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Table 1: HPE720 FPGA Resource Table

	Logic Resources			Memory Resources			Clock Resources		Embedded Hard IP Resources & Speed Grades*					
	Slices	Logic Cells	CLB Flip-Flops	Max. Dist. RAM (kbits)	Block RAM/ FIFO w/ ECC (36 kbits each)	Total Block RAM (kbits)	Digital Clock Mgrs. (DCMs)	Phase Locked Loop (PLL)/ PMCD	DSP48E Slices	PCIe Endpoint Blocks	PowerPC 440 Blocks	Speed Grade	RocketIO GTP (run at 3.125 GHz or lower)	RocketIO GTX (run at 6.25 GHz or lower)
LX330T	51,840	331,776	207,360	3,420	324	11,664	12	6	192	1	0	-1	24	0
SX240T	37,440	239,616	149,760	4,200	516	18,576	12	6	1,056	1	0	-1	24	0

*Note: These features are specific to using the FPGAs on the HPE720 and do not reflect all of the capabilities of the FPGAs themselves.

The HPE720 is supported by the Fusion XF Suite, which provides infrastructure and support for HDL development, software, and multi-processing applications, including Serial RapidIO® (SRIO). VxWorks® and Linux® are supported operating systems for the MPC8640D.

Xilinx Virtex-5 FPGAs

At the heart of the HPE720s processing are two Xilinx Virtex-5 FPGAs in the FF1738 package FPGAs, the largest FPGAs in the Virtex-5 family. FPGAs provide parallel processing capabilities, reducing processor count and system size. Operations such as FFTs, FIR filters and other fixed-point and/or repetitive processing tasks are highly suited for placement inside FPGAs. The two large FPGA nodes can process input from the two FMC mezzanine sites or backplane I/O, or can simply function as additional compute resources to the general purpose system processor.

The FPGA nodes on the HPE720 support device families from the Xilinx Virtex-5 family. By using the LXT for logic-intensive applications and the SXT for DSP applications, developers can tailor their hardware resources to match their algorithm needs. See the HPE720 FPGA Resource table.

Curtiss-Wright Controls Defense Solutions supports the LX330T devices. With over 330,000 logic cells, the LXT family gives FPGA designers the most amount of space to program their algorithm. In the SXT family, the SX240T device is supported. With 1,056 DSP slices and over 240,000 logic cells, the SXT device is ideal for filtering algorithms where the DSP48E slices can be used to maximum benefit.

Larger Chips Reducing Development Time

The use of large FPGA nodes simplifies algorithm development, as processing can be done inside a single device or a reduced number of devices. When compared with the smaller package FPGAs, the larger FPGAs have more logic slices available. The availability of more logic gives designers greater freedom, making timing easier to close, and hence shortening development cycles. Additionally, as more FPGAs are used, greater complexity is needed to partition the algorithm and link the devices together. These I/O resources come at a greater expense in smaller devices, which already have less logic. When combined with a large amount of memory and I/O resources, the larger devices can fulfill processing needs for a variety of applications while still easing customer development.

FPGA Architecture

The FPGA nodes on the HPE720 have industry leading I/O and memory resources to maximize the effectiveness of the devices in a variety of applications.

Memory

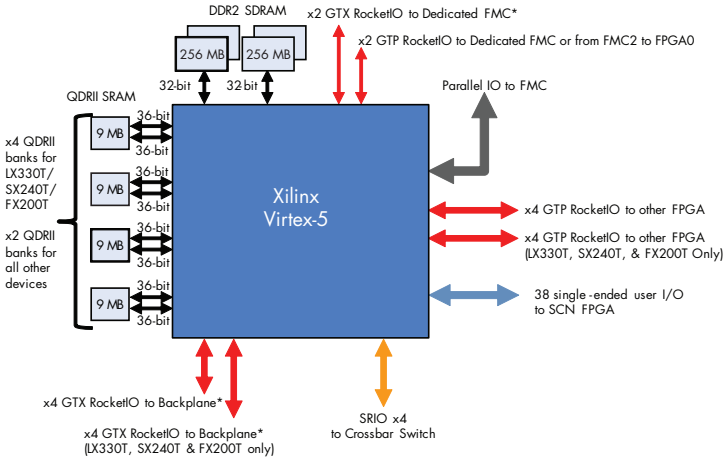
The memory resources on each FPGA node of the HPE720 give users the ability to process and store data sets for the most demanding applications. Each FPGA node has both DDR2 and QDR-II SRAM available. The DDR2 is organized into two banks, with each bank providing a x32 bus width using two x16 devices. Up to 512 MB of memory is available from each DDR2 bank, providing a large amount of storage space for data sets. Complementing the DDR2 for more processing intensive tasks are four independent

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banks of QDR-II SRAM. The banks each have a x36 bus width, and provide immense bandwidth as they are dual data rate on separate read and write ports. Each bank is 9 MB, for a total of 36 MB available from each FPGA. The LX330T and SX240T support all four banks; smaller devices only support two banks each.

Figure 1: FPGA Memory & I/O



FPGA I/O

The FPGA nodes on the HPE720 have an ample amount of I/O resources for connecting to other parts of the system. In terms of RocketIO™ high-speed serial links, the FPGA nodes have utilized the maximum available for the device selected on the HPE720. For the larger devices, such as LX330T and SX240T, all 24 links are used. These links are divided between I/O to the mezzanines, between the two FPGAs, to the backplane, and the SRIO fabric. In Virtex-5 FPGAs, Xilinx classifies the RocketIO into two categories: GTP and GTX. The GTPs can run at a maximum frequency of 3.125 GHz, and are used on the SXT and LXT devices. These connections can also run at lower frequencies, but this extra capability allows customers to bring I/O into the FPGAs at the fastest speed possible. Parallel I/O is also used, with 160 lines routed to the dedicated FMC site, and 38 single-ended I/Os routed to the System Control Node.

Table 2: GTP/GTX Speed/Clock Sources

Speed	Protocol	Clock Source
3.125 GB/s	Aurora, SRIO type 3	156.25 MHz
2.5 GB/s	Aurora, sFPDP, PCIe, SRIO type 2	125 MHz
2.125 GB/s	Aurora, sFPDP, 2x Fibre Channel	106.25 MHz
1.25 GB/s	Aurora, 1x Gigabit Ethernet	125 MHz
1.0625 GB/s	Aurora, sFPDP, 1x Fibre Channel	106.25 MHz

MPC8640D Power Architecture Processor

Dual CPU Cores

The Freescale MPC8640D forms a fully integrated processor node with dual CPUs, memory controllers, DUART, Ethernet controllers, PCI Express® (PCIe) and SRIO. The e600 Power Architecture CPU cores include floating-point units for high-performance DSP processing. The processor core frequency is 1.0 GHz. Each core has access to board management functions (temperature sensors, RTC and voltage monitors).

Memory

The MPC8640D has two integrated memory controllers. Each controller supports 512 MB to 1 GB of DDR2 SDRAM memory for a total of 1 to 2 GB. The memory is configured as 64-bit data and 8-bit ECC, operating at 200 MHz. The peak total memory bandwidth is 3.2 GB/s. Each e600 core has its own 1 MB L2 cache.

Flash

The HPE720 has a total of 128 MB of flash that can be split between two banks or used as one larger bank. The flash can be used for non-volatile storage of the HPE720's bootloader, applications and FPGA configuration images. The HPE720 has a switch to protect the bootloader image and/or data from being accidentally overwritten.

Each FPGA has local Flash which is used to store the boot image for the FPGA.

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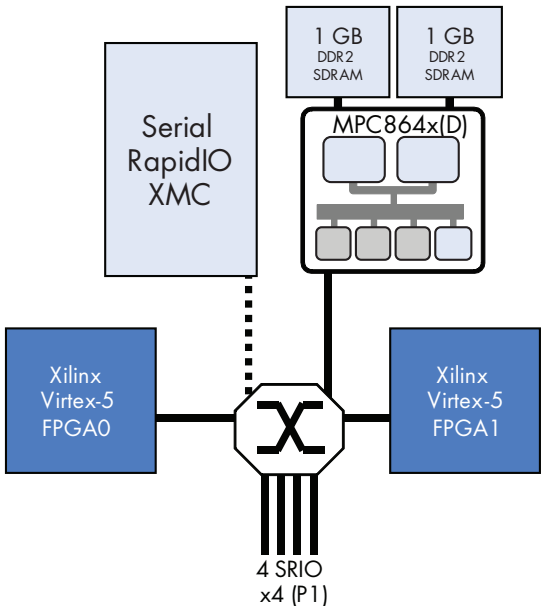


Board Connectivity

Serial RapidIO Infrastructure

An 8-port SRIO switch connects the MPC8640D processor, both Virtex-5 FPGAs, XMC site (optional), and provides four connections to the backplane through the P1 VPX connector. Each connection has four lanes, with each lane running at 3.125 GHz. The SRIO infrastructure can be used to connect with other Curtiss-Wright boards, including the CHAMP-AV6, CHAMP-FX2, VPX6-185 and MFC700.

Figure 2: Serial RapidIO Infrastructure



PCI Express

PCIe x8 can be run from the processor to the XMC site or to the backplane. If run to the backplane, there is a connection to the P2 VPX connector.

Ethernet

There are two GbE connections to the front panel, and two GbE connections to the backplane. The front panel connections are copper and available through a breakout cable, while the backplane connections are 1000Base-X. All Ethernet connections are supported by the MPC8640D processor.

Serial I/O

The HPE720 has two UART ports connected to the MPC8640D. An EIA-232 connection is available through the breakout connector and an EIA-232/422 port is available to the backplane.

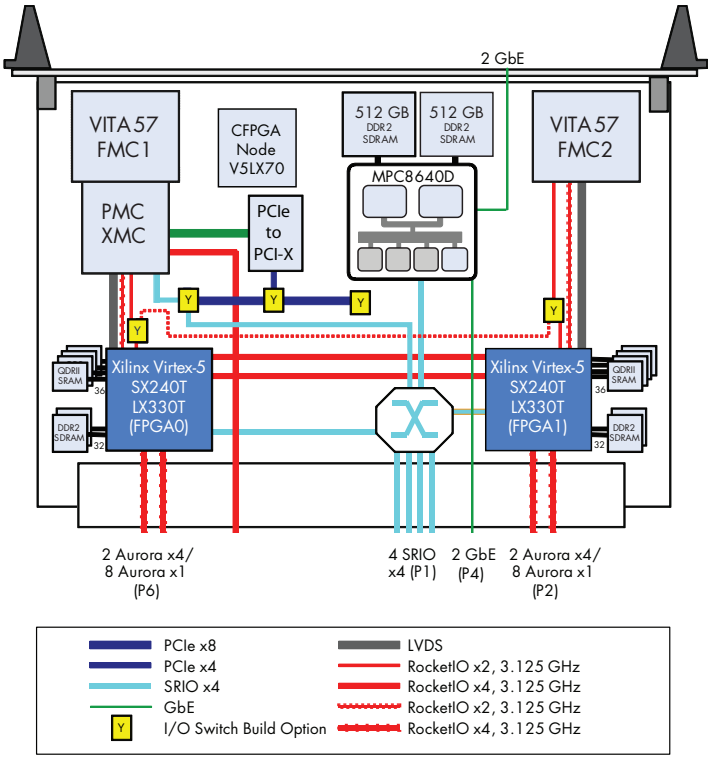
Cabling

A break-out cable connecting to the front panel connector provides access to a EIA-232 connection, two GbE connections, JTAG and a reset button.

Configuration FPGA & Chassis Management

The onboard Configuration FPGA Node (CFPGA) controls chassis management, power and temperature monitoring, bit-stream encryption, and routing of single-ended I/Os. The CFPGA is controlled by the MPC8640D's local processor bus. The CFPGA's ability to function as a switch for single-ended I/Os can be seen in the CFPGA I/Os diagram.

Figure 3: Configuration FPGA Node I/Os

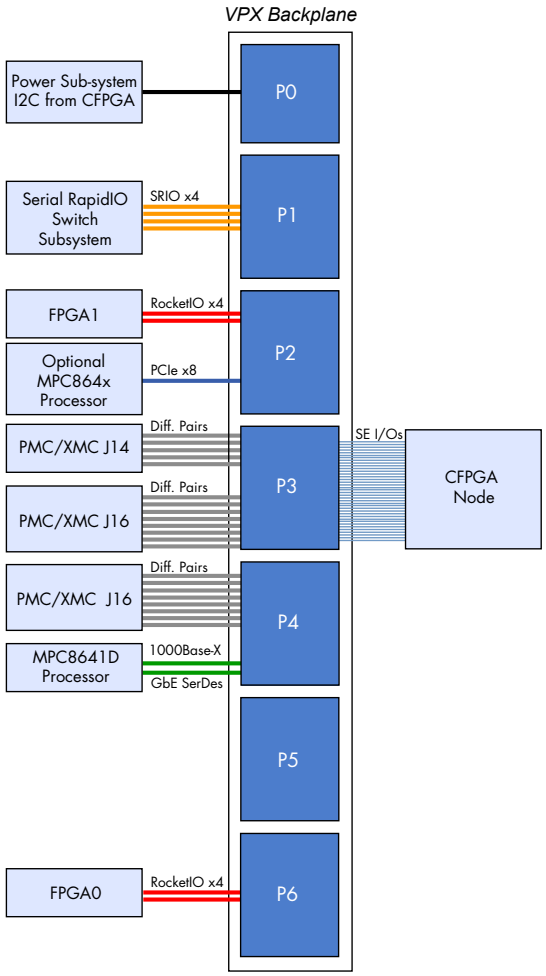


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Backplane I/O

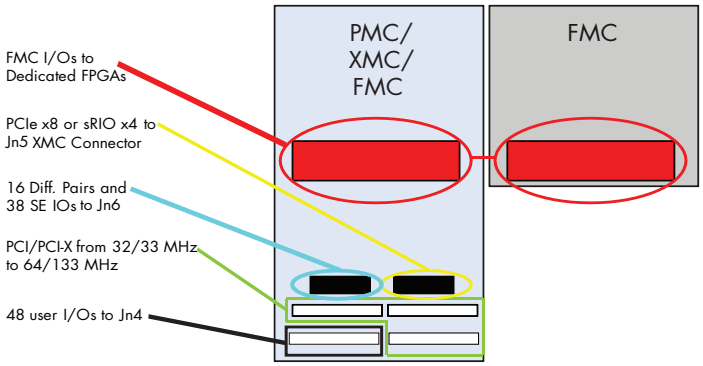
Figure 4: Backplane Connectivity



Mezzanine Sites

The HPE720 includes a versatile set of I/O options through dual mezzanine sites, one FMC (VITA 57) and a second site that can host a FMC, PMC or XMC. The combination of FMC/PMC/XMCs provides flexibility for the latest I/O such as A/D converters, sFPDP, LVDS, and Fibre Channel, but also allows support for legacy I/Os. The board can be used as a front-end solution, streaming in data using the dual mezzanine sites for inputs, before passing data forward for further processing using SRIO or other high-speed interconnects. For space constrained applications, the board functions as a system-onboard, providing the ability to input and output data in a single-slot with two mezzanines.

Figure 5: Mezzanine I/O Support



FMC Site

The VITA 57 FPGA Mezzanine Card (FMC) sites utilize 120 user I/O pins from the dedicated FPGA nodes:

- LA[00-33]_P/N = 34 differential pairs / 68 single-ended with DCI termination
- HA[00-16]_P/N = 17 differential pairs / 34 single-ended with DCI termination
- HB[00-08]_P/N = 9 differential pairs / 18 single-ended No DCI termination.

Customer developed, third party, or Curtiss-Wright FMC modules can be used with the HPE720. Announced FMC products from Curtiss-Wright include analog I/O boards, such as the ADC512/513 and ADC520, which can be used to tailor the I/O capabilities of the HPE720 to customer project specific needs.

PMC/XMC Site

One mezzanine site supports either PMC and XMC. The XMC site supports up to PCIe x8 or SRIO x4. The PCIe port goes directly to the MPC8640D processor, while the SRIO option goes through the crossbar switch. Because these two standards use the same pins, this is a factory configurable option. PMCs are also supported on the site. A PCIe-to-PCI-X bridge provides the PMC connectivity to the rest of the system. PCI-X up to 64-bit 133 MHz is supported, as well as conventional PCI.

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Software and HDL

Board Support Packages

The HPE720 can be delivered with Wind River VxWorks or Wind River GPP Linux Board Support Packages (BSP). The BSP is accompanied by a bootloader which contains the necessary drivers for enumerating and enabling all onboard hardware devices, such as memories, bridges, and Ethernet controllers. The bootloader is responsible for booting the operating system. The BSP also contains a number of useful functions and drivers for flash programming, debugging, real time clock management, watchdog timers, etc.

FusionXF FPGA Development Kit

FusionXF provides FPGA HDL functions, application APIs, drivers, and utilities to simplify the task of integrating FPGAs into an embedded real-time DSP system design. It aids customers in the development of their FPGA algorithms and logic for Curtiss-Wright customer- programmable FPGA products. All the building blocks are provided to build a fully functional FPGA design into which a customer can integrate its FPGA logic and algorithms. It provides mechanisms for communication between FPGAs as well as communication between FPGAs and processors. Also included in the Kit are example designs that show how to implement common FPGA functions such as control registers, DMA engines, interrupts, and how to control these functions and communicate with them from software. FusionXF is comprised of a Hardware Development Kit (HDK) and Software Library.

FusionXF contains software libraries, drivers, and utilities for use in VxWorks and Linux environments to facilitate the initialization and control of FPGAs, and to communicate and move data between FPGAs and application software. Software drivers and libraries are provided to allow processing nodes to utilize FPGAs as co-processors, DMA engines, and memory pools. Utilities are provided to perform functions such as loading new images into the FPGA's flash memory.

The FusionXF HDK contains HDL functions that are common to most FPGA applications. There are HDL functions provided such as DDR and QDR memory controllers, RocketIO interfaces, parallel I/O interfaces, and commonly used FPGA functions such as DMA engines and register sets. In addition, there are HDL functions provided to implement protocols such as PCIe and SRIO. The hardware independent HDL code resides in the VM Library. The hardware dependent HDL code resides in the BSIP.

FMC (VITA 57)

Traditional open standard bus-based structures like PCI-X (for example, PCI-X) are less suitable for FPGA I/O, because they can slow data transfer rates while consuming valuable FPGA resources. FPGA I/O is inherently configurable and can be adapted to a wide range of I/O structures. FPGA I/O is best optimized when FPGAs are not treated the same way as CPUs, rather are connected directly with I/O devices or ports. The VITA 57 FMC open standard has been developed to capitalize on these FPGA attributes.

The FMC standard provides an industry standard mezzanine form factor in support of a flexible, modular I/O interface to an FPGA located on a baseboard or carrier card. It allows the physical I/O interface to be physically separated from the FPGA design while maintaining a close coupling between a physical I/O interface and an FPGA through a single connector, P1.

There is a choice of two very high-bandwidth connectors to interface the FMC to an FPGA on a carrier: a Low Pin Count (LPC) connector with 160 pins and a High Pin Count (HPC) connector with 400 pins. An FMC with the LPC connector can mate with a carrier that utilizes either an LPC or HPC connector.

The use of the FMC standard simplifies FPGA designs, reduces cost, and makes the design of I/O mezzanine modules simple and straightforward. Development cycles can be shortened and costs lowered by utilizing a single FPGA design in multiple applications, by simply mounting different FMC modules.

Typical FMC modules will have an I/O device, such as an ADC (with front end signal conditioning), buffer and connectors. Since FPGAs can interface directly to I/O device pins, there is no need for any bus interfaces like PCI. Therefore bus converters are an unnecessary overhead that can be left out of the design.

FMCs can be used to provide analog I/O, digital I/O, fiber-optic interfaces, camera interfaces, frame grabbers, additional memory or even dedicated DSP functions.

FMC modules are of a similar width, but half the size of PMC or XMC modules, but provide higher density host I/O.

Key FMC features include:

- Up to 192 differential I/O pairs
- Up to 10 high-speed serial I/O links
- Air and conduction-cooled variants
- Module size 69 x 76.5 mm

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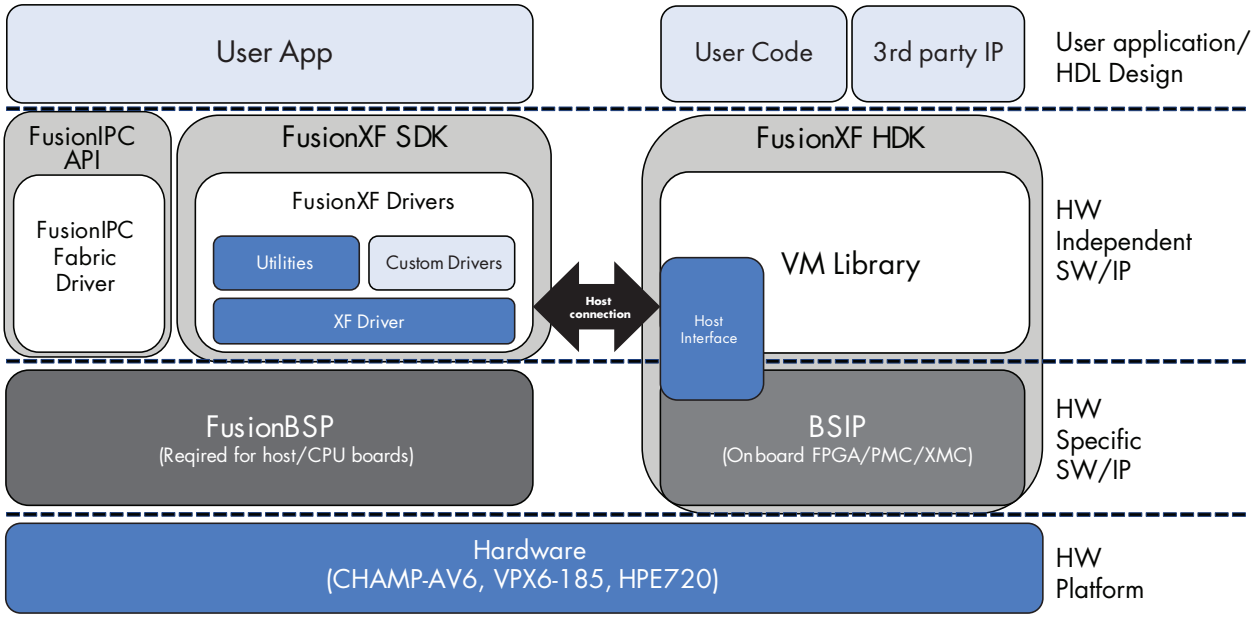


FusionIPC Development Kit

FusionIPC provides Inter-Processer Communications (IPC) capabilities targeted at Distributed Multi-Processing (DMP) applications. It provides a simple, yet high-performance, low latency mechanism for bulk data transfers between distributed processors. FusionIPC consists of a FusionIPC driver that provides peer-to-peer communication capabilities between processors over a system interconnect fabric, and a FusionIPC library that provides POSIX APIs.

FusionIPC is based on a Shared Memory Buffer (SMB) communication approach that is independent of the lower layer transport protocol. The first transport protocol supported by FusionIPC is SRIO.

Figure 6: FusionXF & FusionIPC



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Table 3: Specifications

FPGA	
Device	Xilinx Virtex-5, LX330T and SX240T
No. of FPGAs	2
Memory (per FPGA)	4x 9 MB QDRII SRAM (36-bit data paths) 2x 256 MB - 512 MB DDR2 SDRAM (32-bit data paths) 16 MB flash (for storing FPGA images only)
Connectivity	x8 GTP RocketIO per FPGA to backplane (P2 & P6) x8 GTP RocketIO between FPGAs for LX330T/SX240T x2 GTP/GTX to dedicated FMC site x2 GTP to FPGA 0 from FMC 1 (default) or FMC 2 x2 GTP to FPGA 1 from FMC 2 (default) x4 SRIO to crossbar switch 38 single-ended I/Os or 19 differential pairs to CFPFA
Configuration	JTAG, MPC8640D processor, CFPFA, off-board I/Os and onboard flash
Power Architecture CPUs	
Device	Freescale MPC8640D
CPU cores	2, e600
Speed	1.0 GHz
Memory	64 KB L1 cache per core, 1 MB L2 cache per core (inc. ECC), 512 MB - 1 GB DDR2 per bank
Flash	128 MB, arranged as two 64 MB banks or a single 128 MB bank
NvSRAM	128 KB per MPC8640D with RTC
Mezzanine Sites	
FMC/VITA 57	Quad RocketIO x1 and 74 Differential Pairs
XMC/VITA 42 & 46.9	J15 - PCIe x4/x8 or SRIO x4 J16 - 38 single-ended I/Os to CFPFA FPGA - up to 16 differential pairs (P3/P4)
PMC/IEEE 1386.1	PCI (33/66 MHz), PCI-X (66/133 MHz), 32/64-bit, 3.3 V signaling
Jn4/VITA 46.9	38 single-ended I/Os to the CFPFA FPGA or 18 differential pairs and 2 single-ended I/Os
Ethernet	
Front Panel	Dual 1000Base-T (front panel RJ45)
Backplane	Dual 1000Base-X to P4 Connector
Device	Embedded within MPC8640D
Speed	10/100/1000 MB/s
PCI Express	
Connectivity	Optional to XMC (x4, x8), MPC8640D, Backplane (x8 on P2), all at 2.5 Gb/s
Serial RapidIO	
Switch Device	Tundra TSI578 8-port SRIO switch
Connectivity	Both FPGAs, MPC8640D, optional to XMC, 4 connections to P1 fabric connector, all lanes at 3.125 Gb/s

Serial I/O	
Device	DUART embedded within MPC8640D
Front Panel	Dual EIA-232
Backplane	Dual EIA-232/422 to P4
Backplane	
Compliance	VPX (VITA 46) and VPX REDI (VITA 48)
Connectivity	
P0	Power and CFPFA utility signals (I2C)
P1	4 SRIO x4 to Switch
P2	2 RocketIO x4 to FPGA 1 and x8 PCIe (optional)
P3	5 differential pairs from J14, 8 differential pairs from J16 and 38 single-ended I/Os from CFPFA
P4	8 differential pairs from J16, 2GbE SerDes
P5	Unused
P6	2 RocketIO x4 to FPGA 0
Processor Local Bus	
Connectivity	32-bit wide connection from CPU to CFPFA
System Control Node	
Device	Xilinx Virtex-5 LX110
Connectivity	32-bit wide connection to MPC8640D Dual I2C buses 38 single-ended connections to Jn4 38 single-ended connections to Jn6 Up to 38 single-ended connections to P3 38 single-ended connections or 19 differential pairs to FPGA 0 and FPGA 1
Software/HDL Code	
Operating System	VxWorks 6.5/6.7, Linux 3.0 (MPC8640D CPUs)
Utilities	Flash programming, diagnostics
HDL Code	FusionXF FPGA Development Kit, FusionIPC Development Kit and U-Boot
Standards	
Compliance	VITA 20, 42.0, 42.2, 42.3, 46.0, 46.3, 46.9, 48 and IEEE 1386
Miscellaneous	
Power	VPX 5 V (PMC/XMC only) +12 V (103.8 W @ 50°C)
Cabling	Break-out cable with 4x EIA-232 connections, dual GbE, JTAG & Reset button (CABLE-1002)
Weight	Air-cooled: 2.6 lbs (1.18 kg)

Notes:
1. These are GTP connections and run at 3.125 GHz.

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Table 4:

Environmental Specifications

		Commercial
Part Number Extension (Note 1)		-
Temperature	Operational (at sea level)	0°C to +55°C (15 CFM air flow) (Note 2)
	Non-Operational	-40°C to +85°C
Vibration	Operational (Random)	-
Shock	Operational	-
Humidity	Operational	5-95% non-condensing
Altitude (Note 4)	Operational	-
Conformal Coating (Note 5)		No

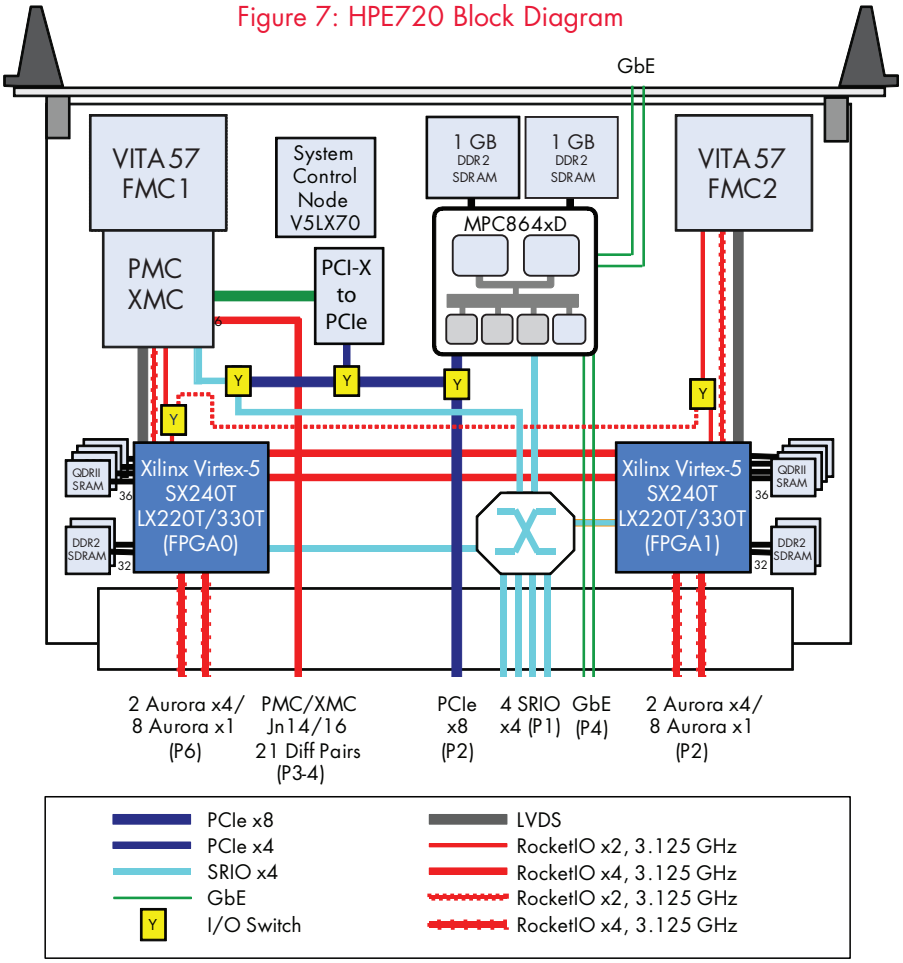
Notes

1. Availability of the ruggedization levels are subject to qualifications for each product.
2. For operation at altitudes above sea level, the minimum volume flow rate shall be adjusted to provide the same mass flow rate as would be provided at sea level. Additional airflow might be required if the card is mounted together with, or next to, cards that dissipate excessive amounts of heat. Some higher-powered products may require additional airflow.
3. The contacting surface on the rack/enclosure must be at a lower temperature to account for the thermal resistance between the plug-in unit and rack/enclosure.
4. Depending on the technology used, the risk for Single Event Upsets will increase with altitude.
5. Coated with Humiseal 1B31 or 1B73EPA.
   (ref. http://humiseal.com for details)

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Figure 7: HPE720 Block Diagram



Warranty

This product has a one year warranty.

Contact Information

To find your appropriate sales representative:

Website: www.cwcdefense.com/sales

Email: defensesales@curtisswright.com

Technical Support

For technical support:

Website: www.cwcdefense.com/support

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