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LOW40/LOW40P

40-Channel High Power Low-Side Driver IP Module Hardware Reference

Document No. B-T-MR-LOW40###-A-0-A3

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Revised: October 12, 2001

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This is a reference manual for Systran's 40-channel, high-power, low-side driver IP Module boards, herein referred to as the LOW40 (part number BHAS-LOW40) and LOW40P (part number BHAS-LOW40P), respectively.

1.1.2 Scope

This reference manual covers the physical and operational description of the LOW40/LOW40P, both from hardware and software perspectives. This reference manual also contains detailed technical information about the LOW40/LOW40P's performance characteristics, and a few typical applications. The reader should have a general understanding of computer processing, software and/or hardware applications experience, and a working knowledge of using IP Modules on their carrier(s) of choice.

1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7E.
- An 'Active Low' signal on a hardware product has a slash (/) prefix. For example, /SYNC.
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- *American National Standard for IP Modules (ANSI/VITA4 - 1995)* published by the VMEbus International Trade Association, 7825 Gelding Dr., Suite 104, Scottsdale, AZ 85260
- *LOW40/LOW40P Software Library Manual* (Doc. No. B-T-ML-LOW40), Systran Corporation
- *LOW40/LOW40P Software Library Manual for PCI/CPCI IP Carriers Using Windows NT 4.0* (Doc. No. B-T-ML-NTAMP)

1.3 Quality Assurance

Systran Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Systran's Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Systran's Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Systran's registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

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2. PRODUCT OVERVIEW

2.1 Overview

The LOW40/LOW40P is a singlewide IP Module, conforming both mechanically and electrically to the American National Standard for IP Modules (ANSI/VITA 4-1995) specification. For a typical IP Module carrier that holds four IP Modules, it can provide up to 160 channels of low-side drivers for a single slot on a computer bus backplane, or be mixed with other IP Modules for a more customized, modular I/O system solution.

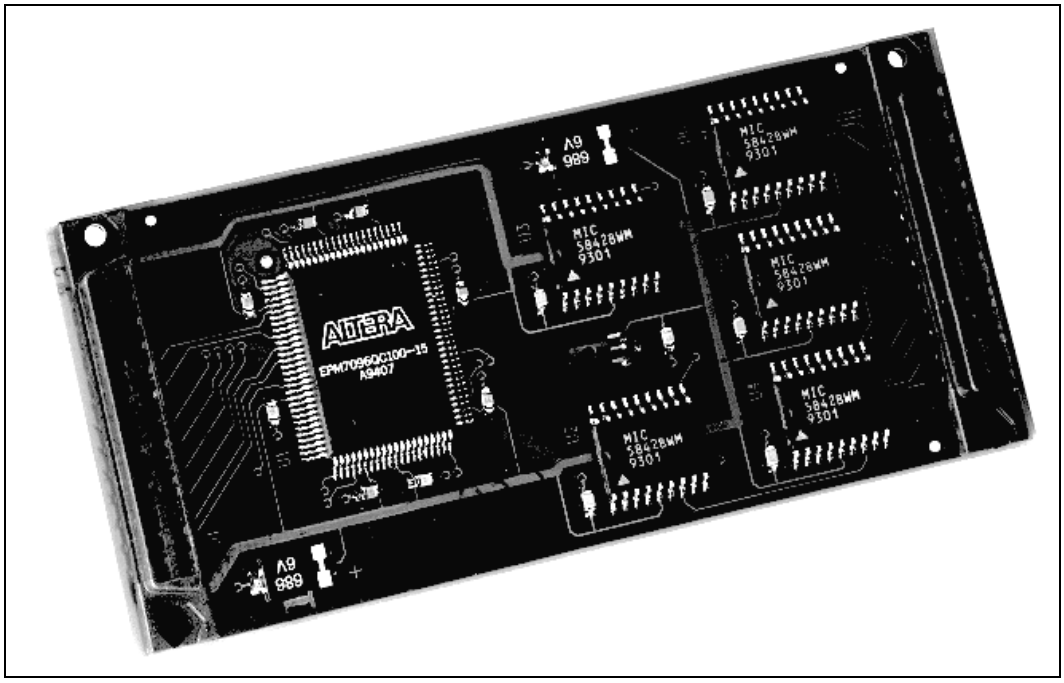


Figure 2-1 LOW40/LOW40P IP Module

2.2 Features

- Per byte-lane 8 channels of low-side (open-collector) drivers
- Minimum breakdown voltage ratings of 80 V (50 V sustaining) @ up to 500 mA per channel (See page 2-5)
- Board-level emitter commons all brought out to 8 pins of the I/O connector
- Per-channel transient diode cathode commons brought out to the I/O connector
- Per byte-lane output enabling via host software
- Ambient temperature sensor on the board, providing +10 mV/°F output
- Per-channel over-current shutdown 500 mA typical (LOW40P only)
- Under-voltage lockout (LOW40P only)
- Thermal shutdown (LOW40P only)
- Per byte-lane over-current shutdown reset via host software (LOW40P only)

2.3 Related Products

- OS-9 SCF device-driver routines and documentation.
- Windows NT 4.0 software library and documentation

2.4 Block Diagram Description

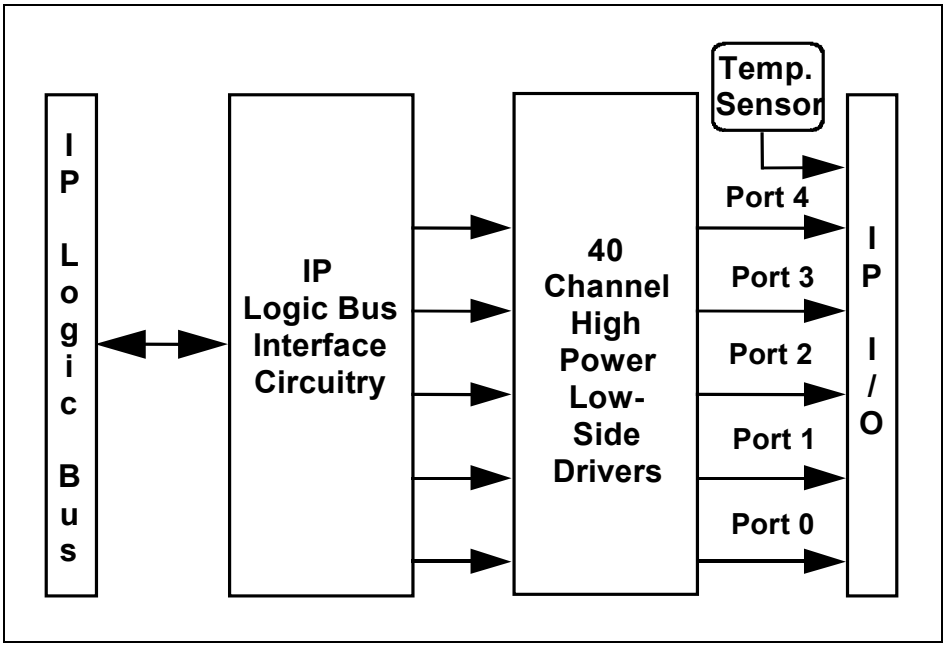


Figure 2-2 LOW40/LOW40P Simplified Block Diagram

Figure 2-2 is a simplified block diagram of the LOW40/LOW40P. On the left side is the IP Module's Logic Bus connector through which all transfers between the carrier and the LOW40/LOW40P's registers and data sources are conducted. The block labeled "IP Logic Bus Interface Circuitry" contains all of the write/read-back data registers, the ID "PROM" data, control (output-enable) register, serial-data-stream engine for driver inputs, and IP Module transfer sequence/control and data bus interface logic. All of this logic is implemented in one EPLD. The block labeled "40 Channel High Power Low-Side Drivers" contains the five 8-bit serial latched drivers, implemented with individual logic devices, housed in wide small outline integrated circuit packages (SOIC). The block labeled "Temp. Sensor" is the precision ambient Fahrenheit temperature sensor. On the right side is the LOW40/LOW40P's I/O connector, providing sink currents for all 40 discrete lines, ground and cathode references, and the single-temperature sensor signal line.

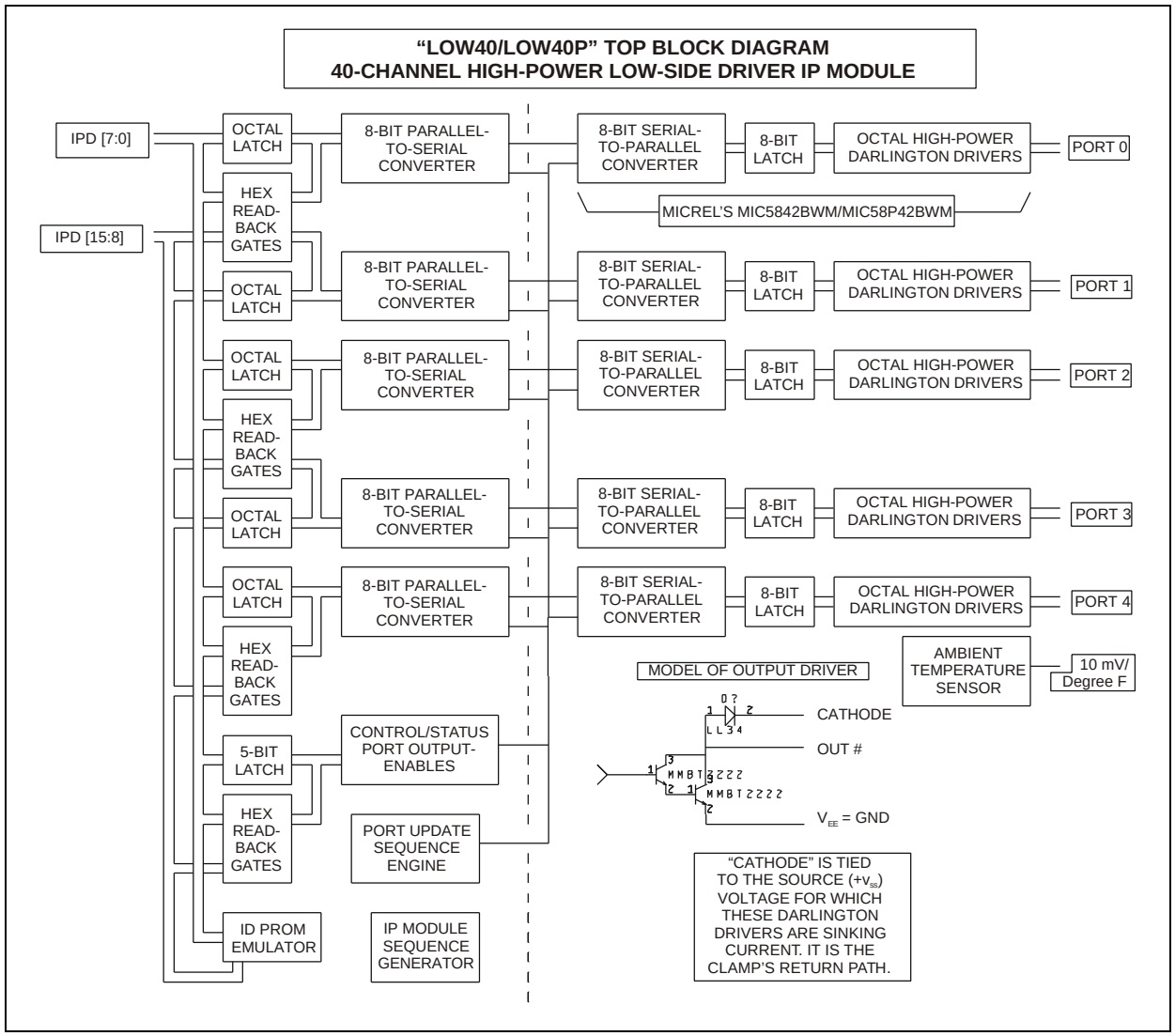


Figure 2-3 LOW40/LOW40P Detailed Block Diagram

Figure 2-3 presents a detailed block diagram of the LOW40/LOW40P. Again, on the left side of the vertical dotted line is the IP's Logic Bus interface through which all host carrier transfers take place. The five 8-bit ports are paired-off into three 16-bit "words". Each "word" contains two 8-bit registers: a 16-bit tristateable gate for driving the IPDbus during I/O reads. Also in the IP Logic Bus interface there is an 8-bit serial driver port that directly feeds each of the low-side output driver MIC5842BWM/MIC58P42BWM's. The architecture supports byte-writes to either octal register, or to both as 16-bit writes. All I/O register reads are performed at the "word" width of 16-bits, only.

The control register has a similar IP Module carrier interface, lacking the octal tristate gate interface. Its function is to register the output-enable control signals for each port.

The ID PROM Emulator is the circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero-fills, during the ID (read) transfers. Emulating the never-changing ID information in this way reduces parts count and costs, and increases system reliability and its associated Mean Time Between Failures (MTBF) value.

The sequence control logic performs orderly IP logic bus transfers between the LOW40/LOW40P and its carrier, and the power-up state logic for this board.

On the right side of the vertical dotted line are the five octal low-side port drivers that receive the 8-bit serial data from the IP logic bus interface. The ambient Fahrenheit temperature sensor is shown with its voltage output corresponding to 10 mV/°F. Also a model of the low-side driver outputs (which is a Darlington pair) is shown.

2.5 Detailed Description

The LOW40 and LOW40P were developed using VHDL and synthesis, targeted to an Altera EPLD, schematic captured and integrated into standard logic devices, connectors and discrete components using Viewdraw by VIEWlogic and associated packages. This top-down design methodology is evident in the product design material presented in this document.

2.5.1 LOW40/LOW40P Components

All IP Logic Bus transfers take place across J1, the IP Logic Connector, located on the left side of all block diagrams. Refer to the ANSI/VITA 4-1995 IP Module specification for details about the signals on this connector. Generally speaking, this IP Module does not support DMA or Interrupts, and has no memory accesses. It performs no-wait ID reads, and no-wait reads from and writes to a short, four-location I/O map.

LOW40/LOW40P CONTROLLER

The LOW40/LOW40P's primary activity "CONTROLLER" is housed within the EPM7096QC100 EPLD located at U1. It serves as the primary IP Module transfer sequence engine, whose responsibilities include: detection of valid I/O and ID transfer operations within their respective, fully decoded address ranges, including the support of HOLD cycles when generated by a carrier; ID PROM emulation data pattern generation for ID read transfers; port output-enable control circuitry with power-up default initialization circuits; encoding of registration (for I/O writes) and IPDbus output enable (for I/O reads), and parallel-to-serial conversion of the registered data for each port with strobe, clock, and enable signals.

The Controller's "Parallel-to-Serial" data-handling function consists of five 8-bit write-read-back registers that converts 8-bit parallel data for each port to serial data. The low-side driver's data update is initiated by an I/O write to any of the five data ports and then updates all five ports simultaneously. The I/O write transfers, after being detected as being valid, consist of any one of four individual byte-wide writes to the first two I/O locations (IPA = 0x00 and 0x01) or individual byte-wide writes in byte-lane 0 to the next two locations (IPA = 0x02 and 0x03), or as any one of four double-byte (word, 16-bit) writes, while the read operations are always as full-word accesses.

LOW40/LOW40P LOW-SIDE DRIVERS

The five byte-wide low-side drivers consist of MIC5842BWM/MIC58P42BWM devices in wide SOIC packages, located at U2-U6. Each port driver contains eight bipolar current-sink Darlington output drivers with a minimum breakdown voltage rating of 80 V (50 V sustaining) at up to 500 mA per channel (1 Amp per 8-bit port). The LOW40/LOW40P's outputs (with integral transient-suppression diodes per channel) are suitable for use with lamps, relays, solenoids, and other inductive loads. The low-side driver outputs and per channel diode cathode and emitter commons connect directly to the I/O connector.

Per byte-lane output enabling is conducted via host software. After power-up or a system reset the output-enable reset bits default to "disabled", which is a logic '0.' A driver is turned on (output near ground) when both its data bit and control register output-enable bits are logic '1's. Otherwise, the output is off (floating, not sinking current).



NOTE: (LOW40P Only) After an over-current shutdown occurs, the channel output is off (floating, not sinking current), and must be reset by toggling the output-enable bit to '0' and back to '1.'

2.5.2 MIC5842BWM/MIC58P42BWM Low-Side Driver Details

The purpose of this short subsection is to provide some additional background material relating to proper use of this product.

At normal operating conditions of free-air temperature equal 25°C , V_{DD} = 5 V and V_{SS} = V_{EE} = 0 V the maximum collector-emitter saturation voltage V_{CE} (sat) = 1.1 V @ 100 mA I_{OUT} current per channel, and V_{CE} (sat) = 1.3 V @ 200 mA I_{OUT} current.

The following list contains the absolute maximum ratings for the MIC5842BWM/MIC58P42BWM low-side drivers at 25°C free-air temperature and Vss=0 V (ground):

Output voltage, V_{CE} .....80 V
Output voltage sustained, V_{CE} .....50 V
Continuous output current, I_{OUT} .....500 mA
Package power dissipation.....1.2 W

In addition, the MIC58P42BWM low-side drivers on the LOW40P provide thermal shutdown at temperatures above 165°C and under-voltage lockout for V_{DD} < 3 V.

Table 2-1 shows the maximum allowable duty cycle for the MIC5842BWM/MIC58P42BWM low-side drivers.

Table 2-1 Maximum Allowable Duty Cycle

Number of Outputs ON (I_{OUT} = 200 mA V_{DD} = 5.0 V)	Max. Allowable Duty Cycle at Ambient Temperature of:				
	25°C	40°C	50°C	60°C	70°C
8	85%	72%	64%	55%	46%
7	97%	82%	73%	63%	53%
6	100%	96%	85%	73%	62%
5	100%	100%	100%	88%	75%
4	100%	100%	100%	100%	93%
3	100%	100%	100%	100%	100%
2	100%	100%	100%	100%	100%
1	100%	100%	100%	100%	100%

2.5.3 Temperature Sensor Details

The ambient temperature sensor (U7) labeled “LM34DZ" is a precision integrated-circuit temperature sensor, whose output voltage is linearly proportional to the Fahrenheit temperature. This has an advantage over linear temperature sensors calibrated in degrees Kelvin, as the user is not required to subtract a large constant voltage from it's output to obtain convenient Fahrenheit scaling. The LM34DZ has ±½°F accuracy (at 77°F) with a linear +10 mV/°F scale factor.



CAUTION: All 40 drivers’ cathodes are combined onto a single I/O connector pin. Consequently, all the loads for which the LOW40/LOW40P is providing sink switching must be powered from the same power source to provide adequate functionality from the diode clamping circuits.

2.5.4 LOW40/LOW40P Cleaning

If, for some reason, this product requires cleaning after delivery, most solvents that are based on: Fluorine, Chlorine, Aqueous, and Alcohol are safe to use.



CAUTION: Do NOT use gasoline or thinner type solvents on this product.

3. INSTALLATION

3.1 Overview

This chapter explains how to unpack and install the LOW40/LOW40P board. IP Module Logic Bus pin assignments and IP Module I/O pin assignments are included for your information.

3.2 Unpack the LOW40/LOW40P

The contents of the LOW40/LOW40P shipping packages are listed in Table 3-1:

Table 3-1 Contents of LOW40/LOW40P Shipping Packages

Qty	Description
1	LOW40/LOW40P Printed Circuit Assembly
1	LOW40/LOW40P Hardware Reference *

The Printed Circuit Assembly is enclosed in an anti-static box. The box and the manual are packaged together in a larger box. Save the shipping material in case the board needs to be returned.

* One manual is shipped for each board ordered. Extra manuals may be purchased by calling Systran or by mail. Use the prefix "BTMR-" followed by the product order part number (for example, BTMR-LOW40).

3.3 Visually Inspect the LOW40/LOW40P

Examine the LOW40/LOW40P to determine if any damage occurred during shipping.

3.4 Install the LOW40/LOW40P



NOTE: The LOW40/LOW40P is an Electrostatic Sensitive Device (ESD). Install the LOW40/LOW40P on an anti-static workbench to protect the IP Module and carrier boards.

The LOW40/LOW40P installation requires the following tools:

Table 3-2 LOW40/LOW40P Installation Tools

Qty	Description
1	ESD Static Control Kit/Ground Strap/Etc.
1	Standard Flat Head Screwdriver (Optional)

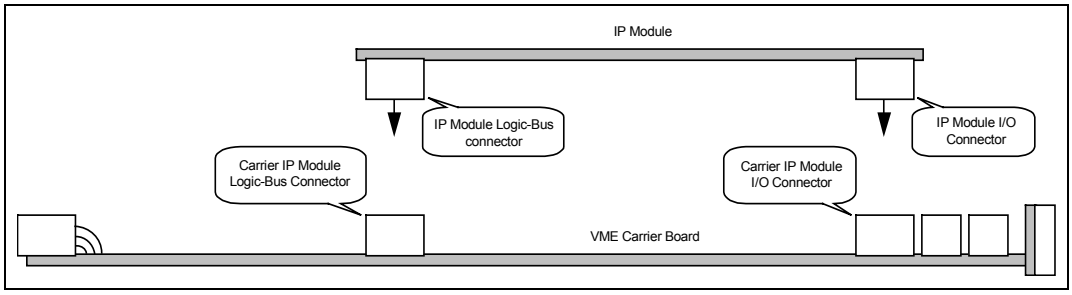


Figure 3-1 Installation of the LOW40/LOW40P on a VME IP Module Carrier Board

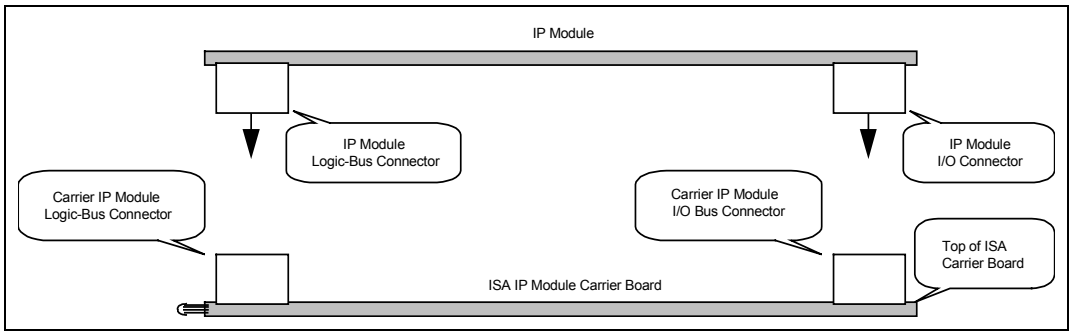


Figure 3-2 Installation of the LOW40/LOW40P on an ISA IP Module Carrier Board

Figure 3-1 shows how the LOW40/LOW40P is installed on a VME IP Module carrier, and Figure 3-2 shows how it is installed on an ISA carrier.

Table 3-3 shows the pin assignments for the IP Module Logic Bus connector. The signals on the left side of the connector are of the original IP Module signal nomenclature, and the signals on the right are those used by Systran Corp. Table 3-4 shows the pin assignments for the I/O connector. Refer to the IP Module Carrier board hardware reference for more information.

Referring to the appropriate figures and table described above, perform the following steps. The asterisk (*) denotes optional items.

1. Turn off all power to the host system.
2. Remove the target IP Module carrier and move it to the ESD controlled area where the installation of the LOW40/LOW40P can be made.
3. Remove the LOW40/LOW40P from the shipping package and place it on the ESD bench.
4. Install the LOW40/LOW40P onto the carrier board by applying adequate and equal pressure to the LOW40/LOW40P board at both ends.

*5. Install four M2x5mm flat head machine screws onto the IP Module carrier's IP Module connectors.

This completes the installation of the LOW40/LOW40P to the carrier board.

Table 3-3 IP Module Logic Bus Pin Assignments

Original IP Module Signals Names	IP Module Logic Bus Pin #	Systran Signal Names
GND	50	GND
reserved	49	RESERVED1
Ack*	48	N_ACK
A6	47	IPA6
Strobe*	46	N_STROBE
A5	45	IPA5
IntReq1*	44	N_INTREQ1
A4	43	IPA4
IntReq0*	42	N_INTREQ0
A3	41	IPA3
Error*	40	N_ERROR
A2	39	IPA2
DMAEnd*	38	N_DMAEND
A1	37	IPA1
reserved	36	RESERVED2
IOSel*	35	N_IOSEL
DMAck0*	34	N_DMACK0
IntSel*	33	N_INTSEL
DMAReq1*	32	N_DMAREQ1
MemSel*	31	N_MEMSEL
DMAReq0*	30	N_DMAREQ0
IDSel*	29	N_IDSEL
R/W*	28	IPR_N_W
+5V	27	+5VDC
GND	26	GND
GND	25	GND
+5V	24	+5VDC
+12V	23	+12VDC
-12V	22	-12VDC
BS1*	21	N_BS1
BS0*	20	N_BS0
D15	19	IPD15
D14	18	IPD14
D13	17	IPD13
D12	16	IPD12
D11	15	IPD11
D10	14	IPD10
D9	13	IPD9
D8	12	IPD8
D7	11	IPD7
D6	10	IPD6
D5	9	IPD5
D4	8	IPD4
D3	7	IPD3
D2	6	IPD2
D2	5	IPD1
D0	4	IPD0
Reset*	3	N_RESET
CLK	2	ICLK
GND	1	GND

Table 3-4 IP Module I/O Connector Pin Assignments

IP Module I/O Pin #	Signal Name
50	GND
49	Temperature
48	GND
47	P4B7
46	P4B6
45	P4B5
44	P4B4
43	P4B3
42	P4B2
41	P4B1
40	P4B0
39	GND
38	GND
37	P3B7
36	P3B6
35	P3B5
34	P3B4
33	P3B3
32	P3B2
31	P3B1
30	P3B0
29	GND
28	CATHODE
27	GND
26	P2B7
25	P2B6
24	P2B5
23	P2B4
22	P2B3
21	P2B2
20	P2B1
19	P2B0
18	GND
17	P1B7
16	P1B6
15	P1B5
14	P1B4
13	P1B3
12	P1B2
11	P1B1
10	P1B0
9	GND
8	P0B7
7	P0B6
6	P0B5
5	P0B4
4	P0B3
3	P0B2
2	P0B1
1	P0B0

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4. PERFORMANCE

4.1 Overview

Several sets of empirical data are provided that present typical performance parameters beyond those provided in the specification. The important point is that these are typical responses for the configuration cited, and do not supplant the maximum and minimum envelopes presented in appendix A: SPECIFICATIONS.

4.2 State Timing Diagrams

The state waveforms for Figures 4-2 through 4-6 were made using the HP 1GHz Timing Master Module and the Systran IP Module Logic Bus Extender (IPLBE) with the IP Module Logic Bus Breakout Board (IPLBB). Several of the signals on the logic analyzer‘s screen are active-low, and are represented by a ‘/’ as the first character as opposed to the ‘N_’ used elsewhere, due to the limited amount of character spacing.

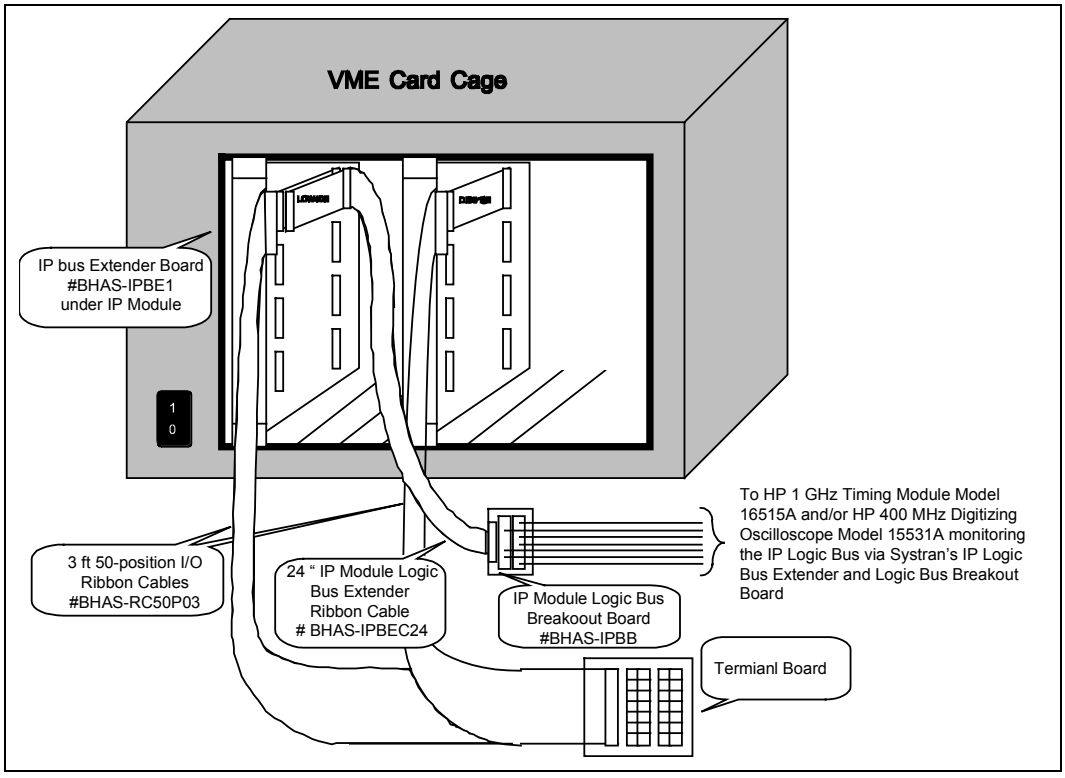


Figure 4-1 IP Module Test Configuration for State Timing Measurements

4.2.1 ID Read Cycle

Figure 4-2 is a complete LOW40/LOW40P ID read cycle. The signals of interest are /IDSEL, N_ACK, and the four IPD0-3 signals.

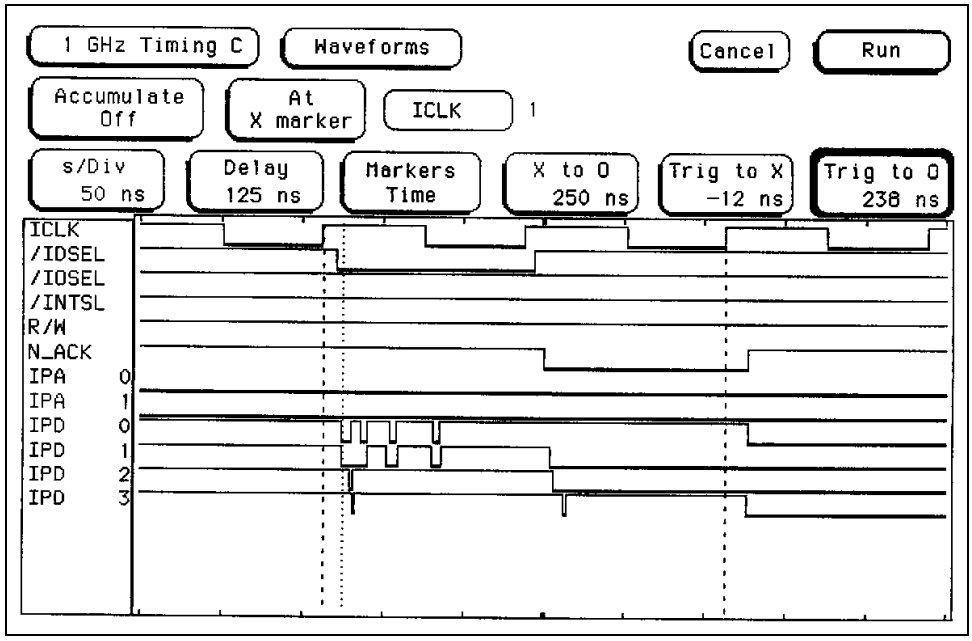


Figure 4-2 Complete LOW40/LOW40P ID Read Cycle

Figure 4-3 is a zoomed in view of the LOW40/LOW40P ID cycle driving the N_ACK and IPD0-3 signals; showing a typical response time of about 18 nanoseconds for driving these signals. The ANSI/VITA 4-1995 specification requires these signals be driven within 40 nanoseconds.

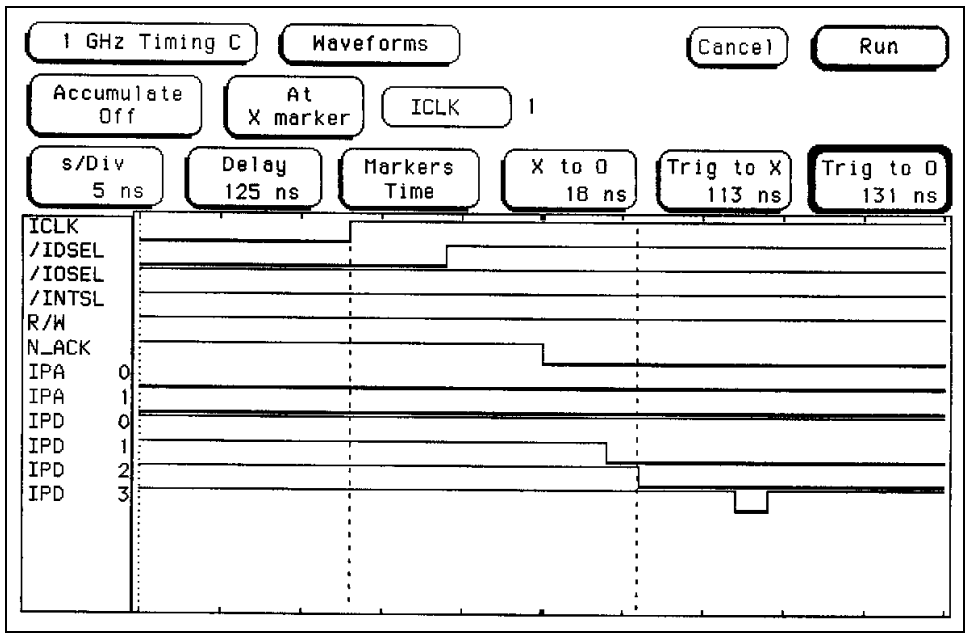


Figure 4-3 Zoomed-in Version of ID Cycle Driving N_ACK and IPD0-3

4.2.2 I/O Read Cycle

Figure 4-4 is a complete LOW40/LOW40P I/O read cycle. The signals of interest are /IOSEL, N_ACK, and the four IPD0-3 signals. Figure 4-5 is a zoomed- in view of the LOW40/LOW40P IO read cycle driving the N_ACK and IPD0-3 signals showing a typical response time of about 18 nanoseconds for driving these signals.

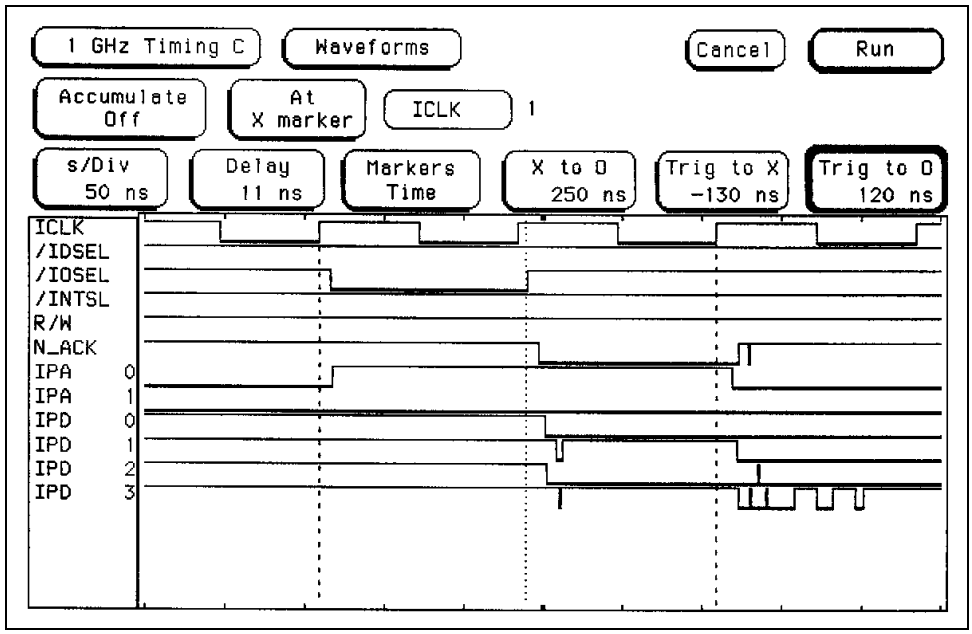


Figure 4-4 Complete LOW40/LOW40P I/O Read Cycle

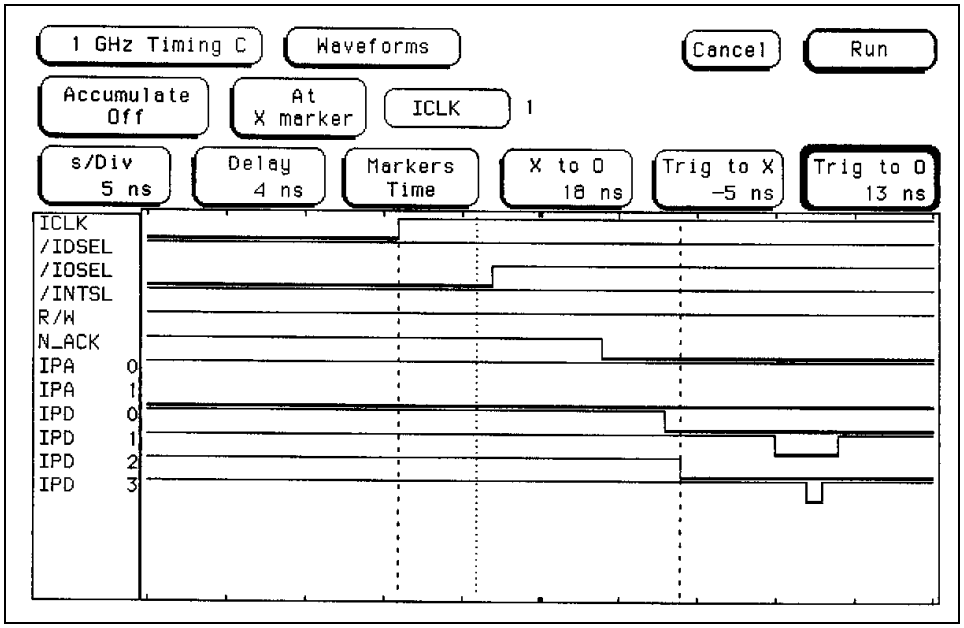


Figure 4-5 Zoomed-in Version of I/O Read Cycle Driving N_ACK and IPD0-3

4.2.3 Typical Output Response Time

Figure 4-6 shows a typical board response time of an output being asserted after an I/O write. In this figure the signal of interest is the Port 0 Bit 0 (which is the **PRT0B0** signal label on the waveform diagram) being asserted 4.698 µs after the end of the termination cycle of the I/O write to this data port. This delay, which is measured in microseconds rather than nanoseconds, is due to the parallel-to-serial conversion in the LOW40/LOW40P "Controller" module then the serial-to-parallel conversion in the MIC5842BWM/MIC58P42BWM low-side drivers.



NOTE: Figure 4-6 is very important information for users concerned about system response time. An I/O write to any data port will result in approximately a 4.7 µs delay until the output bit or bits are asserted.

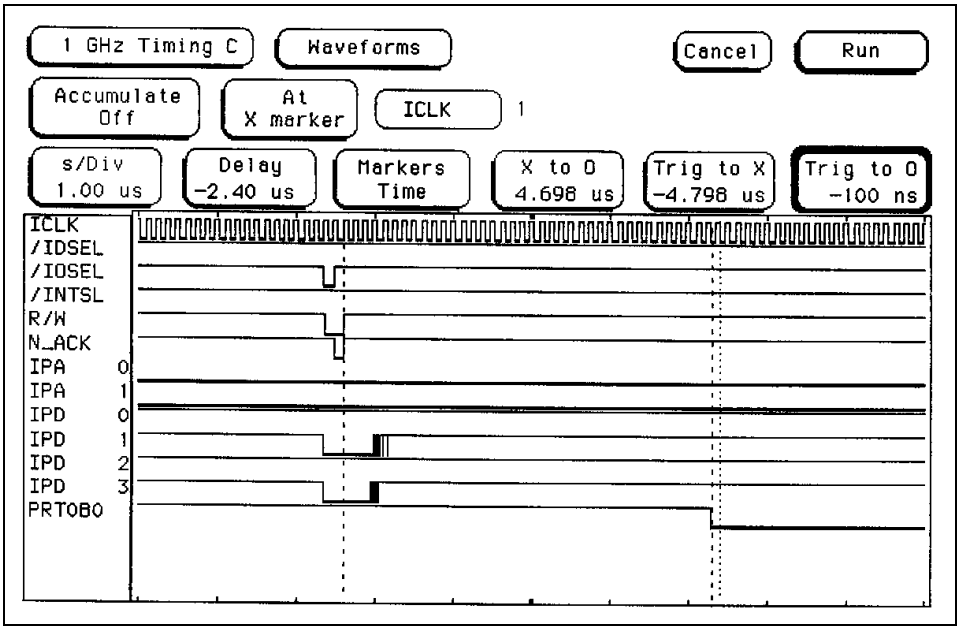


Figure 4-6 LOW40/LOW40P Typical Output Response Time



NOTE: For back-to-back writes to the LOW40/LOW40P, the serial transmission process to the drivers is terminated mid-stream without affecting the port outputs, and is restarted including the data from the latest write. All outputs are modified with the current data register information simultaneously within 4.7 µs of the last data register write transfer from the carrier.

APPENDIX A

SPECIFICATIONS

A.1 Specifications

MECHANICAL

Measurements ..... 1.800 inches x 3.900 inches x 0.303 inches (above board),
4.572 cm x 9.906 cm x 0.770 cm
Weight ..... 0.976 oz., 27.67 grams
Board thickness ..... 0.062 inches, 0.157 cm, nominally, (4 layer)

PROTOCOL

Clock rate ..... 8 MHz
Wait cycles ..... None on any transfer types
Hold cycles ..... Supported on all valid transfer types
Address decoding ..... Complete (no partial)
I/O transfers
- Writes ..... 8-bit and 16-bit
- Reads 16-bit

I/O locations ..... Four, 16-bit
- Ports 3
- Control 1
- Maximum read/write rate ..... 4 MTransfers/second, sustained

ID transfers ..... 8-bit read (only)
Zero-fill on upper byte
12 bytes, including CRC
Systran's manufacturer's ..... ID = 0x45, = E ASCII
LOW40/LOW40P's model number ..... 0x67, = g ASCII
Cyclic Redundancy Check value 0x60
Maximum read rate ..... 4 MTransfers/second, sustained
Memory transfers ..... Not supported
Interrupt Vector transfers ..... Not supported
Interrupt requests ..... None generated
DMA activity ..... Not supported
Acknowledgment on unsupported transfer attempts ..... None generated
- Memory read and write
- Interrupt read
- ID write, and addresses beyond those needed for valid transfers

POWER-UP DEFAULT CONDITION

All data registers power up as all 0's (I/O read of all 0's— '0x0000')
No accesses permitted or acknowledged during RESET

POWER REQUIREMENTS

Power: ..... +5 Vdc @ 87 mA (typical no load)

PERFORMANCE CHARACTERISTICS

Electrical Characteristics ..... Refer to Chapter 4, PERFORMANCE

ABSOLUTE MAXIMUM RATINGS:

Supply voltage with respect to ground:

Minimum ..... -0.3 V
Maximum ..... +5.55 V

RECOMMENDED OPERATING CONDITIONS:

Supply voltage:
Maximum ..... +4.75 V → +5.25 V
Logic Interface ..... ANSI/VITA 4-1995 specification compliant carrier

ENVIRONMENTAL SPECIFICATIONS:

Temperature (Operating): ..... 0°C to +70°C
Temperature (no bias, storage): ..... -65°C to +150°C
Humidity (Non-condensing): ..... 5% to 95%

MEAN TIME BETWEEN FAILURES (MTBF)

MIL-HDBK-217F ..... 2,533,419 hours
Bellcore 332, Issue 6..... 1,954,484 hours

The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

APPENDIX B

TYPICAL APPLICATIONS

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Figure B-2 LOW40/LOW40P Used for Lamp Drivers B-3

B.1 Applications

Systran extends an open invitation to all users to freely submit their applications that might, or do, use the LOW40/LOW40P IP Module to solve a problem. This section of the manual will be revised periodically to include new application ideas for all subsequent readers to consider. Help advance the level of technology by participating with our team, while simultaneously publishing your ideas.

Submission constitutes permission to publish without additional consent or compensation, and the author reserves the right to modify submissions to provide for more generic appeal, when necessary.

B.2 A Short Glossary Of Low-Side Driver Applications

The following typical applications were developed by using one or more channels on the LOW40/LOW40P IP Module. Most of the common low-side configuration operations may be performed (within limits) by proper connections and software manipulations.

B.2.1 Solenoid Driver

Figure B-1 is an application example that describes one of many possible configurations for using the LOW40/LOW40P as a peripheral power driver. This application is a Relay/Solenoid Driver example. The relays or solenoids can be turned on or off individually with I/O writes to the corresponding data port (with outputs already enabled) or by port (8-bits wide) by writing to the enable bits at IPA = 0x03.

B.2.2 Incandescent Lamp Driver

Figure B-2 is an application example of using the LOW40/LOW40P as an Incandescent Lamp Driver. The user can turn on or off the lamps individually with I/O writes to the corresponding data port (with outputs already enabled) or by port (8-bits wide) by writing to the enable bits at IPA = 0x03. Select lamps with proper current ratings to keep the overall power dissipation per port driver package below the absolute maximum rating of 1.2 W. For example, select eight 100 mA lamps @ a 100% duty cycle which would yield 0.88 W package power dissipation, or use four 200 mA lamps @ a 85% duty cycle yields 0.88 W of package power. Limit lamps in-rush currents to 500 mA to the LOW40/LOW40P low-side drivers.

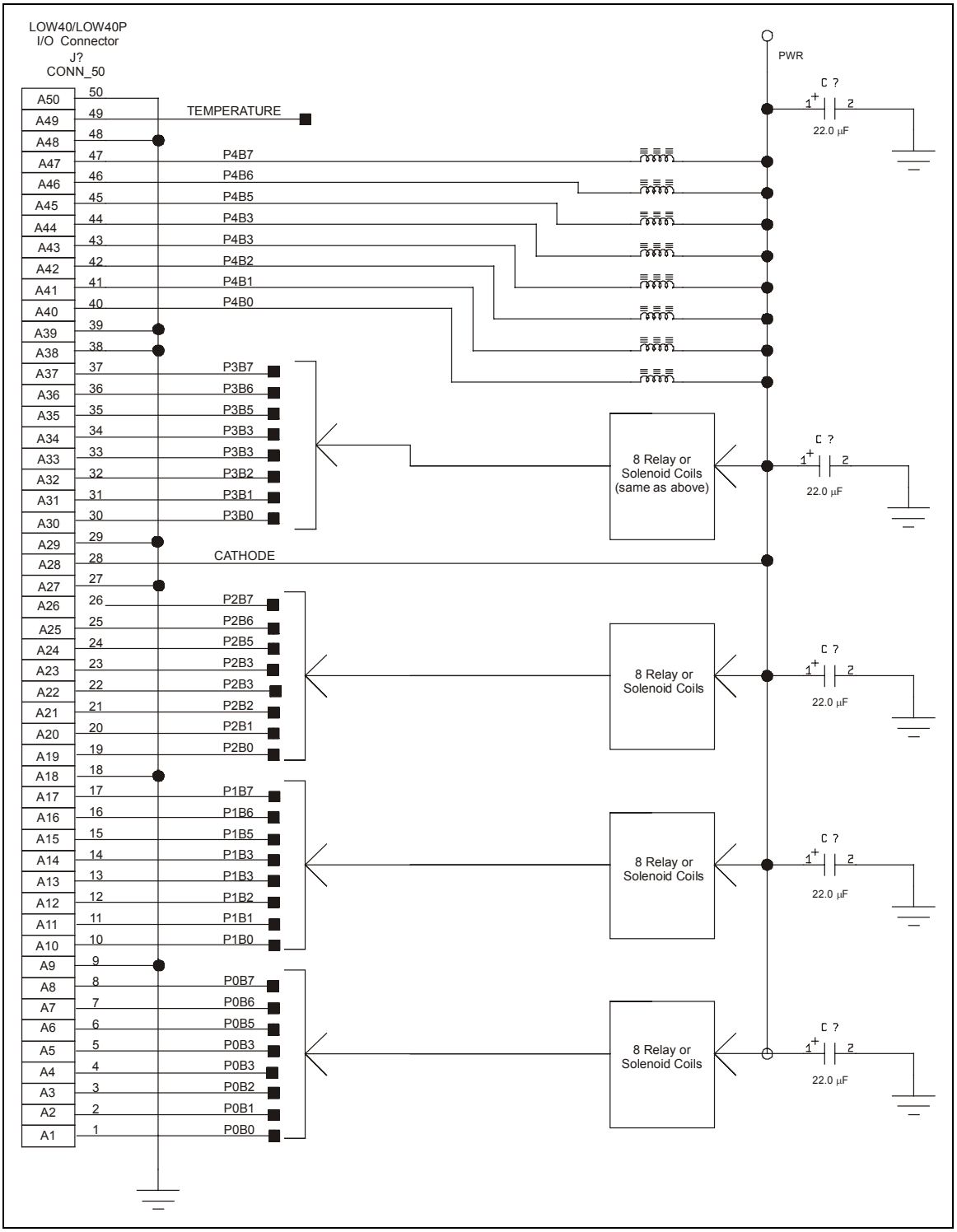


Figure B-1 LOW40/LOW40P Used for Relay/Solenoid Drivers

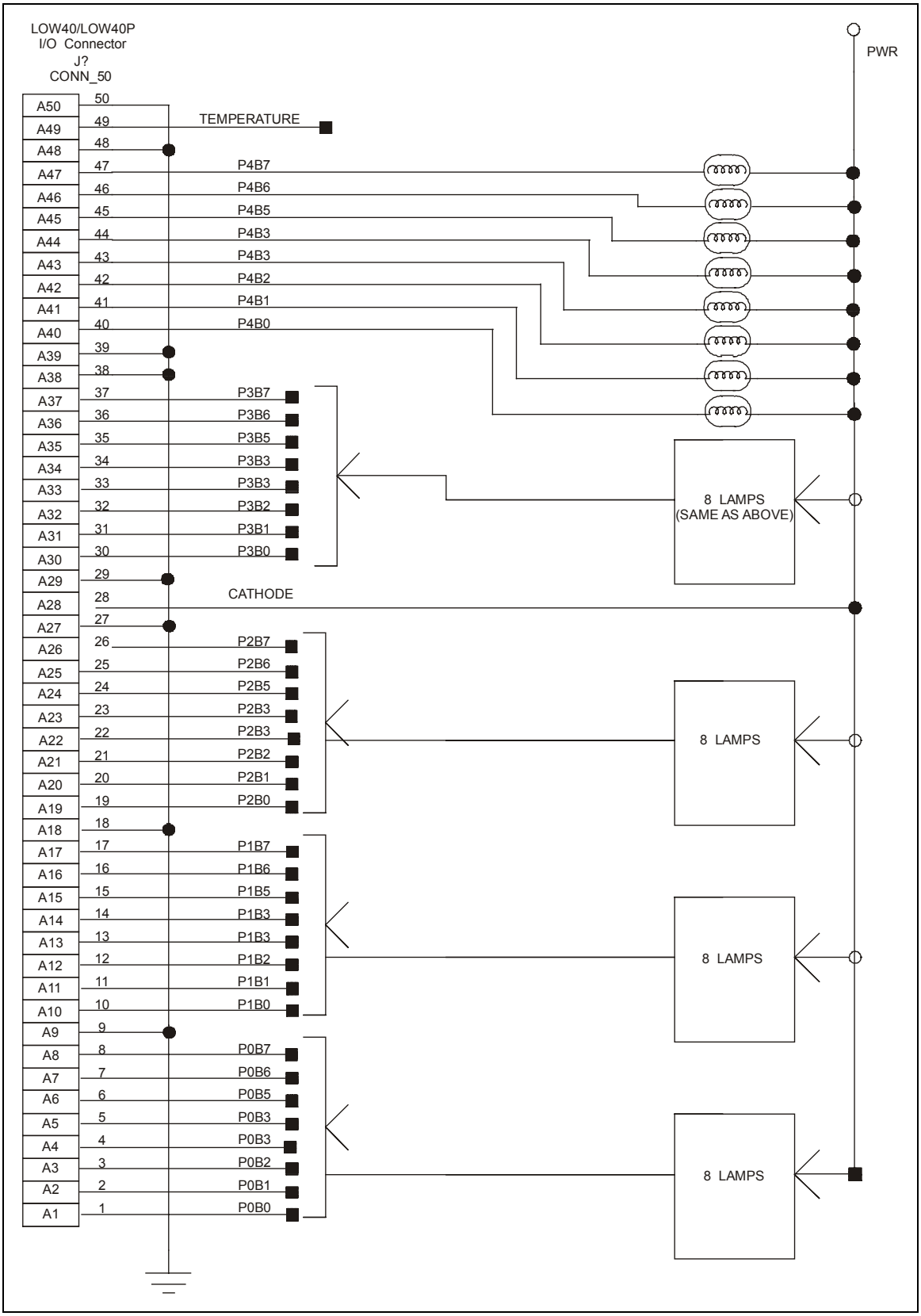


Figure B-2 LOW40/LOW40P Used for Lamp Drivers

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APPENDIX C

PROGRAMMING GUIDE

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C.1 Overview

This section of the manual describes the operation of the LOW40/LOW40P from the software perspective, detailing the LOW40/LOW40P registers and providing programming examples. A more detailed description of the hardware can be found in chapter 2 PRODUCT OVERVIEW and the application examples sections of this manual.

C.2 Description

The LOW40/LOW40P is an easy-to-use 40-channel low-side driver card. The outputs can be software enabled/disabled on byte boundaries. The LOW40/LOW40P has four 16-bit-wide registers: three data and one control. The data registers may be viewed as either three 16-bit registers or five 8-bit ports (IPA= 0x02 has port 4 data in byte-lane 0 and the upper byte-lane 1 (IPD[15:8]) reads as all zeroes). The single control register allows user control of output enable on byte boundaries. Byte writes to any of these registers are non-destructive to adjacent bytes.

C.3 IP Module ID PROM Listing

Emulating the ID PROM function is possible due to the never-changing information presented by it. It saves space, lowers costs, improves reliability, and enables this IP Module to provide “no-wait" read accesses of this information.



NOTE: The ID address space is fully decoded. Therefore, any attempt to access IPA addresses at and above IPA = 0x0C, or any attempt to write to ID space (if a carrier supports such a transfer) will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

The IP Module ID data is presented only on byte-lane 0 (IPD[7:0]). The upper byte-lane 1 (IPD[15:8]) reads as all zeroes during valid ID read-only accesses.

Table C-1 is the LOW40/LOW40P emulated ID Address Space PROM listing:

Table C-1 LOW40/LOW40P ID Address Space Listing

IP Module Address	Description	Data Read
IPA = 0x00	ASCII “I”	0x49
IPA = 0x01	ASCII “P”	0x50
IPA = 0x02	ASCII “A”	0x41
IPA = 0x03	ASCII “C”	0x43
IPA = 0x04	SYSTRAN’s ID	0x45
IPA = 0x05	LOW40/LOW40P’s Model Number	0x67
IPA = 0x06	Revision Level	0x30
IPA = 0x07	Reserved	0x00
IPA = 0x08	Low Byte Driver ID	0x00
IPA = 0x09	High Byte Driver ID	0x00
IPA = 0x0A	Number of Bytes Used	0x0C
IPA = 0x0B	CRC	0x60

C.4 IP Module I/O Address Map

The LOW40/LOW40P’s I/O Address Map was designed with efficiently located data and control/status registers in the IP Module I/O space (IPA = 0x00 ⇒ 0x03*)*.



NOTE: The address detector circuitry is fully decoded. Therefore, attempted accesses to IPA addresses at and above IPA = 0x04 will result in no acknowledgment and its subsequent bus time-out error on the carrier upon which this IP Module resides.

On power-up, all forty (40) data and five control bits defined below are cleared to a zero-state. This equates to the outputs being disabled and at a logic-high (near cathode potential) on the I/O connector’s port lines.

The first location (IPA = 0x00*)* is the write-and-read-back Data Register 0 for the output ports 0 and 1. Port 0 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 1 resides on byte lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte lanes simultaneously, and 16-bit reads of both bytes simultaneously.

The second location (IPA = 0x01*)* is the write-and-read-back Data Register 1 for the output ports 2 and 3. Port 2 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Port 3 resides on byte lane 1 such that accesses occur on IPD[15:8]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 8-bit writes to byte-lane 1 only, 16-bit writes to both byte-lanes simultaneously, and 16-bit reads of both bytes simultaneously.

The third location (IPA = 0x02*)* is the write-and-read-back Data Register 2 for the output port 4. Port 4 resides on byte-lane 0 such that accesses occur on IPD[7:0]. Valid accesses to and from this location include: 8-bit writes to byte-lane 0 only, 16-bit writes to both byte-lanes simultaneously (with byte-lane 1 data ignored), and 16-bit reads of both bytes simultaneously with the upper byte-lane 1 (IPD[15:8]) read as all zeroes. An 8-bit write to byte lane 1 is not supported, and will result in no acknowledgment and its subsequent bus time-out error.

The fourth location (IPA = 0x03) is the write-and-read-back Control Register for the control and status of the output-enable bits (referred to as CR, and CR bits as CR or CR[:]). There are five (5) functional bits in this CR that are defined as follows. Bits [4:0] are the output-enable bits with bit 4 to control Port 4 down to bit 0 for Port 0. When a bit is set to a '1' (logic high) the corresponding output port is enabled, and when it is set to a '0' (logic low) the corresponding output port is disabled. In the CR, bits [15:5] are not used and are read as zeros.



NOTE: (LOW40P Only) After an over-current shutdown occurs, the channel output is off (floating, not sinking current), and must be reset by toggling the output-enable bit to '0' and back to '1.'

Table C-2 is the LOW40/LOW40P I/O Address Map and contains the data register.

Table C-2 LOW40/LOW40P I/O Address Map

IP Module Address	Byte-Lane 1	Byte-Lane 0	Description
IPA = 0x00	Data Port 1	Data Port 0	Data Register 0 = Ports 1 and 0, 8 bits each
IPA = 0x01	Data Port 3	Data Port 2	Data Register 1 = Ports 3 and 2, 8 bits each
IPA = 0x02	[XXXX,XXXX]	Data Port 4	Data Register 2 = Port 4, 8 bits
IPA = 0x03	[XXXX,XXXX]	[XXX] [4:0]	Control Register 0, (CR0) output enables/reset for ports 4 to 0, 0 = Disabled, 1 = Enabled

C.5 Word Access Address Translation

Table C-3 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for word accesses. In the table, BASE represents the I/O or ID base address. All addresses are in hexadecimal.

Table C-3 Word Access Address Translation Table

VMEBus Address	PC-AT Bus Address	NuBus Address	IP Module Address
BASE + 0x00	BASE + 0x00	BASE + 0x02	IPA = 0x00
BASE + 0x02	BASE + 0x02	BASE + 0x06	IPA = 0x01
BASE + 0x04	BASE + 0x04	BASE + 0x0A	IPA = 0x02
BASE + 0x06	BASE + 0x06	BASE + 0x0E	IPA = 0x03
BASE + 0x08	BASE + 0x08	BASE + 0x12	IPA = 0x04
BASE + 0x0A	BASE + 0x0A	BASE + 0x16	IPA = 0x05
BASE + 0x0C	BASE + 0x0C	BASE + 0x1A	IPA = 0x06
BASE + 0x0E	BASE + 0x0E	BASE + 0x1E	IPA = 0x07
BASE + 0x10	BASE + 0x10	BASE + 0x22	IPA = 0x08
BASE + 0x12	BASE + 0x12	BASE + 0x26	IPA = 0x09
BASE + 0x14	BASE + 0x14	BASE + 0x2A	IPA = 0x0A
BASE + 0x16	BASE + 0x16	BASE + 0x2E	IPA = 0x0B

C.6 Byte Access Address Translation

Table C-4 shows the relationship between VME, PC-AT, and NuBus local bus addresses, and the IP Module address for byte accesses. In the table, BASE represents the I/O or ID* base address. All addresses are in hexadecimal.

Table C-4 Byte Access Address Translation Table

VMEBus Address	PC-AT Bus Address	NuBus Address	IP Module Address	Byte-Lane*
BASE + 0x01	BASE + 0x00	BASE + 0x03	IPA = 0x00	0
BASE + 0x00	BASE + 0x01	BASE + 0x02	IPA = 0x00	1
BASE + 0x03	BASE + 0x02	BASE + 0x07	IPA = 0x01	0
BASE + 0x02	BASE + 0x03	BASE + 0x06	IPA = 0x01	1
BASE + 0x05	BASE + 0x04	BASE + 0x0B	IPA = 0x02	0
BASE + 0x04	BASE + 0x05	BASE + 0x0A	IPA = 0x02	1
BASE + 0x07	BASE + 0x06	BASE + 0x0F	IPA = 0x03	0
BASE + 0x06	BASE + 0x07	BASE + 0x0E	IPA = 0x03	1
BASE + 0x09	BASE + 0x08	BASE + 0x13	IPA = 0x04	0
BASE + 0x08	BASE + 0x09	BASE + 0x12	IPA = 0x04	1
BASE + 0x0B	BASE + 0x0A	BASE + 0x17	IPA = 0x05	0
BASE + 0x0A	BASE + 0x0B	BASE + 0x16	IPA = 0x05	1
BASE + 0x0D	BASE + 0x0C	BASE + 0x1B	IPA = 0x06	0
BASE + 0x0C	BASE + 0x0D	BASE + 0x1A	IPA = 0x06	1
BASE + 0x0F	BASE + 0x0E	BASE + 0x1F	IPA = 0x07	0
BASE + 0x0E	BASE + 0x0F	BASE + 0x1E	IPA = 0x07	1
BASE + 0x11	BASE + 0x10	BASE + 0x23	IPA = 0x08	0
BASE + 0x10	BASE + 0x11	BASE + 0x22	IPA = 0x08	1
BASE + 0x13	BASE + 0x12	BASE + 0x27	IPA = 0x09	0
BASE + 0x12	BASE + 0x13	BASE + 0x26	IPA = 0x09	1
BASE + 0x15	BASE + 0x14	BASE + 0x2B	IPA = 0x0A	0
BASE + 0x14	BASE + 0x15	BASE + 0x2A	IPA = 0x0A	1
BASE + 0x17	BASE + 0x16	BASE + 0x2F	IPA = 0x0B	0
BASE + 0x16	BASE + 0x17	BASE + 0x2E	IPA = 0x0B	1

* Byte-lane 1 is not applicable for ID space

C.7 Data Register 0 (IPA = 0x00)

This 16-bit read/write register is the data register consisting of the 8-bit-wide ports 0 and 1. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of '1' and turned off with a bit value of '0'. On power-up, all bits are set to '0'.

Table C-5 Data Register 0 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Pn7 - Pn0 : Port n data bits 7 through 0.
Bit 0 is the least significant bit.

C.8 Data Register 1 (IPA = 0x01)

This 16-bit read/write register is the data register consisting of the 8-bit-wide ports 2 and 3. These two 8-bit ports can also be viewed as a single 16-bit register. When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of '1,' and turned off with a bit value of '0.' On power-up, all bits are set to '0.'

Table C-6 Data Register 1 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20
R/W	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

C.9 Data Register 2 (IPA = 0x02)

This 16-bit read/write register is the data register for the 8-bit-wide port 4. This 8-bit port can also be accessed as a 16-bit register with bits 15 through 8 set as “don't care”. When this register is written to, it sets the on/off state of the drivers. When read, the register returns the on/off state of the drivers. A driver is turned on with a bit value of ‘1’, and turned off with a bit value of ‘0’. On power-up, all bits are set to ‘0’.

Table C-7 Data Register 2 Bit Descriptions

Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bit Name	X	X	X	X	X	X	X	X	P47	P46	P45	P44	P43	P42	P41	P40
R/W	Read as 0’s, Writes discarded								RW	RW	RW	RW	RW	RW	RW	RW
Power-Up State	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0

X = Don’t care

C.10 Control Register (IPA = 0x03)

This 16-bit-wide read/write register selects the output-enable control. The output-enable control can be selected on 8-bit port boundaries. A bit value of ‘0’ disables the corresponding port's output, and a bit value of ‘1’ enables the port’s output. On the LOW40P, a bit value of ‘0’ also resets the channel output if an over-current shutdown occurs.

Table C-8 Control Register Bit Descriptions

Bit #	Bits 15 to 5	4	3	2	1	0
Bit Name	Not used	P4 0E	P3 0E	P2 0E	P1 0E	P0 0E
R/W	Read as 0’s Writes discarded	RW	RW	RW	RW	RW
Power-Up State	N/A	0	0	0	0	0

Table C-9 OE: Output-Enable/Reset Control Bits

OE Bit Value	Output Enable Selection Per Port
0	Port outputs disabled
1	Port outputs enabled

C.11 Programming Example

This example illustrates output-enable control of the LOW40. Only port 0 is controlled in this example, however, the mechanism is the same for all the ports.

- At power up, the data registers are all cleared (value of '0x0000').
- At power up, the control register is cleared (value of '0x0000'). At this point, the outputs are disabled.
- Write '0xFF' to the port 0 data register.
- At this point the outputs are still disabled (drivers off) because the output-enable control bit for this port is 0 (disabled).
- Write '0x0001' to the control register enabling port 0's outputs. At this point the outputs are enabled (drivers on, outputs near ground).
- Write '0x00' the port 0 data register.
- At this point the outputs are disabled (drivers off) because the data register value of '0x00' turns off the drivers.
- Write '0x0000' to the control register to return to the power-up state.

GLOSSARY

[x:y]	Nomenclature designating a bit-range, where “x” is the left-most bit and “y” is the right-most bit. (e.g. Data bus [7:0] refers to the Least Significant eight bits).
byte-lane	8-bits of a data bus on octal boundaries.
CAE	Computer Aided Engineering.
channel	One of the eight low-side driver outputs on a port.
doublewide	An IP Module that is twice the size of the singlewide board.
EPLD	Erasable Programmable Logic Device.
ID PROM	The circuitry that presents the proper data patterns to the low 8-bits of the IPDbus, with upper-byte zero fills, during the ID (read) transfers.
IP Module	Business-card size mezzanine-type subsystems designed with a common digital interface known as the IP bus. These field-installable plug-and-play modules are automatically recognized by system software. An open industry standard defines the mechanical and electrical interface to the carrier board.
I/O	Input/Output.
IP Module logic bus	A synchronous, 8 Mbytes/sec, 16-bit wide bus that includes I/O, memory, ID PROM, interrupts. The address bus is 6-bit wide, except in memory mode. Then the data bus is multiplexed for the upper portion of the address bus, resulting in 22 bits of address. This results in up to 4 Mwords of memory space per IP Module.
IPDbus	IP Module Data Bus.
MTBF	Mean Time Between Failures.
ns, μs, ms	Nanoseconds, microseconds, and milliseconds, respectively.
singlewide	An IP Module printed circuit board (3.9" by 1.8"). Each module has two 50-pin connectors.
SOIC	Small outline integrated circuit packages
VHDL	Very high-speed integrated circuit Hardware Description Language.

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