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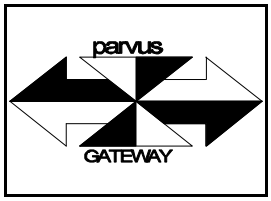
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CORPORATION

USER MANUAL

parvus' QUAD ARINC 429 SMCARD





2/3/2000

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parvus' QUAD ARINC 429 SMCard

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INTRODUCTION

The parvus ARINC 429 SMCARD provides an interface between the an ARINC 429 or similar protocol and shared memory. The SMCARD is intended to be used with an SMCARD socket such as those found on PC/104 Multi-Function DPRAM Boards, ISA DPRAM Boards, parvus Handhelds, or DPRAM Gateways.

The QUAD ARINC 429 SMCARD has four receiver ports and no transmitter ports. The receivers are optically isolated with an input impedance of greater than 1k ohms.

The receiver of this SMCARD can receive from 1 to 32 bits. The end of the transmission frame occurs when more than 4-8 bit times have passed with no active data present. Bit rates of 12K - 14K, and 100K are possible by setting the crystal frequency and speed select bits in the configuration. The receiver can receive at a data rate of 10-15K and at 90-110K in high and low speed modes. Bipolar RZ signaling is maintained throughout.

Although a transmitter portion is defined in the shared memory map it is for consistency with other parvus products and future versions of this product or similar products. Reads and writes to the transmitter have no effect on the operation of the Quad SMCARD.

The ARINC 429 SMCard is placed on a PC/104 Multi-Function Dual Port RAM Board. The addressing of the SMCard is defaulted to &HD000 or &HD800. The Internal address of the SMCard is fixed at &H4000 for on-board 68HC11 MPUs. The network is attached to the SMCard through a screw clamp header. The SMCard is mounted upside on the MFDPRAM board. Most of the data populated in the shared memory map is for reference only.

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GENERAL SMCARD FUNCTION

A Shared Memory Card or SMCard contains a local processor and the physical medium driver of communications or network style for which it was designed. The local CPU of the SMCard has program and data memory as well as all of the required peripherals for complete implementation of the desired communications protocol. The processors found on SMCards are either the 68HC11, 6805, or the 8051 depending on the card or implementation.

All SMCards contain as a minimum, these similar attributes. They allow the SMCards to be interchanged without the need to be concerned with communications protocol. The primary attributes are:

1. Complete Local CPU
2. Physical network or communication connector
3. Communications media driver
4. Shared memory connection
5. Permanent configuration memory

The memory structure of the SMCard is such that all of the CPU's program and data memory is available for the communications and/or applications driver and that the assess to the shared memory or dual port memory and peripherals are through a paging scheme where possible. The three CPUs are organized as follows:

The 6805 memory structure is that of the component itself as all CPU resources are embedded within the CPU. The communications component and shared memory interface is accessed through a parallel port interface using external latches and buffers. This CPU operates at 4.9152 Mhz for generation of standard baud rates when required.

The 68HC11 has 32k of program space located between 8000h and FFFFh with 32k of RAM located between 0000h and 7FFFh. Shared memory access or 16k is paged between 4000h and 7FFFh and any communications component is accessed in paged space between 0400h and 7FFFh. This CPU operates at 7.3728 Mhz for generation of standard baud rates when required.

The 8051 has 64k of program space located between 0000h and FFFFh with 32k of RAM located in data space between 0000h and 7FFFh. Shared memory access of 16k is available between 8000h and BFFFh and any communications component is accessed between C000h and FFFFh. This CPU operates at 11.059 Mhz for generation of standard baud rates when needed.

These are fairly common memory maps for the associated CPUs and can support almost any communications driver or communications application. Since each of these processors has a local asynchronous serial port, the port is made available for external connection and diagnostics when that port is not needed for its primary communication interface such as on a CAN or multi-bit interface.

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All communications connections exit the board through a common location at the end of the SMCard. The SMCards are a uniform 2.5 x 3.5 size with standardized mounting holes, .2 inch from each corner. The shared memory connection can be mounted on the top or bottom of the board depending on space requirements and is always in the same location.

Software drivers are available for all SMCards and peripherals. By using the parvus MODOBJ application object manager, it is possible to generate customized software for the SMCard by simple setting the properties of the associated application objects and downloading the resultant executable code to the SMCard or program ROM for operation.

The SMCard interfaces to the bus through a dual port RAM component. This component has two specific locations that can be written to cause interrupt generation on the attached bus. The address 7FE hex is written to by the SMCard with a value as to what caused the interrupt. A read of this address clears the interrupt.

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MEMORY ORGANIZATION

The shared memory assignments of the SMCARD are unique to the protocol that they are converting to or from. The ARINC 429 SMCARD has the following memory assignments.

000-00F Identification register

- 0-2 Version, Major, Minor
- 3-A Name (ascii)
  "SM_ARINC"
- B-F unassigned

010-01F Configuration Register

- 10 System Mode (Byte)
  - 0 - Arinc 100K baud select
  - 1 - Arinc 12.5K baud select
  - 2 - Not Used
  - 3 - Source LSB (00-Channel #0) (01-Channel #1)
  - 4 - Source MSB (10-Channel #2) (11-Channel #3)
  - 5 - Error Interrupt Enable
  - 6 - Not Used
  - 7 - Receiver Interrupt Enable
- 11 Status Register (bit mapped)
  - 0 - Current Parity Status
  - 1 - Parity Error
  - 2 - Current Received Composite (1 & 0) Data
  - 3 - Overrun Error
  - 4 - Current Frame Status (1-transmitting)
  - 5 - Frame Transmitted (1 Sent)
  - 6 - Current Frame Status (1=receiving)
  - 7 - Frame received (1=ready)
- 12,13 Channel Dwell Scan Count - MSB, LSB
- 14 Scan Mode Enable
  - 0 - Disabled
  - 1 - Enabled
- 18 Repeat Interval (byte)
  .01 second resolution
- 1F Alive Count (byte)

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020-02F		Receiver Register
	20	Rx Mode (Byte) 0 - No Operation 1 - 2 - 3 - Single Transmission 4 - Continuous Transmission 5 - 6 -
	28,29	Received Packet Count
	2A	Parity Error Count (no rollover from FF to 00)
	2B	Overrun Error Count (no rollover from FF to 00)
	2C	Most Significant Rx Byte
	2D	Middle MSB
	2E	Middle LSB
	2F	Least Significant Rx Byte
030-03F		Transmitter Register
	30	Tx Mode (byte) 0 - No Operation 1 - Clear Status 2 - 3 - Single Transmission 4 - Continuous Transmission 5 - Receiver Echo 6 - Reset System (old method)
	31	Value to be applied with Clear Status (1 in bit position clears bits in register 11, Must be written before Clear Status)
	38,39	Transmitted Packet Count
	3C	Most Significant Tx Byte
	3D	Middle MSB
	3E	Middle LSB
	3F	Least Significant Tx Byte
040-04F		CARA RT register
	00	Host Request
	01	SMCard Response
	02	Altitude MSB
	03	Altitude LSB
	04	Status Flags
	45-4F	Not used

0A0-0AF	Record Information (offset loaded from 0AE)

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	0	Record Command 0 - Disabled 1 - Continuous Read 2 - Single Read 255 - End of record marker
	1	Record Status
	2-3	Received packet count
	4	Mask MSB, 0 - Ignore, 1 - Enable
	5	.
	6	.
	7	Mask LSB
	8	Compare MSB
	9	.
	10	.
	11	Compare LSB
	12	Value MSB
	13	.
	14	.
	15	Value LSB
7FE		SMCard to HOST interrupt register SMCard Write causes Host Interrupt Host Read clears Host Interrupt 00 - Inactive 01 - Receiver Interrupt 02 - Transmitter Interrupt 03 - Parity Interrupt 04 - Overrun Interrupt
7FF		HOST to SMCard interrupt register Host Write causes SMCard Interrupt SMCard Read clears SMcard Interrupt

Notes:

1. This version of hardware does not support data transmission. Ignore all Command input.
2. When transmitter has been started and Tx repeat is active, the hardware will automatically resend the last data at a very high repeat speed with only 6 bit times between frames.
3. Continuous Transmission mode is managed by on-board software and repeats at a used defined interval.
4. Tx and Rx modes and buffers are initialized to zero upon reset.
5. Receiver Echo mode reads in the last received frame and then updates the transmission buffer. The receive and transmits are not synchronized.
6. Status bits are cleared by issuing a Clear Status command with +31 containing the bits to clear.
7. Interrupts are cleared by reading address 7FE hex.
8. Word values are stored in Motorola Format, High Byte first, Little Endian
9. All values and registers are in hex

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SYSTEM MODE BYTE

The System Mode Byte controls the processor interrupt access, the matching ARINC line baud rate and the channel selection. The channel selection is automatically controlled by the processor, but the first two values must be input from direct access using the MEMTOOL utility program and is located at OFFSET 0, LOCATION 10.

The following will explain the 'BIT' definitions:

BIT	
7	Receive Interrupt Enable
6	Not used, must be '0'
5	Error Interrupt Enable
4	Channel Select (processor controlled)
3	Channel Select (processor controlled)
2	Not used
1	Receive 12.5K speed ARINC line (bit 0 must be 0)
0	Receive 100K speed ARINC line (bit 1 must be 0)

The following two examples are the two acceptable bit combinations allowed (Offset 0, Location 10)

COMMAND BITS 76543210	
101xxx10	Enable access for 12.5K baud ARINC line
101xxx01	Enable access for 100K baud ARINC line

CHANNEL DWELL ACCESS CONTROL

The processor will update the Record Table of any selected channel for a specific number of receptions of Raw Data Packets (32 bits) before moving on to the next selected channel for updating.

The number of Packet receptions allowed during any channel Record Table update or 'DWELL', can very simply be controlled. The two bytes at (Offset 0, Location 12 and 13) control this count directly.

Location 12 is the high byte, and Location 13 is the low byte and require hexadecimal values.

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The following are examples:

HIGH BYTE	LOW BYTE	Packet Update Count During Channel Dwell
00	01	One
00	10	Sixteen
01	00	256 (decimal)
10	00	4096 (decimal)

During the period of time that the processor is updating the Record table for a particular channel, the Record tables for the other active channels are not being updated with the identified Label Packets which may be available on their respective ARINC data lines.

Only when one channel is active, are all identified LABEL packets being updated on the Record Table for that channel.

SCAN ENABLE COMMAND BYTE

The byte location a (Offset0, Location 14) provides the means to activate the SCAN process.

If the value here is set to zero, the scan process will terminate for all channels. Any value other than zero will begin the scan process.

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SEMAPHORE ACCESS OF THE ARINC CONTROLLER

A SEMAPHORE ACCESS operation has been provided which allows for data read operations of four data bytes from a Monitor Record during which time Scan Updates have been suspended. This operation guarantees accessing valid data from any Monitor Record without Scan Update occurring.

For each active Monitor Record, the first two bytes are Command and Status respectively. Detailed clarification of these two bytes follows:

COMMAND BITS	DEFINITION
76543210	Bit locations
00000000	Skip this record for all scan updates
00000001	Continuous scan update for this record
00000010	Single scan update only for this record
11111111	End of record scan file for this channel
1xxxxxxx	Request for Semaphore Read Access with return status indication

STATUS BITS	DEFINITION
76543210	Bit locations
xxxxxxx1	Indication of valid scan update of latest record
1xxxxxx1	indication of scan suspend, valid data available
1xxxxxx0	Indication of scan suspend, no valid data available

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The STATUS (1xxxxxx1) indication will only occur after the COMMAND byte is written with (1xxxxxxx). The STATUS (1xxxxxx1) indication will remain valid until the COMMAND (1xxxxxxx) byte is overwritten with either a Continuous (00000001) or Single (00000010) Scan Command.

The value of 'Semaphore Read Access' with 'Return Indication', is that the application program can notify of an impending record read operation by writing (1xxxxxxx) into the command byte, but delay the read operation until the 'Return Status Indication' notification (1xxxxxx1) is read and verified from the Status byte. During this period that (1xxxxxxx) is written to the command byte and the status indications is (1xxxxxx1), all updates are suspended for this record.

It is only bit 7 of the command byte which controls the Semaphore Read Access operation, and only bit 7 of the status byte which indicates record update suspension. The following definitions are provided for the four states which comprise of these two bits:

Command bit 7 = 0	No record data read requested
Status bit 7 = 0	Scan active for this record
Command bit 7 = 1	Data read requested for this record
Status bit 7 = 0	Scan active (read should not be made)
Command bit 7 = 1	Data read requested for this record
Status bit 7 = 1	Record scan suspended (valid read OK)
Command bit 7 = 0	No record data read requested
Status bit 7 = 1	Record scan suspended (system has not yet cleared this bit following the last Command operation)

The 'Return Indication' process is always active. However, the computer 'Turn around time' can be made to operate with less delay time.

The byte at (Offset 0, Location 15) can be used to control this. If this byte is set to zero (00 hex), then the 'Slow' reaction time is active. If any value other than zero is written to this memory location, then the "Fast' reaction time is active. This means that the reaction time between the 'Read Access Request' operation and the 'Return Status Indication' notification will be significantly reduced.

This may be useful for the Application Program when accessing the DPRAM memory if fast response times to the Access requests are beneficial.

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SCAN UPDATE PROCESSING

The process of scan updating can to some extent be controlled. This may be necessary if the processing time of each scan update needs to be kept to a minimum.

This 'Processing Scan Time' becomes critical when operating at the 100K baud rate. If it is desired that all 'Packets' being received on the ARINC429 channel line be processed, then all scan processing must be completed before the next 'Packet' is ready to be processed. If the 'Packets' are being received within the ARINC429 defined minimum 'Intergap time' (four bit times), then the 'Processing Scan Time' must be completed within the time of 360 microseconds. To take longer would mean that packets would be lost. It should be noted that the 'Intergap Time' may not be the minimum four bit times. This is the 'Defined' minimum, but the transmitting device can arbitrarily set this to anything greater. This is simply the 'Defined' minimum.

The actual time required by the processor to scan update a table depends upon the number of records which have been placed. The processor must then process each new 'Packet' and compare the Label and or data with that placed in the Record Table.

It has been made possible to 'Limit' some of the scan processing which then will result in the saving of scan time.

When in Memtool, the memory locations (Offset 0, Location 16) and (Offset 0, Location 17) can be used to reduce the scan time.

Location (Offset 0, Location 16):

If it is desired that the scan process should terminate with one valid record compare of the last packet received, then the value of FF need be placed at the memory location (Offset 0, Location 16). Otherwise, if all records for a channel should be scanned, then 00 should be placed at that memory location.

Location (Offset 0, Location 17):

If it is desired that only the Label byte (the first eight bits) of the last packet received be used for compare with the records on the channel table, then the value of FF need be placed at the memory location (Offset 0, Location 17). Otherwise, if all 32 bits of the last packet should be compared with each of the records on the channel table, then 00 should be placed at that memory location. This will enable the masking operations for all 32 bits.

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Cara R/T Altitude Mode

Register 40 is intended as the primary interface to the host application when using the Altimeter mode. It is a semaphore protected buffer that allows the host to read the multi-byte register without possibility of byte skewing. The host writes any non-zero byte into register +40. This acts as a request for the SMCard. The current altitude information is then transferred to the protected buffer area and the +40 value is transferred to +41 and the +40 location is zeroed. The running total counts can be read at any time or even zeroed. Most operations are managed by mode control values. Transmit and receive mode control values cause specific operations to occur either continuously or as single events.

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SMCARD INSTALLATION

The installation of the ARINC 429 SMCard is quite straightforward. An address is selected on the Multi-Function DPRAM card that is used in the PC/104 memory space. The suggested address for the PC/104 bus side is D000 or D800 hex as these are usually available is a PC/104 system. The secondary side of the MFDPRAM board should be set to an address of 4000. Interrupts do not need to be installed in most cases and can be left without jumpers so as not to conflict with other products. The desired interrupt jumper must be selected and installed if interrupts are to be used.

The SMCARD is mounted upside down on the MFDPRAM board and has no optional jumpers.

Wiring to the screw clamp connector is set up in pairs. With the board upright and the connector at the bottom, the connector is numbered 1 to 8. The channels are as follows:

1 - Channel #1 +
2 - Channel #1 -
3 - Channel #2 +
4 - Channel #2 -
5 - Channel #3 +
6 - Channel #3 -
7 - Channel #4 +
8 - Channel #4 -

Note that the board is placed upside down on the MFDPRAM board and that the numbering is with the board component side up.

When using the board and a channel is continuing to give parity errors, it is possible that the polarity of the channel is reversed. Simply reverse the pair of wires going to that channel to correct the problem.

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CONNECTION

All communications to and from the host system occur through dual port ram. The following describes the pinouts of the DPRAM connector, J1.

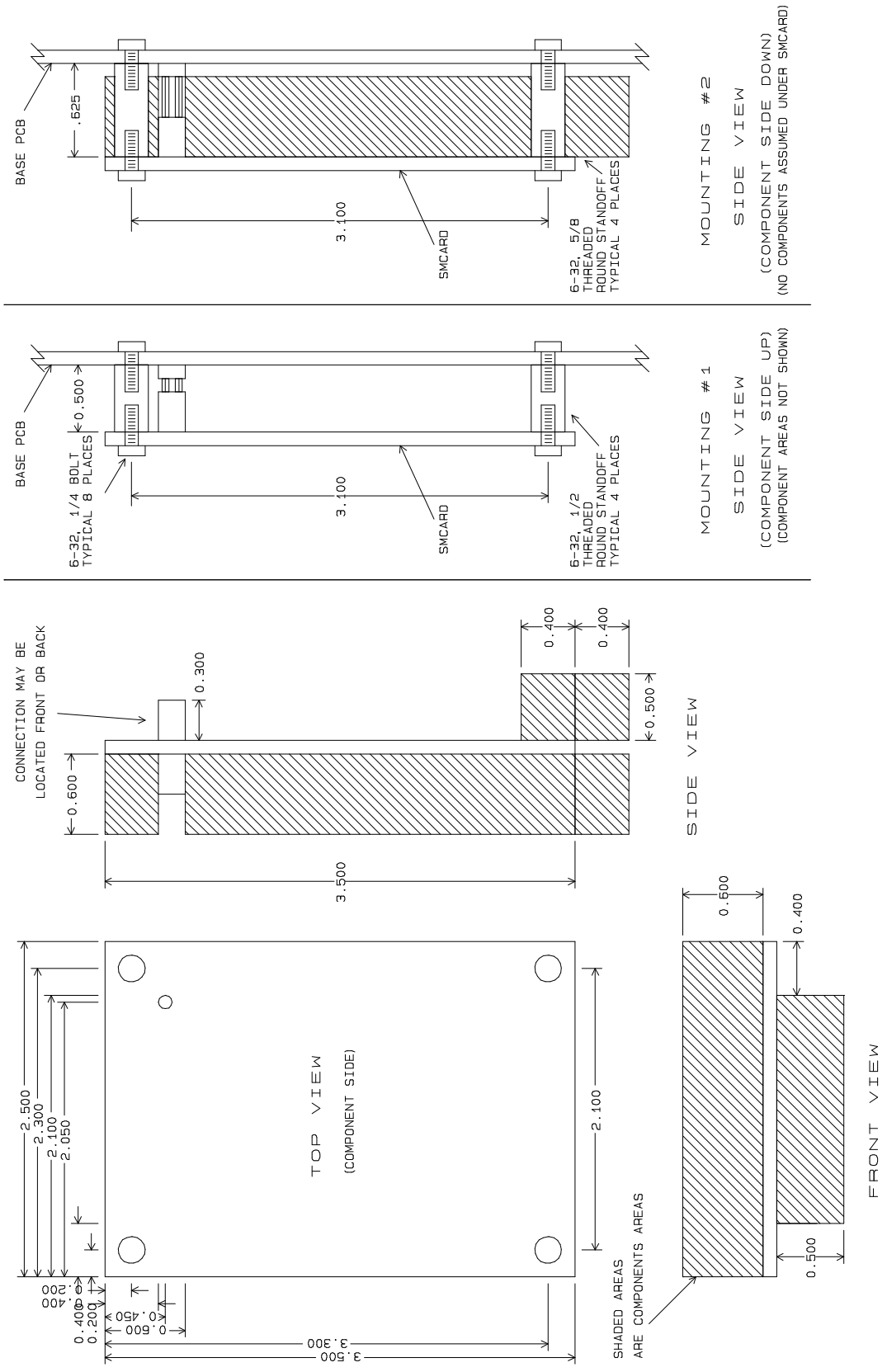
1. +12v	2. NReset
3. nc	4. nc
5. nc	6. nc
7. +5v	8. A14
9. WE-	10. A12
11. A13	12. A7
13. A8	14. A6
15. A9	16. A5
17. A11	18. A4
19. OE-	20. A3
21. A10	22. A2
23. CS-	24. A1
25. D7	26. A0
27. D6	28. D0
29. D5	30. D1
31. D4	32. D2
33. D3	34. GND

DPRAM Connector, J1

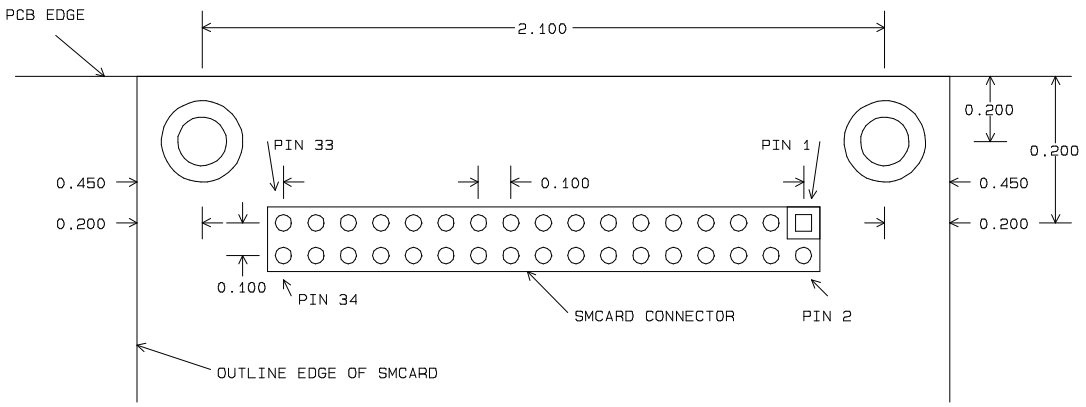
MECHANICAL

The following three drawings provide the user with all the mechanical dimensions necessary to design an SMCARD motherboard and the connector positioning and pinouts.

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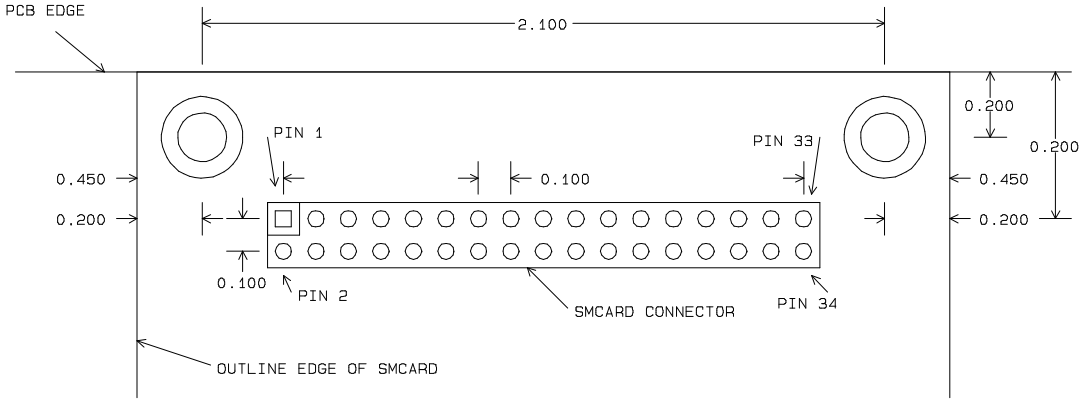


SMCARD WITH COMPONENT SIDE UP

SMCARD Pinout

1 - +V (12vdc)	2 - NRESET
3 - Vcc	4 -
5 - A15/A18	6 - A16
7 - Vcc/A17	8 - A14/A15
9 - NWE/A14	10 - A12
11 - A13	12 - A7
13 - A8	14 - A6
15 - A9	16 - A5
17 - A11	18 - A4
19 - NOE	20 - A3
21 - A10	22 - A2
23 - NCE	24 - A1
25 - D7	26 - A0
27 - D6	28 - D0
29 - D5	30 - D1
31 - D4	32 - D2
33 - D3	34 - GND

* The second address references an EPROM



SMCARD WITH COMPONENT SIDE DOWN

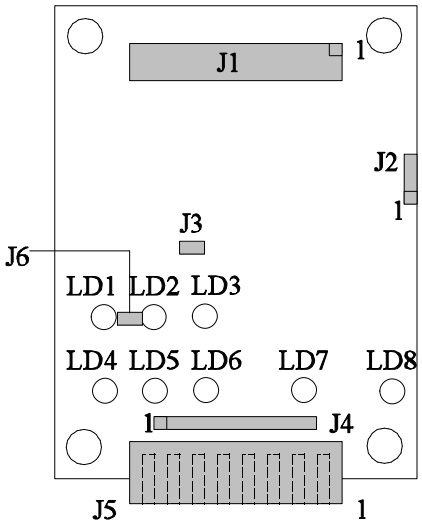
SMCARD Pinout

1 - +V (12vdc)	2 - NRESET
3 - Vcc	4 -
5 - A15/A18	6 - A16
7 - Vcc/A17	8 - A14/A15
9 - NWE/A14	10 - A12
11 - A13	12 - A7
13 - A8	14 - A6
15 - A9	16 - A5
17 - A11	18 - A4
19 - NOE	20 - A3
21 - A10	22 - A2
23 - NCE	24 - A1
25 - D7	26 - A0
27 - D6	28 - D0
29 - D5	30 - D1
31 - D4	32 - D2
33 - D3	34 - GND

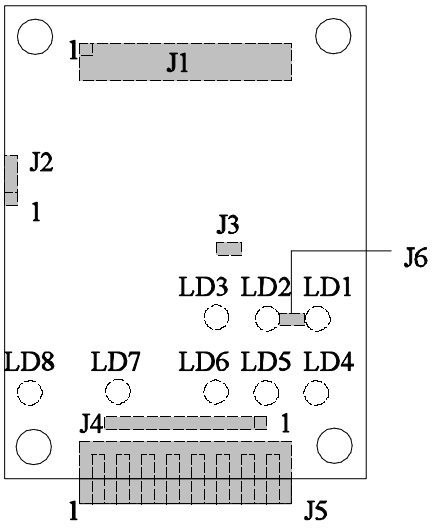
* The second address references an EPROM

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QUAD ARINC 429 SMCARD COMPONENT PLACEMENT



Top View



Bottom View

J1 - **SMCARD Connecter**

Refer to the drawing on page 11

J2, J3, J4, J6 - **N/A**

J5 - **ARINC Connector**

Channel	Pin	Signal
One	1	Receive(-)
One	2	Receive(+)
Two	3	Receive(-)
Two	4	Receive(+)
Three	5	Receive(-)
Three	6	Receive(+)
Four	7	Receive(-)
Four	8	Receive(+)

LD1 thru LD6 - **Activity Indicators**

LED	Channel	LED	Channel
1,2	One	5,6	Three
3,4	Two	7,8	Four

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MESSAGE MONITORING

The Quad ARINC 429 board has a table driven four channel scanner. Using the table approach the user can set up an area in the shared memory space that contains a list of specific ARINC 429 packets that are of interest. This list consists of individual records with specifics of the ARINC message to monitor. The contents of the received packets are then stored in the record for viewing by the host. Each record is made of a 32 bit mask, a 32 bit compare, and a 32 bit received value. A rolling 16 bit counter is also contained in the record to indicate how many of the specified packets have been received.

All multi byte information is stored in little endian format. High byte is first followed by lesser significant bytes.

The Record Information Control data is stored at offset A0 hex from the beginning of shared memory. It contains the information about each channel as well as the location of the monitor records for each channel. Channel specific monitor records can occupy separate or common physical locations in shared memory. The offsets to the location of the beginning of each channel's record storage is from beginning of shared memory.

Record Information Control

xxA0	+0	- Channal Mode #1 (0 - Disables the Scan Channel)
	+1	- Max # of Records to Scan Channel #1
	+2,3	- Offset to records of Channel #1
	+4	- Channal Mode #2 (0 - Disables the Scan Channel)
	+5	- Max # of Records to Scan Channel #2
	+6,7	- Offset to records of Channel #2
	+8	- Channal Mode #3 (0 - Disables the Scan Channel)
	+9	- Max # of Records to Scan Channel #3
	+10,11	- Offset to records of Channel #3
	+12	- Channal Mode #4 (0 - Disables the Scan Channel)
	+13	- Max # of Records to Scan Channel #4
	+14,15	- Offset to records of Channel #4

The monitor records are 16 byte entries that describe a particular data message that is received over the ARINC 429 network. This record uses a mask and compare mechanism to identify the received data messages whose contents should be stored in the live value portion of the record. A continuously updating count of the received message activity is also stored in each record.

Single ARINC 429 Monitor Record

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xxxx	+0	- Record Command 0 - Disabled 1 - Continuous Read 2 - Single Read 255 - End of record marker
	+1	- Record Status
	+2,3	- Received packet count
	+4	- Mask MSB, 0 - Ignore, 1 - Enable
	+5	- .
	+6	- .
	+7	- Mask LSB
	+8	- Compare MSB
	+9	- .
	+10	- .
	+11	- Compare LSB
	+12	- Value MSB
	+13	- .
	+14	- .
	+15	- Value LSB

Count

This 16 bit count is incremented every time the record matched the received data. The increment occurs after the data has been updated in the value register storage.

Mask

The mask is used by setting the bit desired bit to a 1 and the then the compare bit to the desired bit. If the Mask bit is set to a zero then the compare bit must be a zero for the respective bit location to be ignored in the comparison as to weather this record is considered active..

Compare

The bits in the compare registers are compared to the received value after anding with the mask values. If the remaining value is the same as the compare then the record is considered active and the live 32 bit packet is stored in the record for viewing by the host.

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MSDOS TEST SOFTWARE

The ARINC 429 test program is supplied as an example of how to interface to the SMCard as well as a useful tool for working with the product. The test program is written in easy to read BASIC. It can be complied and executed under a variety of BASIC language platforms. It is designed to operate under a DOS environment or a DOS window under win 31/95/98. Execution of the program from the command line is as follows:

ARINC429	- Standard entry with defaults
ARINC429 &HD800	- Entry with D800 hex base address
ARINC429 /P	- Cause parity to be inverted

The program loads a .SET file upon entry and saves the .SET file upon exit. Changes to the operational parameters of the program are stored in the .SET file for usage. This lets the program 'remember' settings from session to session.

Also, .RAM and .IMG files are read upon program startup to initialize the SMCards shared memory. The .IMG file is an ASCII file that can save specific values in the shared memory at specific locations. The .RAM file is a binary image file that is used to completely populate all of the shared memory. The .RAM file is loaded first followed by the .IMG file.

The ARINC test program has two primary operation modes. One is received packet based and displays all packets received in a scrolling list. This list is ordered in the time sequence that the packets are received. The other modes shows a screen full of previously entered received packet records and actively updates them as the received data matches a packet record.

Scrolling Display

The scrolling display can either display generic 429 packets or a packet display formatted for the Cara R/T altimeter information.

Packet Display

The packet display has four columns each reserved for a particular 429 receive channel. The columns show a list of the 429 packets that are to be monitored for the channel that relates to the particular column. The columns can either be the actual value received for that record or the mask data or the compare data. When in the received value mode an indicator of active packets is present.

An additional program called MEMTOOL can be used to directly access the shared memory. The user is presented with a page of 256 bytes. Selection of a single byte for change is easy using the functions provided.

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MAIN SCREEN

The following screen shot shows an actual screen capturing live ARINC 429 data. The information presented is read from the shared memory of the SMCard.

```
parvus Formatted ARINC 429 Test Facility                Version 2.00.00
Copyright 1998-1999 parvus

  R - Reset SMCard    I - Toggle Error Interrupt    S - Suspend Toggle
  Q - Exit Program    E - Zero Errors               A - Base Memory Address
  F - Formatted       M - Arinc Map                 1-4 - Channel Select

                                        Generic ARINC 429
-Count b3..... b2..... b1..... b0.....      Current Statistics
  251 00000000 00010010 00110110 10000000
  252 10000000 00010010 00110100 10000000     Rx Packets.....: 379
  253 00000000 00010010 00110101 10000000     Tx Packets.....: 0
  254 00000000 00010010 00110110 10000000     Parity Errors..: 0
  255 10000000 00010010 00110100 10000000     Overrun Errors.: 0
  256 00000000 00010010 00110101 10000000
  257 00000000 00010010 00110110 10000000     Rx Buffer b0...: 10000000
  258 10000000 00010010 00110100 10000000           b1...: 00110101
  259 00000000 00010010 00110101 10000000           b2...: 00010010
  260 00000000 00010010 00110110 10000000           b3...: 00000000
  261 10000000 00010010 00110100 10000000
  262 00000000 00010010 00110101 10000000     Interrupt Error: Off
  263 00000000 00010010 00110110 10000000     Suspend........: Disabled
  264 10000000 00010010 00110100 10000000
  265 00000000 00010010 00110101 10000000
```

The received 32 bit messages of the 429 protocol are shown. The bit numbering is from right to left, 0 to 32. Note that the first byte of the ARINC 429 protocol (B0) is in reversed bit order. This an oddity of the protocol and is preserved on the screen. Parity is on the far left of the four scrolling bytes.

Commands:

R - Reset SMCARD
A command is issued to the SMCARD to perform a warm boot. The SMCARD will reinitialize its memory and then restart its operation/

I - Toggle Interrupts
The error logging and other event logging are not active on the SMCard until interrupts are enabled. This command toggles the interrupt enable flag.

S - Screen Suspend

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Events can happen rather quickly on the screen. This command enables and disables the screen operation so that the contents of the screen can be viewed in an unchanging state.

Q - Exit to DOS

E - Zero Errors
The errors that are accumulated are returned to zero so that a fresh error count can be made.

A - Change Address
The base memory address of the SMCard can be changed so that the SMCard can be accessed from another location.

F - Toggle Format
Currently this software has two formatted displays. One is specific to the Cara R/T Radar Altimeter that is a 24 bit ARINC 429 bit stream. The other is a generic 429 32 bit display. The format is changed in the scrolling region of the screen.

M - Change to ARINC 429 Map
Another mode of operation of this software is to display the received packet status of the four channels that can be receiving data over the ARINC 429 protocol. A scrolling list of the channels and their associated records is available for viewing and change.

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ALTERNATE MAIN SCREEN

The following is an alternate display of the main screen. This is specifically for usage with radar altimeters. A special 24 bit reduced format can be received and displayed. The screen and command keys work exactly the same as with the main screen only the scrolling portion has been changed.

```
parvus Formatted ARINC 429 Test Facility                    Version 2.00.00
Copyright 1998-1999 parvus

  R - Reset SMCard    I - Toggle Error Interrupt    S - Suspend Toggle
  Q - Exit Program    E - Zero Errors               A - Base Memory Address
  F - Formatted       M - Arinc Map

                                                    Radar Altimeter
| Count   r0     r1 r2  Error  Altitude             Current Statistics
  1238 00000000 00 00     Par    0.0
  1240 00000000 00 00     Par    0.0               Rx Packets.....: 1373
  1243 00000000 00 00     Par    0.0               Tx Packets.....: 0
  1245 00000000 00 00     Par    0.0               Parity Errors..: 0
  1247 00000000 00 00     Par    0.0               Overrun Errors.: 0
  1249 00000000 00 00     Par    0.0
  1252 00000000 00 00     Par    0.0               Rx Buffer b0...: 10000000
  1254 00000000 00 00     Par    0.0                       b1...: 00110100
  1256 00000000 00 00     Par    0.0                       b2...: 00010010
  1258 00000000 00 00     Par    0.0                       b3...: 10000000
  1260 00000000 00 00     Par    0.0
  1262 00000000 00 00     Par    0.0               Interrupt Error: Off
  1264 00000000 00 00     Par    0.0               Suspend........: Enabled
  1267 00000000 00 00     Par    0.0
  1269 00000000 00 00     Par    0.0
```

The scrolling window contains several elements that are calculated or time sensitive. Each new entry into the scrolling window pushes the previous contents up by one line. The data shown in the window are as follows from left to right:

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Altitude Mode

Received Packet Count	This is the actual count recorded by the SMcard. It can be used to determine missed codes in a sequence.
Processed Packet 0-2	These are the processed registers that are bit manipulated from the actual Rx buffer.
Error Flags	If errors are present when the packet is read they are presented here.
Altitude	This is calculated from the processed packets and presented in .5 foot increments.

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ARINC 429 RECORD SCREEN

This screen shows a scrollable list of records that are used to capture specifically defined data messages that are received over the ARINC 429 connection. Each of the four channels available are placed in one of four columns. One channel is shown in this screen shot. The user can scroll through the records as well as the channels, a particular record can be selected, and the contents of that record changed.

```
parvus Formatted ARINC 429 Test Facility                    Version 2.00.00
Copyright 1998-1999 parvus

   Q - Return to Main  T - Cycle Record Type   M - Mask Adjust
   S - Save Image      R - Restore Image       C - Compare Adjust
 Move - Select Cell                          V - Value Adjust
\                                                 Offset:    0
 ----Channel #0-8--
Scan   /00 12 35 80
Off    /00 00 00 00
Off    /00 00 00 00
Off    /00 00 00 00
Off    /00 00 00 00
Off    /00 00 00 00
Off    /00 00 00 00
Off    /00 00 00 00
```

The four byte of a standard 429 packet are shown with bit 1 on the right and bit 32 on the left. This is the also the order that the packet is received. The '/' is a rotating indicator of received activity on this channel and this particular record.

Commands:

Q - Exit To DOS

T - Cycle Record Type
Each record entry has a record type that can be cycled from no-operation to single scan to continuous scan. The command causes the type to cycle. The command cycling only occurs when viewing the value portion of records.

M - View Mask
Change so that the scrollable display shows the mask values of each record

C - View Compare
Change so that the scrollable display shows the compare values of each record

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V - View Values
Change so that the scrollable display shows the stored live values of each record

S - Save Image
The image of the SMCard is saved in memory in a simple byte ordered binary file

R - Restore Image
The image of the SMCard is read from memory and restored to the SMCard.

Up - Move Selection Bar
The arrow keys move the selection bar from column to column and up and down within a column

Ent - Select Record
A record is selected for access and change. Pressing enter will then enter the update mode of the record access. Depending on which values are displayed will depend on what values are allowed to be changed. Pressing enter again will accept the changes. Left and right move between bytes of the record. Typing the hex numbers, 0-9, A-F will change the contents of the entry field. ESC will abort entry without change.

FILE FORMATS

ARINC429.RAM File

This file is stored in a raw binary format. It is the exact size of the shared memory used by the SMCard. The file can also be used by other programs for initializing the SMCard memory to that desired for program operation.

ARINC429.IMG

This file is an ASCII file that specifically initialize locations in memory and can be created by a simple text editor. It is a line by line format with an address and count preceding a list of byte data. Each line must begin with an address and byte count.

Address, Count, data+0,,,,Data+n

Hex values must be preceded by '&H' to be properly recognized

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STANDALONE TEST SYSTEM

The following information is provided as most SMCARD products are shipped with either an adapter or a Generic DPRAM Gateway. These are the sockets that the SMCards plug into thus giving the SMCARD access to a dual port ram device.

Generic DPRAM Gateway - Protocol Diagnostic Application

The Generic DPRAM Gateway provides two upright SMCARD sockets for placement of parvus SMCARD products. Each SMCARD socket has access to one side of the 16k dual port ram located on the generic DPRAM Gateway product. The SMCARD products are each expected to contain a CPU to access the DPRAM port as the Generic DPRAM Gateway contains only power management and a memory component.

The Generic DPRAM Gateway has onboard power regulation and can receive power through a screw clamp connection on the side of the product for permanent applications or through a barrel connector for quicker usage such as field diagnostics. Jumpers exist on the Generic DPRAM Gateway that selectively apply power to the SMCARD sockets. Both +5 and +V are presented to the SMCARD sockets. In most cases these jumpers are installed and are shipped from the factory as installed. The externally applied power is usually +12 vdc.

The primary usage of this product is as a Gateway. A gateway provides the function of converting information from one protocol to another and also the function of converting one communications media to another. It can perform easy conversion from one protocol to another through the usage of shared memory. A section of the memory map from one SMCARD is made available in a section of the other SMCards memory map. Since the Generic DPRAM Gateway contains no CPU or other processing capability the data formatting is controlled by the CPU on each respective SMCARD.

The attached SMCards each contain a local CPU and the necessary drive circuitry to directly connect to the respective communications media that the card has been designed. parvus continually creates new SMCARD products and protocols. The following is a short list of those SMCARD products:

68HC11 Seriplex SMCARD (Slave)
68HC11 DeviceNet Can SMCARD (Master/Slave)
6805 DeviceNet Can SMCARD (Slave)
68HC11 Asynchronous Serial SMCARD
68HC11 Synchronous Serial SMCARD
8051 Asynchronous Serial SMCARD

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68HC11 Display/Keypad Access SMCARD
68HC11 Bel 202 Modem
68HC11 Async Modem

One common usage of the Generic DPRAM Gateway is as a diagnostic device. By placement of a Display/Keypad Access SMCARD on one side of the Generic DPRAM Gateway and a selected network protocol conversion SMCARD on the other the completed assembly can be used to access critical parameters associated with the selected network protocol.

The Access SMCARD provides a simple method of accessing any memory location in the shared memory area for viewing and modification. The data can be displayed as hex values or as displayable ASCII characters. The address can be directly entered as a four digit hex address and once entered it can be scrolled forward and backward. The scrolling keys have a repeat feature for rapid movement through memory. Each newly accessed memory location is immediately display so that memory can be reviewed rapidly. An option exists to access either the shared memory area or the local memory of the SMCARD. The memory addresses start at 0000 and progress to a maximum address of 3FFF or 16k. The 0000 address is at the beginning of the DPRAM component on the Generic DPRAM Gateway. When a value is changed, it takes place as soon as the ENT key is pressed and then the addressed memory location is displayed. If the change to memory was effective the value entered will remain. If the write to memory did not succeed then the new, other value will be immediately displayed. The change of memory occurs in real time and does not effect the CPU of the other SMCARD in any way other that through the memory value change.

By entering an address on the display and accessing the desired memory location the contents of that memory location is continuously display. If the contents of the selected memory location changes, that change is easily detected as the newly changed value is displayed. The display is updated about 20 times per second.

The address entered on the Access SMCARD is actually an offset from the beginning of memory that is shared between the SMCards. The offset entered on the display is not necessarily the actual address of the memory on the SMCARD but only the memory offset for the shared memory. Caution should be exercised when using the Access SMCARD as it can access both the attached shared memory of the other SMCARD or the local memory of the Access SMCARD. The memory accessed is shown on the display by the separator between the address and the data fields. The ':' indicates shared memory while the '=' indicates local memory of the Access SMCARD. Usage will most commonly be with the ':' displayed.

The data presented on the display is selected by address only. It is not formatted other than by address because of the general nature of the device. The documentation for each SMCARD will identify the organization of the data on the SMCARD. By cross referencing the address or offset entered on the Access

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SMCARD it is possible to access all locations of the shared memory and read the desired data associated with that SMCARD.

The uses of the Generic DPRAM gateway with an Access SMCARD and a selected protocol SMCARD include mainly development and diagnostic applications. Since SMCards are available with or without a protocol installed, it is up to the developer to create the protocol conversion software resident in the SMCards that are shipped without protocols. During the development this combination of product can greatly enhance the effort by providing direct access to the shared memory area of the protocol under development. As a diagnostic device it is as excellent tool for viewing the selected protocol in operation. All areas of the shared memory can be accessed for viewing or change therefore allowing unhampered access to the protocol as it is functioning without any degradation in performance. Since this is such a general method of access it works well with any protocol and therefore is a useful as a general purpose network/protocol diagnostic tool.

Caution should be exercised when changing values in shared memory as there may or may not be error checking on the parameter that is changed. It is best to consult the SMCARD documentation for the proper ranges and address to access and change when working with the shared memory of that SMCARD. Since this is direct memory of the other SMCARD, that memory may have been initialized by that SMCARD upon fire up. Change to a value may or may not have effect on the function of the other SMCARD depending on its application.

Detailed information for usage of the Access SMCARD can be found in the Access SMCARD (Display/Keypad SMCARD) operation manual. The Access SMCARD manual may be appended to this document or included with the shipment of the product.

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ACCESS SMCARD OPERATION

The Access SMCARD Display / Keypad module allows direct access to the dual port memory of the SMCARD system. Addresses can be directly entered or sequentially scrolled and the data can be viewed and the changed if desired. The card will eventually have access to not only the dual port memory section of the SMCARD family, but local memory and the parvNET map as well.

The module was created to allow direct access of the shared memory technology employed by parvus for protocol translation. The module can be used to read SMCARD systems as well as SocNet systems. It has a full parvNET port as well as drivers for the display/keypad.

Memory Maps

The memory map information is provided to allow the user access to various section of the SMCARD's internal and shared memory operation.

Dual Port Ram Access

8000-FFFF	32k System EPROM
4000-7FFF	16k Dual Port RAM
3F00-3FFF	Optional I/O
1200-3EFF	Unused
1000-11FF	512 bytes internal RAM
0000-0FFF	Local CPU I/O

Local CPU Memory Access

8000-FFFF	32k System EPROM
1200-7FFF	32k System RAM (minus shadowed portions)
1000-11FF	512 bytes internal RAM
0000-0FFF	Local CPU I/O

Local memory can be accessed between 0000h and FFFFh with no internal offset used. DPRAM memory can be accessed between 0000h and 3FFFh with an internal offset of 4000h added to any entry.

Mode Operation

The SMCARD Display/Keypad operates through the usage of several modes. The mode execution order is controlled by user key entry. The ENT and ESC keys allow movement through the modes. The ENT key accepts and entry in

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a mode and moves to the next logical mode. The ESC key aborts a current and returns to the previous mode.

Press ENT to move down (1, 2, 3) through modes

1. Direct Address Entry Mode

2a. Data Display Mode, Hex

2b. Data Display Mode, ASCII

3. Direct Data Entry Mode

Press ESC to move up (3, 2, 1) through modes

Pressing the ENTER key repeatedly in the Data Display mode while '=__' or ':__' is displayed, the device will cycle between HEX and ASCII display. Whenever the device transitions between the Direct Entry Mode and a Data Display Mode the display method is returned to HEX.

The device can access two distinct memory spaces. By pressing the ESC key when in the Address Entry mode with the '@____' displayed. The separator will change between a '=' and a ':'. The '=' symbol indicates access to local memory of the onboard CPU while the ':' indicates access to the JEDEC standard Dual Port RAM socket.

Actual operation

The following actual operation demonstrates how the device is used. Editing is handled through additional entry or through an ESC or abort key. Once the initial display has been changed it cannot be redisplayed until the memory access operation has been restarted (resetting the SMCARD)

Initial Display

The initial display is achieved when the unit is powered on or when the menu selection accessing memory modification is chosen.

@ _ _ _ _ = No address or data entered

Enter Address 4370 Hex

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All entry is in hex. The address is entered right to left starting with the lowest significant digit. Previous entered digits are shifted left. All digits must be entered including leading zeros for a valid address.

Press 4	@ _ _ _ 4 =	1st digit entered
Press 3	@ _ _ 4 3 =	2nd digit entered
Press 7	@ _ 4 3 7 =	3rd digit entered
Press 0	@ 4 3 7 0 =	4th digit entered

Continue entry until desired address is shown to correct error.

Read Data at Address 4370 Hex

Once the displayed address is correct, the ENT key is pressed to change from address entry mode to data access mode. Use the Up/Down arrows to move through the address range. UP increments the address while DOWN decrements the address. The data is automatically displayed in this mode. ESC will exit data display mode and begin Address entry mode, starting with the previously displayed address.

Press ENT	@ 4 3 7 0 = 2 3	Data at address 4370h
Press UP	@ 4 3 7 1 = 8 4	Data at address 4371h
Press DOWN	@ 4 3 7 0 = 2 3	Data at address 4370h
Press DOWN	@ 4 3 6 F = 9 1	Data at address 436Fh

Enter Data at Address 436F Hex

After the displayed address is correct and the data of that address is displayed, the ENT key can be used to change that data. Enter the data right to left as with the address until the new desired data value is displayed and press ENT again to accept. ESC will abort the entry and back up to data display mode.

Press ENT	@ 6 3 6 F = _ _	Waiting for data entry
Press 6	@ 6 3 6 F = _ 6	1st digit entered

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Press 5	@ 6 3 6 F = 6 5	2nd digit entered
Oops, really wanted 82 not 65		
Press 8	@ 6 3 6 F = 5 8	3rd digit entered
Press 2	@ 6 3 6 F = 8 2	4th digit entered
Press ENT	@ 6 3 6 F = 8 2	Data entered into memory

The data entry mode is now exited and returned to data display mode. If the value that was requested to be stored into memory was NOT then the actual value is displayed. this is a verification that the actual memory storage was correctly performed.

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METHODS for ACCESSING

This following text provides information on accessing a DPRAM memory space. It describes three different methods. The first method involves the use of interrupts. The second method involves the process of forcing a write and then reading the data back to make sure the correct data was written. The third method involves the use of an arbitration byte to determine which side of the DPRAM has sole control of the memory area.

Using Interrupts

The IDT 71321 DPRAM offers interrupt control for interprocessor communications. The interrupt flag permits communication between the DPRAM ports. If the interrupt function is being used, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag is set when the right port writes to the memory location 7FEh. The left port interrupt flag is cleared when the left port reads location 7FEh. The right port interrupt flag is set when the left port writes to memory location 7FFh. The right port interrupt flag is cleared when the right port reads memory location 7FFh. If the interrupt function is not utilized, either port may randomly access memory locations 7FEh and 7FFh.

It is up to the user to define parameters written into the interrupt "mail boxes". Any data may be written to these locations, but it is suggested that a map/register scheme be used. For example, the upper nybble of the interrupt byte may contain the map location (a 256 byte page or 16, 16 byte registers) and the lower nybble may contain a register location (a 16 byte block in a register). When the interrupt control byte is read by the opposite port, the processor would then know which map and register had a value that changed.

Byte location 126h has been changed by the right port. An interrupt will be sent to the left port indicating that a byte has changed.

Example (Motorola 68HC11 Assembly)

```
Right Port:
        LDAA #$55           ;
        STAA $4126          ; write a 55h into 4126h (DPRAM starts at 4000h)
        LDAA #$12           ; map 1, register 2
        STAA $47FE                  ; DPRAM starts at 4000h, set interrupt flag

Left Port:                  (interrupt has occurred)
        LDAA $47FE                  ; clear interrupt (DPRAM starts at 4000h)
        STAA BYTCHG         ; store for later use
```


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Using Blind Writes with Read Backs

This method of writing to DPRAM involves directly writing a data byte to DPRAM and them immediately reading that byte back. If the byte read back matches the byte written, then the write is considered a success. If the byte read back doesn't match, then the write is tried again and a counter is incremented. If the counter reaches a maximum limit, then an error is generated and the program moves to the next data byte to write or the program continues on to the next routine.

Example (Motorola 68HC11 Assembly)

```
?L1   LDAA #$55              ; data = 55h
          STAA TEMPA             ; save value
          STAA $4000             ; write to location 4000h - start of DPRAM
          LDAB $4000             ; read location 4000h - start of DPRAM
          CMPB TEMPA             ; compare data
          BEQ ?LE                ; branch if equal
          LDAA LPCOUNT           ; get loop counter
          INCA                   ; increment loop counter
          STAA LPCOUNT           ;
          CMPA LPMAX             ; has loop limit been reached?
          BNE ?L1                ; try again
          BSET ERRFLAG           ; set error flag
?LE   RTS                    ; return
```

Using an Arbitration Control byte

Using an arbitration control byte is probably the safest and most desirable method of passing data through a DPRAM. This method designates a byte in memory as a control byte. In our example, we will use the last byte in the DPRAM space. We will assign an ID number of 1 to the right side of the DPRAM and 2 to the left. The ID number will determine who has control of the DPRAM. This ID number will be written into the control byte. We will assign the value of 0 to the control byte when neither side has control.

When the initial access to the DPRAM occurs, a loop counter is initialized and the control byte is read. This byte can equal one of four things:

Case
0 - neither side has control
1 - right side has control
2 - left side has control
3 - FF - byte is un-initialized

Case 0

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Neither side of the DPRAM has control and the processor should now attempt to write its control ID into the control byte (1 for right and 2 for left). A loop counter should be incremented at this time.

Case 1

The right side of the DPRAM has control and the left side must wait. A loop counter should be incremented at this time.

Case 2

The left side of the DPRAM has control and the right side must wait. A loop counter should be incremented at this time.

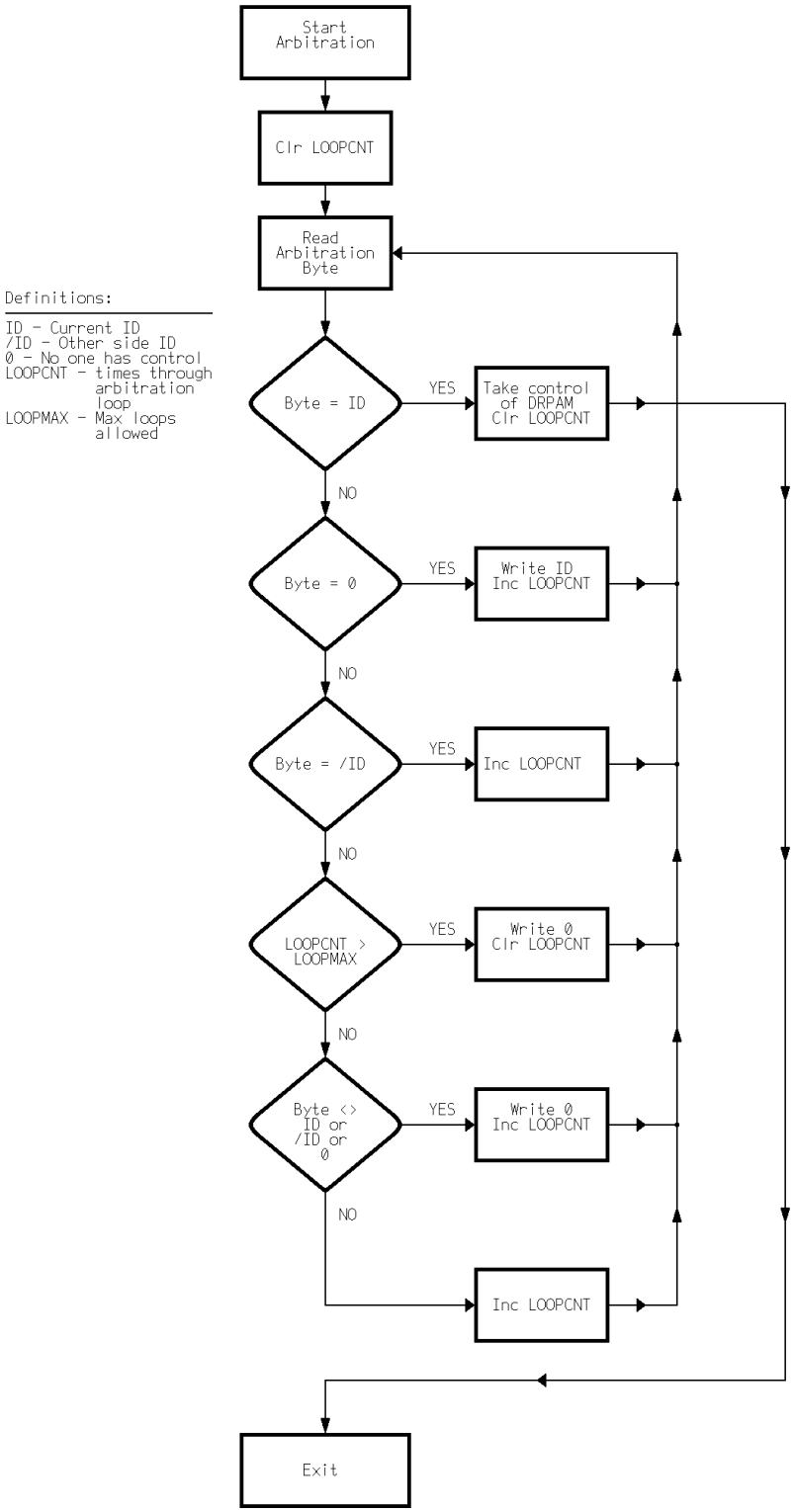
Case 3 - FF

These values can be user defined or they can indicate that the DPRAM is un-initialized in which case both sides of the DPRAM should write a 0 to initialize the location. A loop counter should be incremented at this time.

If the loop counter value reaches some maximum limit, a 0 should be written into the DPRAM control byte by the side that detects the maximum count. This is to prevent the deadly embrace situation. Reaching a maximum loop count could indicate that the processor on the other side of the DPRAM has faulted.

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Arbitration Flow Chart



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Quick BASIC Example Code for using an Arbitration Control Byte
This code is for the right side of the DPRAM

```
'*******************************************************************************************
'* SUBROUTINE DPRAMControl - Gain control of DPRAM area
'*  Definitions:
'*   DPMAPOFF - Memory offset of DRPAM
'*   DPMapSeg - Memory segment of DPRAM
'*   Map - 256 byte page of DPRAM (Map=0 - first 256 bytes)
'*   Reg - 16 byte blocks (Reg=0 - first 16 bytes of a Map)
'*   Offset - Number of bytes offset into a register (Reg)
'*   Typ - Data action
'*   ControlByte - Actual arbitration byte value
'*   LoopCount - Counter for number of wait cycles
'*   LoopMax - Maximum number of wait cycles
'*   ControlFlag - Indicator of DPRAM acquisition status
'*******************************************************************************************

SUB DPRAMControl (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, ControlByte%)
        LoopCount=0
        LoopMax=100
        ControlFlag=0
        DO WHILE ControlFlag=0
                CALL DPRAMByteRead (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%,
ControlByte%)
                IF (ControlByte% = 0) THEN
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%,
1)
                        LoopCount=LoopCount+1
                        ControlFlag=0
                ELSEIF (ControlByte% = 1) THEN
                        ControlFlag=1
                        LoopCount=0
                        EXIT DO
                ELSEIF (ControlByte% = 2) THEN
                        ControlFlag=0
                        LoopCount=LoopCount+1
                ELSEIF (LoopCount > LoopMax) THEN
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%,
0)
                        LoopCount=0
                        ControlFlag=0
                ELSE
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%,
0)
                        LoopCount=LoopCount+1
                        ControlFlag=0
                        END IF
        LOOP
END SUB

'*******************************************************************************************
'* SUBROUTINE DPRAMByteRead - Read a byte from DPRAM area
'*  Definitions:
'*   DPMAPOFF - Memory offset of DRPAM
'*   DPMapSeg - Memory segment of DPRAM
'*   Map - 256 byte page of DPRAM (Map=0 - first 256 bytes)
'*   Reg - 16 byte blocks (Reg=0 - first 16 bytes of a Map)
```


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```
'*   Offset - Number of bytes offset into a register (Reg)
'*   Typ - Data action
'*   Value - Data holder
'*****************************************************************************************

SUB DPRAMByteRead (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, Value%)
        DEF SEG = DPMapSeg
        Value% = PEEK(DPMAPOFF + (Map * 256) + (Reg% * 16) + Offset%)
        DEF SEG
END SUB


'*****************************************************************************************
'* SUBROUTINE DPRAMByteWrite - Write a data byte to DPRAM area
'*  Definitions:
'*   DPMAPOFF - Memory offset of DRPAM
'*   DPMapSeg - Memory segment of DPRAM
'*   Map - 256 byte page of DPRAM (Map=0 - first 256 bytes)
'*   Reg - 16 byte blocks (Reg=0 - first 16 bytes of a Map)
'*   Offset - Number of bytes offset into a register (Reg)
'*   Typ - Data action
'*   Value - Data holder
'*****************************************************************************************

SUB DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, Value%)
        DEF SEG = DPMapSeg
        POKE DPMAPOFF + (Map * 256) + (Reg% * 16) + Offset%, Value%
        DEF SEG
END SUB
```


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ADDITIONAL SMCARD PRODUCT INFORMATION

SMCARD PRODUCT

These cards are 2.5 inches by 3.5 inches and plug onto JEDEC compatible 34 pin connectors, called SMCARDS. They have a local CPU, some communication hardware and some form of network medium driver. They are intended to interface directly to a specific type of communications medium. The SMCARD performs the task of data conversion from the specific network or communications appliance to a general shared memory structure. Most cards have a 68HC11 CPU with 32k each of RAM and EPROM. An 8k EEPROM is used for changeable parameter storage.

Seriplex SMCARD

The Seriplex slave has the ability to emulate all possible Seriplex addresses or none of them depending on configuration. Both peer-to-peer and master/slave modes are supported. As a Seriplex Slave the product can operate as a true slave or as a master monitor with full master capability available in the future. Data rates from 10-200Khz are supported.

Bell 202 Modem SMCARD

A Bell 202 1200 baud modem is fully implemented on board. The modem is driven by a software serial port from the local CPU. The CPU accesses a JEDEC standard pinouts shared memory port and has 8k of onboard EEPROM. With screw clamp connections, this device can be used with a telephone line or as a standalone short haul modem.

Display/keypad SMCARD

Using its 1x8 display and 20 position keypad this SMCARD can read and write to any location in shared memory space. It is an excellent diagnostic tool for shared memory development. It also has a serial port with a DB9 connector for asynchronous communications. The local CPU accesses a JEDEC standard pinouts shared memory port and has 8k of onboard EEPROM.

Asynchronous Serial SMCARD

The external DB9 male connection can be driven by a hardware or software serial port. The software serial driver is interrupt driven and can be used for multi bit (1 to 255 bits) operations. The local CPU accesses a JEDEC standard pinouts shared memory port and has 8k of onboard EEPROM.

Synchronous Serial SMCARD

An NEC 72001 synchronous serial communications components is driven using standard bit and byte synchronous protocols. The external connection is a female DB25 connector. The local CPU accesses a JEDEC standard pinouts shared memory port and has 8k of onboard EEPROM.

Echelon SMCARD

Placing shared memory in the Echelon memory space provides a simple method to interface an Echelon system to other systems. The 315 Neuron uses a simple twisted pair interface as a physical layer. The local 3150 accesses a JEDEC standard pinouts shared memory port.

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parvCAN SMCARD

The conversion of Control Area Network signals and protocol to the shared memory area. Address selection and operation switches are provided to select the CAN addresses and function. A simple CAN interface is provided for twisted pair operation. The output of this device is through the shared memory area.

Async Modem SMCARD

A complete Hayes compatible modem. The local cpu drive the modem from its UART. Two RJ11 connectors are provided to connect to the telephone lines and to pass through to the next telephone device down the line. The modem is implemented with a purchased complete modem component for ease of use and FCC registration. The local CPU accesses a JEDEC standard pinouts shared memory port and has 8k of onboard EEPROM.

SMCARD ADAPTERS

The conversion from a SMCARD and its JEDEC compatible connection to another type of interface is handled by adapters. Adapters may or may not contain a hardware DPRAM component. The adapters have a location for several shared memory products and, usually, at least one location for an SMCARD.

External PC/104 CPU Bus Interface

PC-104 DPRAM / SMCARD Interface

This dual port RAM interface has user selectable address locations and comes in 1k, 2k, and 4k sizes. It attaches directly to the PC/104 8-bit bus. A mounting area for a 2.5 inch x 3.5 SMCARD exists with a 34 pin header that matches the JEDEC EPROM pinouts standard. A 28 pin ribbon cable can extend from that connector to allow the board to plug into a JEDEC RAM or EPROM. User configurable jumpers allow the user to select RAM or EPROM emulation and size. This board is an ideal way to interface between two dissimilar computing systems or network media. When used with an interface board plugged into the JEDEC header, this board may require a double height adapter.

ISA Bus DPRAM / SMCard Interface

This dual port RAM interface has user selectable address locations and comes in 1k, 2k, and 4k sizes. It attaches directly to the ISA 8-bit bus. A mounting area for a 2.5 inch x 3.5 SMCARD exists with a 34 pin header that matches the JEDEC EPROM pinouts standard. A 28 pin ribbon cable can extend from that connector to allow the board to plug into a JEDEC RAM or EPROM. User configurable jumpers allow the user to select RAM or EPROM emulation and size. This board is an ideal way to interface between two dissimilar computing systems or network media. When used with an interface board plugged into the JEDEC header, this board may require a double height adapter.

Dual SMCARD Platform

Connects 2 SMcards to a local dual port RAM and provides local regulated power. This product is ideal as a gateway conversion between two different protocols.

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For more information about the Gateway and other products in the parvus line of development tools or controls systems call (801) 483-1533 from 8:00AM to 5:00PM Mountain Time.

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INSTRUCTIONS TO USER

This equipment generates and uses radio frequency energy and if not installed and used properly, i.e., in strict accordance with the operating instructions, reference manuals, and the service manual, may cause interference to radio or TV reception. It has been designed to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of FCC rules, which are designed to provide reasonable protection against such interference when operated in a residential installation.

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