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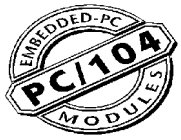
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THE parvus CORPORATION

USER MANUAL

PC/104 MULTI-FUNCTION DUAL PORT RAM





4/14/97

MNL-0395D-01

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INTRODUCTION

The parvus PC/104 Multi-Function Dual Port RAM card allows the user to partition out a section of RAM to be shared between two devices. This shared memory partition contains two ports, one for the PC/104 CPU and the other for either a secondary PC/104 stack or a **SMCard** product. The DPRAM windows come in a 2K x 8 configuration.

When used with two CPU stacks, the dual port RAM allows the two CPU's to communicate information back and forth to each other. The secondary CPU can act as an independent co-processor sharing the same stack and a block of common RAM. When used with a **SMCard** product, the dual port RAM allows the CPU to communicate information back and forth to remote devices via a common medium.

The package contains the following:

PRV-0425A-02	-	PC/104 Multi-Function Dual Port RAM card
DOC-0350A-01	-	User Manual
SFT-0225A-01	-	MEMTEST.EXE Program
SFT-0226A-01	-	MEMTOOL.EXE Program
DOC-0351A-01	-	Memory Test Utilities User Manual

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INSTALLATION

Before installation into a PC/104 system, the card memory addresses need to be set. The following two tables, **Table 1** and **Table 2**, are used to set the address selection for the primary PC/104 bus, **(J1/J2)**. **Table 1** switch settings allow for the major memory blocks to be selected while **Table 2** switch settings allow for the selection of smaller blocks within the major block. **Table 3** and **Table 4** are used to set the address selection for the secondary PC/104 bus, **(J4/J5)**. If one of the **parvus SMCard** products is to be used, switches for **SW2** must be set accordingly.

PRIMARY PC/104 BLOCK ADDRESS SELECTION

ADDRESS BLOCK	SW1-1	SW1-2	SW1-7	SW1-8
0XXXX	ON	ON	ON	ON
1XXXX	ON	OFF	ON	ON
2XXXX	OFF	ON	ON	ON
3XXXX	OFF	OFF	ON	ON
4XXXX	ON	ON	OFF	ON
5XXXX	ON	OFF	OFF	ON
6XXXX	OFF	ON	OFF	ON
7XXXX	OFF	OFF	OFF	ON
8XXXX	ON	ON	ON	OFF
9XXXX	ON	OFF	ON	OFF
AXXXX	OFF	ON	ON	OFF
BXXXX	OFF	OFF	ON	OFF
CXXXX	ON	ON	OFF	OFF
DXXXX	ON	OFF	OFF	OFF
EXXXX	OFF	ON	OFF	OFF
FXXXX	OFF	OFF	OFF	OFF

Table 1

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PRIMARY PC/104 WINDOW ADDRESS SELECTION

ADDRESS WINDOW	SW1-3	SW1-4	SW1-5	SW1-6
X0000-X0FFF	ON	ON	ON	ON
X1000-X1FFF	ON	ON	ON	OFF
X2000-X2FFF	ON	ON	OFF	ON
X3000-X3FFF	ON	ON	OFF	OFF
X4000-X4FFF	ON	OFF	ON	ON
X5000-X5FFF	ON	OFF	ON	OFF
X6000-X6FFF	ON	OFF	OFF	ON
X7000-X7FFF	ON	OFF	OFF	OFF
X8000-X8FFF	OFF	ON	ON	ON
X9000-X9FFF	OFF	ON	ON	OFF
XA000-XAFFF	OFF	ON	OFF	ON
XB000-XBFFF	OFF	ON	OFF	OFF
XC000-XCFFF	OFF	OFF	ON	ON
XD000-XDFFF	OFF	OFF	ON	OFF
XE000-XEFFF	OFF	OFF	OFF	ON
XF000-XFFFF	OFF	OFF	OFF	OFF

Table 2

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SECONDARY PC/104 BLOCK ADDRESS SELECTION

ADDRESS BLOCK	SW2-5	SW2-6	SW2-7	SW2-8
0XXXX	ON	ON	ON	ON
1XXXX	ON	ON	ON	OFF
2XXXX	ON	ON	OFF	ON
3XXXX	ON	ON	OFF	OFF
4XXXX	ON	OFF	ON	ON
5XXXX	ON	OFF	ON	OFF
6XXXX	ON	OFF	OFF	ON
7XXXX	ON	OFF	OFF	OFF
8XXXX	OFF	ON	ON	ON
9XXXX	OFF	ON	ON	OFF
AXXXX	OFF	ON	OFF	ON
BXXXX	OFF	ON	OFF	OFF
CXXXX	OFF	OFF	ON	ON
DXXXX	OFF	OFF	ON	OFF
EXXXX	OFF	OFF	OFF	ON
FXXXX	OFF	OFF	OFF	OFF

Table 3

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SECONDARY PC/104 WINDOW ADDRESS SELECTION

ADDRESS WINDOW	SW2-1	SW2-2	SW2-3	SW2-4
X0000-X0FFF	ON	ON	ON	ON
X1000-X1FFF	OFF	ON	ON	ON
X2000-X2FFF	ON	OFF	ON	ON
X3000-X3FFF	OFF	OFF	ON	ON
X4000-X4FFF	ON	ON	OFF	ON
X5000-X5FFF	OFF	ON	OFF	ON
X6000-X6FFF	ON	OFF	OFF	ON
X7000-X7FFF	OFF	OFF	OFF	ON
X8000-X8FFF	ON	ON	ON	OFF
X9000-X9FFF	OFF	ON	ON	OFF
XA000-XAFFF	ON	OFF	ON	OFF
XB000-XBFFF	OFF	OFF	ON	OFF
XC000-XCFFF	ON	ON	OFF	OFF
XD000-XDFFF	OFF	ON	OFF	OFF
XE000-XEFFF	ON	OFF	OFF	OFF
XF000-XFFFF	OFF	OFF	OFF	OFF

Table 4

Install the IRQ selection jumpers if interrupts are going to be used (refer to tables 5 and 6).

If power is going to be supplied from the primary PC/104 bus to the secondary PC/104 bus, install the jumpers on J6-J9.

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OPERATION

This following text provides information on accessing a DPRAM memory space. It describes three different methods. The first method involves the use of interrupts. The second method involves the process of forcing a write and then reading the data back to make sure the correct data was written. The third method involves the use of an arbitration byte to determine which side of the DPRAM has sole control of the memory area.

Using Interrupts: The IDT 71321 DPRAM offers interrupt control for inter-processor communications. The interrupt flag permits communication between the DPRAM ports. If the interrupt function is being used, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag is set when the right port writes to the memory location 7FEh. The left port interrupt flag is cleared when the left port reads location 7FEh. The right port interrupt flag is set when the left port writes to memory location 7FFh. The right port interrupt flag is cleared when the right port reads memory location 7FFh. If the interrupt function is not utilized, either port may randomly access memory locations 7FEh and 7FFh.

It is up to the user to define parameters written into the interrupt "mail boxes". Any data may be written to these locations, but it is suggested that a map/register scheme be used. For example, the upper nibble of the interrupt byte may contain the map location (a 256 byte page or 16, 16 byte registers) and the lower nibble may contain a register location (a 16 byte block in a register). When the interrupt control byte is read by the opposite port, the processor would then know which map and register had a value that changed. The primary and secondary PC/104 busses may interrupt or be interrupted. The SMCard bus, however, may only interrupt the primary PC/104 bus.

Byte location 126h has been changed by the right port. An interrupt will be sent to the left port indicating that a byte has changed.

Example (Motorola 68HC11 Assembly)

```
Right Port:
        LDAA #$55          ;
        STAA $4126         ; write a 55h into 4126h (DPRAM starts at 4000h)
        LDAA #$12          ; map 1, register 2
        STAA $47FE         ; DPRAM starts at 4000h, set interrupt flag
Left Port:
        (interrupt has occurred)
        LDAA $47FE         ; clear interrupt (DPRAM starts at 4000h)
        STAA BYTCHG        ; store for later use
```


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Using Blind Writes with Read Backs: This method of writing to DPRAM involves directly writing a data byte to DPRAM and them immediately reading that byte back. If the byte read back matches the byte written, then the write is considered a success. If the byte read back doesn't match, then the write is tried again and a counter is incremented. If the counter reaches a maximum limit, then an error is generated and the program moves to the next data byte to write or the program continues on to the next routine.

Example (Motorola 68HC11 Assembly)

```
?L1  LDAA #$55          ; data = 55h
     STAA TEMPA         ; save value
     STAA $4000         ; write to location 4000h - start of DPRAM
     LDAB $4000         ; read location 4000h - start of DPRAM
     CMPB TEMPA         ; compare data
     BEQ ?LE            ; branch if equal
     LDAA LPCOUNT       ; get loop counter
     INCA               ; increment loop counter
     STAA LPCOUNT       ;
     CMPA LPMAX         ; has loop limit been reached?
     BNE ?L1            ; try again
     BSET ERRFLAG       ; set error flag
?LE  RTS                ; return
```

Using an Arbitration Control byte: Using an arbitration control byte is probably the safest and most desirable method of passing data through a DPRAM. This method designates a byte in memory as a control byte. In our example, we will use the last byte in the DPRAM space. We will assign an ID number of 1 to the right side of the DPRAM and 2 to the left. The ID number will determine who has control of the DPRAM. This ID number will be written into the control byte. We will assign the value of 0 to the control byte when neither side has control.

When the initial access to the DPRAM occurs, a loop counter is initialized and the control byte is read. This byte can equal one of four things:

Case
0 - neither side has control
1 - right side has control
2 - left side has control
3 - FF - byte is un-initialized

Case 0: Neither side of the DPRAM has control and the processor should now attempt to write its control ID into the control byte (1 for right and 2 for left). A loop counter should be incremented at this time.

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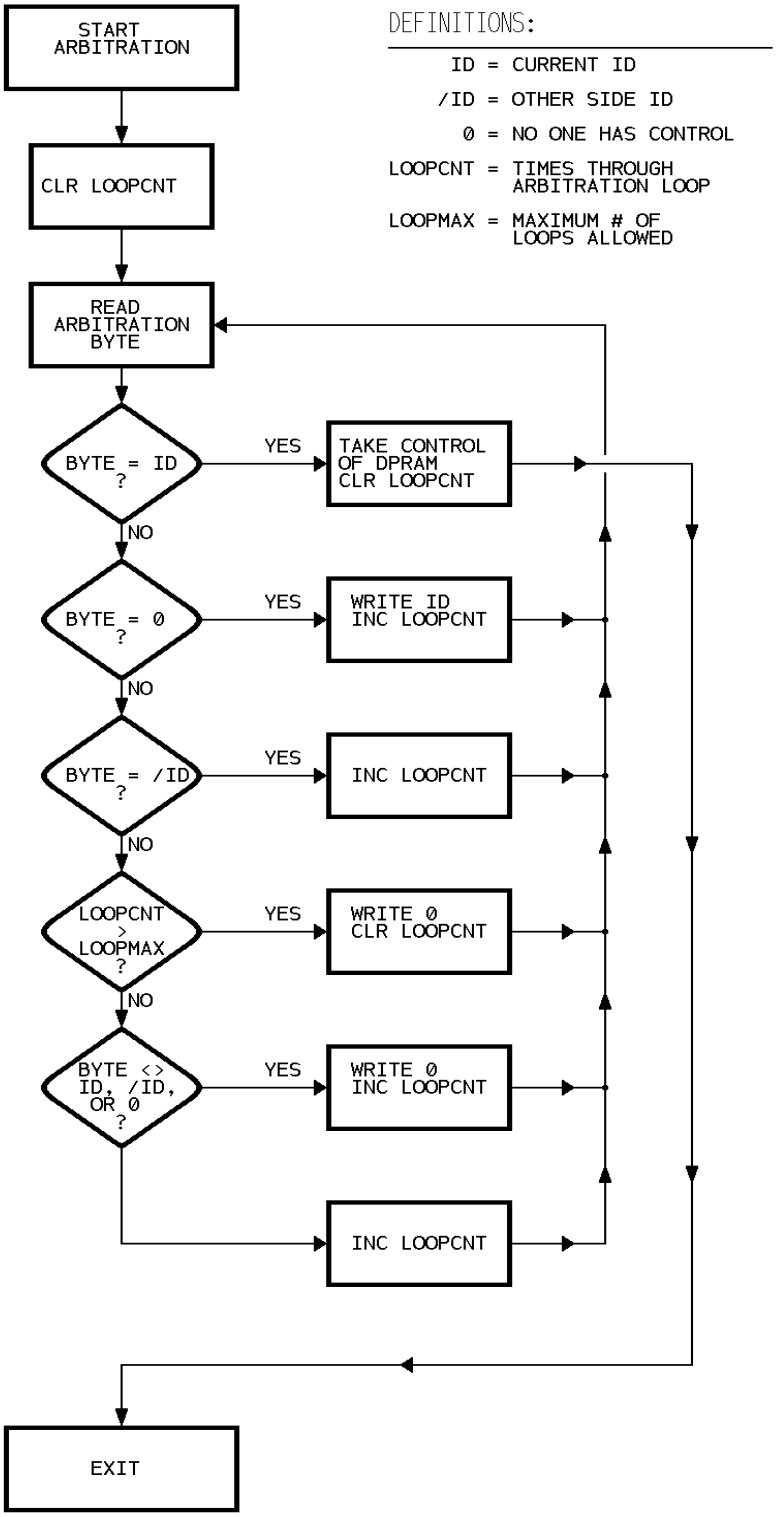
Case 1: The right side of the DPRAM has control and the left side must wait. A loop counter should be incremented at this time.

Case 2: The left side of the DPRAM has control and the right side must wait. A loop counter should be incremented at this time.

Case 3:- FF this value can be user defined or can indicate that the DPRAM is un-initialized in which case both sides of the DPRAM should write a 0 to initialize the location. A loop counter should be incremented at this time. If the loop counter value reaches some maximum limit, a 0 should be written into the DPRAM control byte by the side that detects the maximum count. This is to prevent the deadly embrace situation. Reaching a maximum loop count could indicate that the processor on the other side of the DPRAM has faulted.

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Arbitration Flow Chart



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Quick BASIC Example Code for using an Arbitration Control Byte
This code is for the right side of the DPRAM

```
'*****************************************************************************************
'* SUBROUTINE DPRAMControl - Gain control of DPRAM area
'*  Definitions:
'*   DPMAPOFF - Memory offset of DRPAM
'*   DPMapSeg - Memory segment of DPRAM
'*   Map - 256 byte page of DPRAM (Map = 0 - first 256 bytes)
'*   Reg - 16 byte blocks (Reg = 0 - first 16 bytes of a Map)
'*   Offset - Number of bytes offset into a register (Reg)
'*   Typ - Data action
'*   ControlByte - Actual arbitration byte value
'*   LoopCount - Counter for number of wait cycles
'*   LoopMax - Maximum number of wait cycles
'*   ControlFlag - Indicator of DPRAM acquisition status
'*****************************************************************************************
SUB DPRAMControl (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, ControlByte%)
        LoopCount = 0
        LoopMax = 100
        ControlFlag = 0
        DO WHILE ControlFlag = 0
                CALL DPRAMByteRead (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, ControlByte%)
                IF (ControlByte% = 0) THEN
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, 1)
                        LoopCount = LoopCount + 1
                        ControlFlag = 0
                ELSEIF (ControlByte% = 1) THEN
                        ControlFlag = 1
                        LoopCount = 0
                        EXIT DO
                ELSEIF (ControlByte% = 2) THEN
                        ControlFlag = 0
                        LoopCount = LoopCount + 1
                ELSEIF (LoopCount > LoopMax) THEN
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, 0)
                        LoopCount = 0
                        ControlFlag = 0
                ELSE
                        CALL DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, 0)
                        LoopCount = LoopCount + 1
                        ControlFlag = 0
                        END IF
        LOOP
END SUB

'*****************************************************************************************
'* SUBROUTINE DPRAMByteRead - Read a byte from DPRAM area
'*  Definitions:
'*   DPMAPOFF - Memory offset of DRPAM
'*   DPMapSeg - Memory segment of DPRAM
'*   Map - 256 byte page of DPRAM (Map = 0 - first 256 bytes)
'*   Reg - 16 byte blocks (Reg = 0 - first 16 bytes of a Map)
'*   Offset - Number of bytes offset into a register (Reg)
'*   Typ - Data action
'*   Value - Data holder
'*****************************************************************************************
SUB DPRAMByteRead (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, Value%)
        DEF SEG = DPMapSeg
        Value% = PEEK(DPMAPOFF + (Map * 256) + (Reg% * 16) + Offset%)
        DEF SEG
END SUB

'*****************************************************************************************
'* SUBROUTINE DPRAMByteWrite - Write a data byte to DPRAM area
'*  Definitions:
```


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```
'*    DPMAPOFF - Memory offset of DRPAM
'*    DPMapSeg - Memory segment of DPRAM
'*    Map - 256 byte page of DPRAM (Map = 0 - first 256 bytes)
'*    Reg - 16 byte blocks (Reg = 0 - first 16 bytes of a Map)
'*    Offset - Number of bytes offset into a register (Reg)
'*    Typ - Data action
'*    Value - Data holder
'*****************************************************************************************
SUB DPRAMByteWrite (DPMAPOFF, DPMapSeg, Map%, Reg%, Offset%, Typ%, Value%)
          DEF SEG  =  DPMapSeg
          POKE DPMAPOFF + (Map * 256) + (Reg% * 16) + Offset%, Value%
          DEF SEG
END SUB
```


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CONNECTION

J1/J2 and J4/J5

Pin	Row A	Row B	Row C	Row D
0 -	--	--	GND	GND
1 -	/IOck	GND	/SBHE	/MCS16
2 -	SD7	Rstdrv	LA23	/IOCS16
3 -	SD6	+5v	LA22	IRQ10
4 -	SD5	IRQ9	LA21	IRQ11
5 -	SD4	-5v	LA20	IRQ12
6 -	SD3	DRQ2	LA19	IRQ15
7 -	SD2	-12v	LA18	IRQ14
8 -	SD1	/Exfer	LA17	/DA0
9 -	SD0	+12v	/MR	DRQ0
10 -	IOrdy	(key)	/MW	/DA5
11 -	AEN	/SMW	SD8	DRQ5
12 -	SA19	/SMR	SD9	/DA6
13 -	SA18	/IOW	SD10	DRQ6
14 -	SA17	/IOR	SD11	/DA7
15 -	SA16	/DA3	SD12	DRQ7
16 -	SA15	DRQ3	SD13	+5v
17 -	SA14	/DA1	SD14	/MSTR
18 -	SA13	DRQ1	SD15	GND
19 -	SA12	/Rfrsh	(key)	GND
20 -	SA11	SCLK	--	--
21 -	SA10	IRQ7	--	--
22 -	SA9	IRQ6	--	--
23 -	SA8	IRQ5	--	--
24 -	SA7	IRQ4	--	--
25 -	SA6	IRQ3	--	--
26 -	SA5	/DA2	--	--
27 -	SA4	TC	--	--
28 -	SA3	BALE	--	--
29 -	SA2	+5v	--	--
30 -	SA1	OSC	--	--
31 -	SA0	GND	--	--
32 -	GND	GND	--	--

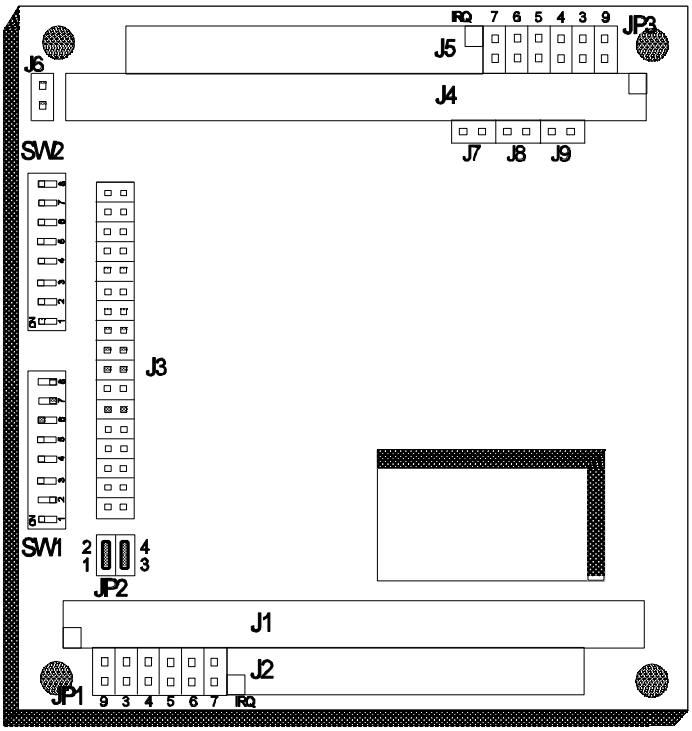


Figure 1

The PC/104 bus always uses Row A and B, while Row C and D are for 16 bit systems. B10 and C19 are keyed locations.

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Connections: (refer to Figure 1)

J1 - PC/104 primary 8 bit bus
J2 - PC/104 primary 16 bit bus
J3 - SMCard interface
J4 - PC/104 secondary 8 bit bus
J5 - PC/104 secondary 16 bit bus
J6 - Secondary bus +5V pass through
J7 - Secondary bus +12V pass through
J8 - Secondary bus -12V pass through
J9 - Secondary bus -5V pass through

SW1 - Primary bus address selection
JP2 - Power selection for J3 (+5VDC and +12VDC)
SW2 - Secondary bus address selection
JP1 - Primary bus IRQ selection
JP3 - Secondary bus IRQ selection

The primary PC/104 connectors, J1 and J2, are the normal stackthrough connectors. When used with one of the **parvus SMCard** products installed on the Multi-Function DPRAM, PC/104 cards can be attached to either side of the board.

The secondary PC/104 connectors, J4 and J5, are the non-stackthrough connectors. When a secondary PC/104 stack is attached to these connectors, primary PC/104 cards can only be attached to the male pin side of J1/J2.

The SMCard Interface, J3, is used for installation of any one of several **parvus SMCard** products. In order to maintain the PC/104 intercard spacing, the **SMCards** are installed upside down on the Multi-Function DPRAM card. Refer to the **SMCard** User Manual for installation instructions.

J3 - SMCard Interface

Pin	Definition	Pin	Definition
33 -	D3	34 -	GND
31 -	D4	32 -	D2
29 -	D5	30 -	D1
27 -	D6	28 -	D0
25 -	D7	26 -	A0
23 -	-CE	24 -	A1
21 -	A10	22 -	A2
19 -	-OE	20 -	A3
17 -	A11	18 -	A4
15 -	A9	16 -	A5
13 -	A8	14 -	A6
11 -	A13	12 -	A7
9 -	-WE	10 -	A12
7 -	VCC *	8 -	N/C
5 -	N/C	6 -	N/C
3 -	N/C	4 -	N/C
1 -	+12V *	2 - N/C	

* User selectable from JP2 (see page 10)

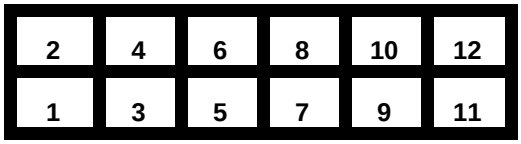
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JP1 is used to select the IRQ that will be used by the primary PC/104 bus. If IRQ is not required by the application program, the shunt plug may be placed on any two pins of the inner row of JP1 for storage purposes. Refer to **Figure 1** and **Table 5** for proper placement of the IRQ selection shunt plug.

Primary Bus IRQ Selection (JP1)

IRQ	9	3	4	5	7	6
Pins	1-2	3-4	5-6	7-8	9-10	11-12

Table 5



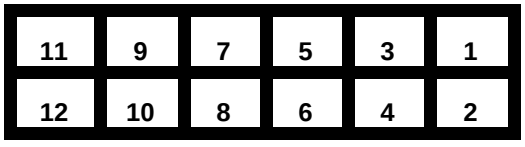
JP1 Pin Orientation

JP3 is used to select the IRQ that will be used by the secondary PC/104 bus. If IRQ is not required by the application program, the shunt plug may be placed on any two pins of the inner row of JP3 for storage purposes. Refer to **Figure 1** and **Table 6** for proper placement of the IRQ selection shunt plug.

Secondary Bus IRQ Selection (JP3)

IRQ	9	3	4	5	7	6
Pins	1-2	3-4	5-6	7-8	9-10	11-12

Table 6



JP3 Pin Orientation

JP2 is used to apply +5VDC and +12VDC (if available on the primary PC/104 bus) to the **SMCard** interface connector, (J3). The default setting is with the shunt plugs installed. Removing the shunt plug from pins 3-4 disconnects J3 from the +12VDC coming from J1. Removing the shunt plug from pins 1-2 disconnects J3 from the +5VDC coming from J1.

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NOTES:

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