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Product Manual

MPV924

Digital I/O Board

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MPV 924

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MPV924 OPERATING MANUAL

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1 - INTRODUCTION

1.1 ABOUT THIS MANUAL

The **MPV924** Digital I/O Board is a member of a family of analog and digital I/O boards from Burr-Brown which share a common memory architecture and provide a number of system orientated attributes :

- Separate system configuration and functional address maps.
- Software relocatable functional address map.
- Software selectable address modifier response.
- Programmable interrupt levels.
- Board identification registers.
- Supervisory/non- privileged access modes

This manual includes a full description of these common attributes, and instructions on how to configure, install and operate the boards. Application suggestions and example programs are provided to illustrate the use of an **MPV924** Board in a standard VMEbus system.

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2 - GENERAL DESCRIPTION

2.1 INTRODUCTION

Chapter 2 provides a brief description of the **MPV924 Digital I/O Board**. It also includes a summary of the key features of the product and a full technical specification.

2.2 KEY FEATURES

- 96 digital inputs / outputs
- Channels can be software configured in groups of eight as either an inputs or outputs
- 16 channels with software programmable "change of state" response
- 7 levels of VMEbus interrupt, selectable through software.
- Software relocation of functional memory map.
- Software reset register
- Compatible with PCI-20058T-1 and PCI-20025T-2 termination panels available from Burr-Brown
- Architecturally compatible with MPV908A/B Analog I/O Boards from Burr-Brown

2.3 DESCRIPTION OF MPV924

The **MPV924** is supplied as single 6U card and is electrically and mechanically compatible with the VMEbus specification IEEE STD 1014-1987.

The board provides 96 TTL-compatible digital channels which may be programmed in groups of eight under control of the DATA DIRECTION REGISTER to act as either inputs or outputs.

An added feature of the board is a custom-programmable chip which can monitor 16 I/O lines and under software control of two 16-bit interrupt registers, become the source of VMEbus interrupts.

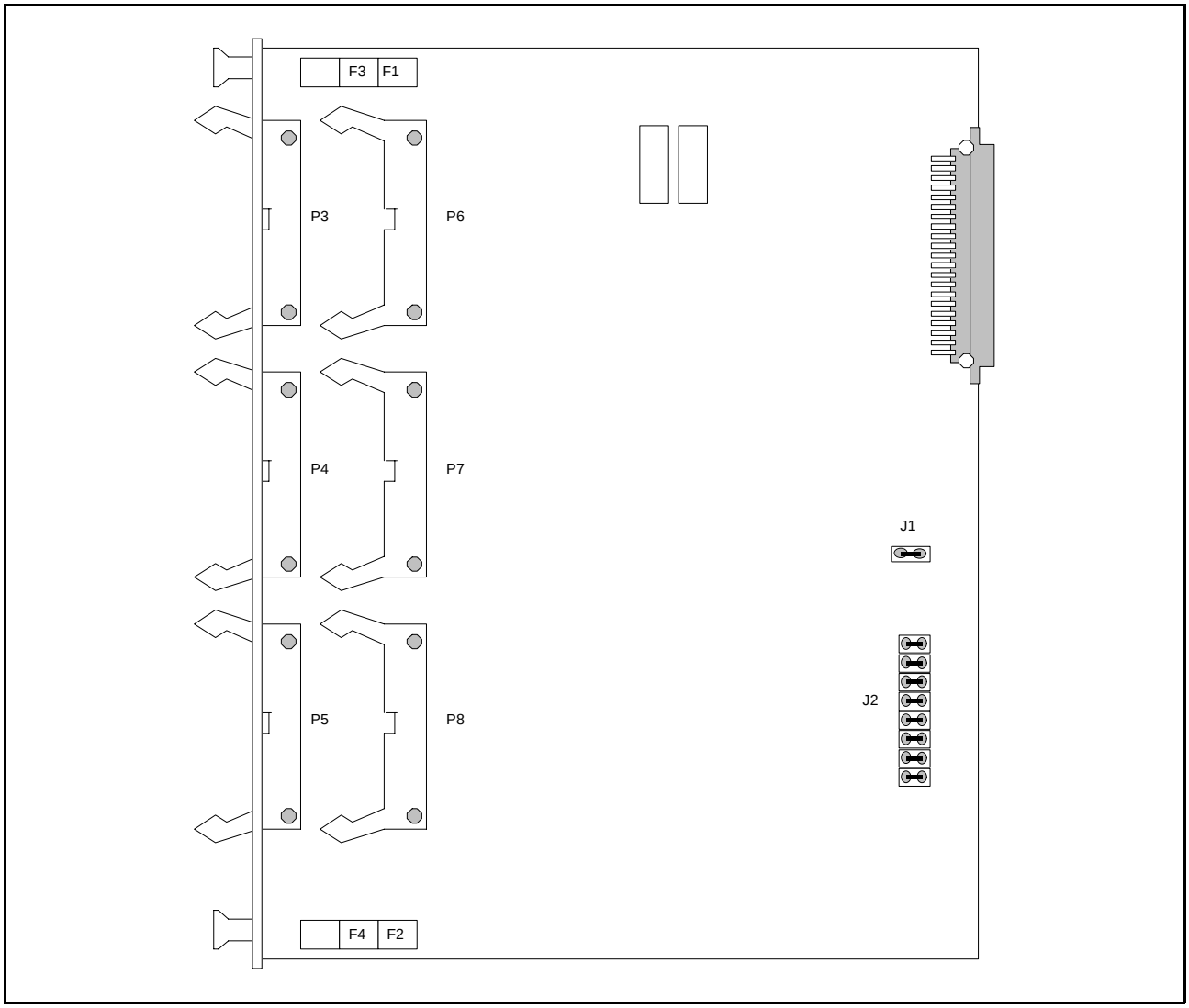
Upon power-up, after a SYSRESET or after a SOFTRESET - (generated through the system memory map), all software programmable registers are reset to 00(H) and all digital I/O channels are configured as inputs.

Each digital I/O channel is accessed via one of the six 34-way latching IDC connectors. The pinouts of these connectors are fully compatible with the PCI-20058T-1 and PCI-20025T-2 termination panels available from Burr-Brown. These termination panels provide a convenient method of connecting from the field to the bus by means of screw terminals.

Figure 2.1 shows the relative positions of connectors on the MPV924.

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Figure 2.1 - MPV924 Board Layout



The memory map as shown in Figure 2.2, is split into a jumper configurable 'System Configuration Map' and a software relocatable 'Functional Memory Map'.

2.3.1 System Configuration Map

The System Configuration Map is located in an area of memory in VMEbus short address space and is jumper selectable to any 128 word block within this space.

The 128 registers contained in the system configuration map support features which are normally required by the system configuration software during initialisation.

These features include -

- Board identification.
- Functional memory map base address selection.
- Functional memory map address modifier response selection.
- Interrupt response selection.
- Software reset.

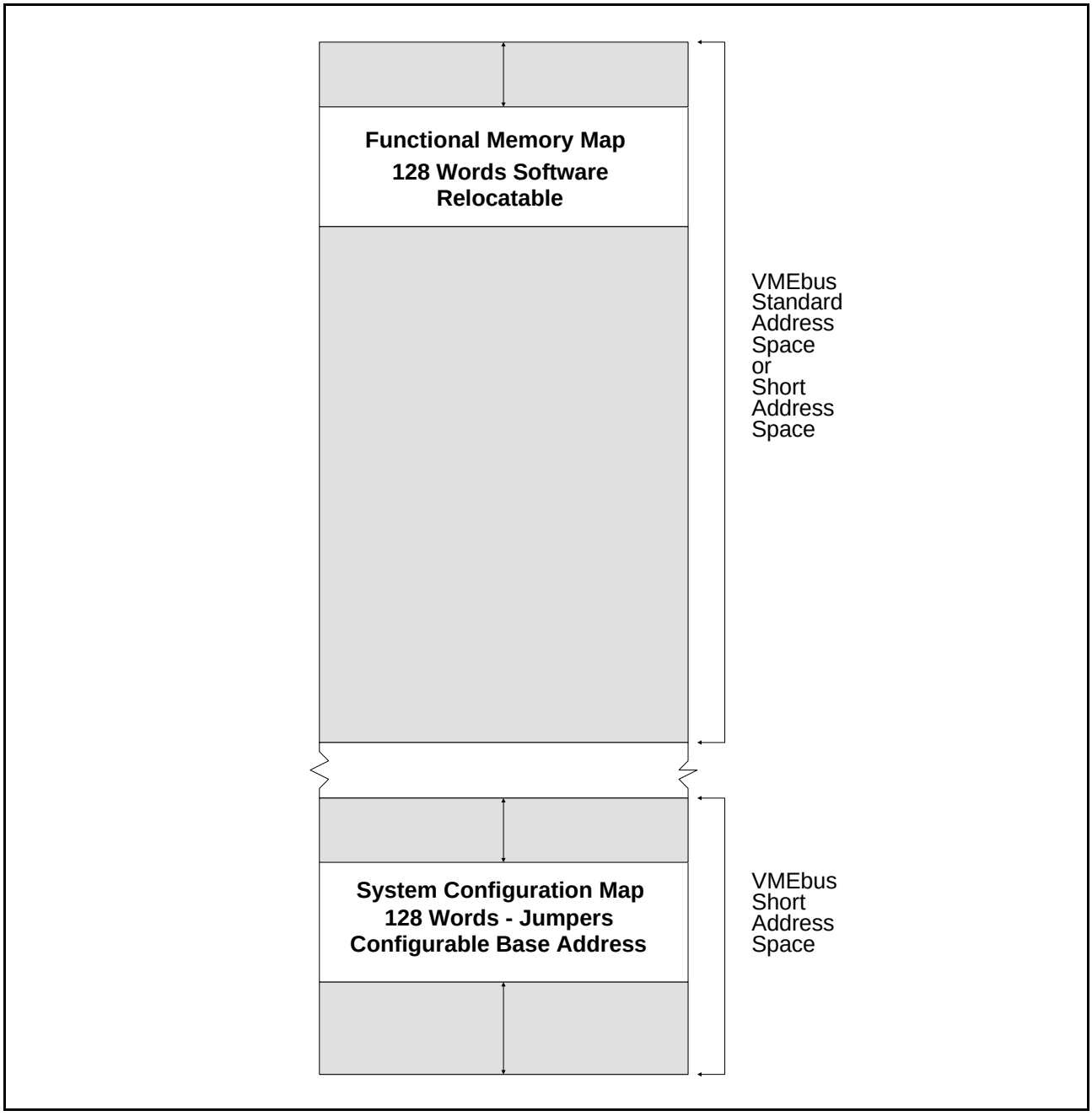
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Access to this area of memory may be restricted to supervisory access only by means of a hardware jumper.

2.3.2 Functional Memory Map

All other control and status registers which define the functionality of the board are contained in the **functional memory map.**

Figure 2.2 - MPV924 Memory Map



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2.4 SPECIFICATION

2.4.1 Digital I/O

Number of Channels	96 Digital

2.4.2 Digital Inputs

Low level input voltage	0.8V DC max
High level input voltage	2.0V DC min
Hysteresis (COS inputs only)	0.2V DC min
Low level input current	-0.62 mA DC max
High level input current	60 µA DC max

Note: Input device used is a 74LS374. Refer to Fig. 6.5 for configuration.

2.4.3 Digital Outputs

Low level output voltage (IOL=24mA)	0.5V DC max
High level output voltage	2.4V DC min
Low level output current	24mA max.
High level output current	-2.6mA max

Note: Output device used is 74LS374. Refer to Fig. 6.5 for configuration.

2.4.4 +5V Output (P3-8)

450mA DC typical (Fused)

2.4.5 VME Interface

Board Type	Slave
Addressing Modes	Standard A24 Short A16
Data Transfers	Word D16 Byte D08 (Odd or Even)
DSA low to DTACK low	700nS
DSA high to DTACK high	400nS
Signal Drive Current	As defined by ANSI/IEEE 1014-1987
Signal Loads	As defined by ANSI/IEEE 1014-1987

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2.4.6 Power Requirements

+5V@ 5.25V @ 2A maximum plus +5V output supply current

PSU Rise Time from 2.0V to Vcc min	10mS Max

2.4.7 Environmental

Operating Temperature	0℃ to 60℃
Storage Temperature	-25℃ to 85℃
Relative Humidity	5 to 90% non-condensing

2.5 ACCESSORIES

The following accessories are compatible with the MPV924 Digital I/O Board:

PCI-20058T-1 High Density I/O Panel

PCI-20025T-2 Digital I/O Customiser Panel

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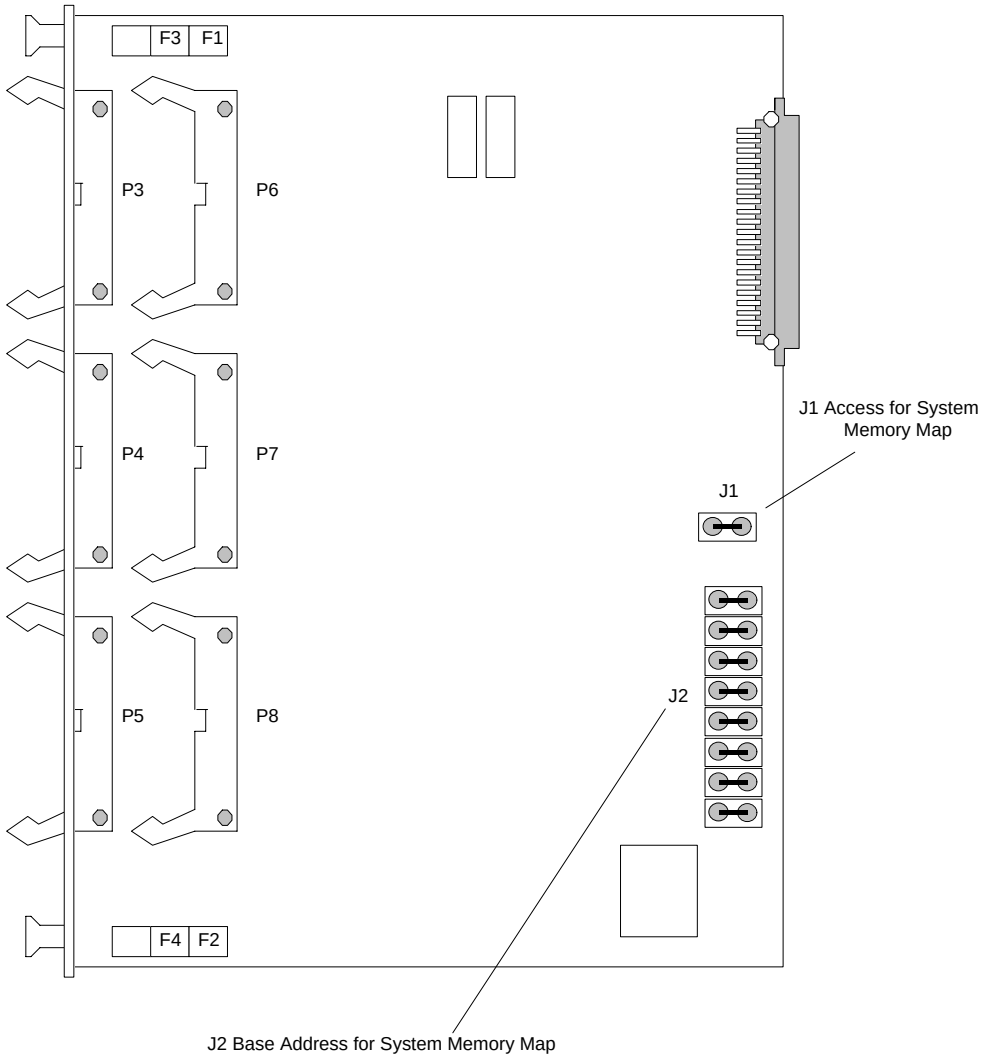
3 - HARDWARE CONFIGURATION

3.1 INTRODUCTION

The **MPV924** has a number of user-definable options which are selected using a series of jumpers. Boards are shipped from the factory configured with the default options detailed in Figure 3.1. Users who do not wish to alter the default settings should proceed to Chapter 4 - "Cables and Connections".

Figure 3.1 - Default Jumper Settings

J1	System Memory Map Access	Short Supervisory Access only
J2	Base Address for System Memory Map	VME Short I/O Base Address + 0000H



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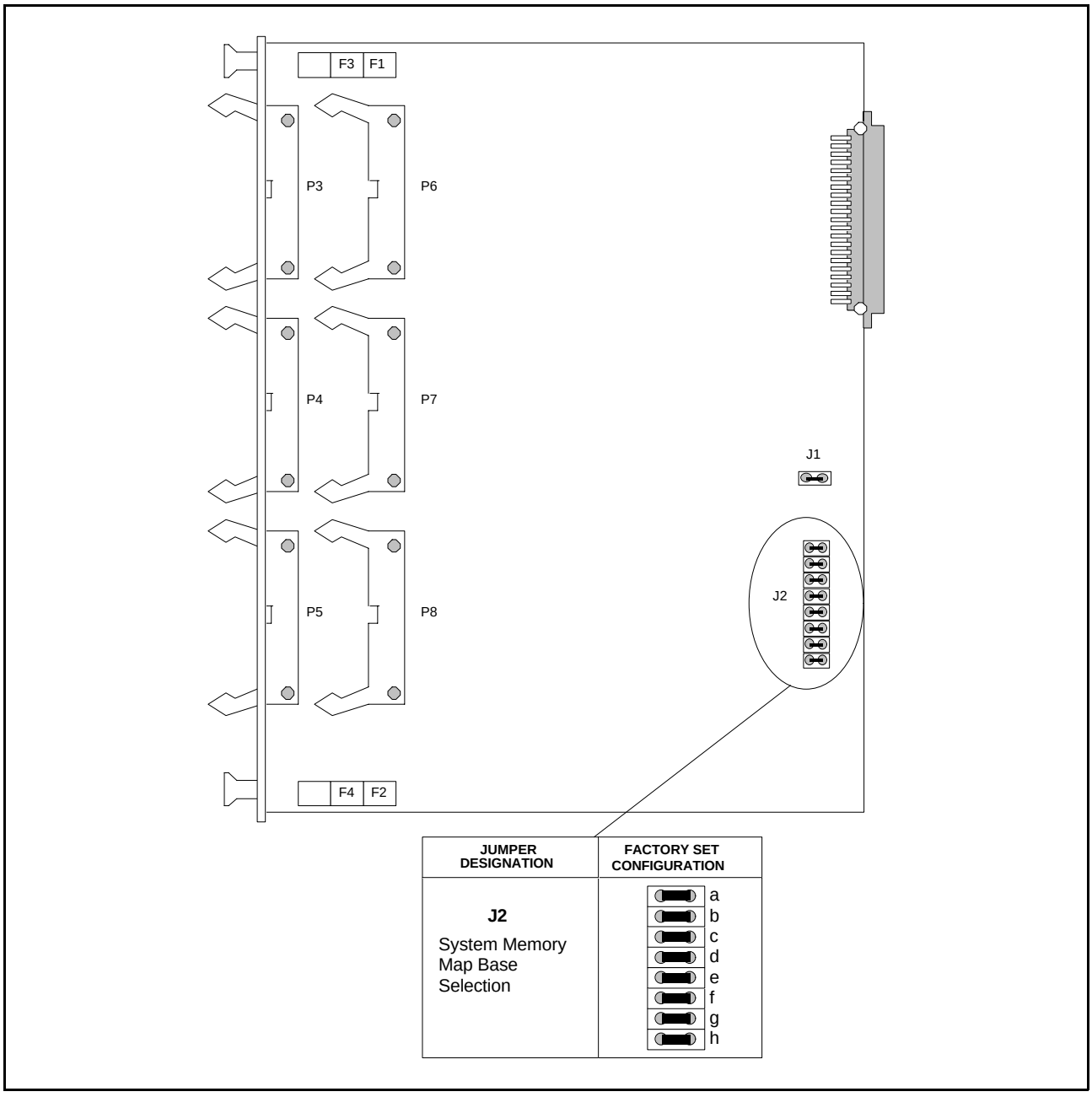
3.2 PREPARING THE BOARD

While every precaution has been taken during design to eliminate the effects of static electricity, we recommend that normal anti-static precautions should be observed when unpacking or handling the board.

3.3 CHANGING THE BASE ADDRESS (J2)

The system configuration memory map of the **MPV924** occupies 128 words of memory at any one of 256 offset locations within the VME short I/O space. The location of the VME short I/O space is dependent on the choice of CPU installed in the system.

Figure 3.2 - Base Address Offset Selection



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The base address of the system configuration memory map is determined from the VME short I/O base address, plus an offset which is selected using jumper J2.

Figure 3.2 shows the position of J2 and table 3.1 gives the possible jumper settings and their corresponding address offsets. The **MPV924** is shipped from the factory with all jumpers on J2 inserted which gives a default offset of 0000H

Table 3.1 - Base Address Offset Options

h	g	f	e	d	c	b	a	Address Offset
IN	IN	I N	I N	I N	I N	I N	I N	0000H
IN	IN	I N	I N	I N	I N	I N	OUT	0100H
IN	IN	I N	I N	I N	I N	OUT	I N	0200H
IN	IN	I N	I N	I N	I N	OUT	OUT	0300H
IN	IN	I N	I N	I N	OUT	I N	I N	0400H
IN	IN	I N	I N	I N	OUT	I N	OUT	0500H
IN	IN	I N	I N	I N	OUT	OUT	I N	0600H
IN	IN	I N	I N	I N	OUT	OUT	OUT	0700H
IN	I N	I N	I N	OUT	I N	I N	I N	0800H

and so on, until .....

OUT	OUT	OUT	OUT	I N	OUT	OUT	OUT	F700H
OUT	OUT	OUT	OUT	OUT	I N	I N	I N	F800H
OUT	OUT	OUT	OUT	OUT	I N	I N	OUT	F900H
OUT	OUT	OUT	OUT	OUT	I N	OUT	I N	FA00H
OUT	OUT	OUT	OUT	OUT	I N	OUT	OUT	FB00H
OUT	OUT	OUT	OUT	OUT	OUT	I N	I N	FC00H
OUT	OUT	OUT	OUT	OUT	OUT	I N	OUT	FD00H
OUT	OUT	OUT	OUT	OUT	OUT	OUT	I N	FE00H
OUT	OUT	OUT	OUT	OUT	OUT	OUT	OUT	FF00H

Example:

If the VME Short I/O Address Space of the selected CPU is located at FFFF0000H, then the Base Address of the system memory map for the MPV924 can be set at FFFF0500H by removing jumpers J2a and J2c.

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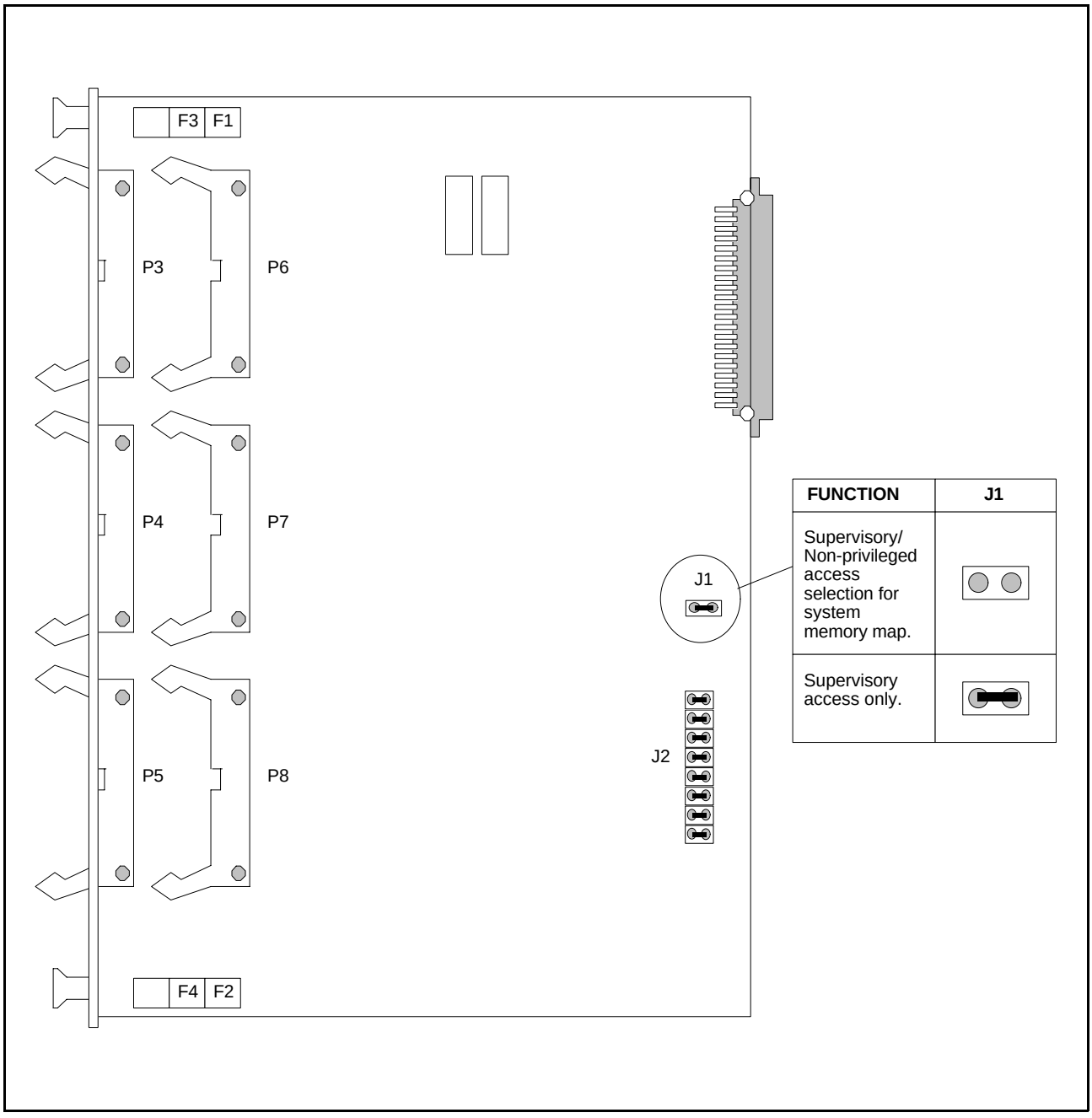
3.4 SUPERVISORY/NON PRIVILEGED ACCESS SELECTION (J1)

Jumper J1 is used to select the system configuration map address modifier response and can be used to restrict accesses to this area of memory.

When Jumper J1 is removed the board will respond to CPU's operating in supervisory or non-privileged mode. When inserted, only CPUs operating in supervisory mode may access the system configuration registers.

The MPV924 is shipped from the factory with J1 inserted so that it will respond only to CPUs operating in supervisory mode.

Figure 3.3 - Supervisory / Non-priviledged Access



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Note: For CPU cards driven by a 68000 series processor the mode of operation of CPU card is determined by the contents of the processor's control/status register. This register can be written to by software to switch from supervisory mode to non-privileged but will only return to supervisory mode following an exception condition such as a cold reset or interrupt.

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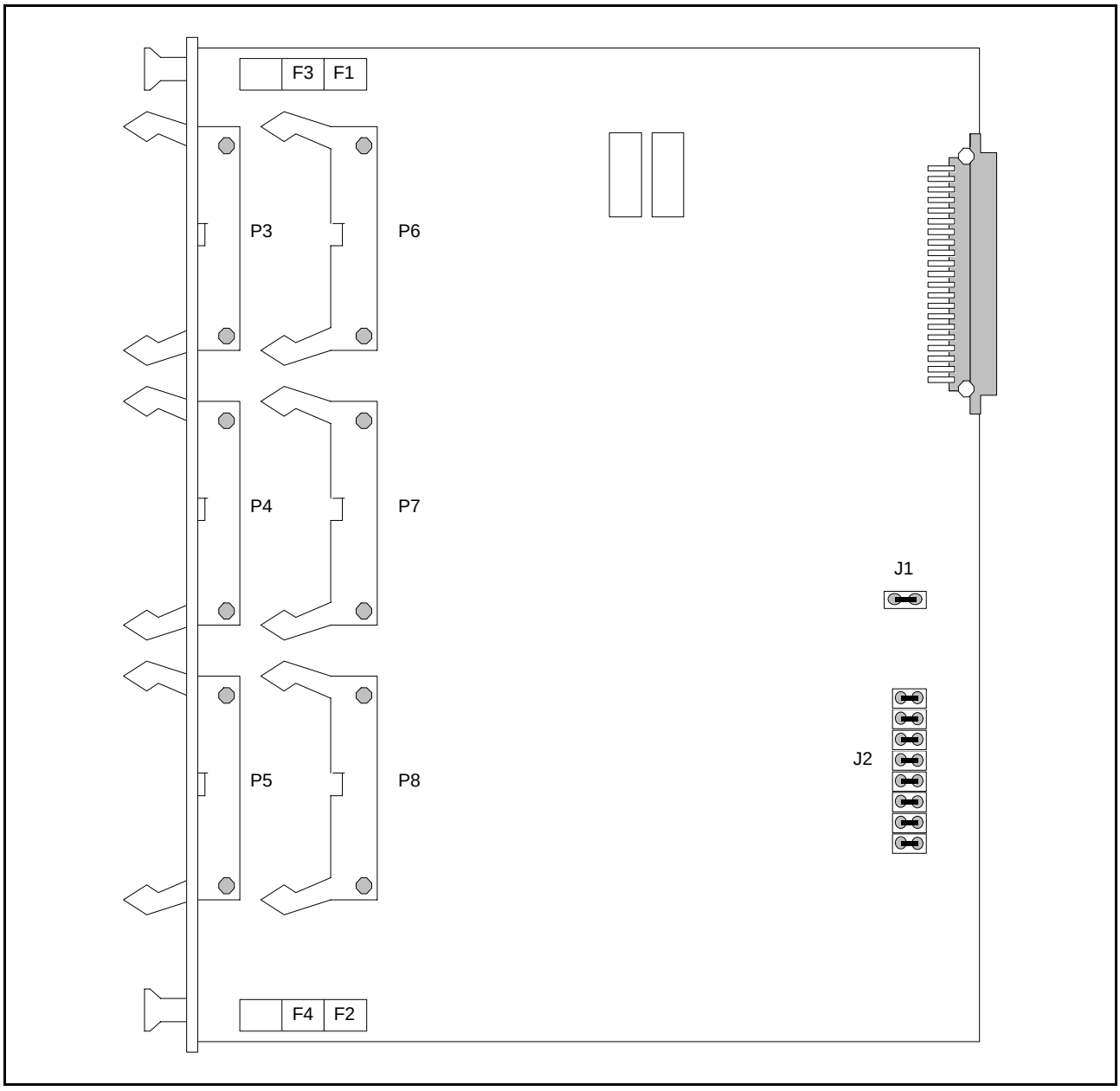
4 - CABLES AND CONNECTIONS

4.1 CONNECTING THE MPV924

Communication between the **MPV924** and the **VMEbus** is performed via the 96-way P1 connector and digital I/O signals are applied to the six 34-way IDC connectors P3, P4, P5, P6, P7 and P8.

The location of each connector is shown in Figure 4.1.

Figure 4.1 - Location of Input and Output Connectors



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4.2 CONNECTOR PIN ASSIGNMENTS

4.2.1 P1 Pin Assignment

The 96-way P1 connector on the **MPV924** mates with J1 on the VME Backplane.

Table 4.1 - P1 Pin Assignment

Pin	(a)	(b)	(c)
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22

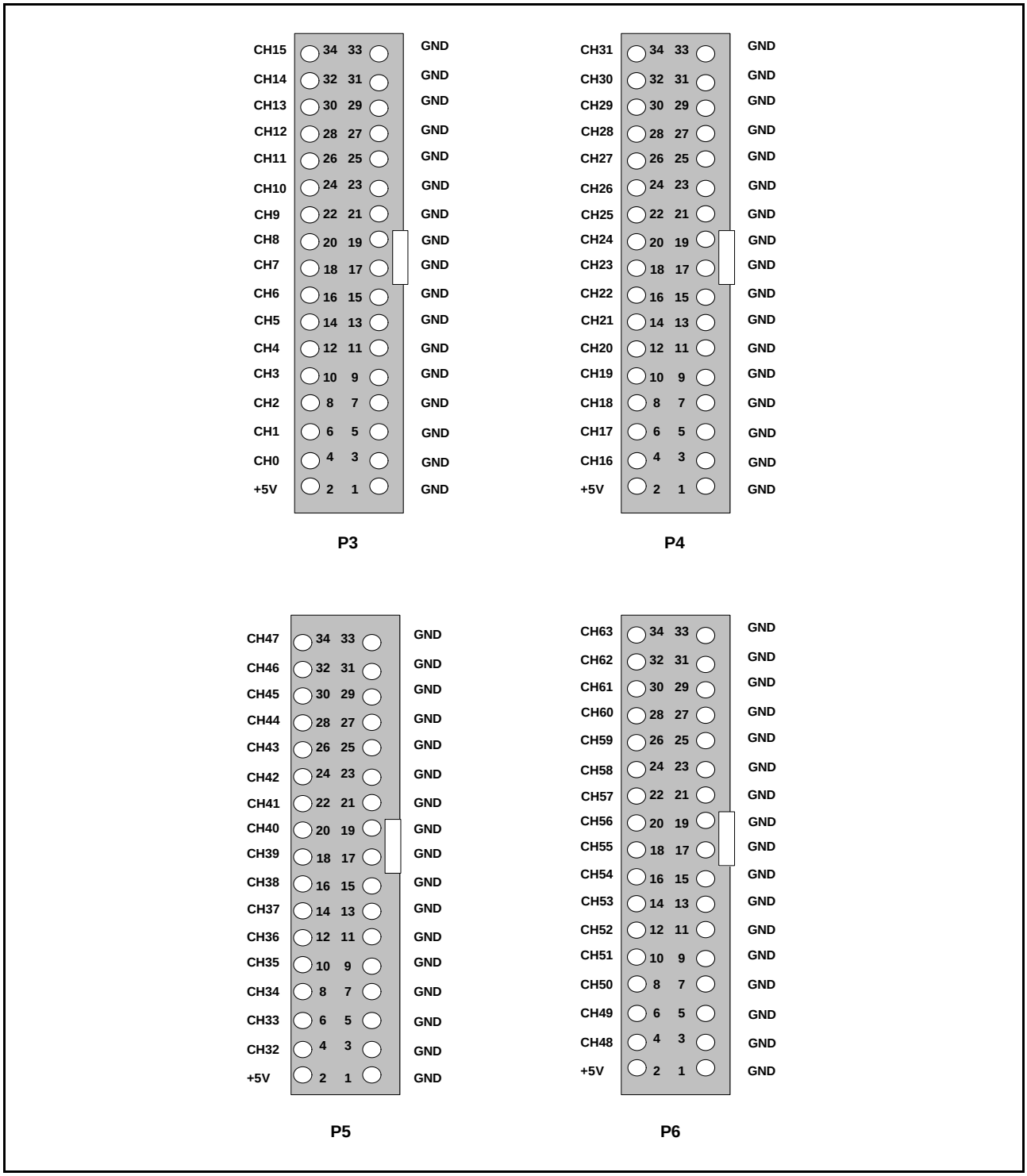
Pin	(a)	(b)	(c)
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	SERCLK	A17
22	IACKOUT*	SERDAT*	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

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4.2.2 Digital I/O Connections (P3, P4, P5, P6, P7 and P8)

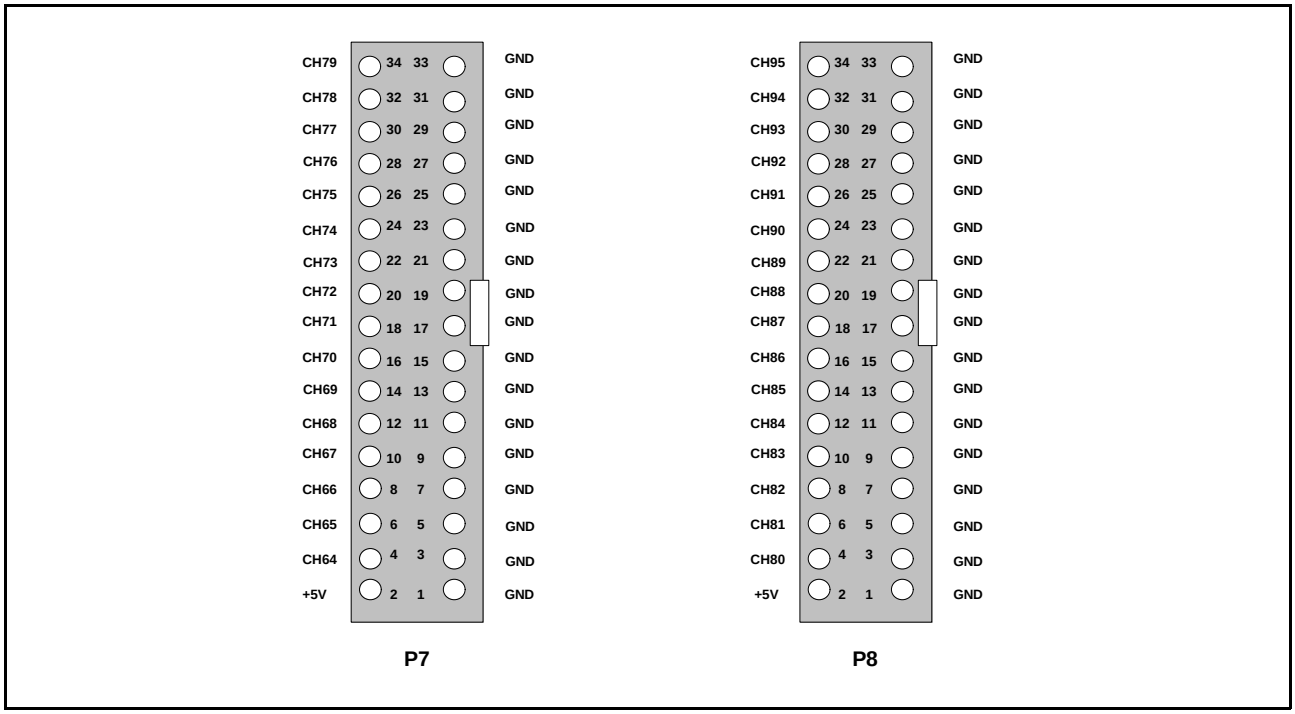
Up to 96 Digital I/O signals can be connected to the **MPV924.** The pin assignments of the digital I/O connectors P3, P4, P5, P6, P7 and P8 are shown in Figure 4.2 and 4.3.

Figure 4.2 - Digital I/O Connections (P3, P4, P5, P6)



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Figure 4.3 - Digital I/O Connections (P7, P8)



4.3 CONNECTING TO BURR-BROWN TERMINATION PANELS

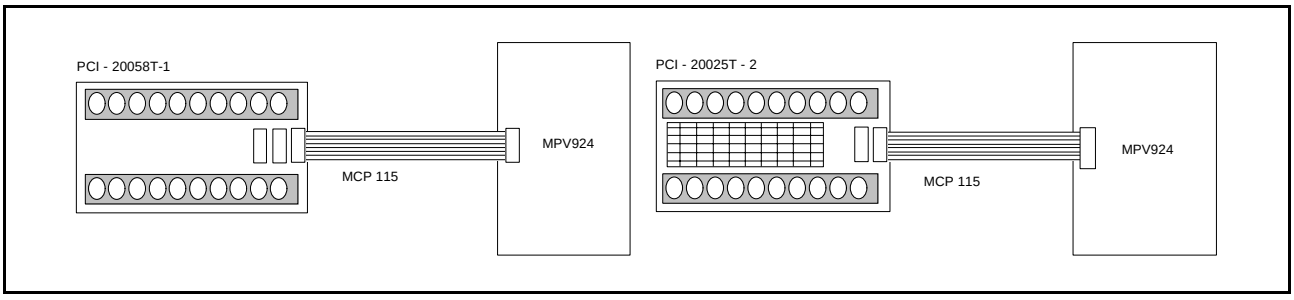
Burr-Brown supply a variety of termination panels to simplify connecting signals to the **MPV924.**

Table 4.2 lists the various termination panels and their associated mating cables which are illustrated in Figure 4.4.

Table 4.2 - Compatible Termination Panels

Termination Panel	Description
PCI-20058T-1	High Density Digital I/O Panel
PCI-20025T-2	Digital I/O Customizer Panel

Figure 4.4 - Burr-Brown Termination Panels



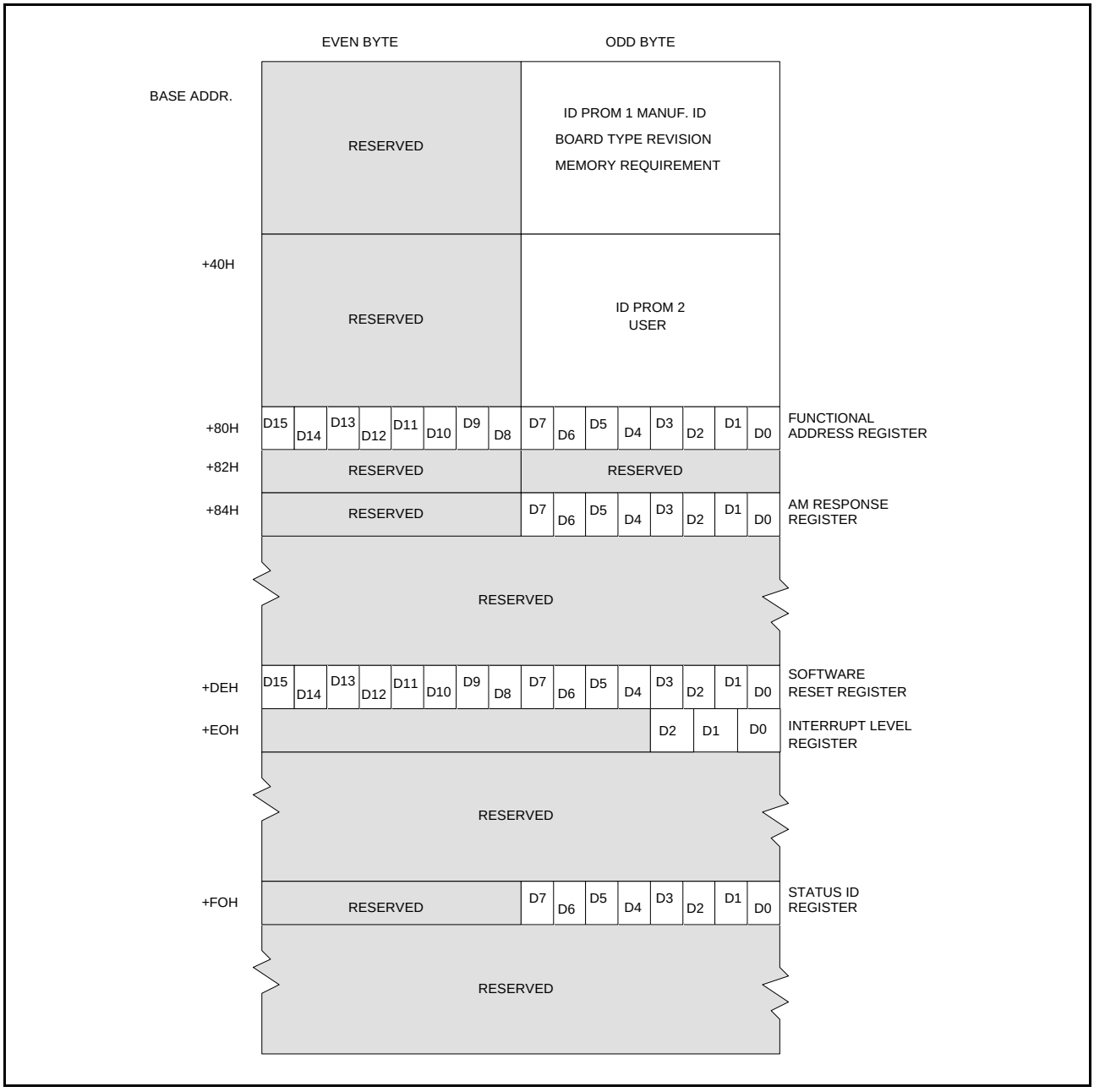
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5 - SOFTWARE CONFIGURATION

5.1 INTRODUCTION

The software configurable options of the **MPV924** are controlled by five registers and two ID PROMS which occupy an area of System Configuration Memory located within the short I/O address space of the VMEbus. The base address of the System Configuration Memory Map is set using jumper J2 to select an offset from the base address of the short I/O space. (see chapter 3)

Figure 5.1 - System Configuration Memory Map



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5.2 BOARD ID PROM (01(H) to 3F(H))

The **MPV924** board ID PROM occupies the first 32 odd bytes of the system configuration memory map.

The PROM contains ASCII character codes which identify the board by name and revision number,and which indicate the amount of memory it requires. This information can be used by system configuration software when allocating memory for the **MPV924**.

Figure 5.2 shows the contents of the PROM as shipped from the factory.

Figure 5.2 - Board ID PROM

Address Offset	HEX CODE	ASCII CHAR	DESCRIPTION
01	42	B	MANUFACTURER'S NAME
03	42	B	
05	20	SPACE	UNASSIGNED
07	4D	M	BOARD NAME
09	50	P	
0B	56	V	
0D	20	SPACE	
0F	39	9	
11	32	2	
13	34	4	
15	20	SPACE	
17	20	SPACE	UNASSIGNED
19	20	SPACE	
1B	20	SPACE	
1D	20	SPACE	
1F	52	R	BOARD REVISION NUMBER
21	45	E	
23	56	V	
25	20	SPACE	
27	XX		
29	2E	.	
2B	XX		
2D	20	SPACE	UNASSIGNED
2F	32	2	MEMORY REQUIREMENT
31	35	5	
33	36	6	
35	42	B	
37	20	SPACE	UNASSIGNED
39	20	SPACE	
3B	20	SPACE	
3D	20	SPACE	
3F	20	SPACE	

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5.3 USER ID PROM (41(H) to 7F(H))

The **MPV924** is fitted with an empty socket which allows the user to add an additional ID PROM between locations 41H and 7FH.

The recommended device for this socket is a 32 Byte, Tri-state Output, 25nS PROM such as Texas Instruments TBP18S030 or equivalent.

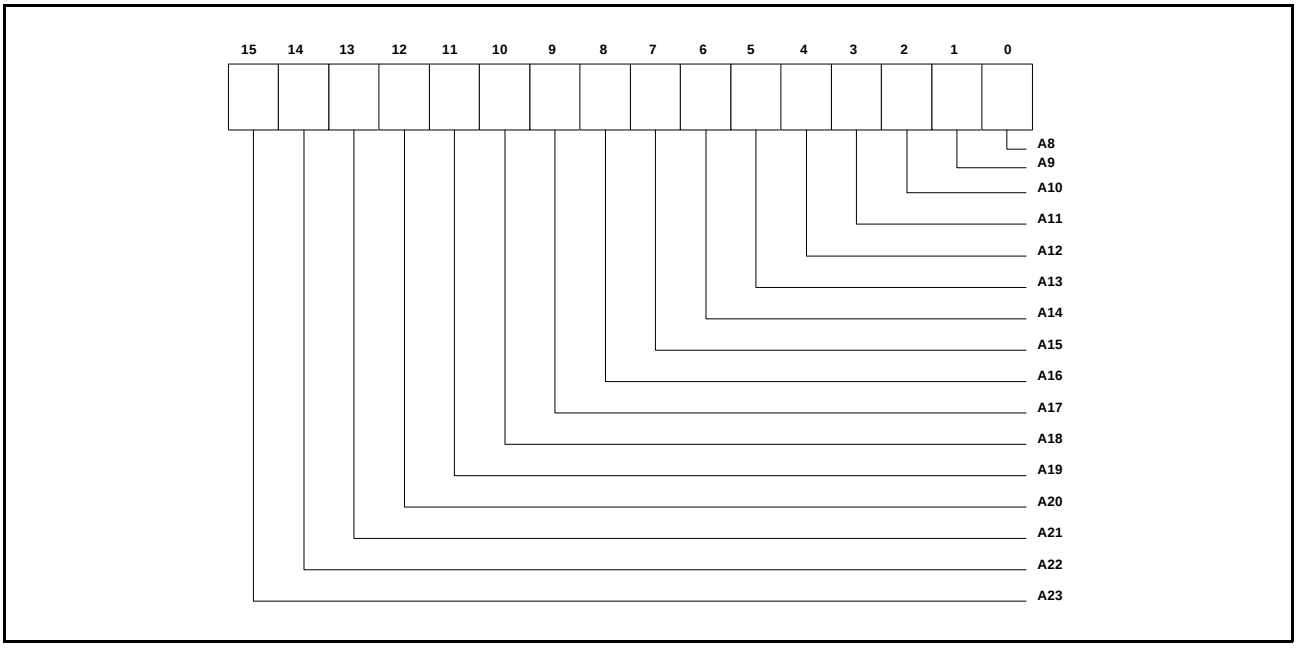
5.4 FUNCTIONAL ADDRESS REGISTER (80 (H) + 81(H))

Operation of the **MPV924 i**s controlled by the registers which make up the Functional Memory Map. The Functional Memory Map can be located anywhere in the VMEbus standard or short address space by entering an offset value into the Functional Address Register.

The functional address register is a 16bit register located at an offset of 80H from the base address of the system configuration memory map.

When mapping the functional memory map into short address space ensure that it does not overlap the system memory map. If this occurs the affected registers will not respond to a VME access. A SYSRESET will then be required before the functional memory map can be moved.

Figure 5.3 - Functional Address Register



EXAMPLE:

To position the functional memory map starting at 1D4000(H). Then program 1D40(H) to the functional address register

```
MOVE.W #$1D40,BaseAddress80(H)
```

or

```
MOVE.B #$1D,BaseAddress80(H)
MOVE.B #$40,BaseAddress81(H)
```


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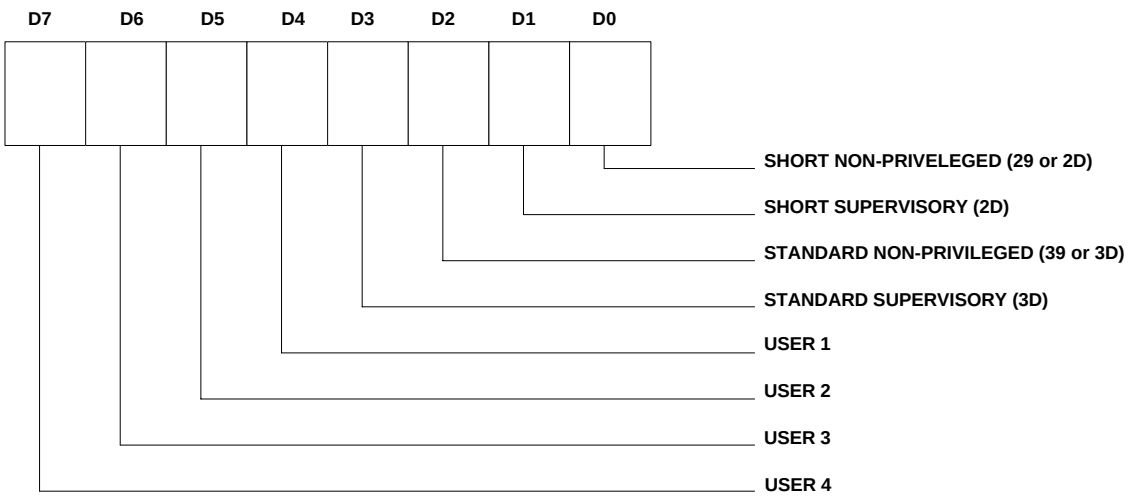
5.5 ADDRESS MODIFIER RESPONSE REGISTER (85(H))

Address modifiers are used to control access to the functional memory map.

The **MPV924** will only respond to addresses which include the expected AM code. The code is defined by the bits set in the address modifier response register as shown in Figure 5.4.

For most applications the address modifier response register will be set to either 04(H) or 08(H) to select either standard non- privileged response or standard supervisory response. The power-up condition is 00(H) which prevents access to the functional memory map.

Figure 5.4 - Address Modifier Response Register



D7	D6	D5	D4	D3	D2	D1	D0	AM CODES	RESPONSE
0	0	0	0	0	0	0	0	Default	Access Denied
0	0	0	0	0	0	0	1	29 or 2D	Short Non-privileged or supervisory
0	0	0	0	0	0	1	0	2D	Short supervisory
0	0	0	0	0	1	0	0	30 or 3D	Standard non-privileged or supervisory
0	0	0	0	1	0	0	0	3D	Standard supervisory only
0	0	0	1	0	0	0	0	1D	Respond to USER1 code only
0	0	1	0	0	0	0	0	19	Respond to USER2 code only
0	1	0	0	0	0	0	0	15	Respond to USER3 code only
1	0	0	0	0	0	0	0	11	Respond to USER4 code only

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5.6 SOFTWARE RESET REGISTER (DE(H))

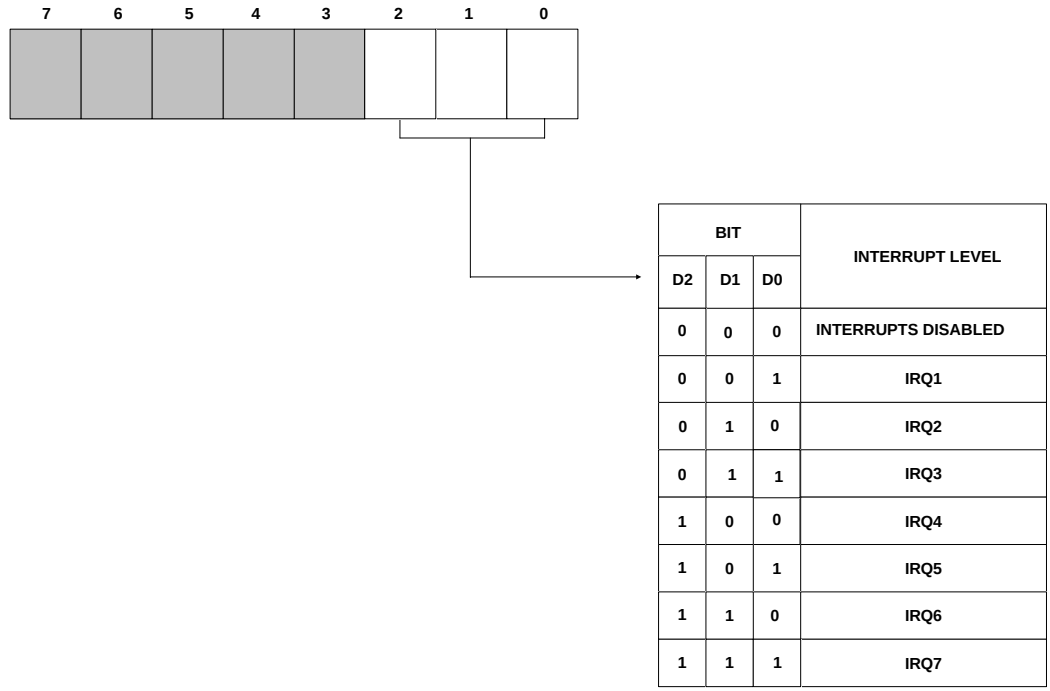
Writing any value to the software reset register will reset all the **MPV924** registers to their power-up conditions.

5.7 INTERRUPT LEVEL REGISTER (EI(H)

The interrupt level register is a single-byte width register which uses three bits to define the level of interrupts generated by the **MPV924.** Bits 3 to 7 are not driven.

The power up condition is 000 Binary i.e.: Interrupts disabled.

Figure 5.5 - Interrupt Level Register Key



BIT			INTERRUPT LEVEL
D2	D1	D0	
0	0	0	INTERRUPTS DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

5.8 STATUS ID REGISTER (FIH)

The **MPV924** has an 8 bit status ID byte which will be read by the **interrupt handler** during a valid interrupt cycle. This byte is used by the **CPU** to determine of the **interrupt vector,** which in turn, is used to point to the **interrupt service routine.**

> The status ID register is located in both the system configuration map and the functional memory map at offset address +F0(H).

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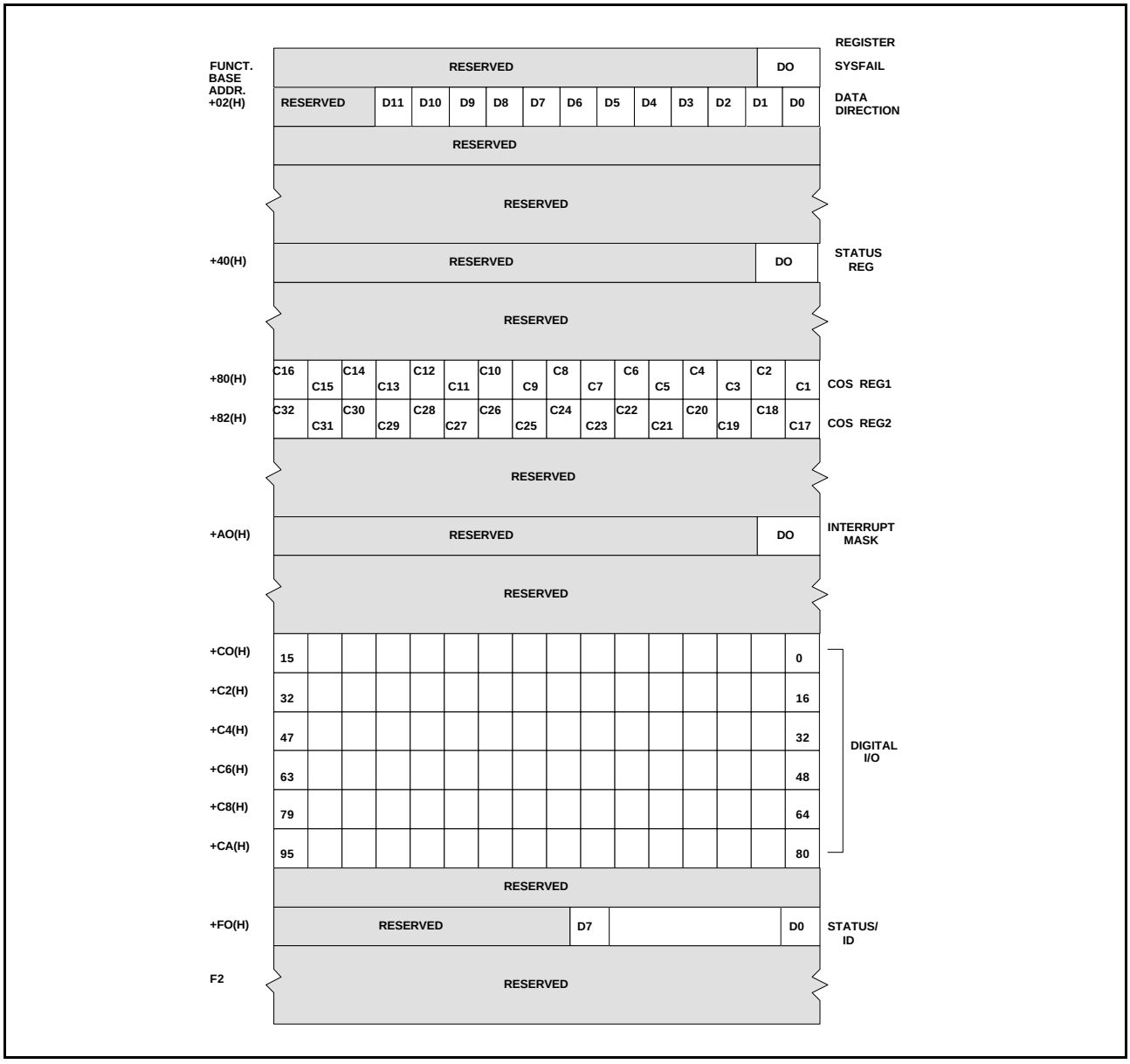
6 - OPERATING THE MPV924

6.1 THE FUNCTIONAL MEMORY MAP

The operation of the **MPV924** is controlled by a selection of registers which form part of the **Functional Memory Map**. The functional memory map occupies 256 words within the standard or short VME address space and includes control registers, the "change-of-state" registers and an area used for digital data.

The location of the functional memory map within VME address space is controlled by entering an offset value in the **Functional Address Register** (see section 5.4)

6.1 - Functional Memory Map



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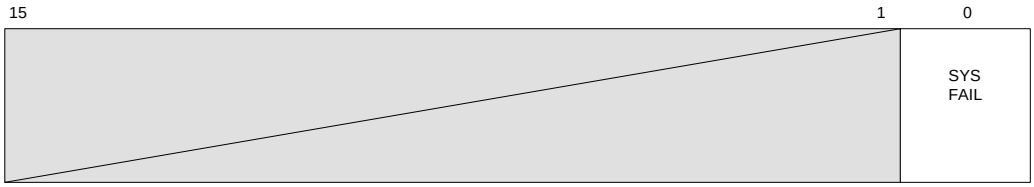
6.2 CLEARING THE SYSFAIL CONDITION (00(H))

At power-up, or after a board reset the **MPV924** drives the VMEbus SYSFAIL* line low (as suggested in ANSI/IEEE Std 1014-1987), and indicates this condition by illuminating the front panel LED red.

> A master CPU which monitors SYSFAIL* may also light an LED to indicate that SYSFAIL* is low. THIS IS NOT A FAULT CONDITION. The LED will be extinguished when SYSFAIL* is released.

SYSFAIL* can be released by writing a logic one to bit zero of the SYSFAIL register (base address +00H). Any further accesses to the **MPV924** will now cause the LED to flash green.

6.2 - SYSFAIL Register

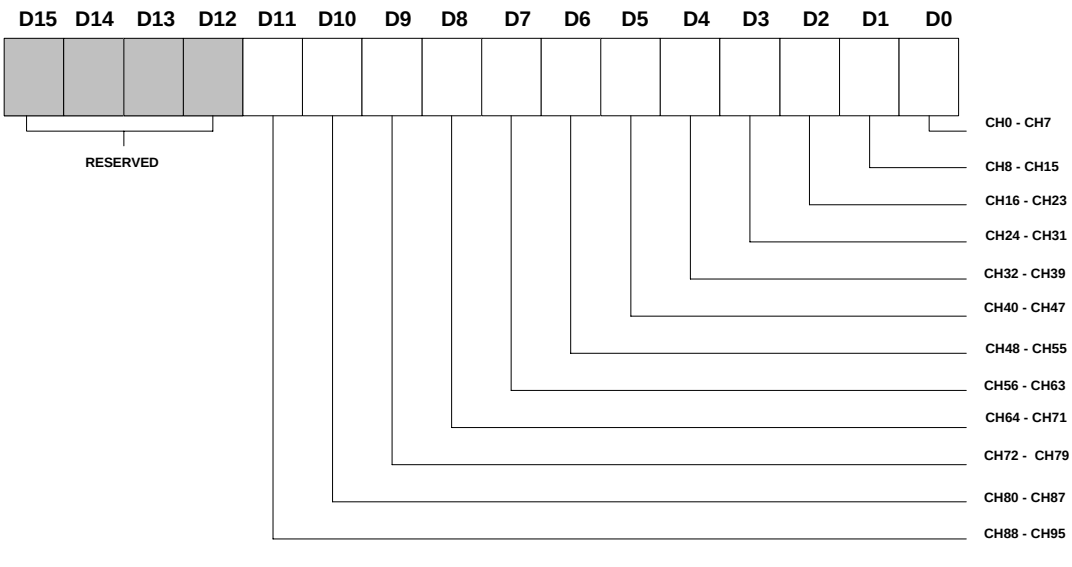


Note: Board operation is unaffected by the state of this register.

6.3 READING AND WRITING DIGITAL DATA

Channels can be programmed in groups of eight to act either as digital inputs from which data may be read, or outputs to which data may be written. A 12 bit Data Direction Register (DDR) is used to select and maintain the channel configuration.

6.3 - Data Direction Register



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6.3.1 Data Direction Register (02(H))

The data direction register resides at an offset of 02(H) from the base address of the functional memory map. As shown in Figure 6.3, a single bit in the data direction register corresponds with each group of eight consecutive channels. A logic 1 written into a bit in the data direction register configures the corresponding 8 channels as digital outputs. The outputs will remain high inpedance however, until data is written to the byte or word . A logic 0 will configure the channels as inputs.

For example :

1. To configure channels CH0 to CH47 as inputs and channels CH48 to CH95 as outputs, 0FC0(H) must be written to the DDR.

2. To configure channels CH0 to CH7 as outputs and all other channels as inputs, 0001(H) must be written to the DDR.

The power-up and reset condition of the data direction register is 0000(H) which configures all 96 channels as inputs. The hardware prevents the user from writing data to a channel which has been configured as an input.

Bits D12 to D15 are always driven low when the DDR is read.

6.3.2 Digital I/O Registers (C0(H) to CA(H))

The **MPV924** has 96 bits arranged as 6 x 16 bit registers starting at offset address +C0(H) which form part of the functional memory map, and which are used to store digital data either obtained from an input channel, or prior to being made available at an output.

6.4 - Digital I/O Registers

+CO(H)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	DIGITAL I/O REG 1
+C2(H)	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	DIGITAL I/O REG 2
+C4(H)	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	DIGITAL I/O REG 3
+C6(H)	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	DIGITAL I/O REG 4
+C8(H)	79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64	DIGITAL I/O REG 5
+CA(H)	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	DIGITAL I/O REG 6

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6.3.2.1 Reading from Input Channels

When a channel has been configured to act as an input channel (by clearing the corresponding bit of the data direction register), a logic level applied to the input will be latched into the relevant bit of the digital I/O registers. From here it may be read under software control. Since channels are configured in groups of eight, a byte access can be used to read a digital code applied to the inputs.

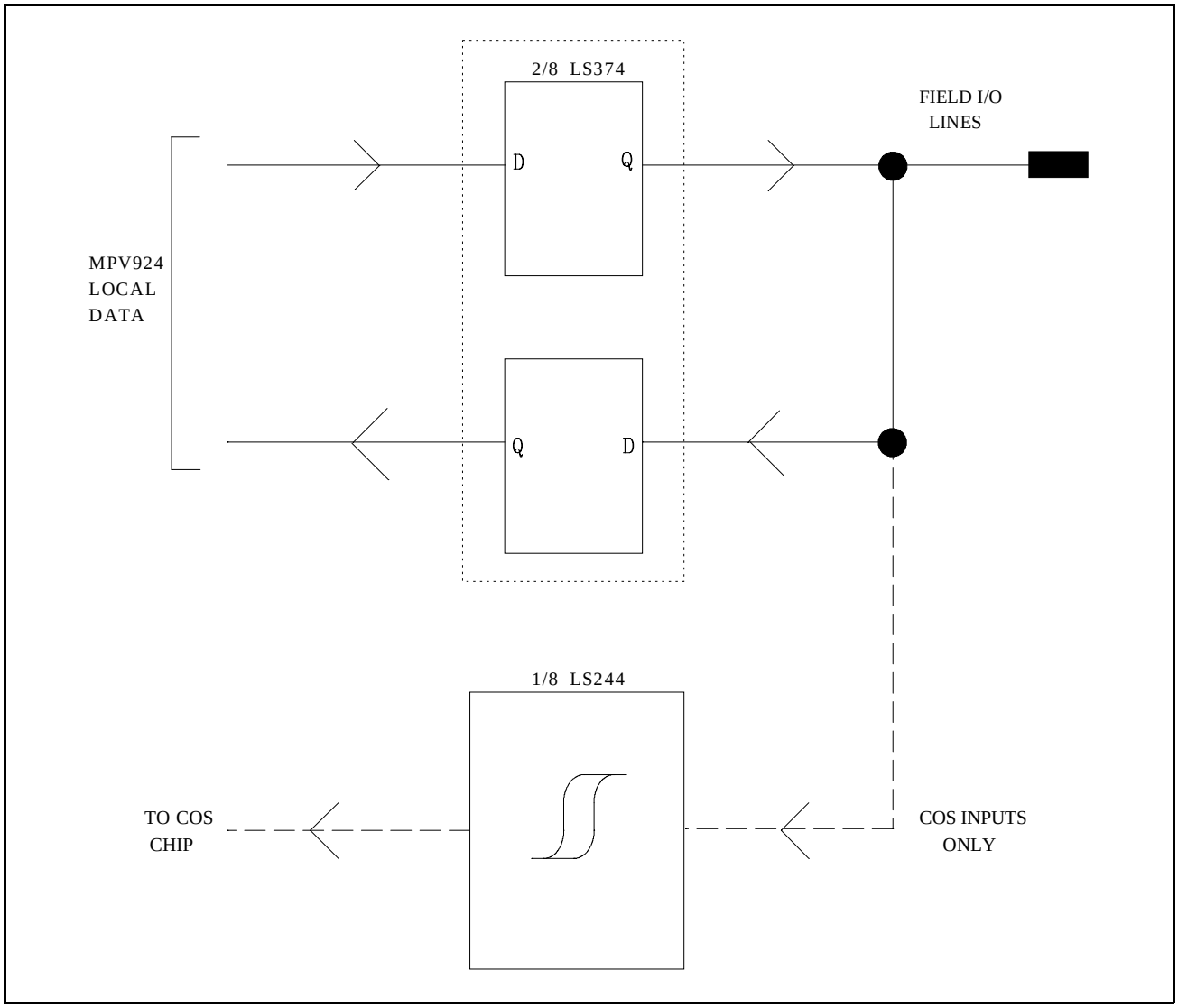
Special circuitry prevents software from writing to channels configured as inputs.

6.3.2.2 Writing to Output Channels

Digital codes written into the digital I/O registers are made available at the channels which have been configured as outputs. Special circuitry prevents data from being written to channels which have been configured as inputs.

Figure 6.5 shows the I/O hardware configuration used.

Figure 6.5 - I/O Configuration



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6.4 INTERRUPTING ON A CHANGE-OF-STATE

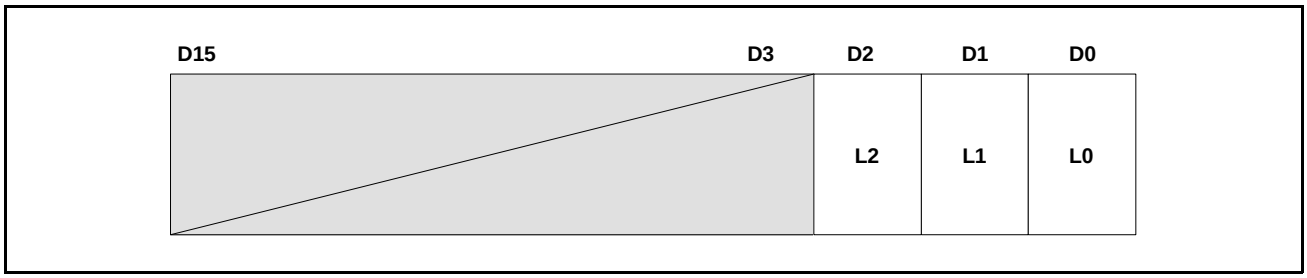
Sixteen of the channels of the **MPV924** (CH0 - CH15) are capable of generating an interrupt when a "change-of-state" occurs. Interrupts are "edge-triggered" and can be programmed to occur on receipt of a rising edge, a falling edge or when either occurs.

The "change-of-state" channels will cause an interrupt to be generated whether they are configured to act as inputs or outputs. In normal operation, the "change-of-state" function should be left disabled when the channels are configured as outputs.

6.4.1 Selecting the Interrupt Level

The **MPV924** can generate an interrupt on any of the seven VMEbus interrupt lines (IRQ1 - IRQ7). Selection of the interrupt level is acheived by writing to the interrupt level register located in the System Configuration Memory Map at offset E0(H). At power-up all bits in this register are set to zero, disabling all interrupts.

6.6 - Interrupt Level Register

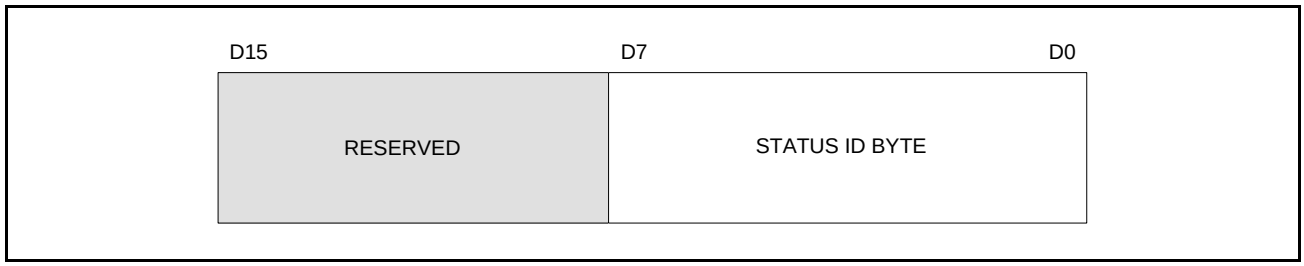


6.4.2 Setting the Status ID Byte

The **MPV924** has an 8 bit status ID byte which will be read by the interrupt handler during a valid interrupt cycle. This byte is typically used by the interrupt handler to determine the location of the interrupt vector which, in turn, is used by the CPU to find the interrupt service routine.

The status ID register is located in both the system configuration memory map and the functional memory map at offset F1(H).

Figure 6.7 - Status ID Byte Register



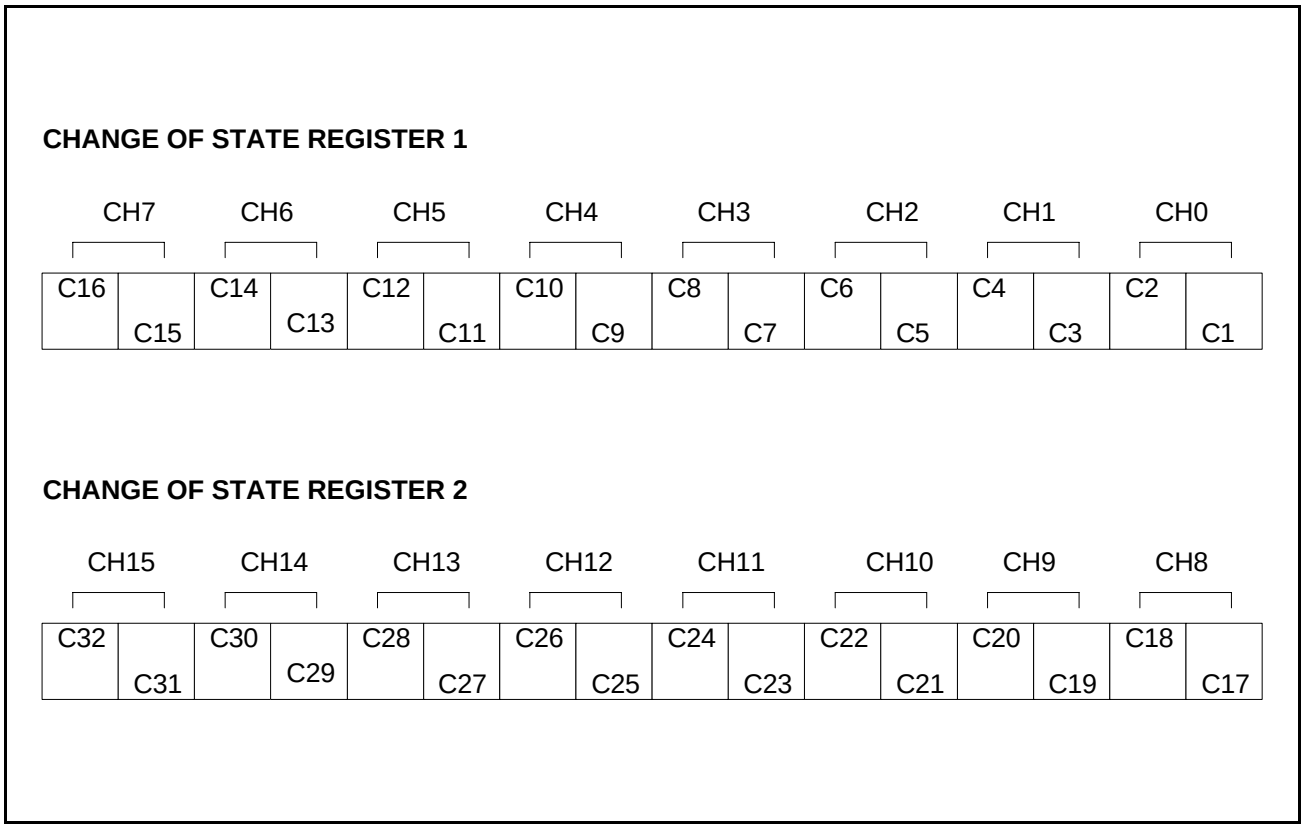
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6.4.3 Selecting “Change-of-State” Conditions

CH0 to CH15 can be programmed to respond to a change in their input logic level by generating an interrupt. The conditions under which interrupts are generated is controlled by two 16bit change of state registers located in the functional memory map at offset 80(H) and 82(H) respectively.

The response of each channel is controlled by two corresponding bits in one of the change of state registers as shown in figure 6.8.

Figure 6.8 - Change-of-State Register



The two bits controlling the interrupt response of a given channel can be used to disable the interrupt option for that channel, generate an interrupt on a rising edge, generate an interrupt on a falling edge or generate an interrupt when any “change-of-state” occurs, according to the following truth table.

Table 6.1 - "Change-of-State" Truth Table

C2n	C2n-1	Function
0	0	No change-of-state generated
0	1	Generate a change-of-state on a high-to-low transition only
1	0	Generate a change-of-state on a low-to-high transition only
1	1	Generate a change-of-state on a low-to-high or high-to-low transition

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For example :

1. If CH0 is to generate an interrupt whenever its input changes from a logic 1 state to a logic 0 state then bit C1 of interrupt control register 1 must be set to 1 and bit C2 must be set to 0.

2. If CH0 to CH7 are to respond to any change in the state of their inputs, and the "change-of-state" response of channels CH8 to CH15 is to be disabled then all of interrupt control register 1 must be set to 1, and all of interrupt control register 2 must be set to 0.

The power-up condition of the interrupt control registers is Cn=0 which ensures that all interrupts are initially disabled.

NOTE: Do not modify the Change of State Registers whilst interrupts are enabled.

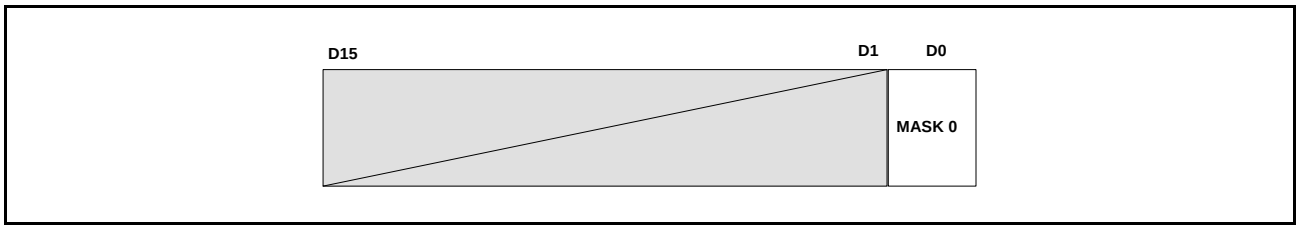
Initialising Change of State conditions must be done with interrupts disabled. Once the desired Change of State criteria has been selected, interrupts may be (re)enabled.

6.4.4 Enabling & Disabling Interrupts

Interrupts are enabled/disabled by writing to D0 in the Interrupt Mask Register located at offset A0(H). The interrupt mask register must be set high to enable interrupts.

On power-up the interrupt mask register is held low, ensuring that interrupts are disabled.

Figure 6.9 - Interrupt Mask Register



6.4.5 Clearing an Interrupt

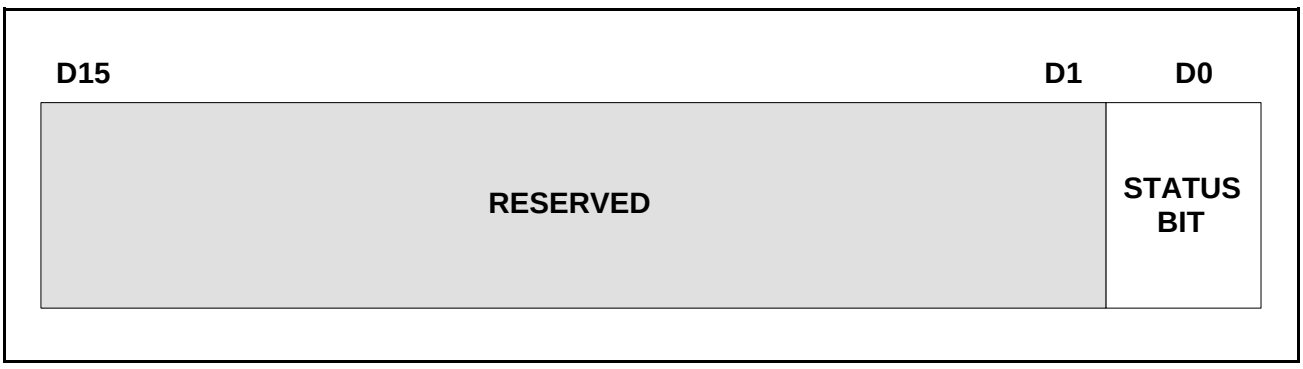
When a Change-of-State has occurred and an interrupt is generated. The interrupt routine, as a minimum, should read: (1) Clear the status register, then (2) Read the input byte or word.

These two operations clear the interrupt.

The status register is located at an offset of 40(H) from the base address of the functional memory map.

The power-up condition of the status register is logic 0, and thereafter a logic 1 is written to this register whenever Change-of-State occurs.

Figure 6.10 Status Register



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6.5 POLLING A CHANGE-OF-STATE

By periodically reading the status register to determine it's condition, the CPU can poll for a change-of-state. When this occurs the status register must be cleared by writing a logic 0 into D0 to return it to it's initial condition.

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7 - EXAMPLE PROGRAMS

7.1 EXAMPLE 1

```
*******************************************************************************
*       TITLE:          FLASH.SRC                                             *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                   *
*       DATE:           11TH DECEMBER 1989                                    *
*******************************************************************************
*
* This program locates the Functional Memory Map in Standard VME space
* (MVME-133XT CPU), permits supervisory and non-proviledged access,
* clears SYSFAIL and flashes the front panel LED on the MPV924 by
* writing to the board.
*
*******************************************************************************
*                       SYSTEM MAP                                            *
*******************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*******************************************************************************
*                       FUNCTIONAL MAP                                        *
*******************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
```


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```
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA

*****************************************************************************
*                           DATA
*****************************************************************************
*
* Not required
*
*****************************************************************************
*                       PROGRAM START                                       *
*****************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * CLEAR SYSFAIL

                JSR     WAIT
FLASH   .       MOVE.B  #$1,SYSFAIL             * WRITE TO SYSFAIL (flash 1)
 .  .  .        JSR     WAIT
 .  .  .        MOVE.B  #$FF,DD_REG             * WRITE TO DDR     (flash 2)

                TRAP    #2

WAIT    .       MOVE.L  #$FFFFFFFF,D0
 .  .  .        MOVE.L  #$00000000,D1
LOOP    .       CMP     D0,D1
 .  .  .        DBEQ    D0,LOOP
 .  .  .        RTS

END
```


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7.2 EXAMPLE 2

```
*****************************************************************************
*       TITLE:          OUT-1.SRC                                           *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                   *
*       DATE:           11TH DECEMBER 1989                                    *
*****************************************************************************
*
* Configures MPV924, all channels outputs and sets all outputs to Logic 0
*
*****************************************************************************
*                       SYSTEM MAP                                          *
*****************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*****************************************************************************
*                       FUNCTIONAL MAP                                      *
*****************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*******************************************************************************
*                           DATA
*******************************************************************************

ALL_LOW         EQU     $00                     * DATA TO OUTPUT LOGIC 0
ALL_HI          EQU     $FF                     * DATA TO OUTPUT LOGIC 1

*******************************************************************************
*                        PROGRAM START                                        *
*******************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * SWITCH OFF RED LEDS

START           MOVE.W  #$0FFF,DD_REG           * SET CH0-CH95 AS OUTPUTS

DATA_OUT        MOVE.B  #ALL_LOW,BYTE0          * OUTPUT CH0-CH7 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE1             * OUTPUT CH8-CH15 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE2             * OUTPUT CH16-CH23 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE3             * OUTPUT CH24-CH31 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE4             * OUTPUT CH32-CH39 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE5             * OUTPUT CH40-CH47 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE6             * OUTPUT CH48-CH55 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE7             * OUTPUT CH56-CH63 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE8             * OUTPUT CH64-CH71 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE9             * OUTPUT CH72-CH79 LOGIC 0
 .   .   .      MOVE.B  #ALL_LOW,BYTE10            * OUTPUT CH80-CH87 LOGIC 0
                MOVE.B  #ALL_LOW,BYTE11            * OUTPUT CH88-CH95 LOGIC 0

                TRAP    #2


END
```


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7.3 EXAMPLE 3

```
*****************************************************************************
*       TITLE:          OUT-2.SRC                                           *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                  *
*       DATE:           11TH DECEMBER 1989                                   *
*****************************************************************************
*
* This program configures CH0 - CH15 as outputs. Toggles through the outputs
* from CH0 to CH7 until all are set to logic 0.
*
*****************************************************************************
*                       SYSTEM MAP                                          *
*****************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*****************************************************************************
*                       FUNCTIONAL MAP                                      *
*****************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*******************************************************************************
*                           DATA
*******************************************************************************
*
* not required
*
*******************************************************************************
*                        PROGRAM START                                        *
*******************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * SWITCH OFF RED LEDS
                MOVE.W  #$0001,DD_REG           * SET CH0-CH7 ONLY AS OUTPUTS


 .  .  .        MOVE.B  #$00,D0                   * USE D0 FOR ZERO CHECK
 .  .  .        MOVE.B  #$0F,D2                   * REPEAT 16 TIMES
REPEAT          MOVE.B  #$08,D3                   * TOGGLE CH0-CH8
 .  .  .        MOVE.W  #$00FE,D5             * START WITH CH0

START  .        MOVE.B   D1,BYTE0             * LOAD INTO BYTE0
 .  .  .        JSR     WAIT                  * DELAY BETWEEN CHANNELS
                 ROL    #1,D1                 * NEXT CHANNEL
 .  .  .        CMP     D3,D0                 * FINISHED COUNT?
 .  .  .        DBEQ    D3,START              * IF NOT, NEXT CHANNEL
 .  .  .        CMP      D2,D0                * FINISHED SEQUENCE
 .  .  .        DBEQ     D2,REPEAT            * IF NOT, REPEAT COUNT

 .  .  .        MOVE.B  #$FF,BYTE0            * SWITCH OFF TO FINISH

                 TRAP    #2

WAIT    .       MOVE.W  #$FFFF,D4
LOOP    .       CMP     D4,D0
 .  .  .        DBEQ    D4,LOOP
 .  .  .        RTS

END
```


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7.4 EXAMPLE 4

```
*****************************************************************************
*       TITLE:          OUT-3.SRC                                           *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                 *
*       DATE:           13TH DECEMBER 1989                                  *
*****************************************************************************
*
* This program configures CH0 - CH15 as outputs. Performs four data sequences
* and returns to all input condition.
*
*****************************************************************************
*                       SYSTEM MAP                                          *
*****************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*****************************************************************************
*                       FUNCTIONAL MAP                                      *
*****************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*******************************************************************************
*                           DATA
*******************************************************************************
*
ALL_ON          EQU     $00
ALL_OFF         EQU     $0FF
ALT_ON1         EQU     $0AA
ALT_ON2         EQU     $055
*
*******************************************************************************
*                        PROGRAM START                                        *
*******************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * SWITCH OFF RED LEDS
                MOVE.W  #$0003,DD_REG           * SET CH0-CH15 ONLY AS OUTPUTS
 .  .  .        MOVE.B  #$00,D0                    * USE D0 FOR ZERO CHECK

 .  .  .        JSR     SEQ2
 .  .  .        JSR     SEQ4
 .  .  .        JSR     SEQ2
 .  .  .        JSR     SEQ3
 .  .  .        JSR     SEQ2
 .  .  .        JSR     SEQ1
 .  .  .        JSR     SEQ2

 .  .  .        MOVE.W  #$0000,DD_REG

 .  .  .        TRAP    #2

*******************************************************************************
*SEQUENCE 1
*******************************************************************************

SEQ1    .       MOVE.B  #$08,D2                    * REPEAT 8 TIMES

REPEAT1         MOVE.B  #$08,D3                    * TOGGLE CH0-CH15
 .  .  .        MOVE.W  #$00FF,D5           *
 .  .  .        MOVE.W  #$00FF,D6

START1          MOVE.B  D5,BYTE0            * LOAD DATA
 .  .  .        MOVE.B  D6,BYTE1            *
```


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```
 .  .  .       JSR     WAIT                    * DELAY BETWEEN CHANNELS
               ROL     #1,D5                   * NEXT CHANNEL
 .  .  .       ROR     #1,D6                   *
 .  .  .       CMP     D3,D0                   * FINISHED COUNT?
 .  .  .       DBEQ    D3,START1               * IF NOT, NEXT CHANNEL
 .  .  .       CMP      D2,D0                  * FINISHED SEQUENCE
 .  .  .       DBEQ     D2,REPEAT1             * IF NOT, REPEAT COUNT

 .  .  .       MOVE.B  #ALL_OFF,BYTE0          * SWITCH OFF TO FINISH
 .  .  .       MOVE.B   #ALL_OFF,BYTE1                *

 .  .  .       RTS

*****************************************************************************
*SEQUENCE 2
*****************************************************************************

SEQ2   .       MOVE.B  #$05,D2                 * REPEAT 5 TIMESM

REPEAT2        MOVE.B  #ALL_ON,BYTE0           * START WITH ALL LOGIC 0
 .  .  .       MOVE.B  #ALL_ON,BYTE1           *
 .  .  .       JSR     WAIT
 .  .  .       JSR     WAIT
 .  .  .       MOVE.B  #ALL_OFF,BYTE0          * FLASH OFF
 .  .  .       MOVE.B  #ALL_OFF,BYTE1          *
 .  .  .       JSR     WAIT
 .  .  .       JSR     WAIT
 .  .  .       CMP     D2,D0
 .  .  .       DBEQ    D2,REPEAT2

 .  .  .       RTS


*****************************************************************************
*SEQUENCE 3
*****************************************************************************

SEQ3   .       MOVE.B  #$0F,D2
REPEAT3        MOVE.B  #ALT_ON1,BYTE0          * SET ALTERNATE ON/OFF
 .  .  .       MOVE.B  #ALT_ON1,BYTE1
 .  .  .       JSR     WAIT
 .  .  .       JSR     WAIT
 .  .  .       MOVE.B  #ALT_ON2,BYTE0          * SWAP TO ALTERNATE OFF/ON
 .  .  .       MOVE.B  #ALT_ON2,BYTE1
 .  .  .       JSR     WAIT
 .  .  .       JSR     WAIT
```


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```
 .  .  .       CMP     D2,D0
 .  .  .       DBEQ    D2,REPEAT3

 .  .  .       MOVE.B  #ALL_OFF,BYTE0
 .  .  .       MOVE.B  #ALL_OFF,BYTE1

 .  .  .       RTS

*******************************************************************************
*SEQUENCE 4
*******************************************************************************

SEQ4   .       MOVE.B  #$02,D3
 .  .  .       MOVE.B  #ALL_ON,BYTE0         * START ALL ON
 .  .  .       MOVE.B  #ALL_ON,BYTE1
 .  .  .       JSR     WAIT

REPEAT4        MOVE.W  #0001,D1
 .  .  .       MOVE.B  #08,D2
REP0   .       MOVE.B  D1,BYTE0              * RUN UP FIRST 8 CHANNELS
 .  .  .       JSR     WAIT
 .  .  .       ROL     #1,D1
 .  .  .       CMP     D2,D0
 .  .  .       DBEQ    D2,REP0

 .  .  .       MOVE.W  #0001,D1
 .  .  .       MOVE.B  #08,D2
REP1   .       MOVE.B  D1,BYTE1              * RUN UP SECOND 8 CHANNELS
 .  .  .       JSR     WAIT
 .  .  .       ROL     #1,D1
 .  .  .       CMP     D2,D0
 .  .  .       DBEQ    D2,REP1

 .  .  .       MOVE.B  #08,D2
REP2   .       MOVE.B  D1,BYTE1              * RUN DOWN SECOND 8 CHANNELS
 .  .  .       JSR     WAIT
 .  .  .       ROR     #1,D1
 .  .  .       CMP     D2,D0
 .  .  .       DBEQ    D2,REP2

 .  .  .       MOVE.B  #08,D2
 .  .  .       MOVE.W  #0008,D1
REP3   .       MOVE.B  D1,BYTE1              * RUN DOWN FIRST 8 CHANNELS
 .  .  .       JSR     WAIT
 .  .  .       ROR     #1,D1
 .  .  .       CMP     D2,D0
```


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```
  .   .   .       DBEQ    D2,REP3

  .   .   .       CMP     D3,D0
  .   .   .       DBEQ    D3,REPEAT4

  .   .   .       RTS
  .   .   .
*******************************************************************************
*DELAY
*******************************************************************************

WAIT    .       MOVE.W  #$FFFF,D4
LOOP    .       CMP     D4,D0
  .   .   .       DBEQ    D4,LOOP
  .   .   .       RTS

END
```

7.5 EXAMPLE 5

```
*******************************************************************************
*       TITLE:          IN-1.SRC                                              *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                   *
*       DATE:           13th DECEMBER 1989                                    *
*******************************************************************************
*
* Simple program to leave in default channel configuration and read initial
* data at inputs
*
*******************************************************************************
*                       SYSTEM MAP                                            *
*******************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*******************************************************************************
*                       FUNCTIONAL MAP                                        *
*******************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*******************************************************************************
*                        PROGRAM START                                        *
*******************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * SWITCH OFF RED LED

               MOVE.B  BYTE0,D0                * READ INITIAL DATA
 .  .  .       MOVE.B  BYTE1,D1
 .  .  .       MOVE.B  BYTE2,D2
 .  .  .       MOVE.B  BYTE3,D3
 .  .  .       MOVE.B  BYTE4,D4
 .  .  .       MOVE.B  BYTE5,D5

                TRAP    #2


END
```


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7.6 EXAMPLE 6

```
*******************************************************************************
*       TITLE:          IN-2.SRC                                              *
*       AUTHOR:         MHAIRI WATT, BURR-BROWN, LIVINGSTON                   *
*       DATE:           13th DECEMBER 1989                                    *
*******************************************************************************
*
* configures CH0 - CH15 as outputs and all other channels as inputs. Reads
* data from CH16 - CH31 and then makes this available at outputs. (Timing
* only controlled by WAIT routine)
*
*******************************************************************************
*                       SYSTEM MAP                                            *
*******************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*******************************************************************************
*                       FUNCTIONAL MAP                                        *
*******************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*****************************************************************************
*                        PROGRAM START                                      *
*****************************************************************************

                ORG     $10000
                LEA.L   *,SP

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG       * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG           * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL                 * SWITCH OFF RED LED
  .  .  .       MOVE.W #$0003,DD_REG                * CH0 - CH15 OUTPUTS

  .  .  .       MOVE.B #$00,D0                      * SET UP FOR 16 REPEATS
  .  .  .       MOVE.B #$0F,D1

REPEAT          MOVE.B BYTE2,D2                     * READ CH16 - CH31
  .  .  .       MOVE.B BYTE3,D3
  .  .  .       JSR    WAIT                         * WAIT
  .  .  .       MOVE.B D2,BYTE0                     * WRITE TO CH0 - CH15
  .  .  .       MOVE.B D3,BYTE1
  .  .  .       CMP    D1,D0
  .  .  .       DBEQ   D1,REPEAT

                TRAP   #2

WAIT    .       MOVE.L #$FFFFFFFF,D4
LOOP    .       CMP    D4,D0
  .  .  .       DBEQ   D4,LOOP

END
```


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7.7 EXAMPLE 7

```
*******************************************************************************
*       TITLE:          COS-1.SRC                                             *
*       AUTHOR:         DAVID SCOTT, BURR-BROWN, LIVINGSTON                    *
*       DATE:           30th NOVEMBER 1989                                     *
*******************************************************************************
*******************************************************************************
*                       SYSTEM MAP                                             *
*******************************************************************************

SYSTEM_BASE     EQU     $FFFF0000
FUNCT_BASE_REG  EQU     SYSTEM_BASE+$80
FUNCT_AM_REG    EQU     SYSTEM_BASE+$85
INT_LEV_REG     EQU     SYSTEM_BASE+$E1
STAT_ID_REG     EQU     SYSTEM_BASE+$F1

*******************************************************************************
*                       FUNCTIONAL MAP                                         *
*******************************************************************************

FUNCT_BASE      EQU     $400000
SYSFAIL         EQU     FUNCT_BASE+$1
DD_REG          EQU     FUNCT_BASE+$2
STATUS_REG      EQU     FUNCT_BASE+$41
COS_REG1        EQU     FUNCT_BASE+$80
COS_REG2        EQU     FUNCT_BASE+$82
INT_MASK_REG    EQU     FUNCT_BASE+$A1
BYTE0           EQU     FUNCT_BASE+$C1
BYTE1           EQU     FUNCT_BASE+$C0
BYTE2           EQU     FUNCT_BASE+$C3
BYTE3           EQU     FUNCT_BASE+$C2
BYTE4           EQU     FUNCT_BASE+$C5
BYTE5           EQU     FUNCT_BASE+$C4
BYTE6           EQU     FUNCT_BASE+$C7
BYTE7           EQU     FUNCT_BASE+$C6
BYTE8           EQU     FUNCT_BASE+$C9
BYTE9           EQU     FUNCT_BASE+$C8
BYTE10          EQU     FUNCT_BASE+$CB
BYTE11          EQU     FUNCT_BASE+$CA
```


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```
*****************************************************************************
*                       PROGRAM START                                       *
*****************************************************************************

                ORG     $10000
                LEA.L   *,SP
                ANDI    #$F0FF,SR               * ENABLE 68000 INTERRUPTS

CONFIGURATION   MOVE.W  #$4000,FUNCT_BASE_REG   * LOCATE BOARD IN STD VME SPACE
                MOVE.B  #$04,FUNCT_AM_REG       * RESPOND SUP & NON-PRIV ACCESS
                MOVE.B  #$1,SYSFAIL             * SWITCH OFF RED LED
                MOVE.B  BYTE0,D0                * READ INITIAL DATA

INT_SET_UP      MOVE.B  #$7,INT_LEV_REG
                MOVE.B  #$40,STAT_ID_REG        * ROUTINE ADDR PLACED AT $100
                MOVE.L  #INT_ROUTINE,$100

COS_SET_UP      MOVE.W  #$3,COS_REG1            * ANY CHANGE OF LEVEL ON BIT0
                MOVE.W  #$0,COS_REG2

                MOVE.B  #$1,INT_MASK_REG        * ENABLE INTERRUPTS

                MOVE.W  #$1,D7
WAIT            CMPI.W  #$1,D7                  * WAIT FOR INTERRUPT
                BEQ     WAIT

                TRAP    #2

*****************************************************************************
*                       INTERRUPT ROUTINE                                   *
*****************************************************************************

INT_ROUTINE     CLR.B   STATUS_REG               * CLEAR INTERRUPT FLAG
                MOVE.B  BYTE0,D1                 * STORE DATA & CLEAR INTERRUPT
                CLR.B   D7                       * INDICATE INT TO MAIN PROG
                RTE
END
```


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Boards are fully tested and temperature-cycled before leaving the factory to ensure reliable operation. However in the event of failure requiring a board to be returned for repair, the follow ing points apply :

1. Warranty is valid for one year from receipt of board.

2. Before returning a board, a Return Authorisation number (PAR No.) must be obtained from the original supplier. On receipt of this number, the board should be returned to the original supplier.

3. The board must be returned in the original packing to avoid mechanical or electrostatic damage.

4. If the warranty period has expired, then the user is liable for full costs of board repair and shipping.

5. Any attempt to modify or repair a board by the user will render the warranty void.

Completion of the form below will expedite board repair. Please enclose with board.

Company :		
Contact :		**Tel. No. :**
Board Type : MPV924	**Serial No. :**	**PAR No. :**
Purchase Date :		**Return Date :**
Fault Description :		

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