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PENTLAND SYSTEMS LIMITED

OPERATING MANUAL - OM904

MPV904

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** THIS MANUAL APPLIES TO THE MPV904 - REV 4 ONLY**

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1. Warranty is valid for one year from receipt of board.

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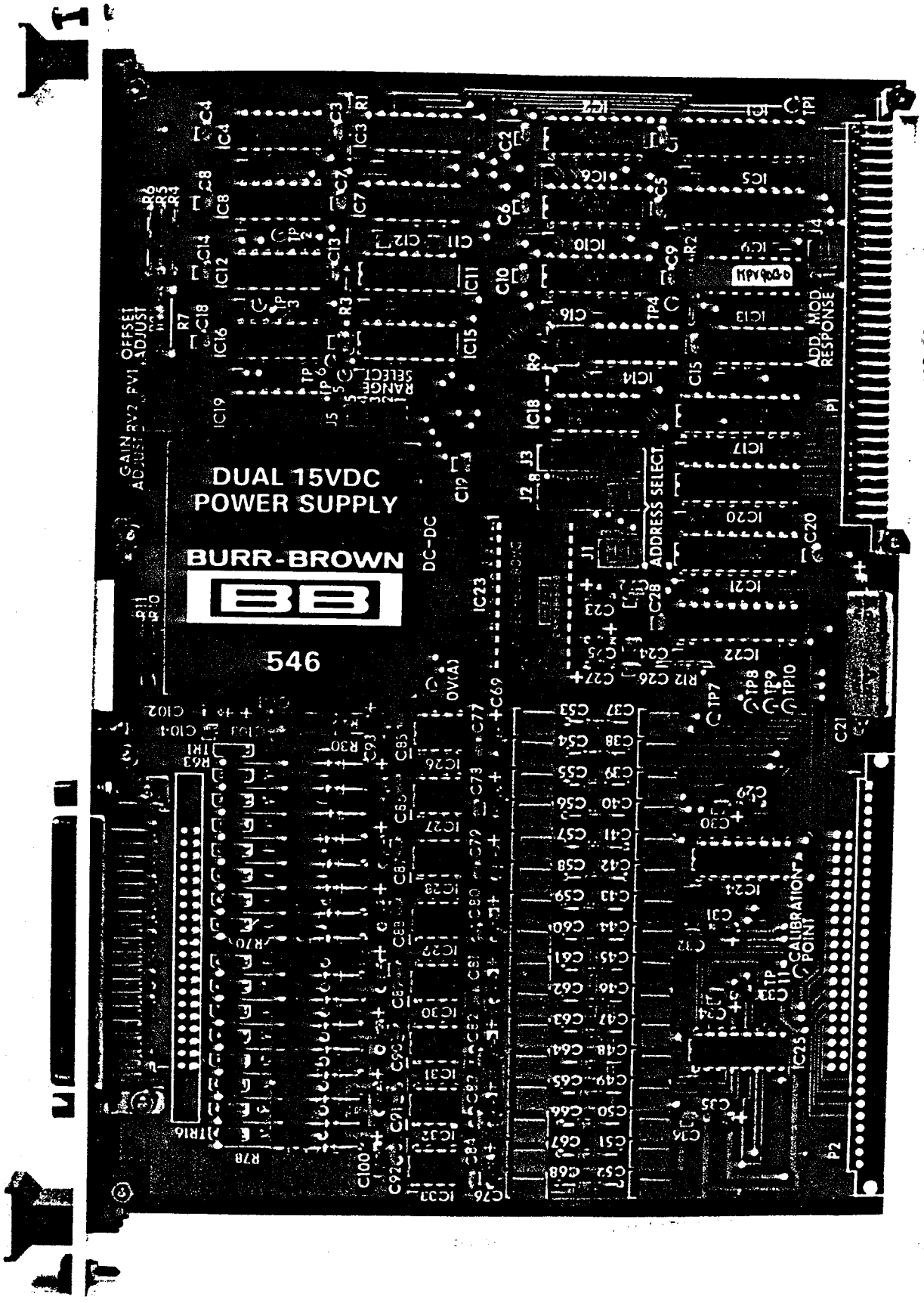
6.1 VMEbus Spec - Address Modifier Codes

6.2 Digital to Analog Converter DAC800 Data Sheet

Appendix A - VMEbus Backplane Connectors and VME Board Connectors

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Figure 1.1 MPV904



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Chapter 1 - GENERAL INFORMATION

1.1 INTRODUCTION

This manual provides general information, installation instructions, operating instructions, functional description and applications software examples for the MPV904 voltage output board.

1.2 GENERAL DESCRIPTION

The MPV904 analog output board is electrically and mechanically compatible with, and interfaces directly to the VMEbus.

The features of the MPV904 include:-

- 16 channels.
- 12 bit resolution.
- Single gain and offset adjustment.
- Address block selectable in 16 Mbyte memory space.
- Single +5V supply operation.

Dynamic analog outputs allow the MPV904 to provide high channel density on a single board. This approach frees system space for other peripherals and minimizes per channel power requirement. An on-board DC to DC converter powers the MPV904 from the +5V system supply. Output data is stored in on-board RAM and used by the refresh circuit to update the outputs. Each channel has been designed such that system calibration can be accomplished with a single gain and offset adjustment. Address and Address Modifier (AM) decoding are jumper programmable in the 16Mbyte memory space.

The sixteen analog outputs can be jumpered for unipolar or bi-polar operation.

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1.3 SPECIFICATION

ELECTRICAL

Typical at +25&C and rated power supplies unless otherwise stated.

OUTPUT CHARACTERISTICS	
Number of Channels	16
Output Voltage Ranges (Jumper Selectable)	0 to +5V, 0 to +10V ±2.5V, ±5V, ±10V, at 5mA
Short Circuit Protection, Duration	Indefinite to Common
ACCURACY	
Total Error [1] Max	±0.05% FSR[2]
Linearity	±0.012% FSR
Gain Error	±0.05% FSR
Offset Error	±0.012% FSR
ACCURACY OVER TEMPERATURE	
Accuracy Drift	±30ppm of FSR/&C
TRANSFER CHARACTERISTICS	
Resolution	12 bits
Settling Time, max	
To 0.1% of FSR	3.5ms
To 0.01% of FSR	5.0ms
POWER REQUIREMENTS	+5V ±5% at 1.5A max
ENVIRONMENTAL	
Operating Temperature	0&C to + 60&C
Storage Temperature	-25&C to +85&C
Relative Humidity	90% noncondensing

NOTES:
[1] With gain and offset error adjusted to zero.
[2] FSR means full scale range.

MECHANICAL

Compatible with double-height VMEbus card-racking systems.

Minimum card spacing 20.34mm (0.8") (VMEbus specification compatible).

One 37-pin 'D' type connector on board for analog outputs.

Use Cannon 'D' type connector part number DC37P/1A1N or equivalent.

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Chapter 2 - INSTALLATION INSTRUCTIONS

2.1 INTRODUCTION

This chapter provides installation instructions and an overview of the user selectable options on the MPV904.

2.2 PREPARING THE BOARD

This section describes the hardware preparation of the MPV904 prior to installation in a VMEbus system. Following the instructions described in this section will ensure that the board is configured as desired and will function as expected when installed.

MPV904 boards are factory calibrated and tested prior to shipment with jumpers in pre-determined positions.

Figure 2.1 indicates the physical position of the jumpers on the board.

Table 2.1 lists each jumper, its function and the factory set position.

A detailed description of each jumper is given in sections 2.2.1 through 2.2.3.

To alter the address modifier code response from the factory set values, the user must program the decoding PROM as described in section 2.2.3.

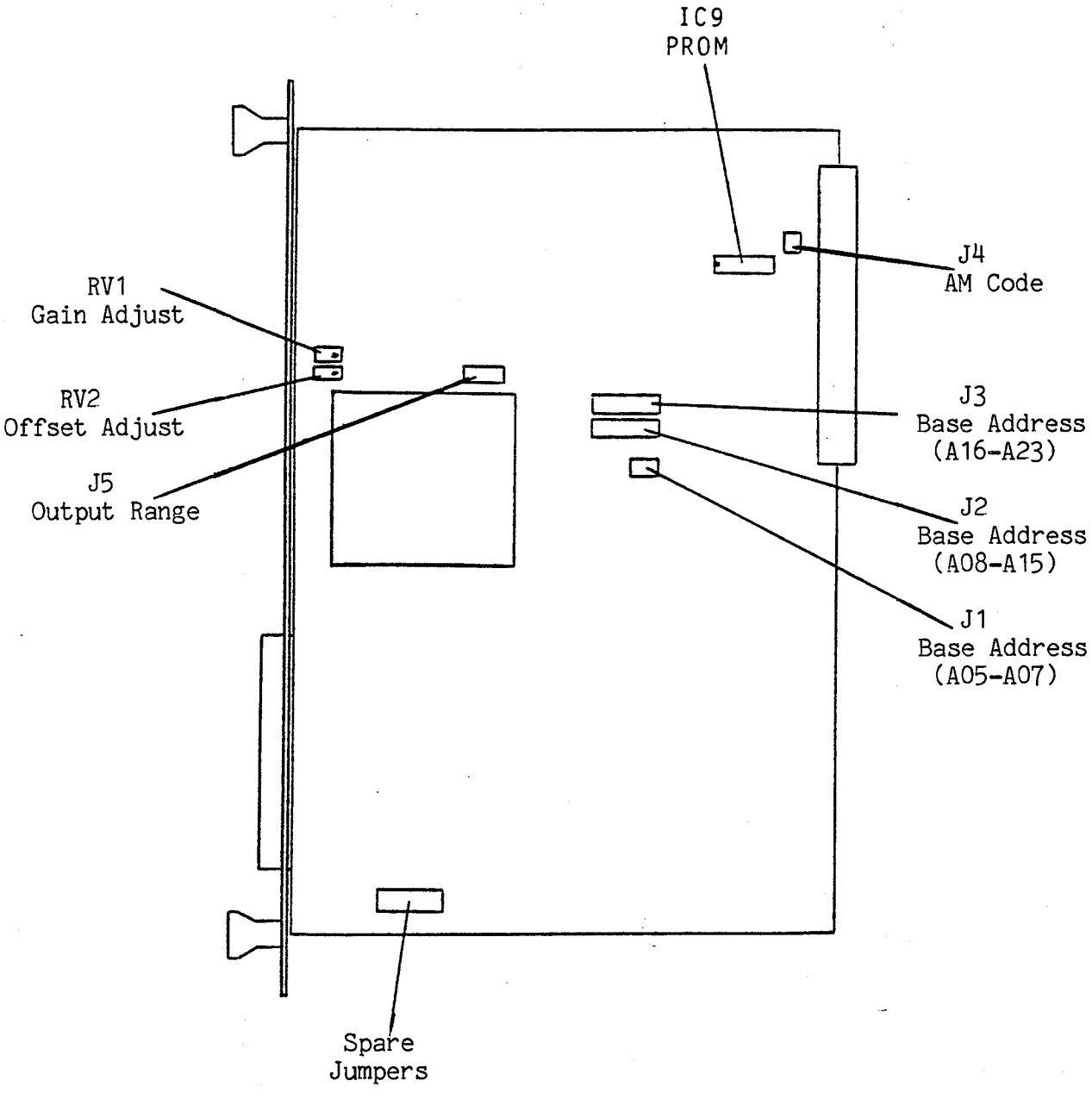
Before installation, the user should verify the configuration of the jumpers and, if necessary, alter the configuration to suit particular system requirements.

The board should not be installed or removed while power is applied to the VMEbus system.

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Figure 2.1

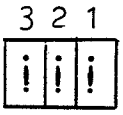
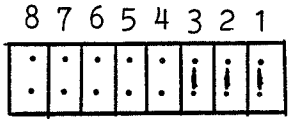
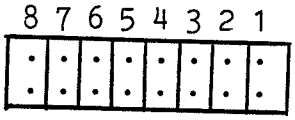
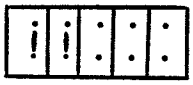
Position of Jumpers and Pots



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Table 2.1

JUMPER FUNCTIONS & FACTORY SETTINGS

JUMPER DESIGNATION	FUNCTION	FACTORY SET CONDITON
J1	Base Address Selection (A05-A07)	
J2	Base Address Selection (A08-A15)	
J3	Base Address Selection (A16-A23)	
J4	AM Code Response	
J5	Output Range Selection	

! Jumper Inserted

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2.2.1 Base Address Selection

The base address of the MPV904 can be set to any value by selecting the appropriate combination of positions on jumpers J1, J2 and J3. The factory set configuration is FFF800H. To change the sense of a bit simply change the jumper setting for that bit.

The MPV904 occupies 16 successive memory locations (word locations) within the system memory map.

Figure 2.2 shows the location and factory set configuration of the jumpers J1, J2 and J3.

Table 2.2 lists the jumper positions that determine which base address is selected.

Figure 2.2
Base Address Selection Jumpers

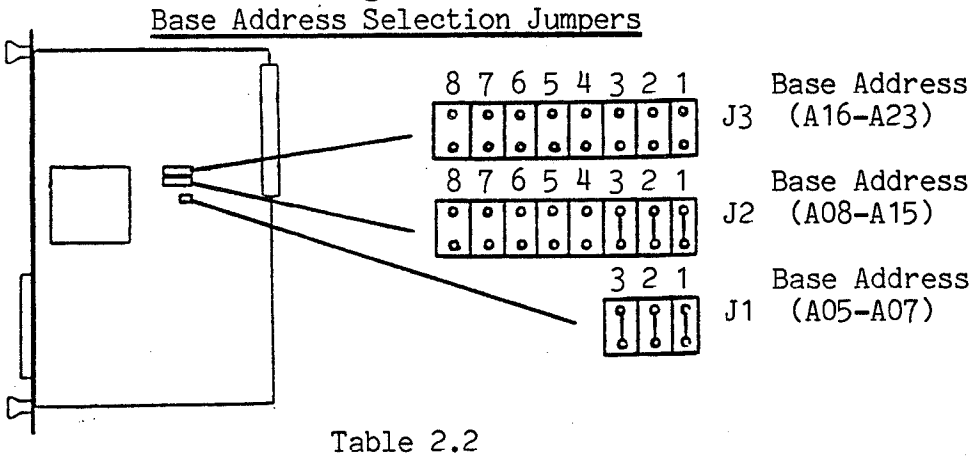


Table 2.2
Base Address Jumper Selection

ADDRESS LINE	FACTORY SET	JUMPER	
A05	0	J1 Position	1
A06	0		2
A07	0		3
A08	0	J2 Position	1
A09	0		2
A10	0		3
A11	1		4
A12	1		5
A13	1		6
A14	1		7
A15	1		8
A16	1	J3 Position	1
A17	1		2
A18	1		3
A19	1		4
A20	1		5
A21	1		6
A22	1		7
A23	1		8

NOTE: 0 = Jumper Inserted
1 = Jumper Removed

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2.2.2 Output Voltage Range Selection

Jumper J5 is used to set the output voltage range of all the analog outputs.

Each output is set at the factory for 0 to +10V operation (complementary straight binary coding).

When changing the output voltage range first remove all the jumper links on J5 and then insert those required for the desired range. Table 2.3 lists the available analog output ranges and the appropriate jumper settings.

The position of J5 is shown in Figure 2.3

Figure 2.3
Analog Output Range Selection Jumper

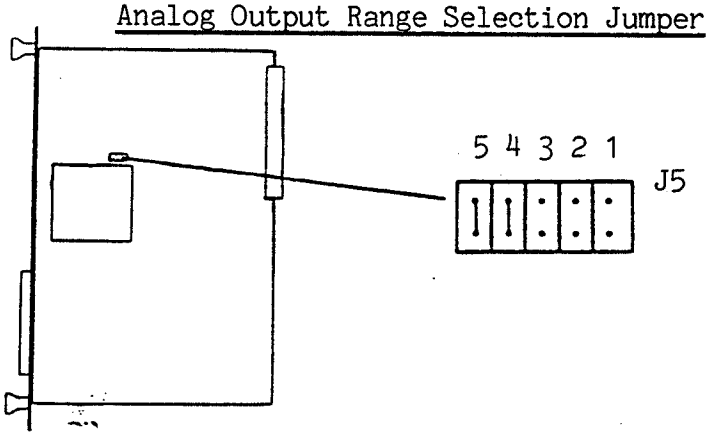


Table 2.3
Analog Output Range Selection

RANGE	J5 JUMPER SELECTION	
	INSERT	REMOVE
±10V	2,3	1,4,5
±5V	2,4	1,3,5
±2.5V	1,2,4	3,5
0 to +5V	1,4,5	2,3
* 0 to +10V	4,5	1,2,3

* NOTE:- Factory Set Condition

2.2.3 Address Modifier Code Response

IC9 is a PROM, which in conjunction with jumper J4, positions 1 and 2, allows the response to address modifier codes to be varied to suit user requirements. The PROM/jumper combination offers the options shown in Table 2.4. The PROM program which enables this response is shown in the programming chart of Figure 2.5, at the end of this chapter.

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The positions of IC9, jumper J4 and its factory set condition are shown in Figure 2.4 below:-

Figure 2.4
Address Modifier Code Jumper

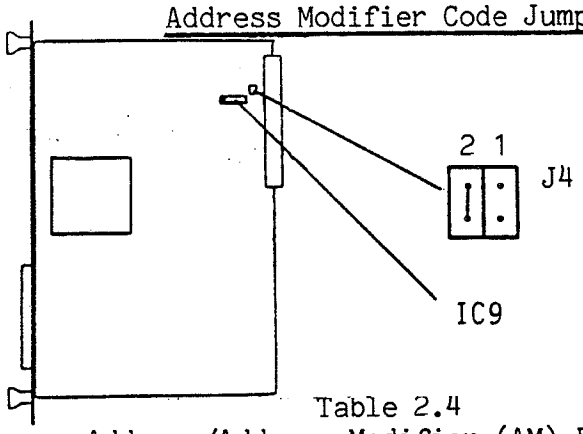


Table 2.4
Address/Address Modifier (AM) Response

	J4 Position 2	J4 Position 1	AM CODES	ADDRESS DECODING
1	Insert	Insert	N/A	A01-A15
* 2	Insert	Remove	N/A	A01-A23
3	Remove	Remove	3D, 39	A01-A23

* NOTE :- Factory set condition

A new PROM can be programmed to provide an alternative AM code response. The PROM is a 256 x 4 bit open-collector 82S126 type. The following section explains the interaction between jumper J4 and the codes stored in the PROM. An understanding of this section should allow the user to select the correct jumper/PROM code combination for a given response.

A list of VMEbus address modifier codes is given in section 6.2.

2.2.3.1 Programming the PROM

There are three allowable combinations of the J4 jumper links. These combinations are given in Table 2.4 and are referred to as (1), (2), (3). It is intended that combinations (1) and (2) be reserved for the responses detailed in Table 2.5, ie, short addressing with no AM codes and standard addressing with no AM codes respectively.

Combination (3) however, (both links removed), in conjunction with the information stored in the PROM, is designed to allow the response to address/AM codes to be modified, to suit system requirements, as shown in Table 2.5. Setting the two most significant data bits (D3 and D2) to a low level allows responses (1) and (2) as shown in Table 2.5. With both jumper links removed it is the setting of data bits D0 and D1 which determines the response.

The following section (2.2.3.2) illustrates the method to be used when programming the PROM to produce a given response.

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Table 2.5
Address/AM Response Options with Jumper Links Removed

AM CODE NOTE (1)	DATA BIT D3 D2 D1 D0	RESPONSE
XY	0 0 0 0	Short addressing with AM
XY	0 0 0 1	Short addressing with AM
XY	0 0 1 0	Standard addressing with AM
XY	0 0 1 1	No response to address/AM

NOTE :- The AM code indicated as XY can take any of the possible values defined in the VMEbus specification Revision B. (See Section C).

2.2.3.2 Programming Examples

The Factory Response

Referring to Table 2.4 the programming of the PROM to give the factory set response is as follows.

1. Decide upon STANDARD or SHORT addressing - STANDARD (ie, A01-A23 decoded)

2. Decide upon AM codes to which the board will respond - 3D, 39.

3. Refer to Table 2.5 and under "response" heading look for "Standard addressing with AM". The data to be stored at the relevant memory addresses can then be read from the table (in this case 0010,(02H)).

4.Place the code obtained in (3),(ie 02H), at memory locations 3D and 39.

5. Refer to Table 2.5 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses, (in this case all locations other than 3D and 39), can then be read from the table, (in this case 0011, (03H)).

6. Place the code obtained in (5), (ie 03H), at all memory locations other than 3D and 39.

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Short Addressing With AM

Assume that the following response is desired - Short Address decoding, (ie, A01 -A15 decoded) and AM codes 2D and 29* to be responded to. The following steps would yield the data to be placed in the PROM.

1. Addressing mode - SHORT.

2. Code response - 2D and 29.

3. Refer to Table 2.5 and under "response" heading look for "Short addressing with AM" (Note - there are two entries under this heading). The data to be stored at the relevant memory address can then be read from the table, (in this there is a choice of two codes - 0000 (00H) or 0001 (01H)).

4. Place either of the codes obtained in (3), (ie, 00H or 01H), at memory locations 2D and 29.

5. Refer to table 2.5 and under "response" heading look for "No response to address/AM". The data to be stored at the relevant memory addresses (in this case all locations other than 2D and 29), can then be read from the table, (in this case 03H).

6. Place the code obtained in (5), (ie 03H) at all memory locations other than 2D and 29.

Similar reasoning applies to any other combination of address/AM response.

*Any number and combination of AM codes may be catered for.

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Chapter 3 - OPERATING INSTRUCTIONS

3.1 INTRODUCTION

This chapter provides the necessary information to allow the use of the MPV904 in a VMEbus system.

3.1.1 Jumper Setting Checklist

Before plugging the board into a VMEsystem and applying power, check, to ensure proper system operation, that the following options have been correctly set.

1. Base Address.
   Has the Base Address of the board been set to suit system requirements? (Section 2.2.1)

2. Address Modifier Response.
   Has Address Modifier Response been correctly set? (Section 2.2.3)

3. Output Range.
   Has the correct voltage output range been selected? (Section 2.2.2)

3.2 OPERATING PROCEDURE

The board is shipped from the factory in a calibrated condition and ready for use. Installation only requires plugging the card into an empty slot in the VMEbus card cage and wiring the analog connector. However, the board can be adapted to suit user requirements therefore, some features of the board are jumper selectable. These features are covered in chapter 2 which should be referred to before using the board or if a configuration other than the factory set condition is desired.

3.2.1 Programming

The board is programmed as 16 successive memory locations (word locations), jumper selectable within the 16 Mbyte address range, in 16 word blocks, commencing at address 000000H. The analog output has a resolution of 12-bits and therefore word accesses are required for each channel.

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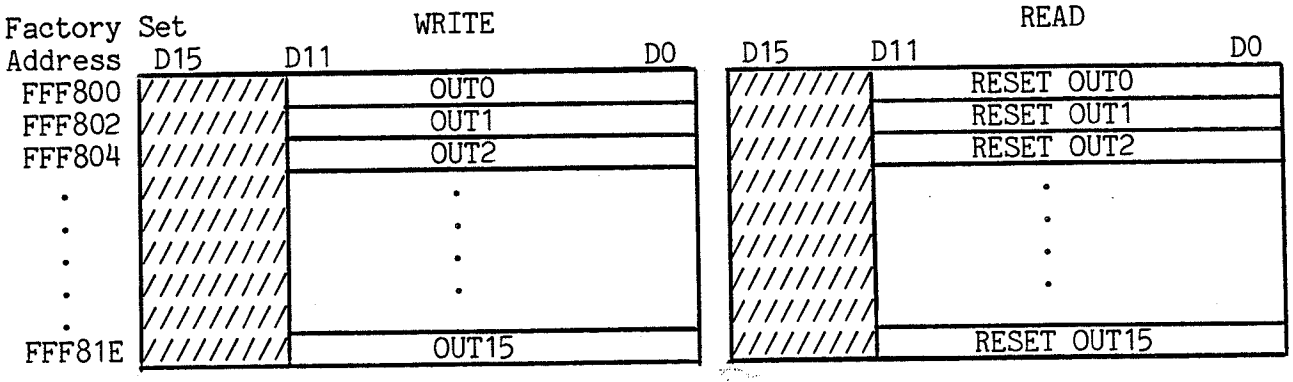
3.2.1.1 Address Map (Memory Map)

The address map (memory map) for the MPV904 board is shown in Figure 3.1. The base address is jumper selectable. (Section 2.2.1)

Output data (i.e. data to set an analog output to a particular value) is transferred to the board from the CPU with MOVE instructions to the appropriate addresses. 16 consecutive addresses are used, starting from the base address XXXXX0, (the X-states are selected as previously described). As each operation is a word access, word addressing must be used (even addresses only).

NOTE : A read operation to a channel results in the channel being reset to its most negative value.

Figure 3.1
MPV904 Address (Memory) Map



3.2.2 CPU Instructions

The CPU transfers data to the MPV904 by using MOVE instructions, using the addresses and data lines shown in the address (memory) map of Figure 3.1. These instructions are described in the following list. The selected base address of the board is XXXXX0 (factory set to FFF800H). The CPU register Dn is used as the data register (and may be any of the allowable registers within the CPU).

MOVE.W Dn,FFF800 - This instruction moves the contents of data register Dn, within the CPU, to analog output OUT0.

MOVE.W Dn,FFF802 - This instruction moves the contents of data register Dn, within the CPU, to analog output OUT1.

MOVE.W Dn,FFF81E - This instruction moves the contents of data register Dn, within the CPU, to analog output OUT15.

This illustrates the procedure for transferring data to the MPV904 to allow each output to be individually set.

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3.2.3 Analog Output Section

3.2.3.1 Analog Output Voltage and Converter Input Codes

The digital input value of a selected output is converted to a voltage. The digital to analog converter offers two output coding schemes - complementary straight binary (for unipolar ranges) and complementary offset binary (for bipolar ranges).

Tables 3.1 and 3.2 illustrate the full-scale negative, mid-scale and full-scale positive output voltages for the five output ranges with the corresponding digital input codes of the digital to analog converter and the value of the least significant bit (LSB).

Figures 3.2 and 3.3 show, in graphical form, the relationship between the digital input codes and the output voltages.

e.g. In Table 3.2 a digital input code of (X)FFFH corresponds to an output voltage of -10V in the range ±10V. In the same range a value of (X)000H will produce an output voltage of +9.9951V.

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Table 3.1
Complementary Straight Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(X)FFFH	(X)7FFH	(X)000H	
	0 to +5V	0.000V	+2.500V	+4.9988V	1.22mV
	0 to +10V	0.000V	+5.000V	+9.9976V	2.44mV

NOTE:- X indicates don't care states

Figure 3.2
Complementary Straight Binary

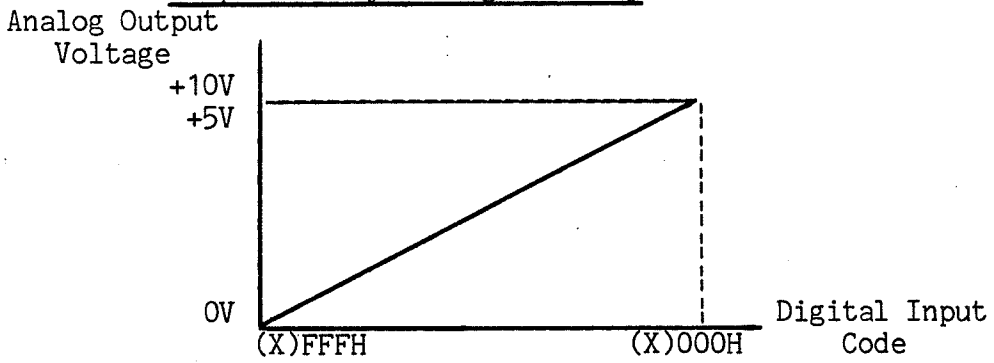
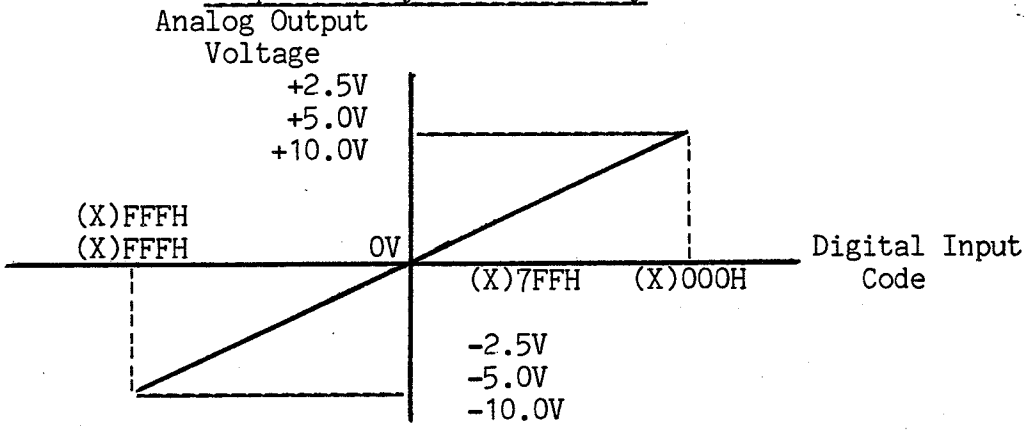


Table 3.2
Complementary Offset Binary

	SELECTED RANGE	NEGATIVE FULL SCALE	MIDSCALE	POSITIVE FULL SCALE	RESOLUTION
OUTPUT CODE		(X)FFFH	(X)7FFH	(X)000H	
	±2.5V	-2.5V	0.000V	+2.4988V	1.22mV
	±5.0V	-5.000V	0.000V	+4.9976V	2.44mV
	±10.0V	-10.000V	0.000V	+9.9951V	4.88mV

NOTE:- X indicates don't care states

Figure 3.3
Complementary Offset Binary



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3.2.3.2 Calculating Output Voltage From Input Code

The analog output voltage may be calculated from the input code, written by the CPU, as shown below.

$$\text{Output Voltage} = \text{Negative Full Scale} + (4095-\text{code}) \times \frac{\text{range}}{4096}$$

where,

range = theoretical range of values in the selected output range.
code = DECIMAL value of code placed in CPU register and written to output (with four MSB's set to zero).

NOTE: The code consists of 12 significant bits; bits D00-D11. In the CPU register bits D12 to D15 can be set to any value before data is written to the output. However, before using the following formula, bits D12 to D15 must be set to 0 for all input codes.

e.g. consider an output range of ±10V and a code of 7FFH. Then,

range = +10V - (-10V)
= 20V

code = Decimal value of 7FFH
= 2047

$$\text{Output voltage} = -10V + (4095 - 2047) \times \frac{20}{4096}$$

$$= 0V$$

Referring to Table 3.2 it can be seen that for a code of 7FFH, the expected voltage is 0V.

3.2.3.3 Output Range Selection

The analog outputs are factory set for a range of 0 to +10V with complementary straight binary coding. Other output ranges can be selected as described in section 2.2.2.

The maximum output current is 5mA per output on all ranges.

3.2.3.4 Output Check

Static checks of the analog outputs can be performed by loading the memory locations with output data words. The base address XXXXX0 is factory set to FFF800H (refer to address map Figure 3.1). The ideal values for positive and negative full scale are shown in Tables 3.1 and 3.2. The most significant four bits of the data word (D11-D15) are don't care states.

A program which performs a simple dynamic check of the analog outputs is listed in section 5.3.

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3.2.4 Output Calibration

The analog outputs can be calibrated by means of a single gain and offset adjustment as follows:-

Install the MPV904 in a VMEsystem and allow it to reach thermal equilibrium (about 20 minutes under power) before commencing the procedure. The positions of the calibration points and adjustment potentiometers are shown in Figure 3.4.

1. Connect a DVM (5 1/2 digit) between the calibration point (TP11) and the 0V(A) test point.
2. Load all memory locations with the code XFFFH.
3. Adjust the offset control, RV2, until the DVM reads for the range of interest, the value indicated in Table 3.3.
4. Load all memory locations with the code X000H.
5. Adjust the gain control, RV1, until the DVM reads the value, for the range of interest, indicated in Table 3.3.

Calibration is now complete.

Figure 3.4

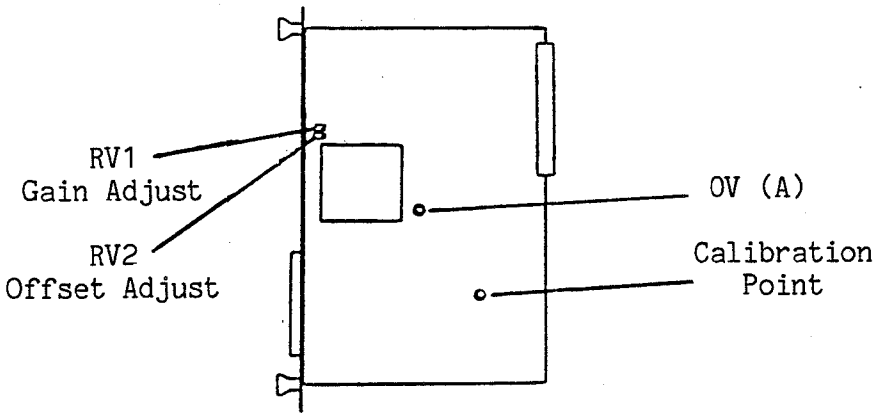


Table 3.3
Calibration Values

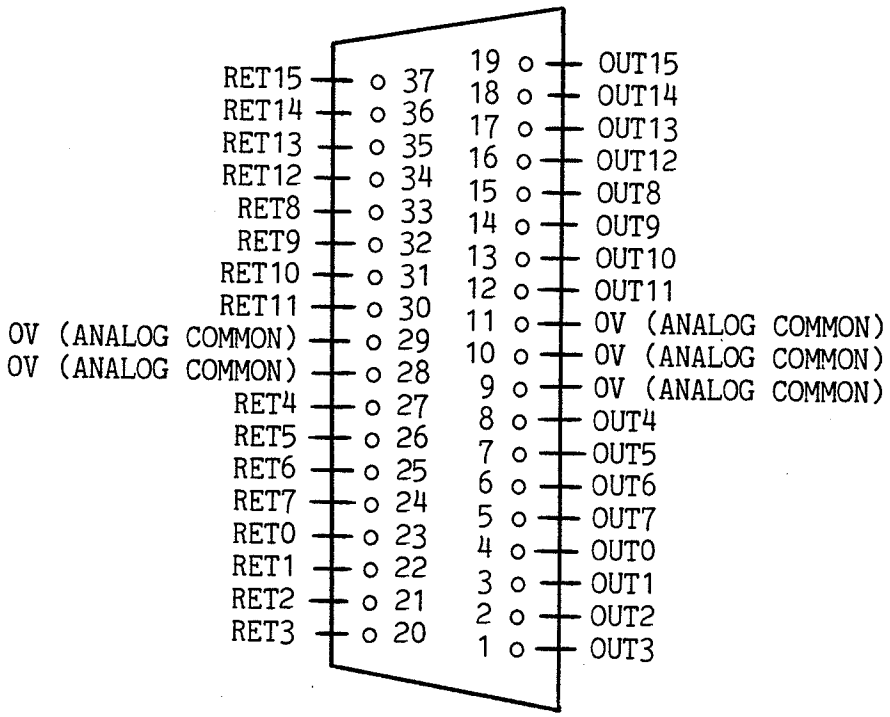
RANGE	DATA (X)FFFH	DATA (X)000H	1 LSB
±10V	-10.0000V	+9.9951V	4.88mV
±5V	-5.0000V	+4.9976V	2.44mV
±2.5V	-2.5000V	+2.4988V	1.22mV
0 to +5V	0.0000V	+9.9988V	1.22mV
0 to +10V	0.0000V	+9.9976V	2.44mV

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3.3 Analog Connector

The analog front panel connector, P3, is a 37 way 'D' type socket (female). The mating connector should be a 37 way 'D' type plug (male). Use Cannon type DC37P/1A1N or equivalent.

'D' Type Connector Pinout



3.4 Factory Set Configuration

All boards are shipped from the factory ready for immediate use, however, they do have a number of user selectable options. These options and their factory set conditions, which have already been described, are summarized below:

BASE ADDRESS FFF800H
ADDRESS/AM RESPONSE ..... STANDARD ADDRESSING/ALL AM CODES
OUTPUT RANGE ..... 0 TO +10V

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4.1 INTRODUCTION

This chapter is intended to provide an overview of the functional implementation for the MPV904 16 Channel Analog Output Board.

4.2 GENERAL INFORMATION

The MPV904 is a 16 channel analog voltage output board with 12 bit resolution, which interfaces directly to the VMEbus. Figure 4.1 shows a block diagram of the board.

4.3 THEORY OF OPERATION

The design of the MPV904 board is based on a dynamic output approach. This uses a single digital-to-analog converter (DAC) to drive all 16 analog outputs. Digital Data for each channel is stored in on-board RAM, while analog output data for each channel is stored in separate sample and hold circuits. The control and refresh circuitry selects from RAM, the appropriate DAC input for the channel being updated and multiplexes the DAC output to the appropriate sample and hold circuit. Therefore the output data is updated independantly of the CPU.

The CPU changes data in the on-board RAM by a write operation on D00-D11, (D00 is the LSB), to the appropriate channel. When this occurs the control logic disables the refresh circuitry to prevent output glitches and to allow the CPU to change the data stored in the on-board RAM.

A VME hold off mechanism as been implemented to ensure that VME accesses are interleaved with output refresh cycles. This will prevent the outputs glitching or decaying as a result of continuous VME accesses to MPV904. In order to ensure proper operation of the MPV904 within a VME system, the VME bus timeout must be greater than 20uS (BTO > 20uS).

4.3.1 Address/AM Decoder

The address decoding section consists of 3 magnitude comparators. These devices monitor address bits A05 through A23 inclusive. Address Modifier decoding is performed by PROM IC9.

Upon initiation of a data transfer on VMEbus, the levels on the address lines A05 through A23 inclusive are compared with the levels set by jumper groups J1, J2 and J3. Similarly, the address modifier lines are decoded to provide an appropriate output.

The board select logic is activated when a valid address modifier in conjunction with a valid address has been successfully decoded. VME address lines A04-A01 are used to select the particular channel being accessed.

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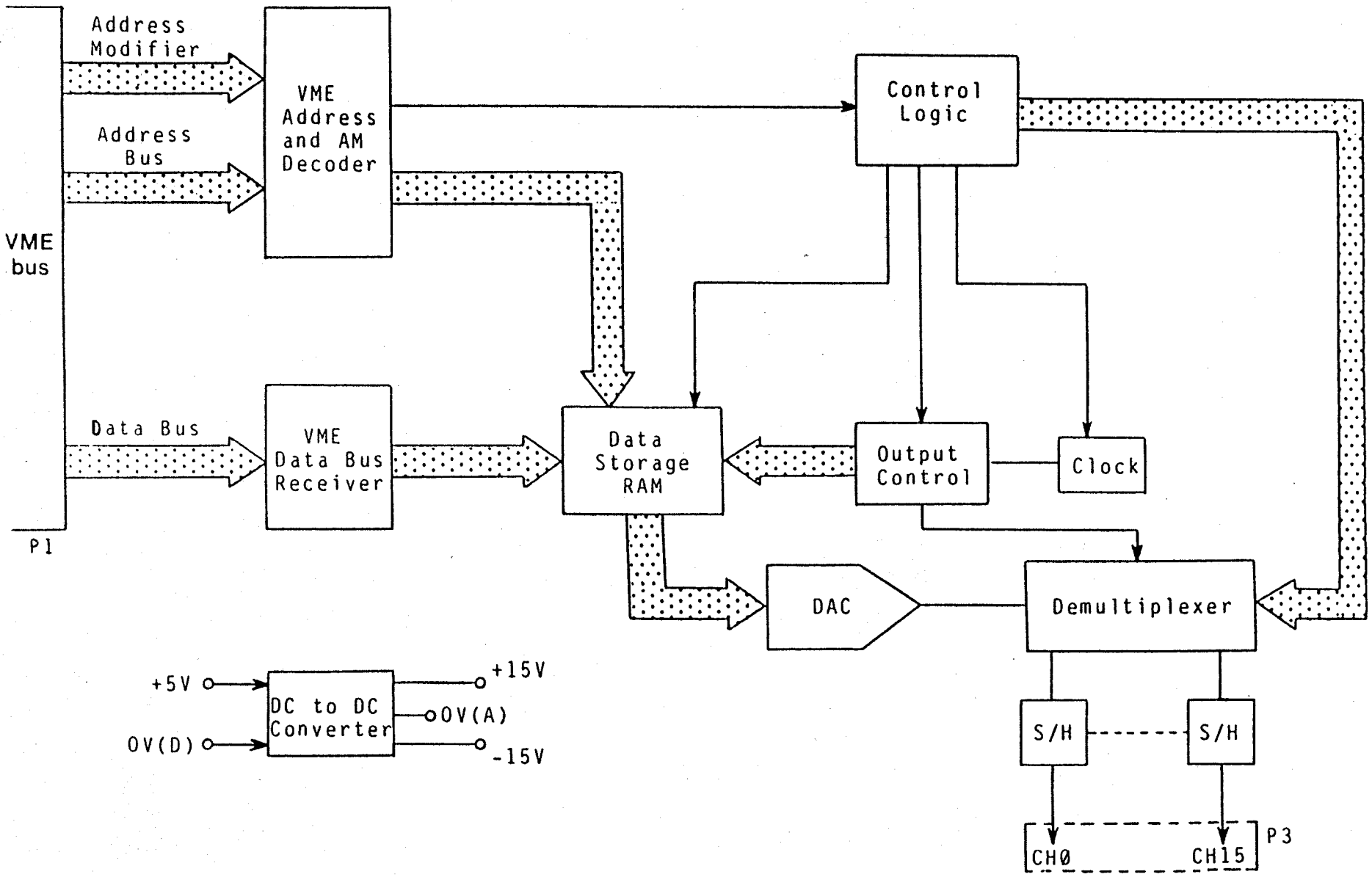


Figure 4.1 **MPV 904** BLOCK DIAGRAM

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4.3.2 Timing and Control Logic

All analog outputs are maintained by a refresh circuit. The refresh logic uses a 50KHz clock (20uS) and a 4-bit counter whose outputs form a 4-bit channel address. The data at the channel address driven by the refresh counter is held valid on the DAC inputs for 10uS, after this time the DAC output will have settled to its final value. A Multiplexer circuit then routes the DAC output to the appropriate channel output, therefore maintaining the channel output at its correct value.

4.3.3 Analog Output

Each of the analog outputs is a combined filter and sample-and-hold device. The filtering ensures that any glitches which occur during the switching process do not appear at the output. The output amplifiers have high input impedance, ultra low input offset and a series output resistor facilitates the driving of capacitive loads.

The circuit configuration of a single analogue output is shown below in Figure 4.2.

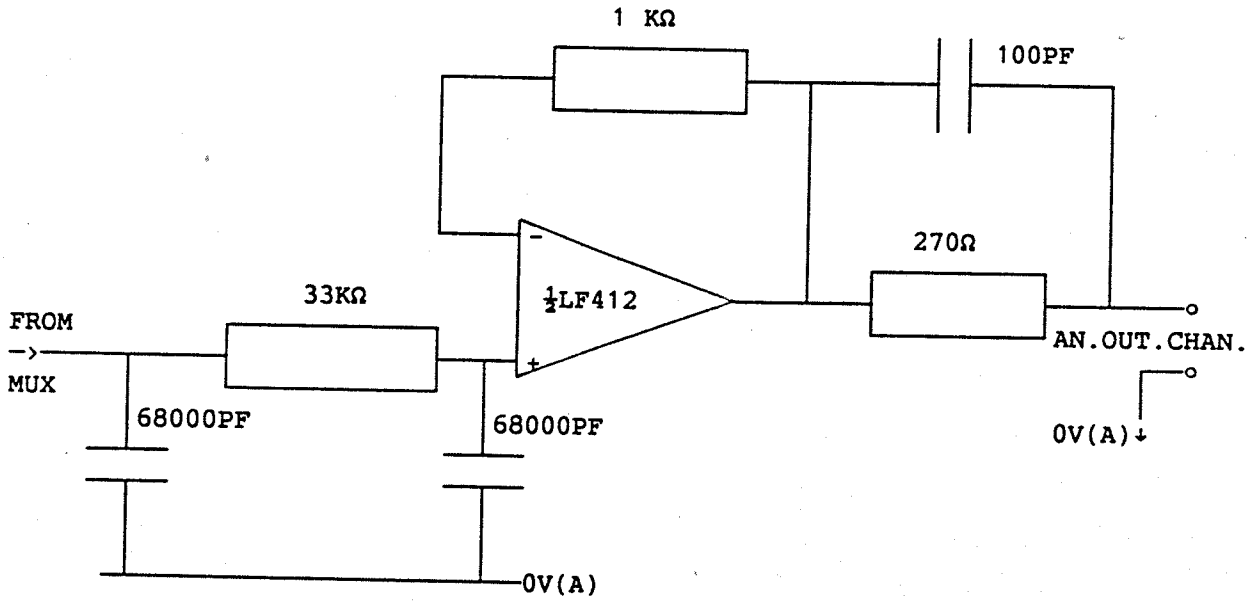


Figure 4.2

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5.1 INTRODUCTION

This section is intended to assist the MPV904 user to quickly gain an understanding of the operation of the board using small, easily understood, applications programs.

The following two programs were written assuming that the board is still in its factory set condition and therefore the memory map in chapter 3, Figure 3.1 applies. The programs are written in Motorola MC68000 assembly language on a FORCE SYS68K system, and stored in RAM starting at location 2000H. Depending upon the type of assembler and monitor programs used, the following programs may require modification, further help can be supplied from the factory. Memory locations 2000H to 2F00H are assumed to be RAM locations. If the available user RAM is at some other location the address in line 1 should be modified accordingly.

5.2 Static Analog Output Check

This program provides a simple static check for the first 10 analog outputs, by outputting the channel number of volts from a particular channel as follows:

```
Channel 0  -  0 Volts
Channel 1  -  1 Volt
Channel 2  -  2 Volts
    .          .
    .          .
Channel 9  -  9 Volts
```

```
            ORG     @$2000;      Start Address of program storage.
BASEADD:    EQU     @$FFF800;    Address of Channel 0.
ENDADD:     EQU     #$FFF814;    Address of last Channel+2.
MINVAL:     EQU     #$0FFF;      Initial output value (0 Volts).
STEP:       EQU     #$019A;      Output step size (1 Volt).

            MOVE.W  MINVAL,D0;   Start with initial value in D0.
            LEA.L   BASEADD,A1;  CH0 loaded in address pointer A1.
LOOP2:      MOVE.W  D0,(A1)+;    Output value and increment A1.
            SUB.W   STEP,D0;     1V added to output value in D0.
            CMPA.L  ENDADD,A1;   Have all channels been done?
            BNE.S   LOOP2;       No... Then repeat.
            TRAP    #14;         Yes.. Then return to the monitor.
```


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5.3 Dynamic Analog Output Check

This program performs a simple dynamic check of all analog outputs. A ramp (sawtooth) waveform with amplitude plus and minus full scale and frequency approximately 20Hz will be produced at each output.

This program can be used to check correct operation of all channels.

```
            ORG     @$2000;         Start address of program storage.
BASEADD:    EQU     @$FFF800;       Address of channel 0.
ENDADD:     EQU     #$FFF820;       Address of channel 15+2.
MAXVAL:     EQU     #$0000;         Maximum output value.
MINVAL:     EQU     #$0FFF;         Minimum output value.
STEP:       EQU     #$0F;           Output step size.


START:      MOVE.W  MAXVAL,D0;      Start with maximum value in D0 and CH0
RAMPDOWN:   LEA.L   BASEADD,A0;     address in A0.
LOOP1:      MOVE.W  D0,(A0)+;       Output a value then increment the
                                    channel address in A0.
            CMPA.L  ENDADD,A0;      Have all channels been done?
            BNE.S   LOOP1;          No... The repeat.
            ADD.W   STEP,D0;        Yes.. Then next value.
            CMPI    MINVAL,D0;      Check for minimum output value and
            BLT     RAMPDOWN;       repeat if not done...
RAMPUP:     LEA.L   BASEADD,A0;     Else begin to ramp up with min value
LOOP2:      MOVE.W  D0,(A0)+;       in D0 and CH0 address in A0.
            CMPA.L  ENDADD,A0;      Have all channels been done?
            BNE.S   LOOP2;          No... Then repeat.
            SUB.W   STEP,D0;        Yes.. Then next value.
            CMPI    MAXVAL,D0;      Check for max output value and repeat
            BGT     RAMPUP;         if not done...
            JMP     START;          Else begin again.
```


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Address Modifier Codes

HEXADECIMAL CODE	ADDRESS MODIFIER 5	4	3	2	1	0	FUNCTION	DEFINED BY
3F	H	H	H	H	H	H	Standard Supervisory Ascending Access	VMEbus Spec.
3E	H	H	H	H	H	L	Standard Supervisory Program access	VMEbus Spec.
3D	H	H	H	H	L	H	Standard Supervisory Data Access	VMEbus Spec.
3C	H	H	H	H	L	L	Undefined	Reserved
3B	H	H	H	L	H	H	Standard Non-Privileged Ascending Access	VMEbus Spec.
3A	H	H	H	L	H	L	Standard Non-Privileged Program Access	VMEbus Spec.
39	H	H	H	L	L	H	Standard Non-Privileged Data Access	VMEbus Spec.
38	H	H	H	L	L	L	Undefined	Reserved
30-37	H	H	L	X	X	X	Undefined	Reserved
2F	H	L	H	H	H	H	Undefined	Reserved
2E	H	L	H	H	H	L	Undefined	Reserved
2D	H	L	H	H	L	H	Short Supervisory I/O Access	VMEbus Spec.
2C	H	L	H	H	L	L	Undefined	Reserved
2B	H	L	H	L	H	H	Undefined	Reserved
2A	H	L	H	L	H	L	Undefined	Reserved
29	H	L	H	L	L	H	Short Non-Privileged I/O Access	VMEbus Spec.
28	H	L	H	L	L	L	Undefined	Reserved
20-27	H	L	L	X	X	X	Undefined	Reserved
10-1F	L	H	X	X	X	X	Undefined	User
0F	L	L	H	H	H	H	Extended Supervisory Ascending Access	VMEbus Spec.
0E	L	L	H	H	H	L	Extended Supervisory Program Access	VMEbus Spec.
0D	L	L	H	H	L	H	Extended Supervisory Data Access	VMEbus Spec.
0C	L	L	H	H	L	L	Undefined	Reserved
0B	L	L	H	L	H	H	Extended Non-Privileged Ascending Access	VMEbus Spec.
0A	L	L	H	L	H	L	Extended Non-Privileged Program Access	VMEbus Spec.
09	L	L	H	L	L	H	Extended Non-Privileged Data Access	VMEbus Spec.
08	L	L	H	L	L	L	Undefined	Reserved
00-07	L	L	L	X	X	X	Undefined	Reserved

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Address Modifier Codes (cont'd)

NOTES:

Short address uses 15 address lines (A01-A15).
Standard address uses 23 address lines (A01-A23).
Extended address uses 31 address lines (A01-A31)

Codes defined by the "VMEbus Spec." should not be used for purposes other than those specified.

Codes defined by "User" may be used for any purpose which the VMEbus user (board vendor or customer) deems appropriate (page switching, memory protection, MASTER or task identification, privileged access to resources, etc.).

Codes defined by "Reserved" should not be used by the user; they are reserved for system use and future enhancements.

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