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Find the *Curtiss-Wright / Pentland Systems VGD4/P2/96* at our website: ***Click HERE***

96 Channels 12/16 bit 85KSPS per Channel Simultaneous Sampling



Click Picture for Bigger Image

Features

- Up to 96 input channels in two slots
- Up to 85kHz Simultaneous Sampling
- 12-bit Resolution (VGD4) or 16-bit Resolution (VGD5)
- Very low digitisation latency for closed loop control
- Wide Input Range
- Software Linearisation via PROM calibration table
- Direct High Speed Links to DSP Engines via VME, VSB, FPDP and C40 comms ports

Applications

- Low Latency Control
- Simulation
- Experimental Research
- Test

VGD 4/5

The VGD4/5 is part of the VGX family of modular high performance VME data acquisition systems providing options for the simultaneous digitisation of up to 96 analog input channels in just two card slots. VGD4/5 has an impressive pedigree in meeting challenging applications such as high energy research where the simultaneous capture of high channel densities without loss of phase integrity between channels is essential. Pentland's analog system design expertise ensures minimum degradation of digitisation ac curacy in today's noisy computer system environments. A version of VGD4/5 is available with a front panel power connection which enables the use of linear supplies for maximum performance. The VGD4/5 family is also available with 64 and 32 channel variants.

Acquisition system solutions can be tailored for individual applications as VGD4/5 can be combined with the full range of VGX interface cards thereby allowing for data interconnection to VME and VSB (VGM1), FPDP (VGI1), and C40 comms port interfaces (VGI2). Systems integration is simplified with the provision of software drivers.

Functional Overview

The VGD4/5 acquisition sub-systems provide both a transient mode for low latency control applications and a continuous capture mode for monitoring applications. Simultaneous capture is synchronised to an external clock input with software programmable active edge polarity. The acquisition process is controlled via a simple memory mapped register set, with process status being available for polling or VME interrupt generation. Captured data is stored into local FIFO memory where it can be transferred to ext ended memory or directly to processing cards via VME, VSB, FPDP or C40 comms port interfaces.

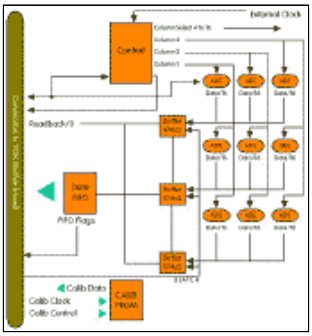
VGD4/5 offer a rugged, reliable high density solution for demanding data acquisition applications. A typical Mean Time Between Failures (MTBF) for VGD4/5 and associated motherboard is >44000 Hrs ground benign.

Ordering Information .

Reference No	Description
1. VGDX/YY/ZZ	Acquisition Daughterboard
2. VGDX/YY/ZZ/M1	As 1 above fitted with VGM1 motherboard and offering VME and VSB Interface
3. VGDX/YY/ZZ/M1C1	As 1 above with FPDP Direct Data Interface
4. VGDX/YY/ZZ/M1C2A	As 2 above with LSI/SPECTRUM C40 Comms Port Interface
5. VGDX/YY/ZZ/M1C2B	As 2 above with Mizar C40 Comms Port Interface
6. VGDX/YY/ZZ/M1C2C	As 2 above with Transtech C40 Comms Port Interface X = 4 VGD4 model X = 5 VGD5 model YY = P2 P2 Power YY = 00 Front Panel Power

Input

- Channel Count = 96, single-ended, simultaneous (also 64 and 32 channel versions)
- Sample Rate = Max 85KSPS Simultaneous All Channels
- Input Range = ±10V
- Maximum Input Range = ±20V Power Off/On without damage
- Input Impedance = >12.8kOhm
- Linearity = ±0.06% (2.5 LSBs) with calibration
- Input Capacitance = <50pF
- Conversion Jitter = <45nS
- Monotonicity = Guaranteed over temperature
- Channel Crosstalk = -80dB for Off to On Channel @ 1kHz



Digital Characteristics

- Sample Trigger - Active = Programmable Edge - Threshold Level = TTL - Input Capacitance = 50pF
- Maximum Trigger Rate = 85 kHz

Data Storage

- Buffer Memory = 4096 Sample FIFO (4K Words)
- Memory Expansion = Expanded data storage capability via VSB

Front Panel Connectors and LEDs

- Analog Input = 68 Way SCSI 11 Type Connector 32 Channels per Connector 1 Signal Return Per Channel
- Trigger Input = SMC
- Optional External Analog Power = Sub Miniature D-Type (+5V)
- Amber LED = Lit while data is held in FIFO

Power Requirements

- From VGX Motherboard = +5V @ 0.4A maximum
- P2 or Front Panel = +5V @ 2.0A maximum

VGD4 Specific Details

- Resolution = 12-Bits
- Gain Error = ±0.06% (2.5 LSBs) with calibration
- Offset Error = ±0.05% (2 LSBs) with calibration
- SFDR = 78dBc (typically)
- SINAD = 64dB (typically)
- THD = -74dB (typically)

VGD5 Specific Details

- SINAD = 83dB (typically)
- THD = -90dB (typically)

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