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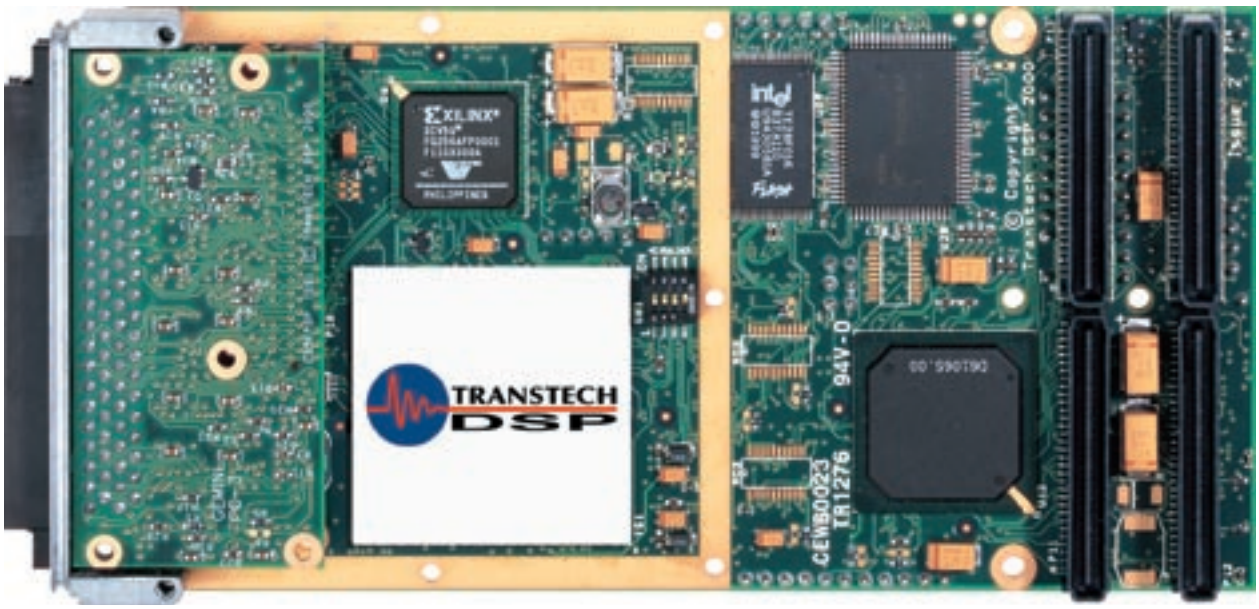
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Find the *Curtiss-Wright / VMETRO / Transtech DSP PMC-FPGA01* at our website: *Click HERE*

PMC-FPGA01

Digital I/O PMC
with Xilinx Virtex™ FPGA



Features

Xilinx XCV300 Virtex™ FPGA

Header module to provide level translation and external connector

Choice of front panel or user I/O routing

Programming FPGA clock

FPDP option

LVDS option

32/64-bit 33/66MHz master/slave PCI interface

128Mbytes SDRAM

2Mbytes SBSRAM

2Mbytes FLASH

The PMC-FPGA01 is a Xilinx XCV300E Virtex FPGA based digital I/O module aimed at high-bandwidth data I/O and ideal for custom interfaces. Typical interfaces include FPDP, LVDS, link port conversion, digital camera interface. This makes the PMC-FPGA01 ideal for imaging and radar applications.

TRANSTECH™ DSP

www.transtech-dsp.com

Hardware

Overview

The PMC-FPGA is a 64-bit/66MHz PMC format high-speed digital I/O module using a Xilinx Virtex-E™ FPGA. I/O is customizable through a front panel adapter. 128Mbytes of SDRAM and 2Mbytes of SBSRAM is also provided for local data buffers.

Xilinx Virtex™ FPGA

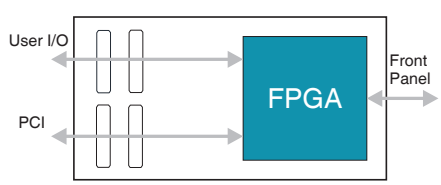
A choice of Xilinx Virtex-E FPGAs are available. A Xilinx XCV300E FPGA is offered as standard. This provides the PMC-FPGA01 with a range of devices, offering different gate densities and cost options to match the user's application.

Digital I/O

The FPGA can be used for digital I/O schemes such as FPDP, digital camera interfaces, serial ports and LVDS. Since the FPGA is used to control the bus protocol and timings, the I/O adapter becomes simple, low cost and easy to develop with the minimum of engineering design. Transtech provides options of FPDP and LVDS.

For digital I/O, 64 signals from the FPGA are routed to a header near the front panel. An I/O adapter module can be plugged onto this header to provide the appropriate external connector for the user's application, including level translation and line buffers where required. 5V and 3.3V power supplies along with voltage regulators are provided by the PMC-FPGA01 to aid level translation.

The 64 FPGA signals are also routed to the PMC's P14 user I/O connector. PMC hosts, such as VME boards, can make use of these signals directly with backplane I/O.



Flexible Data I/O

Programmable Clock

To facilitate designs requiring clock synchronisation, an AV9110-2 PLL programmable clock generator is provided. With the PLL reference clock of 14.31818MHz, the generated clock frequency can be programmed, using a 24-bit register, from 781KHz to 130MHz.

Software Support

FPGA

The Xilinx Virtex FPGA is based on SRAM technology and therefore must be reloaded with application code on each power cycle of the board. Code for the FPGA can be loaded in two ways: from an external host or from the local flash memory.

To allow the FPGA to be configured by a host, Transtech supplies loader utilities for VxWorks and Windows hosts (contact Transtech for the availability of other hosts including linux). This enables developers to use their standard tools [for example, Xilinx Foundation or Synplicity Synplify] for VHDL implementation, simulation and validation, then to transfer the application to the PMC-FPGA01 easily and quickly. Multiple test points are accessible to logic probes, assisting the user in debugging their FPGA based application.

Once the application has been finalised, it can be programmed into flash so that on a system power-up, the FPGA is automatically configured without the need of the host. A host based flash programming utility is provided to facilitate this step.

The PMC-FPGA01 features a high-speed (64-bit/66MHz) Initiator/target PCI interface and includes full FPGA to PCI interrupts and DMA. Example VHDL code is provided to allow the developer accelerated access to the built in resources of the PMC module.

Host Tools

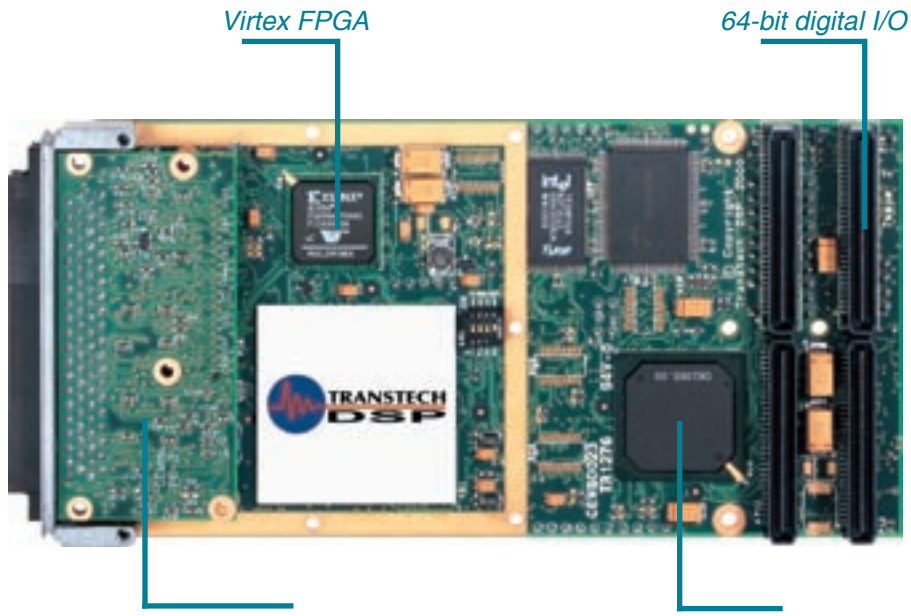
Software development is supported using the most common compilers

for the Operating system platform. This is Microsoft Visual C++ for Microsoft platforms and the GNU compiler for VxWorks, Linux, Solaris, LynxOS etc.

The BSP Library provides integration support for using the PMC-FPGA01 from within a host application. It is a C++ library supporting general hardware access and the implementation of high-speed DMA routines. Full source code for the libraries is included with the release. Example programs using these library routines are included to perform such tasks as setting up various DMAs to and from the board, including 'continuous mode' DMAs and how the board handles interrupts.

The host services provided by the libraries described above usually require the support of an operating system dependent device driver. Drivers for Window 95/98, Windows NT4/2000 and VxWorks operating systems are currently supported.

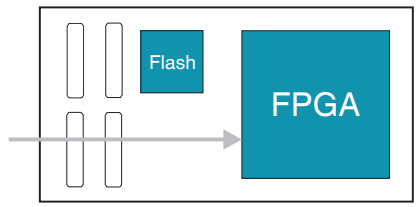
Host utilities are provided to give the user a graphical user interface with a complete view of the board hardware (registers, memory etc.). Other utilities allow for system evaluation and functional testing, as well as configuring the FPGA from the host and loading the ash.



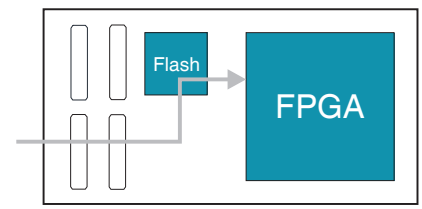
Programming the FPGA

The configuration file for the FPGA can be loaded directly from the host computer's file system across the PCI bus interface using the loader utility or as part of a host application.

The configuration file can be loaded into the ash using the host based programming utility. The ash allows up to eight Virtex 300E configurations to be stored at a time. If the auto-configuration switch is set, the FPGA will load from the ash on power up.



Direct FPGA Programming



Configuring directly from ash

Digital I/O Adapters

FPDP

With the FPDP I/O module fitted, the PMC_FPGA01 can serve as an FPDP Transmit Master, Receive Master and Receiver operating at up to 40MHz. An FPGA firmware example is provided for FPDP recieve. This also includes VHDL source and testbench as a starting point for users wishing to produce custom solutions.

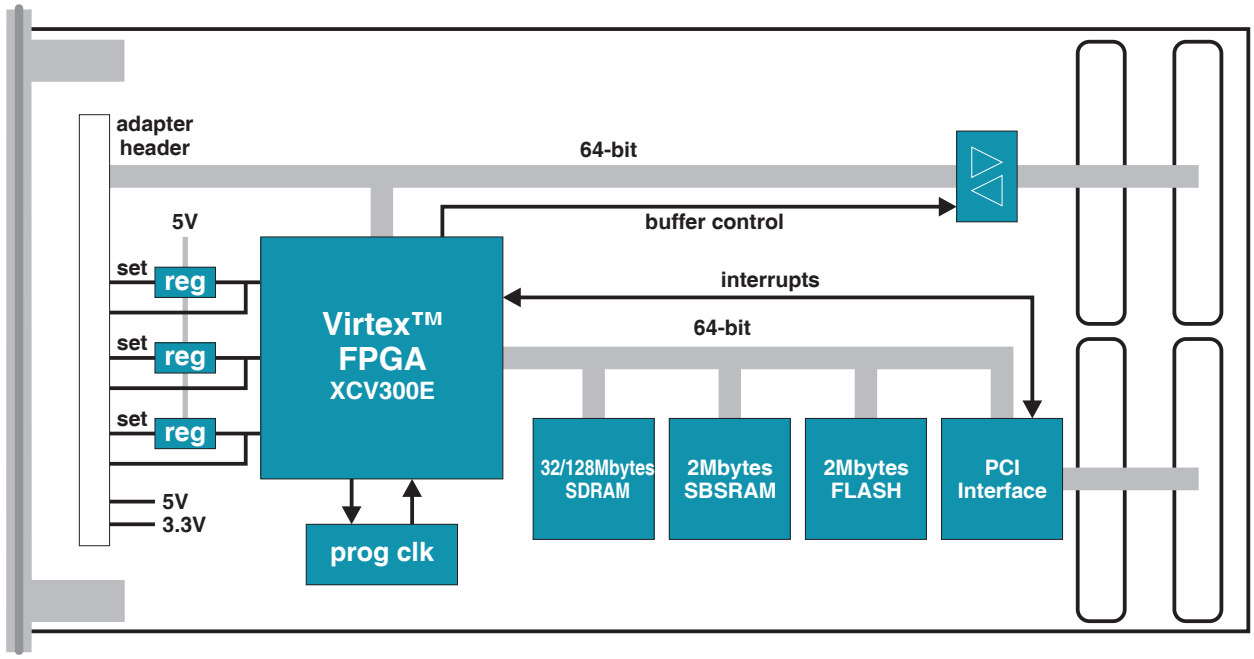
LVDS

Low Voltage Differential Signalling (LVDS) allows for very high data rates. The LVDS I/O module provides for 22 LVDS inputs and 8 LVDS outputs.

Special Variants

Front panel data I/O modules are usually simple and straightforward designs, but occasionally there is a requirement for the PMC-FPGA01 to be shipped with a customer specific I/O module. This might simply be digital I/O with a special connector or it might be a specific bus protocol. Please contact Transtech if you wish to discuss custom options.

Block Diagram



Technical Specification

FPGA

Device	Xilinx Virtex XCV300E (contact Transtech for other FPGAs)
Package	FP BGA256
FPGA boot	Programmable via PMC/PCI interface

Memory

SBSRAM	2Mbytes
SDRAM	128Mbytes
Local Bus	64 bit, 80MHz
FLASH	2Mbytes

PCI

Device	QL5064
Compliance	64-bit, 66MHz PCI 2.2 Master/Slave/ DMA
Enhancements	Endian conversion, DMA, interrupt support
Bandwidth	up to 528Mbytes/sec

Environmental

Signalling	3.3/5V
Operating Temp	0° to 50°C
Power Dissipation	Programming dependent
Relative Humidity	5% - 90% (non-condensing)

Software Support

Runtime Support	Windows 95/98, Windows NT4/2000, VxWorks
Libraries	Application Library in C++, includes full source code
Examples	Host C++ and FPGA VHDL code for DMAs, Interrupt handling and FPDP
Utilities	Load FPGA and Flash, test and probe system hardware.

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