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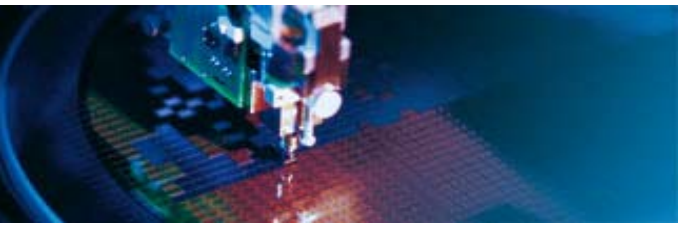
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Find the *Curtiss-Wright / Parvus PRV-1059-21* at our website: ***Click HERE***

USER MANUAL





PRV-1059

5-Port PC/104 10/100 Fast Ethernet Switch

MNL-0490-01 **Rev D4** **REF. ECO-3163** **01 Feb 10**

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Chapter 1 Introduction

This section provides a functional description of the PRV-1059.

Functional Description

PRV-1059 is a rugged VLAN-capable 5-port PC/104 Fast Ethernet switch featuring very low power consumption and highly reliable extended-temperature operation up to +85°C (185°F). Supporting auto-MDI-MDIX network installation, the board is designed for simple plug-and-play operation, enabling up to five embedded computing devices to be networked together using 10BaseT or 100BaseTX Local Area Network (LAN) connections.

Field programmable, port-based VLAN functionality is supported on select models. This powerful feature enables any combination of ports to be connected together in subnets for use in a small secure or non-secure network. Fully IEEE 802.3 and IEEE 802.3u compliant, its five transceiver ports are flexibly designed so that any port can serve as an uplink. The module can either be used as a standalone network switch (no processor board required) or in combination with embedded systems that support a PC/104 (ISA) bus.

The card integrates fully independent media access controllers (MACs), an embedded frame buffer memory, and a high-speed address look-up engine, along with support for auto-crossover, auto-polarity, auto-negotiation, and bridge loop prevention.

Qualified to MIL-STD-810 environmental standards, the compact PRV-1059 switch is ideally suited to space-constrained, high reliability aviation, industrial, military, and transportation applications where extreme temperature and high shock/vibration exist. The unit is only 3.550” x 3.775” (90x96 mm) in size. All versions include mounting holes to facilitate simple installation, as well as support for local or remote monitoring of LED activity for data RX/TX and connectivity.

Ethernet connections are made through either onboard RJ-45 jacks or right-angle, locking Molex connectors. The 4-pin Molex headers enable embedded systems to optionally mount RJ-45 jacks in a faceplate, endcap or enclosure using a Parvus cable set (sold separately), which includes five female Molex to RJ-45 adapters. Power connections can be made through either the PC/104 (ISA) bus or externally through a 2-pin Molex connector.

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Features

- RJ-45 jack or Molex Ethernet connectors
- LED activity indicators
- Link/activity and speed LED's available on separate connectors
- Low power dissipation
- Store-and-forward switching mode
- 5 Auto-configured ports (straight/twist cable connections)
- Auto-negotiation and speed auto-sensing support
- Ports can work at 10Mbps or 100 Mbps, full duplex or half duplex mode
- Simple networking installation through auto-MDI/MDIX (All ports can act as uplink)
- VLAN capability on select models
- Pause frame-based switch fabric delivers true non-blocking switching
- Back pressure-based flow control of half duplex ports
- Baseline wander correction circuitry
- Highly integrated DSP-based 10/100 switch
- Look-up engine supports as many as 1,024 MAC address entries
- 2-Pin Power Header for External Power Connections (select models only)
- 16-bit PC/104 Bus (select models only)

About PC/104

The PC/104 specification is characterized by its small form-factor (3.550" x 3.775"), stackable 104-pin/socket ISA bus connector, and reduced bus signal drive, making PC/104's size, durability, expandability, reliability, quality, and power consumption ideal for embedded computing. PC/104 technology leverages the same readily available development tools used with personal desktop computers to dramatically improve time-to-market for embedded systems development. The full PC/104 specification can be found at the PC/104 Consortium Web site: http://www.pc104.org/technology/pc104_tech.html

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Chapter 2 Quick Start-up

This section describes the installation of the PRV-1059.

Installation

The non-VLAN switch does not require drivers or software configuration. Users can immediately use any of the features of the product simply by attaching the cables and supplying power to the unit through either the PC/104 bus or 2-pin power header, depending on the version purchased. The VLAN-enabled switch requires use of the Parvus cable (sold separately) and software to configure the VLAN settings. Configuration and connection of the VLAN switch is described in chapter 5.

Carefully remove the board from its anti-static bag. For PC/104 applications, make sure power is turned off, then carefully line up all pins before insertion. Attach the 10/100 Ethernet Switch into a PC/104 card stack by mating PC/104 bus connector to PC/104 bus connector.

Installing Network Cables and Establishing Connectivity

The following types of cabling can be used with the 10/100 Ethernet Switch:
10BaseT Category 3,4 or 5 UTP/STP
100BaseTX Category 5 UTP/STP

Twisted-pair crossed cabling (10BaseT or 100BaseT) is recommended yet not required for the uplink connection (switch-to-switch). Straight cabling for the remaining port connections (switch-to-PC) is similarly recommended, but not required.

The board supports Auto MDI-/MDIX Crossover, which allows it to determine whether or not it needs to cross over between receive/transmit pairs, virtually eliminating the need for an external crossover cable. If it interoperates with a device that cannot automatically correct for crossover, the switch makes the necessary adjustment prior to commencing auto-negotiation. Similarly, if the switch interoperates with a device that implements MDI-MDIX crossover, a random algorithm determines which device performs the crossover.

The IEEE802.3ab specification, although well-written, does not clearly specify all linking conditions which may occur between the various modes of operation of Ethernet, taking into account auto-crossover, auto-negotiation, and forced modes of operation (10/100 forced speeds using either full or half duplex). As a result, mixing auto-crossover with forced modes of operation may lead to initial link problems whenever a cable is first “live” connected. Also, because of incompatibilities between various switch IC manufactures related to the IEEE 802.3ab specification, occasionally, link connectivity is not established immediately. When plugging in a new cable, if a link is not established within about 10 seconds (usually much faster!), then the user should simply cycle the power to the switch, turning it off and back on. In all cases, cycling power should result in a successful link, even when auto-detecting through forced modes of operation (10-base T/half, 10-base T/full, 100–base T/half and 100-base T/full). If it isn’t possible to cycle power, then cycling power of the associated link partner may be an option. At worst, and in rare cases, if power cannot be cycled, then eventually (within several minutes at the most) a link should successfully be established. Therefore, in these extreme rare cases, patience may be needed. However, once link is established, the switch will not miss packets outside of normal collision events, even when operating in harsh conditions using very long cables up to 100-meters in length.

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Chapter 3 Connector Description

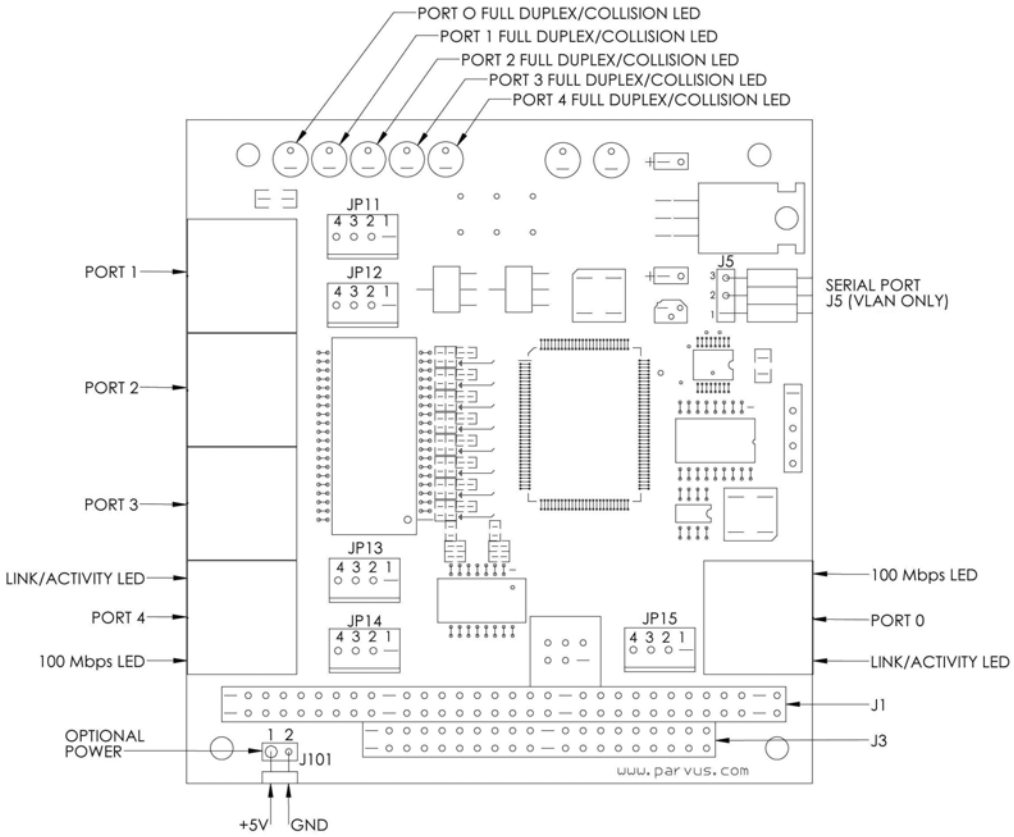
This chapter provides a brief description of the connectors located on the 10/100 Ethernet Switch.

Molex Connectors

Connector	Part Numbers
Ethernet (4-pin right angle)	P/N: 22-12-2044; mating P/N: 10-11-2043
Power (2-pin right angle)	P/N: 22-12-2024; mating P/N: 10-11-2023
LED's (4-pin straight)	P/N: 22-11-2042; mating P/N: 10-11-2043

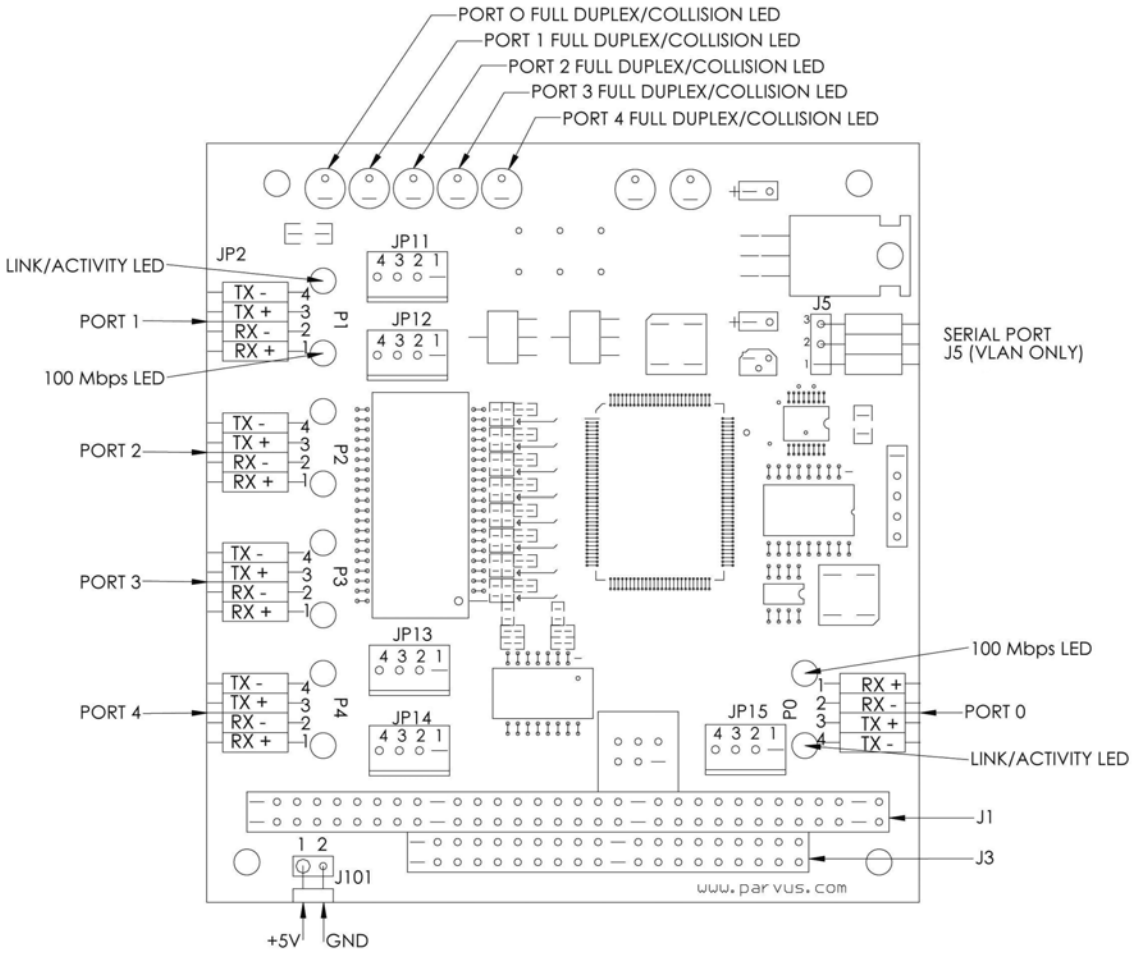
Connector Placement

10/100 Ethernet Switch (w/ local RJ-45 Jacks)



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10/100 Ethernet Switch (w/ 4-pin Molex Ethernet Connectors)



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Connector Pinouts

Molex Ethernet Pin Description: Ports 0-4

Molex Connector P/N: 22-12-2044; mating P/N: 10-11-2043

Pin	Signal
1	RX +
2	RX -
3	TX +
4	TX-

CON2/J101: 2-Pin Power Connector

(Not Loaded on PC/104 Versions)

Molex Connector P/N: 22-12-2024; mating P/N: 10-11-2023

Pin	Signal
Pin 1	+5VDC (closest to mounting hole)
Pin 2	GND

Parallel LED Ports: For All LED Ports JP11 through JP15

Molex Connector P/N: 22-11-2042; mating P/N: 10-11-2043

Pin	Signal
Pin 1	+3.3v
Pin 2	100/10 baseT (speed)
Pin 3	+3.3v
Pin 4	Link/Activity

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J1/J3: PC/104 Bus

Pin	Row A	Row B	Row C	Row D
0	--	--	GND	GND
1	/Iock	GND	/SBHE	/MCS16
2	SD7	Rstdrv	LA23	/IOCS16
3	SD6	+5v	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5v	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12v	LA18	IRQ14
8	SD1	/Exfer	LA17	/DA0
9	SD0	+12v	/MR	DRQ0
10	Iordy	(key)	/MW	/DA5
11	AEN	/SMW	SD8	DRQ5
12	SA19	/SMR	SD9	/DA6
13	SA18	/IOW	SD10	DRQ6
14	SA17	/IOR	SD11	/DA7
15	SA16	/DA3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5v
17	SA14	/DA1	SD14	/MSTR
18	SA13	DRQ1	SD15	GND
19	SA12	/Rfrsh	(key)	GND
20	SA11	SCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	IRQ6	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4	--	--
25	SA6	IRQ3	--	--
26	SA5	/DA2	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5v	--	--
30	SA1	OSC	--	--
31	SA0	GND	--	--
32	GND	GND	--	--

The PC/104 bus always uses Row A and B, while Row C and D are for 16 bit systems. B10 and C19 are keyed locations. For more information about the PC/104 specification, please visit the PC/104 Consortium Web site: http://www.pc104.org/technology/pc104_tech.html

Note. Only +5v and GND are used. All other signals are just pass-through.

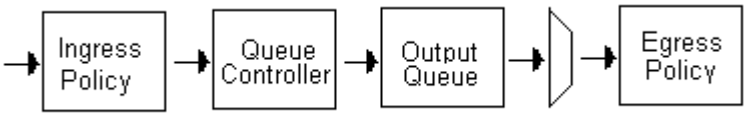
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Chapter 4 Operational Description

This chapter explains the operation of the switch.

Switch Data Flow

The switching portion of the PRV-1059 receives good packets from the MAC's, processes them, and forwards them to the appropriate MACs for transmission. Processing the frames is the key activity, and involves the Ingress Policy, the Queue Controller, the Output Queues, and the Egress Policy blocks shown below. Each port has it's own Ingress and Egress Policies**.**



Media Access Controllers

Five independent Media Access Controllers (MACs) perform the 802.3 protocol functions, including frame formatting, frame stripping, CRC checking, CSMA/CD enforcement, collision handling, etc. Before a packet can be sent out, the transmit block must check if the line is available for transmission. The transmit line is available all the time when the port is in full-duplex mode, but the line could be busy receiving a packet if the port is in half-duplex mode. If the line is busy, the transmitter waits by deferring its transmission. When the line is available, the transmission insures a minimum interpacket gap of at least 96 bits has occurred and then transmits a 56-bit preamble and an 8-bit Start of Frame Delimiter (SFD) ahead the basic frame.

For half-duplex mode, the switch also monitors the collision signals while it is transmitting. If a collision is detected (i.e. both transmitter and receiver of a half-duplex MAC are active at the same time), the MAC transmits a JAM pattern and then delays the retransmission for a random time period determined by the IEE 802.3 backoff algorithm. In full-duplex mode, the collision signal and backoff algorithm is ignored.

Backoff

In half-duplex mode, the Ethernet Switch's MACs implement a truncated binary exponential backoff algorithm, starting with a randomly small backoff time followed by progressively longer and longer random backoff times. The random times prevent two or more MACs from always attempting re-transmission at exactly the same time. The progressively longer backoff times give a wider random range giving congested links a better chance of finding a winning transmitter. The MACs will rest the progressively longer backoff time circuit after 16 consecutive re-transmit trials.

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Half- and Full-Duplex Flow Control

Half- and Full-duplex flow control is used to throttle the end station to avoid dropping packets during network congestion. When the free buffer space is almost empty or the output queue is almost full, the MACs force a collision in the input port when sensing an incoming packet. Full-Duplex uses frame pauses to handle the congestion.

Address Management

The switching function of the module involves the learning how to switch packets to the correct MACs, and only to the correct ones. The switch learns what port to which an end station is connected by remembering each packet's Source Address, and the port number the packet came in on.

When a packet is directed to an unlearned MAC address, the packet is transmitted to all of the ports. When an end-station responds back, its address is learned and stored until it is aged (see section 3.4.4). Once a MAC address/port is learned, all future packets directed to that address will be forwarded solely to that port.

When an end station is moved from one port to another, a new MAC address/port number association will have to be learned, and the new one replaced. For this to occur, the old association needs to expire or "age". These issues are handled by the "Aging" function (see section 3.4.4).

Address Translation Unit

The Lookup Engine or Address Translation Unit (ATU) reads the Destination Address (DA) and Source Address (SA) from each received packet, performing all address searching, learning and aging functions for all five ports at "wire speed" rates. It uses a hashing technique for quick storage and retrieval. If there is a hash collision, there is a four entry bin to hold MAC address with the same hash. The address table has storage for up to 1024 entries in the embedded SRAM, and has a default 300 second (5 min) aging time.

Address Searching

The address search engine searches the address database to obtain the output port number, called the Destination Port Vector (DPV), for each frame's Destination Address (DA). It arbitrates destination address requests from the ports and grants one lookup at a time. The MAC address is hashed, and then data is read from the SRAM table and compared to the MAC address for a match. If the compare matches, the DPV is returned to the output port queue manager, where is may be modified by the VLANTable data. When no match is found, a unique default DPV is returned to the output port queue manger, which typically sends the frame to all ports (to learn the MAC address).

Address Learning

An address-learning engine is used to learn the source address. Up to 1024 MAC address/port number mappings can be stored in the address table.

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When a frame comes in, the MAC address gets hashed into the database. If no match is found, the MAC address/port association needs to be learned. Learning consists of the following: the frame is forwarded to all of the ports, awaiting a response from one the ports. Once a port responds, the association is made and “learned” into the address table. If multiple ports respond, the associations are not learned. Once a MAC address/port is learned, all future packets directed to that address will be forwarded solely to that port.

Address Aging

Continuous address aging ensures an up-to-data address table and rapid address look-up. Once a node is disconnected from the network segment, or if it becomes inactive, its entry is removed from the address table. Every time a MAC address is found in the address table, the age is refreshed, keeping it active. Aging occurs by default every 5 minutes.

Each MAC address entry in the address table contains an age value, Entry_State. The initial value of Entry_State is 0xE. Aging occurs with a sweep of the table, the ATU reads each entry in the address table and decrements its Entry_State. Once the Entry_state of a MAC address reaches zero, the entry is killed and purged from the table. The speed at which aging occurs is default at 300 seconds.

Auto-Negotiation

Auto negotiating occurs when the switch negotiates with a link partner to determine the speed and duplex with which to operate. It the partner is unable to negotiate, the switch goes to a detection mode to determine the speed and the duplex will lock at half-duplex.

Auto MDI-/MDIX Crossover

The board determines whether or not it needs to cross over between pairs, virtually eliminating the need for an external crossover cable. If it interoperates with a device that cannot automatically correct for crossover, the switch makes the necessary adjustment prior to commencing auto-negotiation. Similarly, if the switch interoperates with a device that implements MDI-MDIX crossover, a random algorithm determines which device performs the crossover.

Port-Based VLAN

Select models of the PRV-1059 support field programmable, port-based VLAN functionality. Port-based VLANs are a type of VLAN where packet forwarding decisions are based on the MAC address of the destination and its associated port. With this powerful feature any combination of ports can be connected together in subnets for use in a small secure or non-secure network.

The following diagrams are similar to those which can be seen within the Parvus VLAN software and are included to illustrate the concept of VLAN on the PRV-1059. Figure 1 below shows a switch and all five ports with no restrictions; any port can talk to any other port. This is the state of non-VLAN switches and is also the factory default setting for the VLAN-enabled switch.

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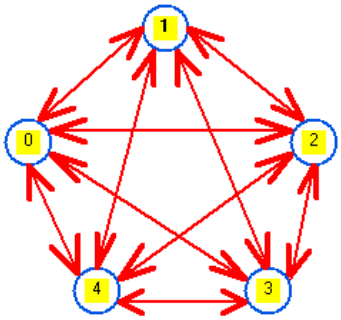


Figure 1) Non-VLAN configured state.

Unlike Figure 1 above, a VLAN configured switch limits which ports can communicate with each other. The following diagram is a sample of the way that the switch may be setup.

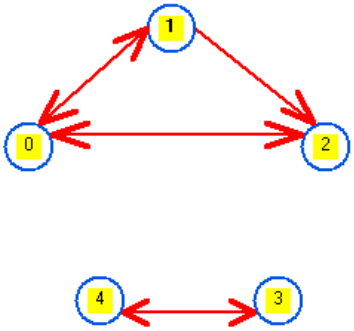


Figure 2) Known VLAN configuration

Figure 2 is VLAN configuration where Ports 0, 1, and 2 form a VLAN. Note that port 2 may talk to port 0 but NOT to port 1. In contrast, port 0 may talk to either port 1 or 2, and port 1 may talk to port 0 or 2. Furthermore, ports 3 and 4 are configured to form a different VLAN and can talk to each other, but not to the first VLAN.

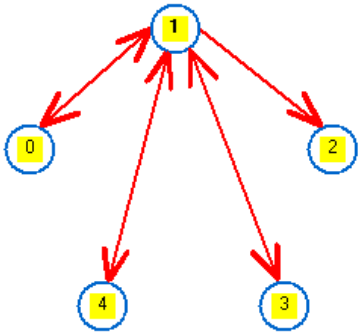


Figure 3) Additional Known Configuration

Figure 3 shows another possible VLAN configuration. In this setup, port 1 can talk to all other ports. Ports 0, 3, and 4 can only talk to port 1 and port 2 is not allowed to send data to any ports.

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VLAN Software Quick Start Setup Guide

In order to change the VLAN configuration on the PRV-1059 5-port Switch, Parvus has provided the user with a simple-to-use GUI program. Implementation of the program is through an RS-232 serial cable connection between a COM port on the host computer and the serial port on the switch.

The following steps describe the process required to setup the VLAN software from an administrator's (user's) standpoint:

I. Connect the serial port of the PRV-1059 (J5) to the COM port of the CPU using the Parvus VLAN serial cable (PRV-1304-01, sold separately).
II. Download the ParVLAN software for the PRV-1059 from www.parvus.com/support
III. Unpack the zip file and run setup.exe to install the software

Once the switch is connected and the software installed, you will be able program the switch with the desired VLAN configuration.

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Software Guide

This section describes how to use the VLAN GUI program to set up VLAN configurations on the PRV-1059. A screen shot of the program is shown below.

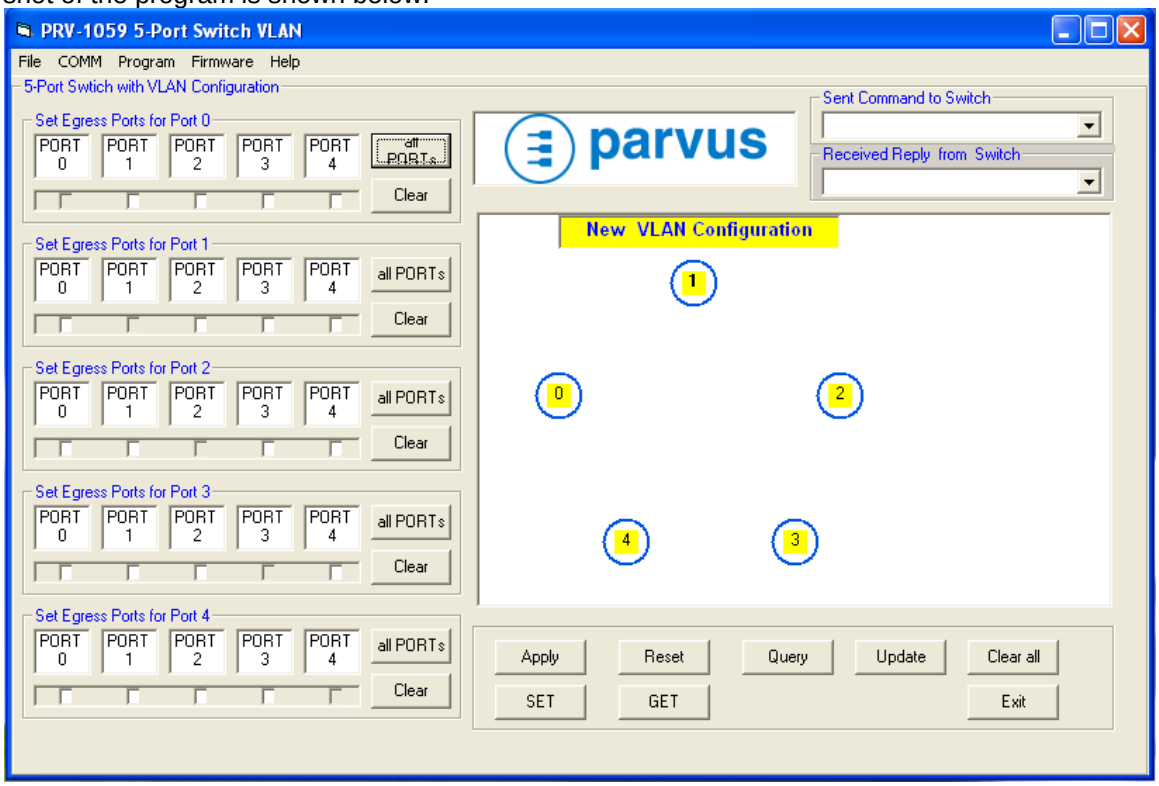


Figure 4) VLAN GUI Window

Com Port

In order to program the PRV-1059, the computer running the software must be connected to the serial port of the switch. The default COM port for the host computer is set to COM 1. If the user uses a different COM port, the COM port setting can be changed by selecting the COMM menu located at the top left of the GUI window.

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Setting the Egress Ports

Since port-based VLANs only govern outgoing traffic, it necessary to define the egress for all ports. An egress port is defined as the port to which data packets are sent. A visual example is provided below.

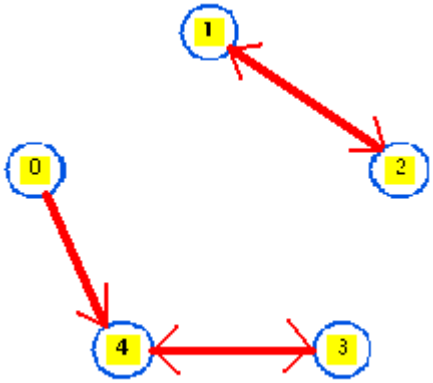


Figure 5) Egress Port

Port-based VLAN egress ports for Figure 5:

Egress port for Port 0 : Port 4
Egress port for Port 1 : Port 2
Egress port for Port 2 : Port 1
Egress port for Port 3 : Port 4
Egress port for Port 4 : Port 3

Each port can only send data to its egress port. In this example, each port has only one egress port, but on the PRV-1059 it is possible for each to have between zero and four egress ports.

There are 5 egress port configuration schemes ranging from “Set Egress Ports for Port 0” to “Set Egress Ports for Port 4” on left side of the VLAN GUI window. The user can enable any possible VLAN configuration by checking or un-checking these boxes. When each of these check-boxes is checked, there is a coordinate displayed in the “New VLAN Configuration” graphics indicating the setting of the VLAN with a line and an arrow pointing to the port where the data packet will be sent. There are also “all PORTs” and “Clear” buttons on right of each scheme which can be used to set or clear all check-boxes.

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Operation of VLAN GUI Window

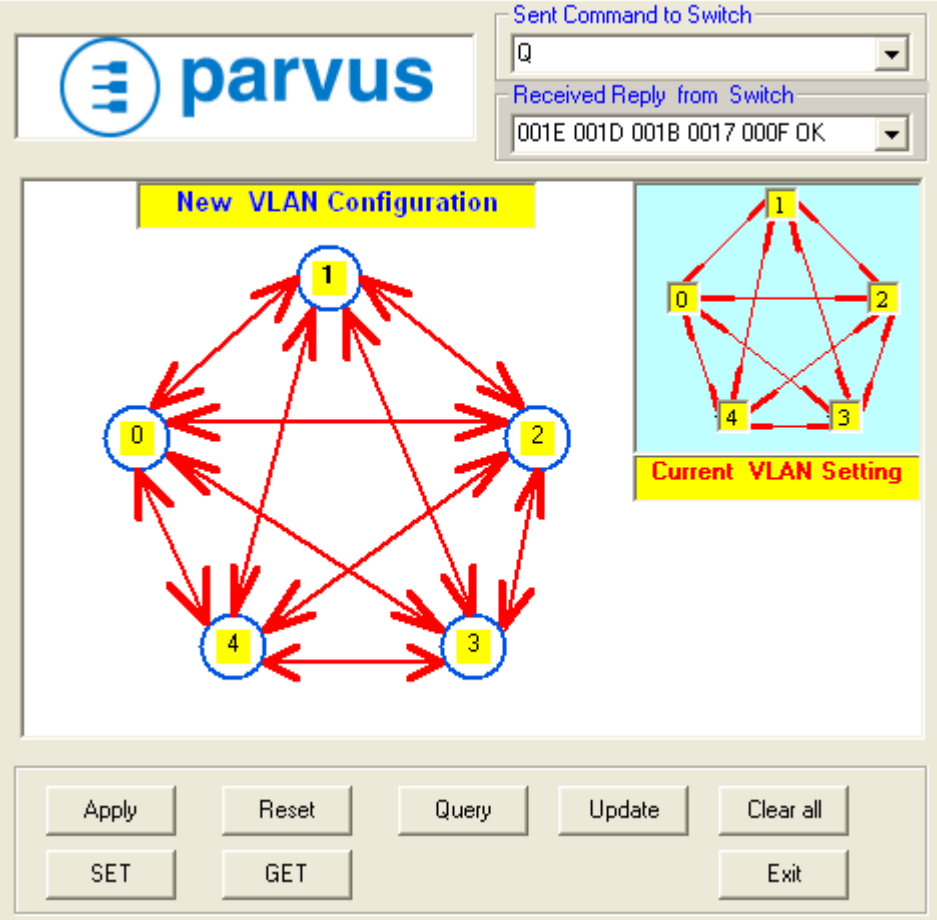


Figure 6) Manipulations of VLAN GUI Window

In the above figure, The GUI is divided into four areas:

a) Text display window area for “Sent Command to Switch” and “Received Reply from Switch”
b) VLAN graphic window area for “New VLAN Configuration” and “Current VLAN Setting”
c) VLAN operation button area for “Apply”, “Reset”, “Query”, “Update”, “Clear all”, “SET”, “GET” and “Exit”.
d) Parvus logo area.

The operation button area is the most important area because all VLAN configurations, setting displays, executing the VLAN commands will be implemented by these buttons.

a) **Apply**– causes the “New VLAN Configuration” to be written to the registers of the PRV-1059 allowing the user to test the VLAN settings. Note that as soon as the switch is powered off, the

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settings in the registers will be lost. The **Program** menu item on the top left of the GUI must be used to write the configuration to the firmware.

b) **Reset**– resets the 5-port Ethernet switch. This clears all VLAN settings and allows all ports to talk to each other through the switch.

c) **Query**– queries the switch's current VLAN settings. The graphics displaying the current VLAN settings on the switch will show up on the right top of the GUI window.

d) **Update**– copies the graphics of "Current VLAN Settings" to the "New VLAN Configuration" window in order to easily change or modify VLAN settings based on the current VLAN settings. Note this does not affect current VLAN settings in the switch, unless the Apply button is pressed.

e) **Clear all**– clears the graphics of "New VLAN Configuration" and un-checks all the check boxes for the five VLAN configuration schemes. Note this does not affect the current VLAN settings of the switch.

f) **SET**– This button is used for internal troubleshooting or testing by Parvus. Typing a command in the text box on the top right of the GUI window, and then pressing this button will set the switch's registers.

g) **GET**– This button is used for internal troubleshooting or testing by Parvus. Pressing this button will show the contents of the switch's registers in the text box of "Receive Reply from Switch".

h) **Exit**– Pressing this button will exit the operation of VLAN program.

Menu Operation

a) **File**– consists of the Password and Exit functions. The Password function is not implemented in VLAN program version V2.0.9. The Exit function exits the program.

b) **COMM**– allows user to select a COM Port on the host computer.

c) **Program**– writes the current VLAN settings to an EEPROM on the PRV-1059. Note that every time when you re-configure the switch using the **apply** button, the new VLANs are only valid until power is lost. Once you save your new VLAN settings by using the **Program** function, the microcontroller on the board reads the contents from the EEPROM when the switch is powered on and initializes the registers to set the VLANs on the switch.

d) **Firmware**– displays the firmware version of the microcontroller's current software.

e) **Help**– has an "About" window to display the Parvus Logo and the program version number.

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Chapter 5 Specifications

This chapter provides the specifications for the PRV-1059.

Technical Specification

Electrical

- Requirements +5VDC Input
- Power Consumption Max: +5 VDC @ 0.44A or 2.2 Watts (0.45W base + 0.35W per port used)

Environmental Specifications

This section describes the environmental standards that the PRV-1059 has either been designed to meet or tested to.

Temperature

- Operating: -40ºC to +85ºC
- Non-Operating: -55ºC to +100ºC

Reliability (MTBF)

The following table shows the predicted values for reliability of the PRV-1059] as a Mean Time Between Failures (MTBF)

1.503 Million Hours @ 40°C (Per MIL-HDBK-217F, Ground Benign, Controlled GB, GC)
157,971 Hours @ 40°C (Per MIL-HDBK-217F, Airborne Inhabit Fighter, AIF)
60,164 Hours @ 40°C (Per MIL-HDBK-217F, Airborne Rotary Winged, ARW)

Mechanical

This section provides details related to the mechanical construction of the PRV-1059.

Weight

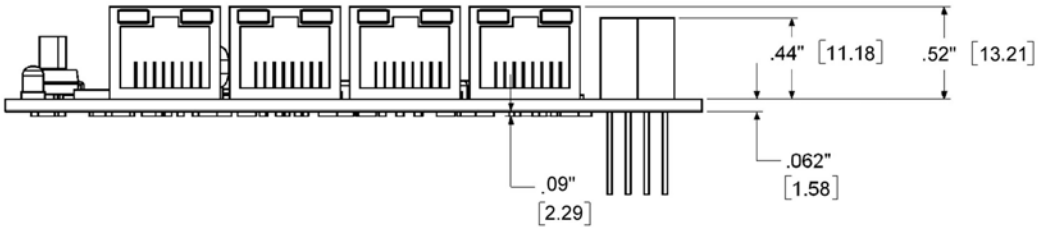
The PRV-1059 assembly weighs up to 88.6 grams (0.195 lbs.)

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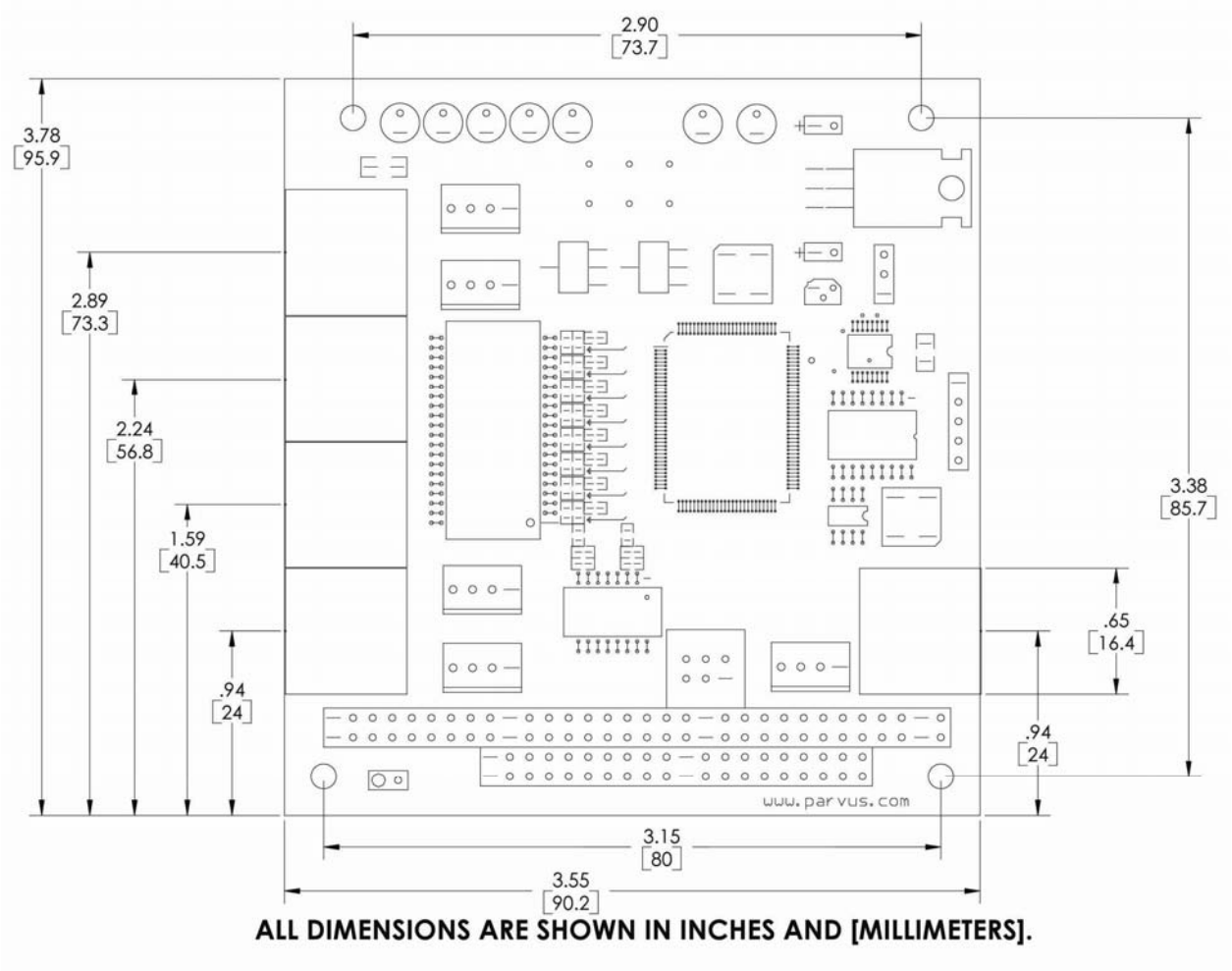
Dimensions

3.550” x 3.775”

RJ-45 Version



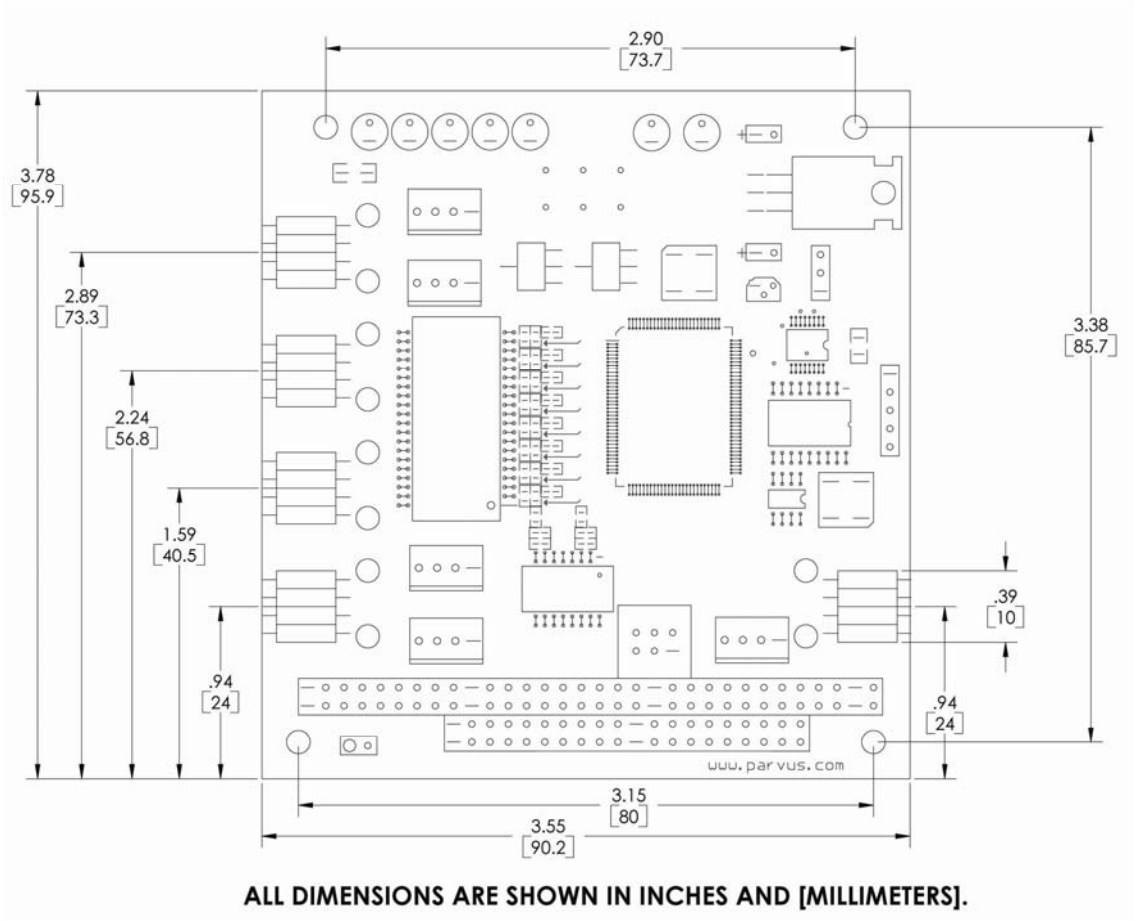
Warning: PC/104 specifications state that max height may only be 0.435”. Be sure that the board height of 0.52” for the RJ-45 version will operate in your application. This applies to the RJ-45 version only.



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Molex Version





Note: The external power connector (J101) on models without the PC/104 bus is a right angle two-pin Molex connector that extends from the board .32”

Note: For further information about the mechanical dimensions of ISA and PCI buses please refer to the PC/104 Consortium site (www.pc104.org)

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Chapter 6 Troubleshooting

Technical Assistance

If you have a technical question or if you cannot isolate a problem with your product, please call or e-mail the Parvus Technical Support team:

- Email: tsupport@parvus.com
- Phone: +1 (801) 433-4322
- Fax: +1 (801) 483-1523

Returning For Service

Before returning any Parvus product, please fill out a Returned Material Authorization (**RMA**) request form available for download from the following website under the support section:

www.parvus.com

Email this form to the email address listed above to receive authorization for shipment. An RMA number will be emailed back to you as soon as possible.

Note. You must have the RMA number in order to return any product for any reason.

Pack the module in an anti-static material and ship it in a sturdy cardboard box with enough packing material to adequately cushion it.

Warning! Any product returned to Parvus improperly packed will immediately void the warranty for that particular product!

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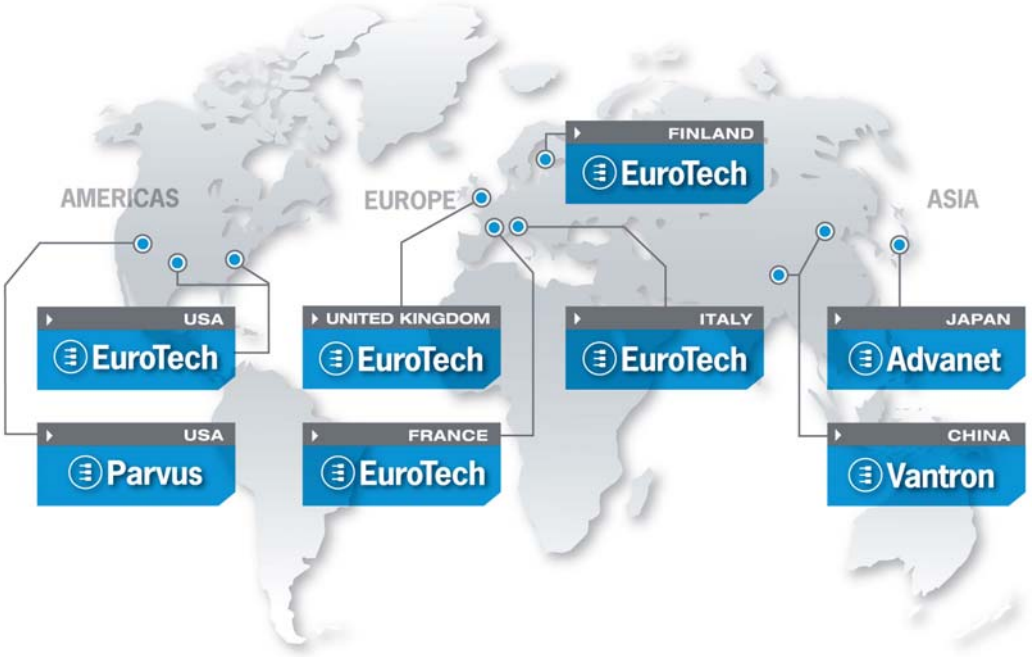
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